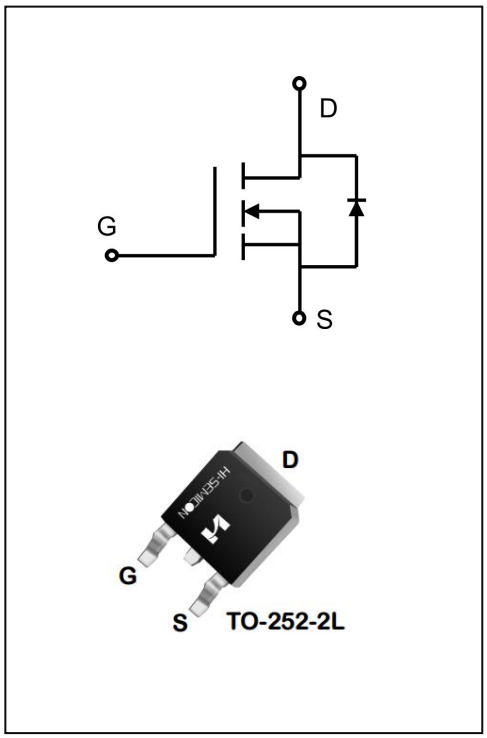
7A, 300V N-CHANNEL POWER MOSFET



GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are produced using Hi-semicon's proprietary, planar stripe, VDMOS technology.

Features

◆V_{DS}(V)=300V, I_D=7A

◆$R_{DS(on)}$

TYP:520mΩ@V_{GS}=10V I_D=3.5A

MAX:600mΩ

Applications

◆Power faction correction (PFC)

◆Switched mode power supplies (SMPS)

◆Uninterruptible power supply (UPS)

◆LED lighting power

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFD7N30TS	TO-252-2L	SFD7N30TS	Pb free	Reel

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	300	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C = 25°C	I_D	7.0	A
	T_C = 100°C		4.8	
Drain Current Pulsed (Note 1)		I_{DM}	28	A
Power Dissipation(T_C=25°C)		P_D	76	W
-Derate above 25°C			0.61	W/°C
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	320	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C
Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds		TL	300	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	MAX	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.6	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	300	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=300V, V_{GS}=0V	--	--	100	nA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	3.0	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	520	600	mΩ
Dynamic Characteristics						
Gate Resistance	Rg	V_{GS}=0V; f=1.0MHZ	--	4.0	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V	--	455	--	pF
Output Capacitance	C_{oss}	V_{GS}=0V	--	70	--	
Reverse Transfer Capacitance	C_{rss}	f=1.0MHZ	--	10.6	--	
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=180V R_G=25Ω	--	13.1	--	ns
Turn-on Rise Time	t_r	I_D=7A (Note 3.4)	--	26.4	--	

Turn-off Delay Time	$t_{d(off)}$	V_{DD}=180V R_G=25Ω	--	20.6	--	ns
Turn-off Fall Time	t_f	I_D=7A (Note 3.4)	--	24.1	--	
Total Gate Charge	Q_g	V_{DS}=240V, I_D=7A	--	11.7	--	nc
Gate-Source Charge	Q_{gs}	V_{GS}=10V	--	4.04	--	
Gate-Drain Charge	Q_{gd}	(Note 3.4)	--	5.37	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	I_S=7A,V_{GS}=0V	--	1.0	1.4	V
Reverse Recovery Time	T_{rr}	I_F=7A,V_R=300V, dIF/dt=100A/μS	--	44.6	--	ns
Reverse Recovery Charge	Q_{rr}		--	59.6	--	nC

1.Pluse width limited by maximum junction temperature

2.L=10mH, I_{AS}=8.0A, V_{DD}=100V, V_G=10V, R_G=25Ω, starting T_J=25°C

3.Pulse Test: Pulse width ≤300μs, Duty cycle≤2%

4.Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

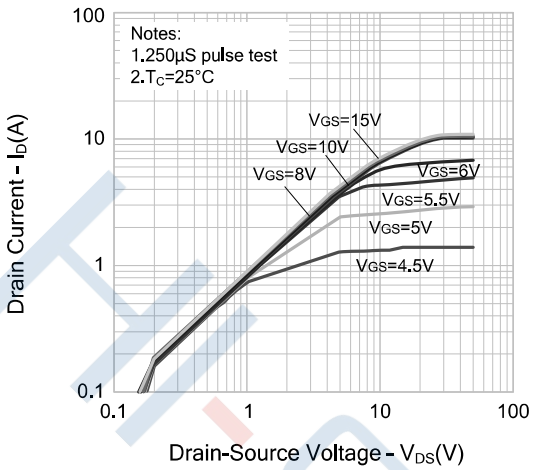


Figure 2. Transfer Characteristics

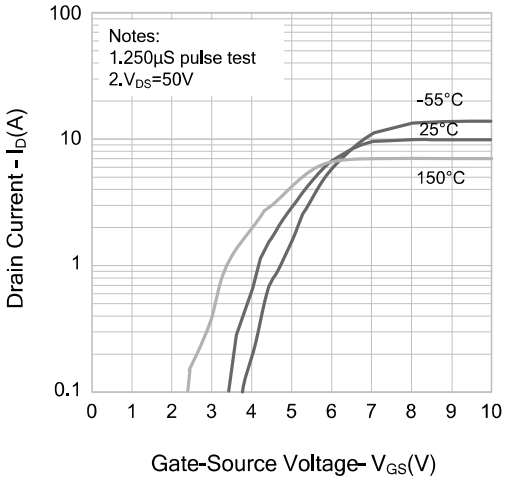


Figure 3. On-Resitance Variation vs. Drain Current

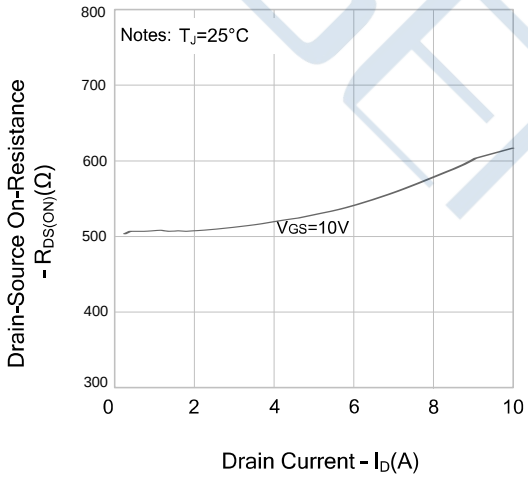


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

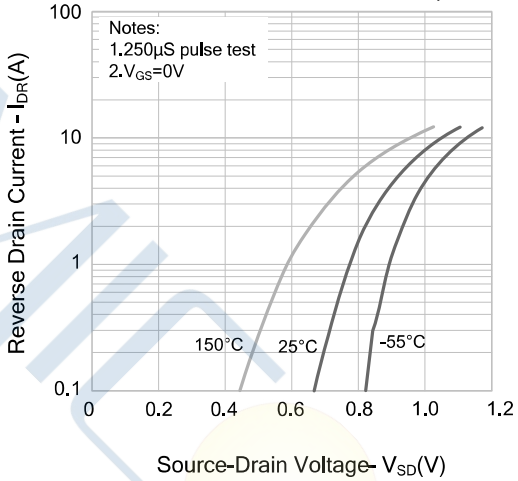


Figure 5. Capacitance Characteristics

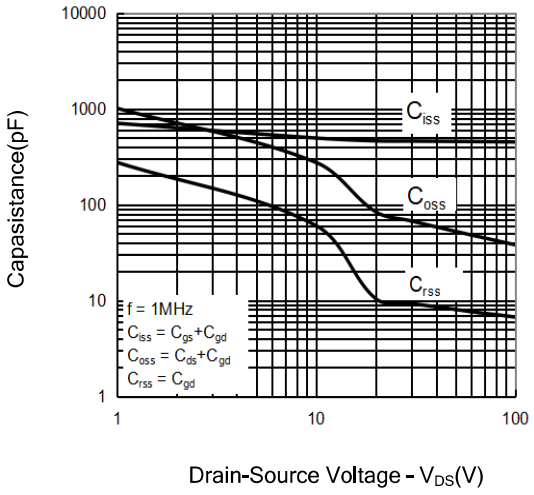
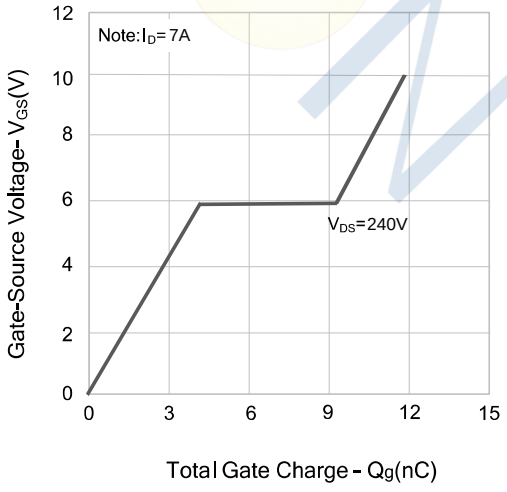


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics

Figure 7. Breakdown Voltage Variation vs. Temperature

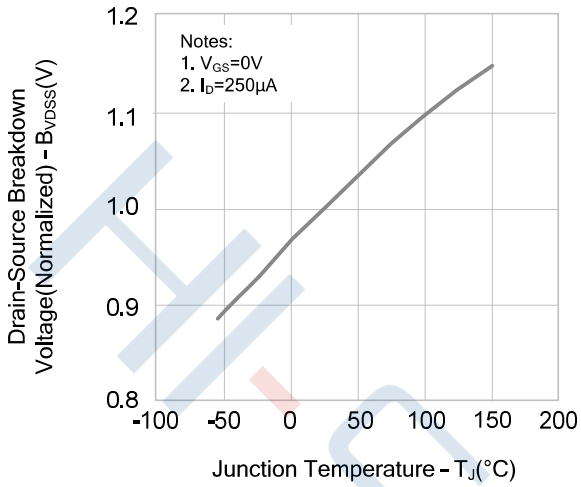


Figure 8. On-resistance Variation vs. Temperature

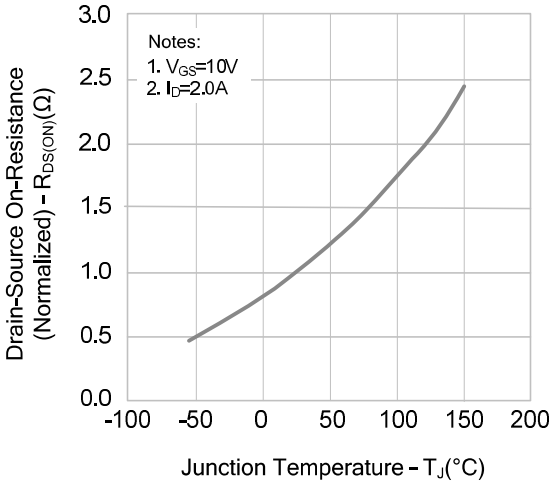


Figure 9 . Max. Safe Operating Area

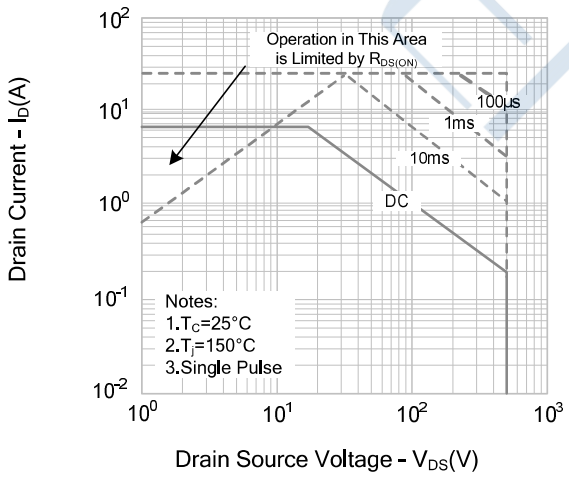
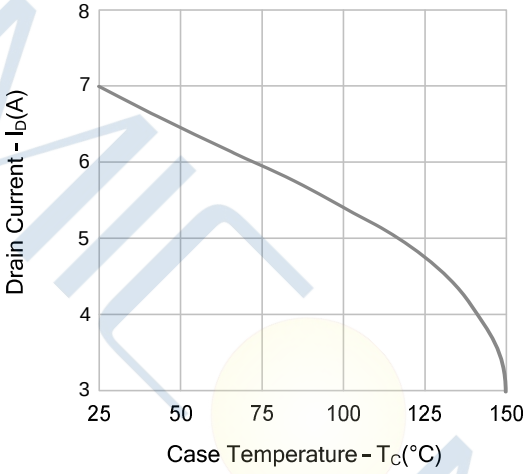
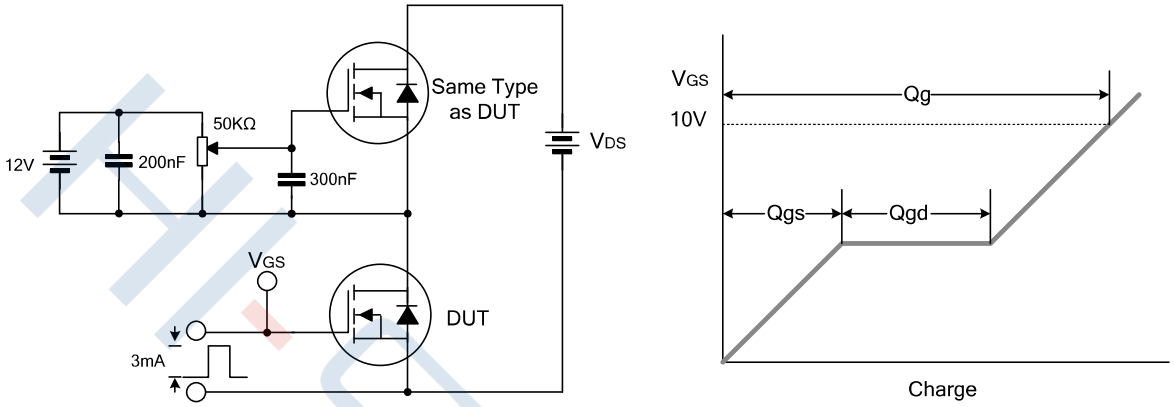


Figure 10. Maximum Drain Current vs. Case Temperature

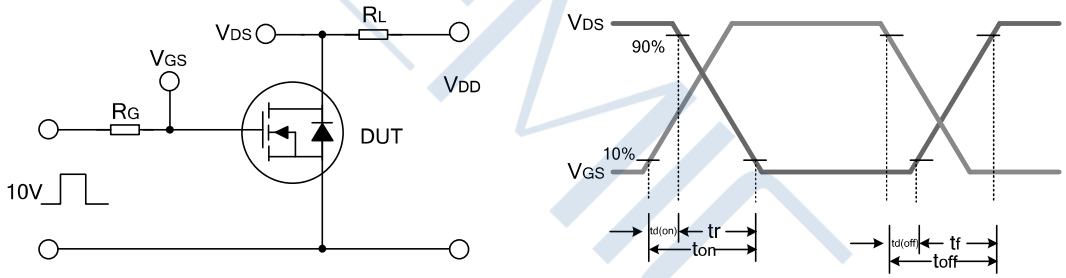


Test Circuit

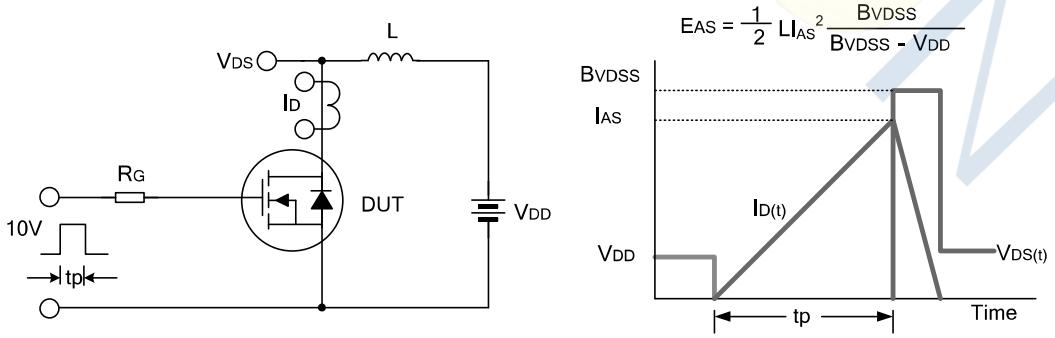
Gate Charge Test Circuit & Waveform



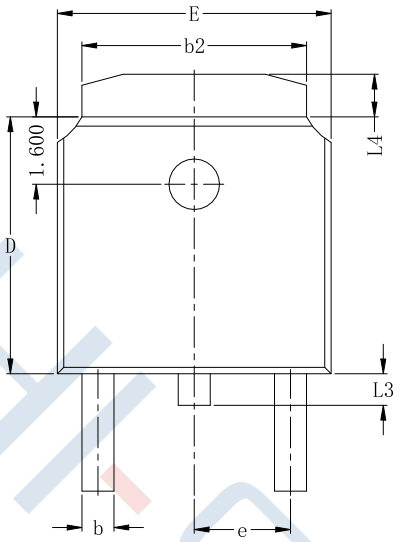
Resistive Switching Test Circuit & Waveform



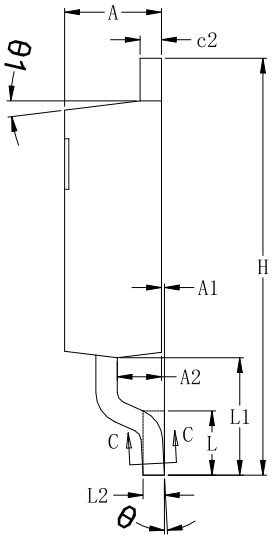
Unclamped Inductive Switching Test Circuit & Waveform



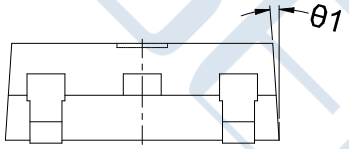
Package Dimensions of TO-252-2L



TOP VIEW



SIDE VIEW(Right)



SIDE VIEW(Front)

SYMBOL \ DIM	MIN.	NOM.	MAX.
A	2.200	2.300	2.400
A1	0.000	0.070	0.130
A2	0.950	1.050	1.150
b	0.700	0.800	0.900
b1	0.660	0.760	0.860
b2	5.134	5.334	5.534
c	0.448	0.548	0.648
c1	0.458	0.508	0.558
c2	0.448	0.548	0.648
D	6.000	6.100	6.200
D2	5.372	5.572	5.772
E	6.400	6.500	6.600
E2	4.900	5.100	5.300
e	2.286 BSC.		
H	9.700	9.900	10.100
L	1.380	1.525	1.725
L1	2.588	2.788	2.988
L2	0.508 BSC.		
L3	0.600	0.750	0.950
L4	0.812	1.012	1.212
θ	1°	3°	5°
θ1	6°	7°	8°

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