super-PFC/PSR™ Controller for LED Lighting

FEATURES

- ***super*-PFC/PSR™ Control Supports Both Primary Side Regulation (PSR) and Secondary Side Regulation (SSR)**
- **Pin Compatible with Popular PFC Controllers**
- **THD<10% using *min*-THD™ Technique**
- **Built-in AC Line and Load Compensation for High Precision LED Output Current**
- **Highly Linear Analog Multiplier with "Frequency Adjusting" for High PF**
- **Max. 90KHz Frequency Clamping for EMI**
- **LED Open/Short Protection**
- **Burst Mode Control @ Light Loading**
- **Trimmed 1.5% Internal Voltage Reference**
- **Very Low Startup Current**
- **Under Voltage Lockout with 8V Hysteresis**
- **Built-in Soft Start**
- **Clear External EA Feedback Network before Power On**
- **Cycle-by-Cycle Current Limiting**
- **Built-in Leading Edge Blanking (LEB)**
- **VCC Over Voltage Protection (OVP)**
- **Audio Noise Free Operation**
- **10V to 32V Wide Range of VCC Voltage**
- **500mA Drive Capability**

APPLICATIONS

- **LED Lighting Application**
- **Single Stage High PF Flyback AC/DC SMPS**

GENERAL DESCRIPTION

SFL900 is a high performance, high power factor flyback PWM controller special for LED lighting applications. The IC adopts unique ***super*-PFC/PSR™** which can support both PSR and SSR applications.

SFL900 is pin compatible with mainstream PFC controllers such as XX6561/6562, XX7527, etc. SFL900 also integrates proprietary ***min*-THD™**, technique, which can achieve less than 10% THD for universal line input.

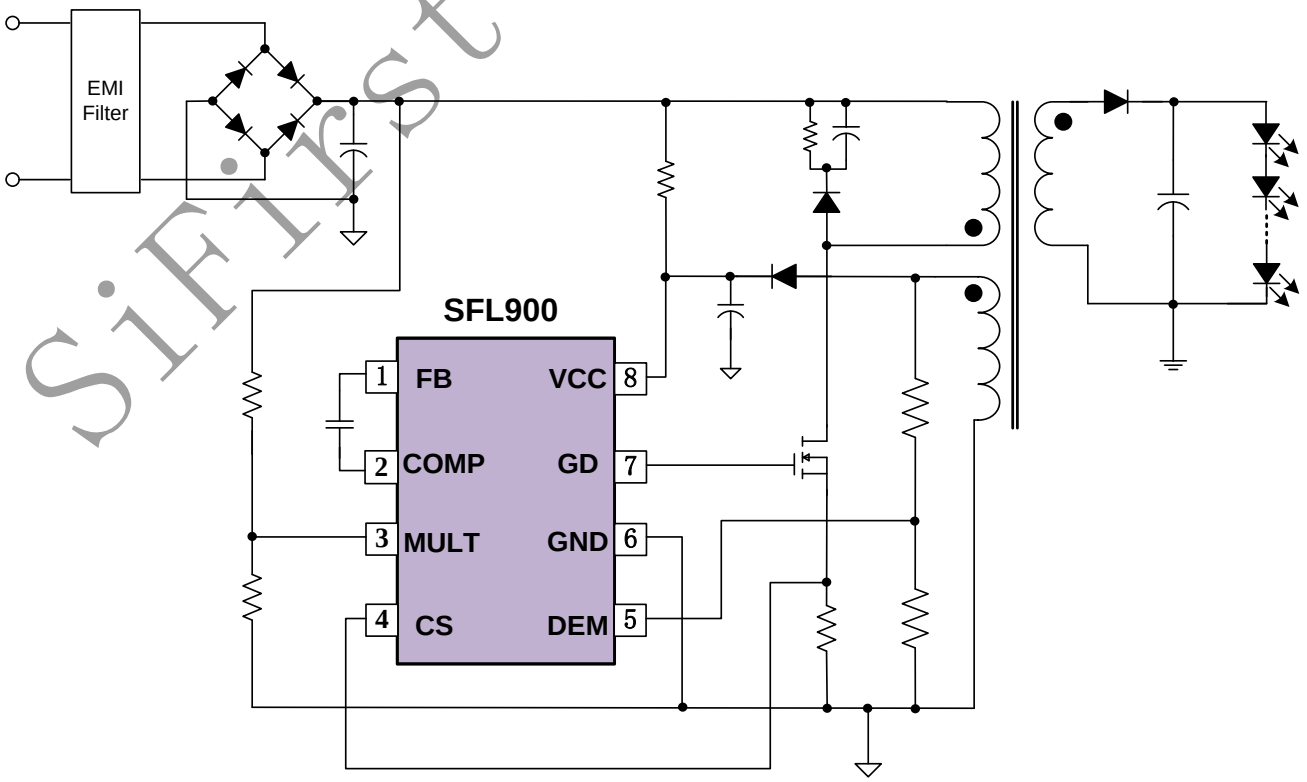
SFL900 has built-in ***Load CC Compensation*** and ***AC Line CC Compensation*** function, which can further increase LED output CC accuracy. The IC has Max. 90KHz Frequency Clamping function and soft totem pole Gate driver to improve system conduction and radiation EMI. The IC will Clear External EA Feedback Network before IC power on, which can reduces startup LED current spike. The IC also has Soft Start control during power on period.

In SFL900, the proprietary "Frequency Adjusting" can help to improve THD performance, while ensures audio noise free operation.

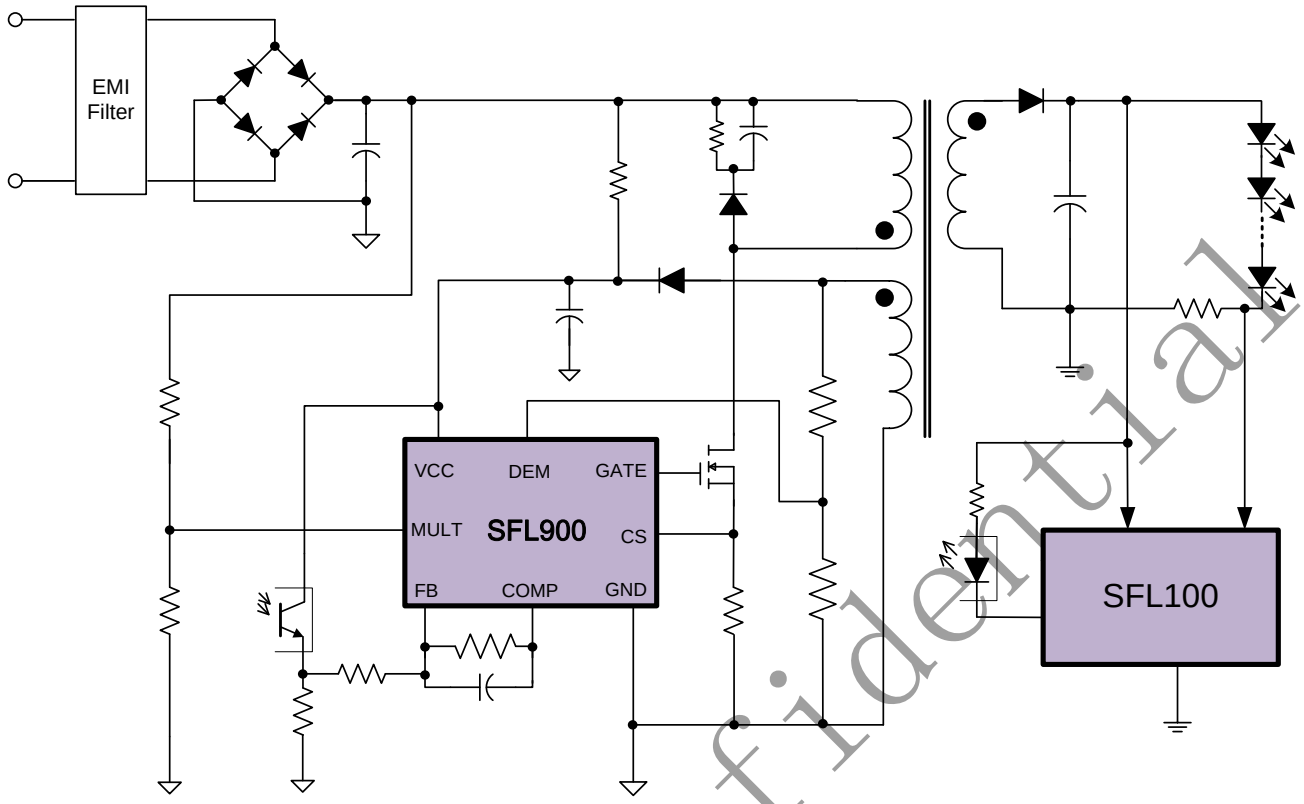
SFL900 integrates functions and protections of Under Voltage Lockout (UVLO), LED Open/Short Protection, VCC Over Voltage Protection (OVP), Load Over Voltage Protection (Load OVP), Soft Start, Cycle-by-cycle Current Limiting (OCP), Burst Mode Control @ Light Loading, GD Clamping, VCC Clamping, etc.

SFL900 is available in SOP-8 and DIP-8 packages.

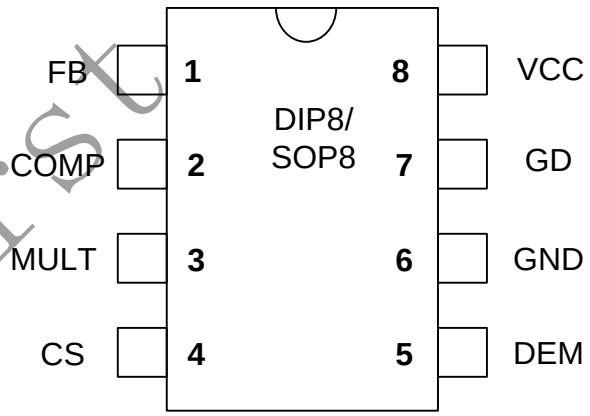
TYPICAL APPLICATION (PSR Application)



TYPICAL APPLICATION (SSR Application)



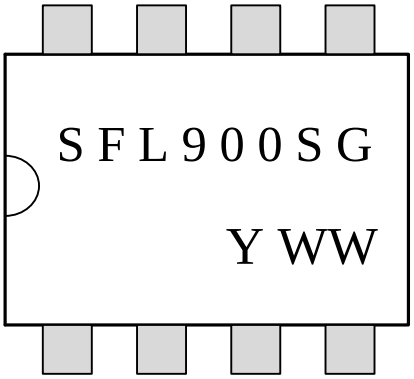
Pin Configuration



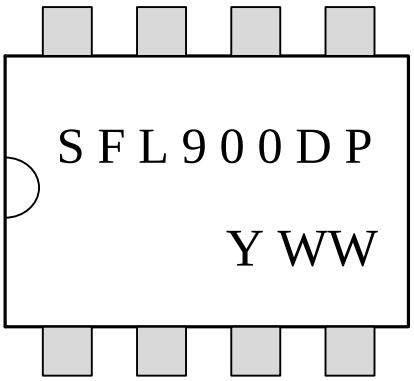
Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SFL900SG	SFL900SG	SOP8	Green	
SFL900SGT	SFL900SG	SOP8	Green	Yes
SFL900DP	SFL900DP	DIP8	RoHS	

Marking Information



YWW: Year&Week code

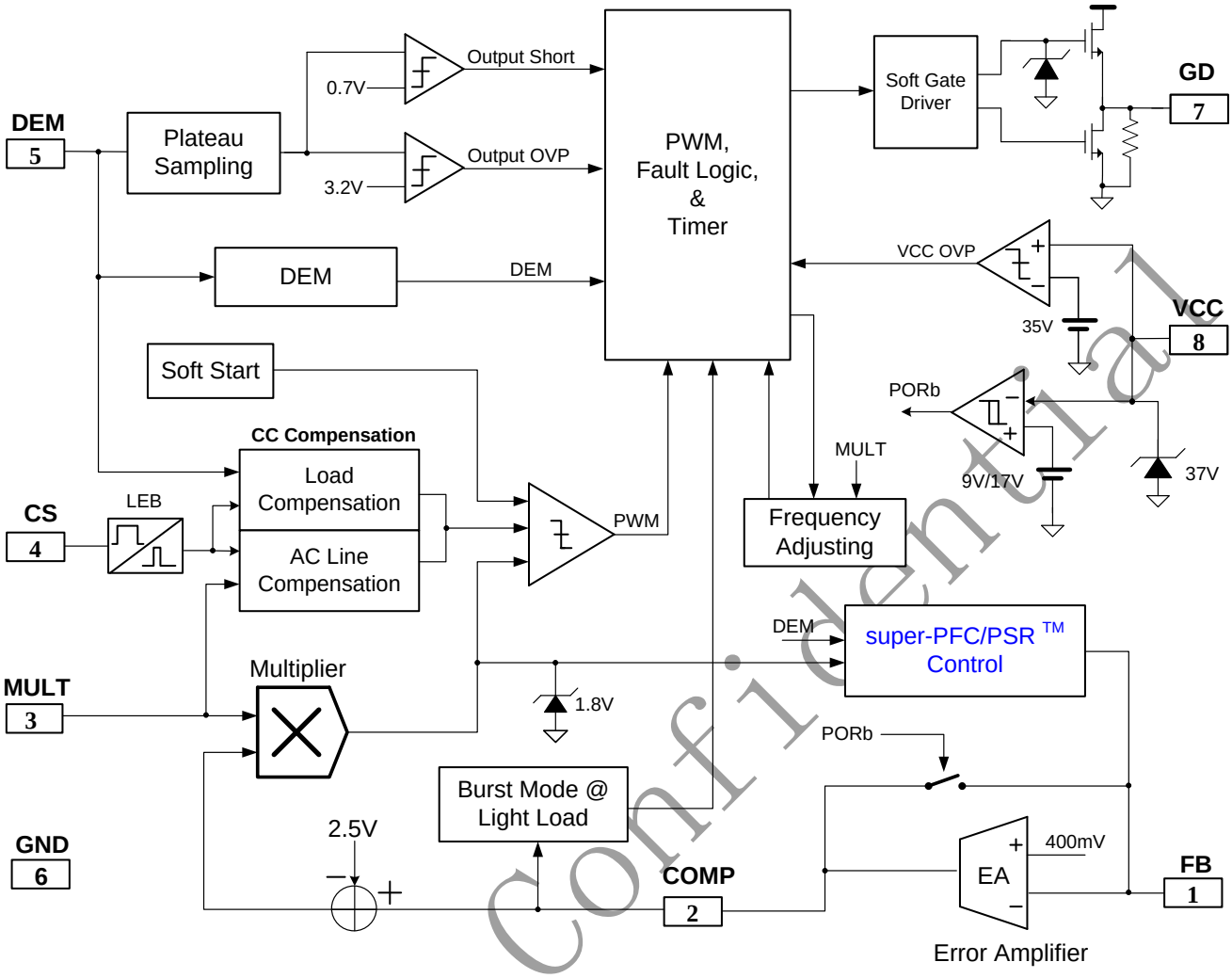


YWW: Year&Week code

Pin Description

Pin Num	Pin Name	I/O	Description
1	FB	I	Inverting input of the error amplifier. Before power on, this pin is internally shorted to COMP pin to clear external feedback network.
2	COMP	O	Output of the error amplifier. A feedback network is placed between this pin and pin 1. In PSR application, the feedback network can be a capacitor. The voltage of COMP and pin CS generates PWM duty cycle.
3	MULT	I	Input to the multiplier stage. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	I	Current sense input pin.
5	DEM	I	Demagnetization detection input from auxiliary winding for ***super-PFC/PSR™*** control. This pin is also used for output over voltage protection and output short circuit protection.
6	GND	P	IC ground pin.
7	GD	O	Totem-pole gate driver output to drive the external MOSFET.
8	VCC	P	IC power supply pin.

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VCC DC Supply Voltage	37	V
VCC DC Clamp Current	10	mA
GD pin	20	V
FB, COMP, MULT, CS, voltage range	-0.3 to 7	V
DEM Pin Max. Sink/Source Current	50(source) /10(sink)	mA
Package Thermal Resistance (DIP-8)	90	°C/W
Package Thermal Resistance (SOP-8)	150	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VCC	10 to 32	V
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS

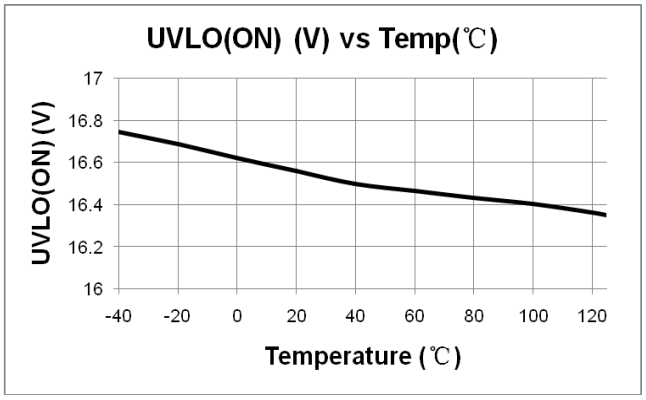
(T_A = 25°C, VCC=18V if not otherwise noted)

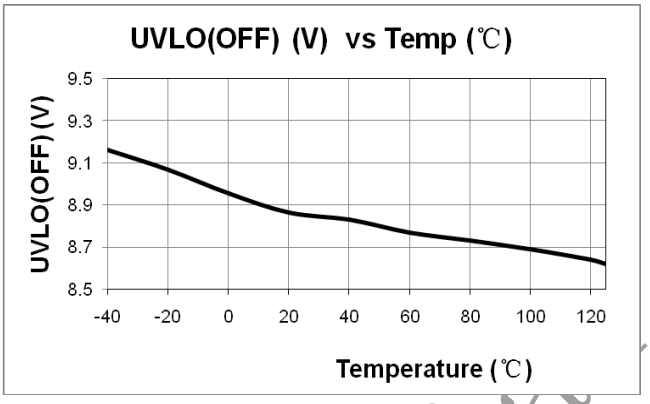
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VCC Pin)						
Ivcc_Startup	VCC Start up Current	VCC=15.5V, Measure current into VCC		5	15	uA
UVLO(ON)	VCC Under Voltage Lockout Exit (Startup)		16	17	18	V
UVLO(OFF)	VCC Under Voltage Lockout Enter		8.0	9	10	V
UVLO(Hys)	UVLO Hysteresis	UVLO(ON)-UVLO(OFF)		8		V
VCC_OVP	VCC Over Voltage Protection trigger		33	35	37	V
VCC_Clamp	VCC Zener Clamp Voltage	I(VCC) = 5mA	35	37	39	V
I_VCC_Op	Operation Current	@70KHz, GD=1nF		4	5.5	mA
I_VCC_quiet	Quiescent Current	No Switching		3	4	mA
T_Softstart	Soft Start Time			8		mSec
Error Amplifier Section (FB and COMP Pin)						
V_{FBREF}	Voltage Feedback Input Threshold		494	400	406	mV
ΔV_{FB_line}	Line Regulation	10V<VCC<32V		1	2	mV
ΔV_{FB_Temp}	Temperature Stability	-40°C <T_A <125°C		1		mV
G_V	Voltage Gain	Note 3	60	80		dB
GBW	Unit Gain Bandwidth	Note 3		1.2		MHz
I_{COMP}_source	Source Current	V_{COMP}=3.6V, V_{FB}=2.4V	-2	-4.8	-10	mA
I_{COMP}_sink	Sink Current	V_{COMP}=3.6V, V_{FB}=2.6V	-2	-4.8		mA
V_{COMP}_Clamp_U	Upper Clamp Voltage	I_{COMP} (source)=0.5mA		5.4		V
V_{COMP}_min_duty	COMP under voltage gate clock is off			2.25		V
Multiplier Section (MULT Pin)						
Vmult	Linear Operating Range		0~3.5			V
K	Multiplier Gain	V_{MULT}=1V, V_{COMP}=3.5V	0.9	1.0	1.1	1/V
ΔVcs/ ΔVmult	Output Max. Slope	V_{MULT}=from 0 to 0.5V, V_{COMP}=Upper Clamp Voltage		1.8		V/V
Current Sense Section (CS Pin)						
V_{CS}_clamp	Current Sense Reference Clamp			1.8		V
T_blanking	CS Input Leading Edge Blanking Time			250		nSec
T_D_OC	Over Current Detection and Control Delay	GD=1nF		100		nSec
Demagnetization Detection Section (DEM Pin)						
V_{TH}_DEM	DEM Comparator Threshold Voltage (Negative going edge)			0.2		V
V_{TH}_DEM_hys	Hysteresis for DEM Comparator			0.1		V
V_{DEM}_clamp_H	High clamp voltage		5.4	6	6.6	V
V_{DEM}_clamp_L	Low clamp voltage	I(DEM)=-2.5mA		0		V
V_{TH}_OVP	Output over voltage protection threshold			3.2		V
N_{TRUE}_OVP	Number of subsequent cycles to be true OVP			2		Cycle
V_{TH}_Output_short	Output Short Circuit Protection Threshold			0.7		V

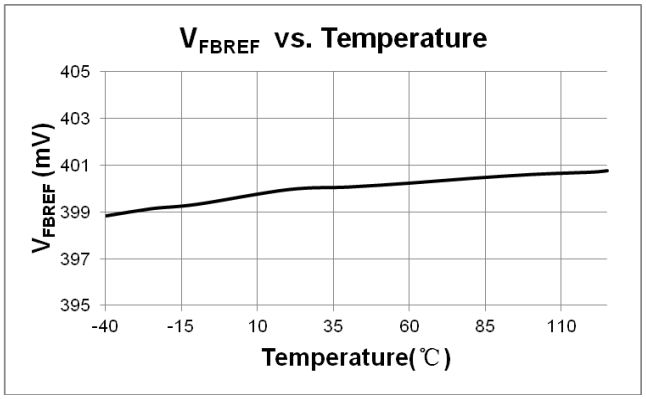
T_{min}_OFF	Minimum OFF time	Note 3		3.4		uSec
I_{DEM}_source	Source Current Capability		-2.5		-5	mA
I_{DEM}_sink	Sink Current Capability	Note 3	3			mA
Starter and Max Switching Frequency Limitation Section						
T_{start}	Start Timer Period		45	55	65	us
f_{sw}_max	Max switching frequency			90		KHz
Gate Drive Section (GD Pin)						
VOL	Output Low Level	Io = 20 mA (sink)			0.5	V
VOH	Output High Level	Io = 20 mA (source)	12			V
GD_Clamp	Output Clamp Voltage Level	VCC=24V		16		V
T_r	Output Rising Time	GD = 1nF		80		nSec
T_f	Output Falling Time	GD = 1nF		50		nSec

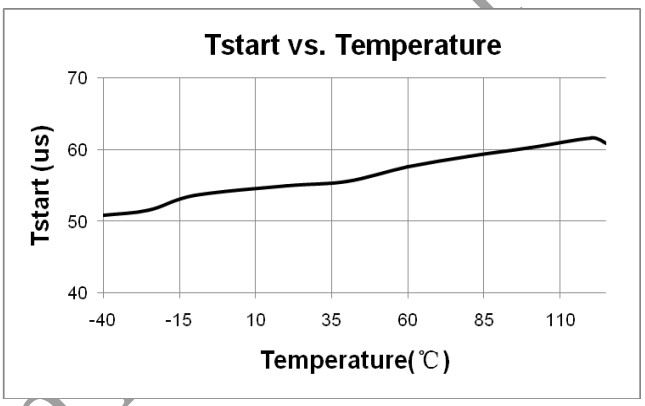
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2. The device is not guaranteed to function outside its operating conditions.
Note 3. Guaranteed by design.

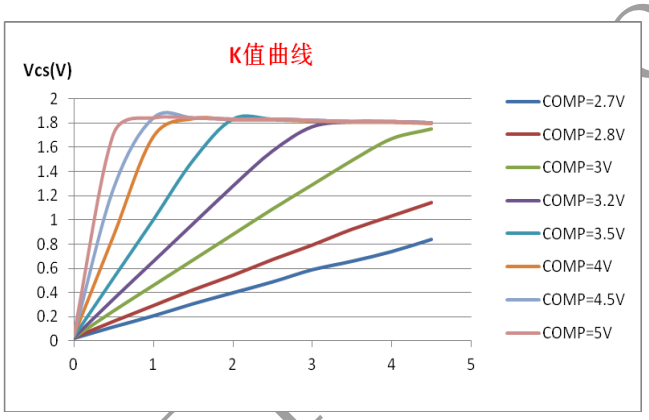
CHARACTERIZATION PLOTS

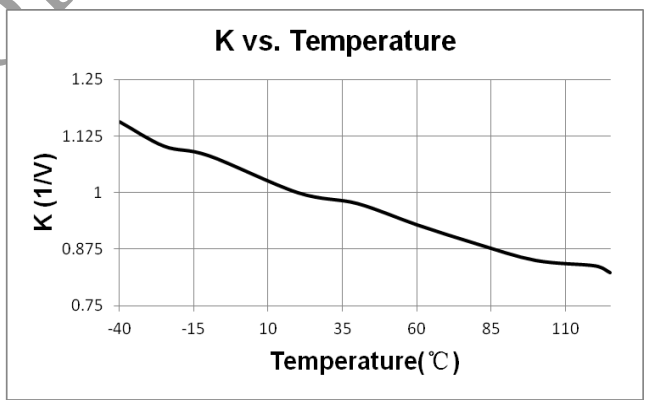


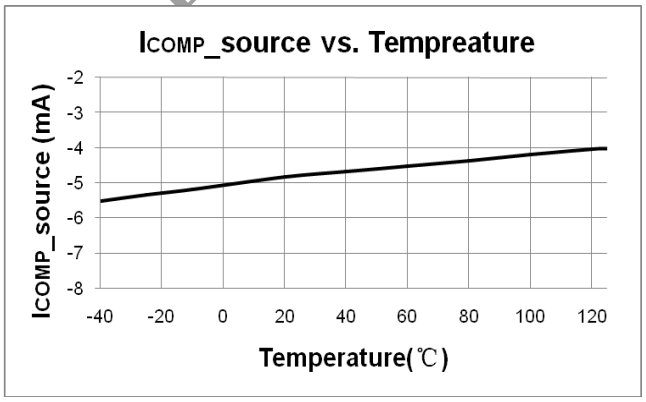


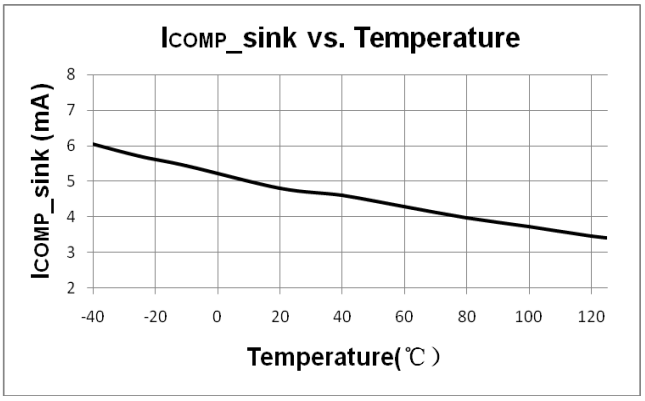












OPERATION DESCRIPTION

SFL900 is a high performance, high power factor flyback PWM controller special for LED lighting applications. The IC adopts unique ***super*-PFC/PSR™** which can support both PSR and SSR applications.

◆ *super*-PFC/PSR™ Support Both Primary Side Regulation (PSR) and Secondary Side Regulation (SSR)

PSR topology requires no secondary feedback circuit (such as TL431, photo-coupler, etc), which reduces system cost greatly. SSR can achieve high accuracy CC (constant current) and CV (constant voltage) performance. Therefore, in small power applications, PSR is the popular topology, while SSR is superior topology in large power applications.

In SFL900, a proprietary ***super*-PFC/PSR™** is adopted, which can support PSR (primary side regulation) and SSR (Secondary side regulation) simultaneously.

◆ *min*-THD™ to Achieve Less than 10% THD Performance for Universal Input

In SFL900, a proprietary ***min*-THD™** technique is built in to improve system THD performance. In general, less then 10% system THD can be achieved.

◆ LED Constant Current (CC) Regulation in PSR Application

When used in primary side regulation occasion, SFL900 can accurately control the LED current by the current feedback control loop. The LED mean current can be approximately expressed as:

$$I_{LED}(mA) = \frac{N}{2} \times \frac{400(mV)}{Rcs(\Omega)}$$

In the equation above,

N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the MOSFET source to GND.

◆ UVLO (with 8V Hysteresis) and 5uA Startup Current

Fig.1 shows a typical startup circuit. Before the IC begins switching operation, it consumes only startup current (typically 5uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 17V(typical), SFL900 begins switching and the IC current consumed increased to 3mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.

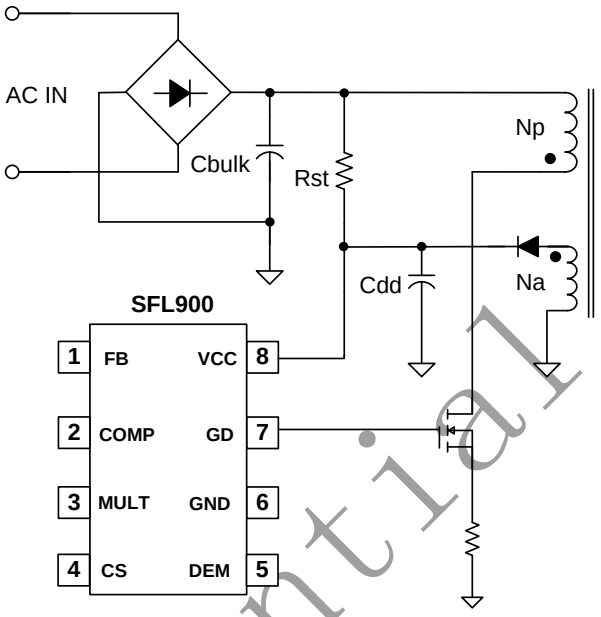


Fig.1

◆ Low Operating Current

The operating current in SFL900 is as small as 3mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ Error Amplifier (EA)

The inverting input of the EA is compared to an internal reference voltage (400mV,internally trimmed with 1.5% precision) to regulate LED output current. An external loop compensation network is placed between COMP and FB.

When COMP voltage is below 2.25V, PWM cycle will stop.

◆ Burst Mode Control @ Light Loading

When the loading is very small, the system enters into burst mode. When VCOMP drops below 2.3V(typical), SFL900 will stop switching and output voltage starts to drop, which causes the VCOMP to rise. Once VFB rises above 2.3V, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

◆ Clear External EA Feedback Network

SFL900 features a control that clear the external EA feedback network before IC power on, as shown in Fig.2. This control can ensure the system start up softly by clearing the residue voltage on C1 and reduce the output LED current spike when system does the ON/OFF testing.

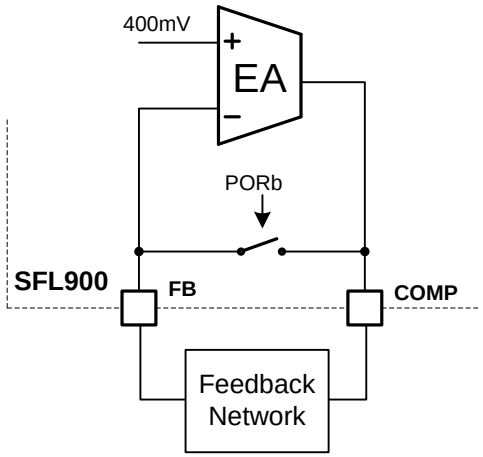


Fig.2

◆ Analog Multiplier for Power Factor Correction

The analog multiplier output limits the MOSFET peak current with respect to the AC half wave rectified input voltage. The multiplier in SFL900 has two inputs. One is the error amplifier (EA) output voltage (V_{COMP}), while the other is V_{MULT} which is obtained by a resistor divider from the rectified line. The multiplier output can be expressed as the following equation:

$$V_{Multiplier} = 1.0 \times V_{MULT} \times (V_{COMP} - 2.5V)$$

The analog multiplier in SFL900 is specially designed to achieve high linearity over a wide dynamic range. The multiplier output is clamped to 1.8V internally.

◆ Frequency Adjusting

In SFL900, a proprietary function of "Frequency adjusting" is integrated. By setting a low frequency clamp which tracks the variation of the AC half wave rectified input voltage, the PFC THD performance can be improved, as shown in Fig.3.

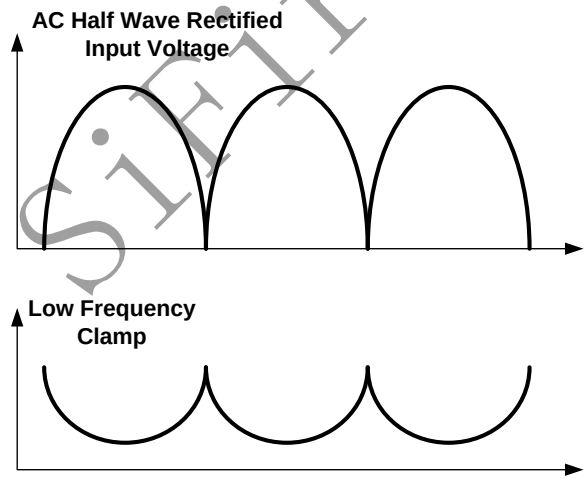


Fig.3

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the current limiting comparator is disabled and cannot switch off the gate driver. Thus, conventional RC filtering is not necessary and the propagation delay of current limit protection can be minimized.

◆ Soft Start

SFL900 features an internal 8ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

◆ 3.3us Minimum OFF Time

In SFL900, a minimum OFF time (typically 3.3us) is implemented to suppress ringing when GATE is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup.

◆ 90KHz Maximum Frequency Clamping for EMI

In SFL900, the maximum system switching frequency is clamped to 90KHz, which can improve system conduction EMI performance. Therefore, SFL900 is actual a mixed control of TM (Transition Mode, or Boundary Conduction Mode) mode and DCM (Discontinuous Conduction Mode) mode. .

◆ Demagnetization Detection

SFL900 can perform demagnetization detection by using an auxiliary winding of the inductor. When the stored energy is fully released to the output, the voltage on DEM goes down. If DEM pin voltage drops below 0.2V, an internal DEM comparator is triggered and a new switching cycle is initiated following the DEM triggering. The power MOSFET is always turned on with zero inductor current such that the turn-on loss and noise can be minimized.
An internal restart timer (55us, typical) is built in to ensure proper start up operation.
The maximum and minimum voltage of DEM pin is internally clamped to 5.8V and 0V respectively.

◆ Built-in Load and AC Line CC Compensation

In conventional PSR system, the output CC (Constant Current) point can vary with output and AC line voltage. In SFL900, the IC has built-in blocks to compensate the variation, as shown in Fig.4. The IC can adjust CC point based on sensed output voltage and AC line input voltage. In this way, CC accuracy can be improved.

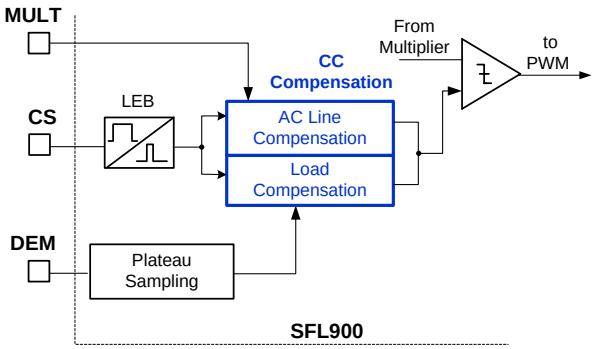


Fig.4

Typically, extra external CC compensation circuits are no needed. If a more précised CC point is needed, conventional external compensation network can be added.

◆ Output Over Voltage Protection (Output OVP) / LED String Open Protection

In SFL900, the output OVP is integrated by plateau sampling the auxiliary winding in flyback phase. The threshold voltage for output OVP is 3.2V, as shown in Fig.5.

If the sampled plateau voltage exceeds the OVP threshold (3.2V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 2 cycles, the controller assumes a true OVP and it stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP threshold less than 2 successive cycles, the internal counter will be cleared and no fault is asserted.

Output OVP is auto-recovery mode protection (mentioned below).

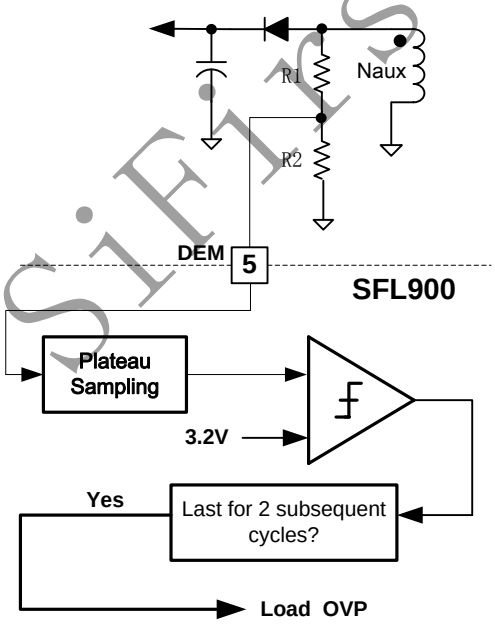


Fig.5

◆ Output Short Circuit Protection / LED String Short Protection

When the output short circuit happens, the positive plateau of auxiliary winding voltage is near zero and DEM voltage is low. If the voltage at DEM pin is lower than a threshold of 0.7V (typical) and lasts for more than 20ms, the IC will shut down and enter into auto-recovery mode protection (as mentioned below).

◆ Pins Floating Protection

In SFL900, if pin floating situation occurs, the IC is designed to have no damage to system.

◆ VCC OVP (Over Voltage Protection)

When VCC voltage is higher than 35V (typical), VCC OVP (Over Voltage Protection) will be triggered in SFL900 and it is a protection of auto recovery mode (as mentioned below).

◆ Auto Recovery Mode Protection

As shown in Fig.6, once a fault condition (VCC OVP) is detected, switching will stop. This will cause VCC to fall because no power is delivered form the auxiliary winding. When VCC falls to UVLO(OFF) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VCC to rise, as shown in Fig.6. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

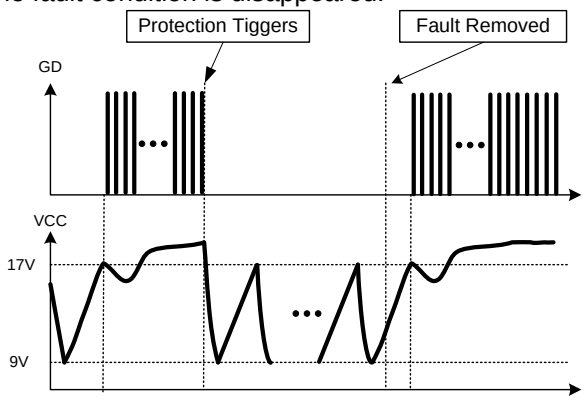


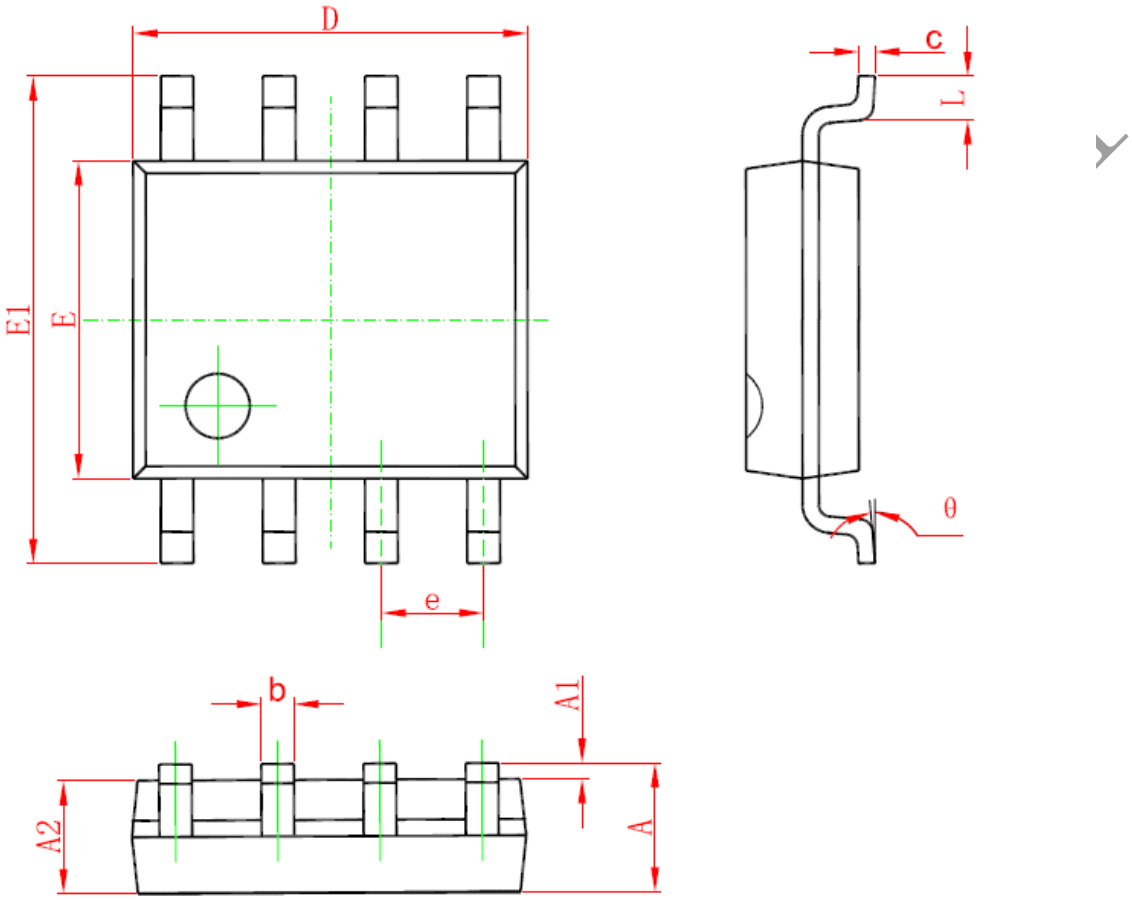
Fig.6

◆ Soft Gate Drive

SFL900 has a fast totem-pole gate driver with 500mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 16V clamp is added for MOSFET gate protection at higher than expected VCC input. A soft driving waveform is implemented to minimize EMI.

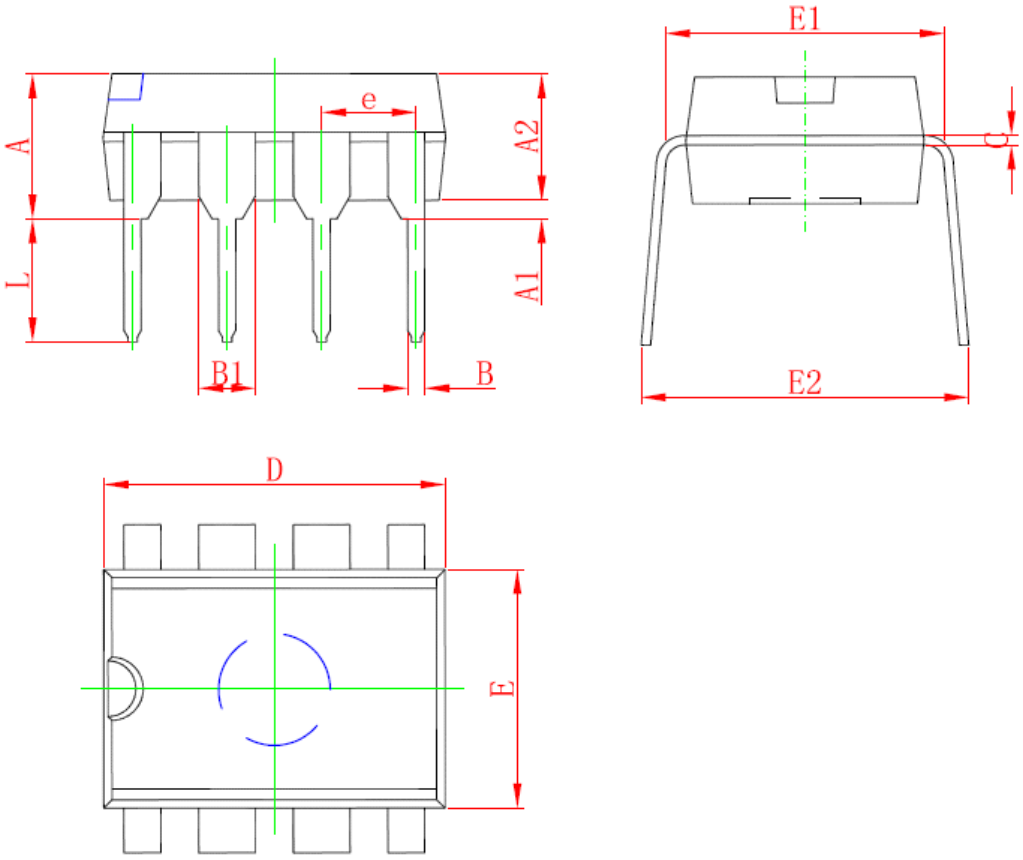
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.06 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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