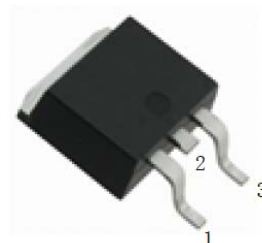
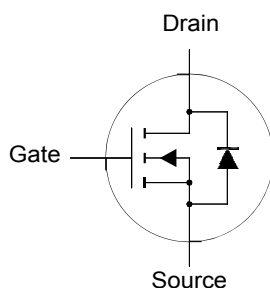


SFTN2922R

N-Channel Enhancement Mode MOSFET



1.Gate 2.Drain 3.Source
TO-252 Plastic Package

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$ 7 $T_C = 100^\circ\text{C}$ 5	A
Peak Drain Current ³⁾	I_{DM}	10	A
Power Dissipation ²⁾	P_D	$T_C = 25^\circ\text{C}$ 17 $T_C = 100^\circ\text{C}$ 8.5	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient ¹⁾ ($t \leq 10$ s)	$R_{\theta JA}$	25	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ¹⁾⁴⁾ (Steady-State)		50	$^\circ\text{C/W}$
Thermal Resistance from Junction to Case (Steady-State)	$R_{\theta JC}$	8.8	$^\circ\text{C/W}$

¹⁾ The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA} t \leq 10$ s and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

²⁾ The power dissipation P_D is based on $T_{J(MAX)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

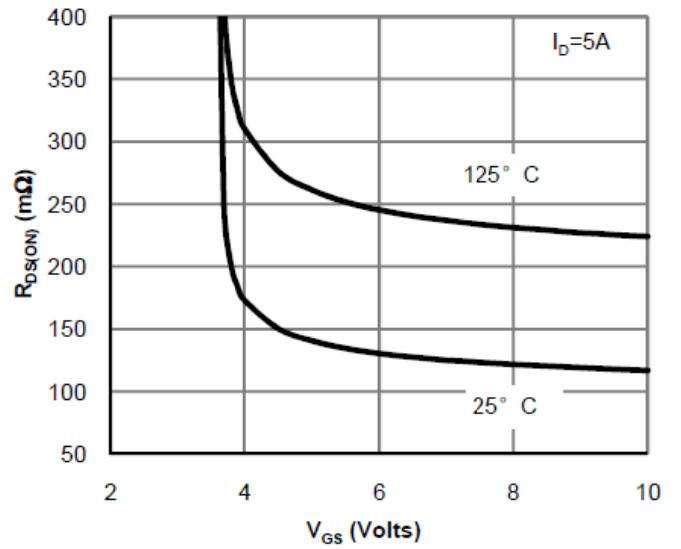
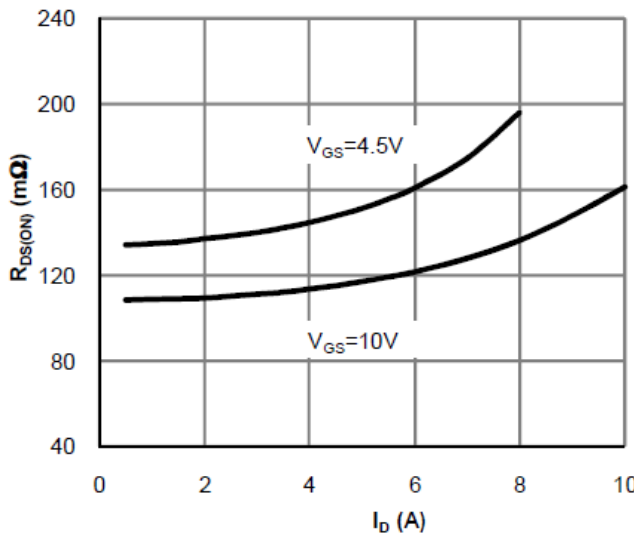
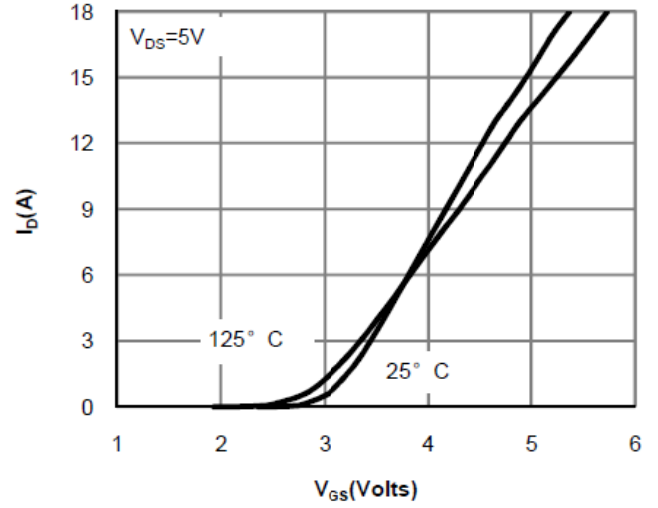
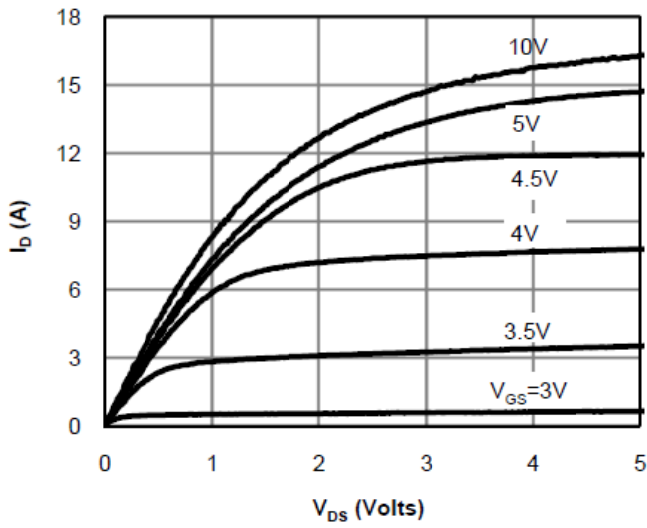
³⁾ Single pulse width limited by junction temperature $T_{J(MAX)} = 175^\circ\text{C}$.

⁴⁾ The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient

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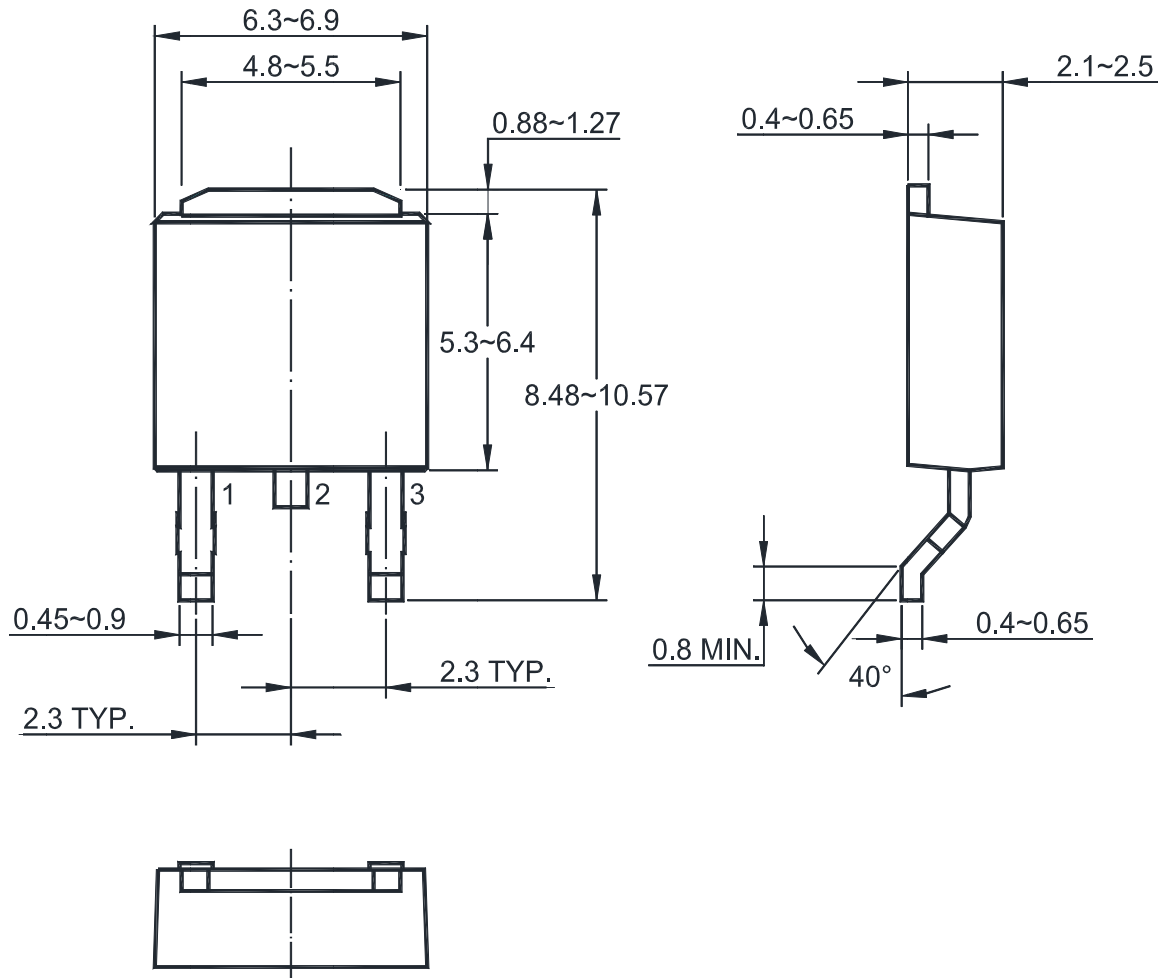
Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage at $I_D = 250 \mu\text{A}$	BV_{DSS}	100	-	-	V
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	$V_{GS(th)}$	1.7	-	2.7	V
Drain-Source Leakage Current at $V_{DS} = 100 \text{ V}$ at $V_{DS} = 100 \text{ V}$, $T_J = 55^\circ\text{C}$	I_{DSS}	- -	- -	1 5	μA
Gate Leakage Current at $V_{GS} = \pm 20 \text{ V}$	I_{GSS}	-	-	± 100	nA
Drain-Source On-State Resistance at $V_{GS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$ at $V_{GS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$, $T_J = 125^\circ\text{C}$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 3 \text{ A}$	$R_{DS(on)}$	- - -	- - -	140 270 176	m Ω
Diode Forward Voltage at $I_S = 1 \text{ A}$, $V_{GS} = 0 \text{ V}$	V_{SD}	-	-	1.1	V
Input Capacitance at $V_{GS} = 0 \text{ V}$, $V_{DS} = 50 \text{ V}$, $f = 1 \text{ MHz}$	C_{oss}	-	-	310	pF
Output Capacitance at $V_{GS} = 0 \text{ V}$, $V_{DS} = 50 \text{ V}$, $f = 1 \text{ MHz}$	C_{oss}	-	-	30	pF
Reverse Transfer Capacitance at $V_{GS} = 0 \text{ V}$, $V_{DS} = 50 \text{ V}$, $f = 1 \text{ MHz}$	C_{rss}	-	-	8	pF
Turn-On Delay Time at $V_{DS} = 50 \text{ V}$, $R_G = 3 \Omega$, $R_L = 10 \Omega$, $V_{GS} = 10 \text{ V}$	t_{on}	-	5	-	ns
Turn-On Rise Time at $V_{DS} = 50 \text{ V}$, $R_G = 3 \Omega$, $R_L = 10 \Omega$, $V_{GS} = 10 \text{ V}$	t_r	-	3	-	ns
Turn-Off Delay Time at $V_{DS} = 50 \text{ V}$, $R_G = 3 \Omega$, $R_L = 10 \Omega$, $V_{GS} = 10 \text{ V}$	t_{off}	-	19	-	ns
Turn-Off Fall Time at $V_{DS} = 50 \text{ V}$, $R_G = 3 \Omega$, $R_L = 10 \Omega$, $V_{GS} = 10 \text{ V}$	t_f	-	5	-	ns



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TO-252 PACKAGE OUTLINE



Recommended Soldering Footprint

