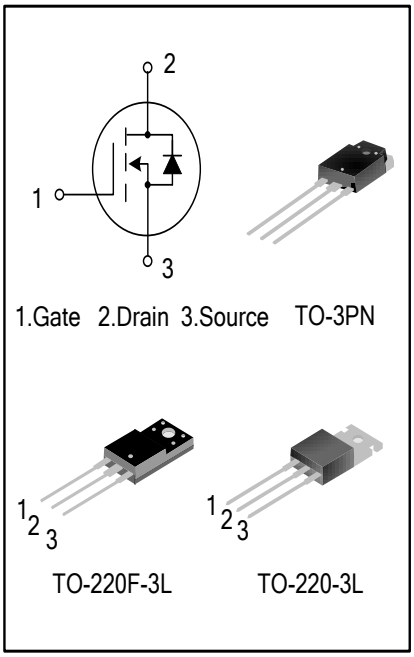
18A, 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are produced using Hi-semicon's proprietary, planar stripe DMOS technology.

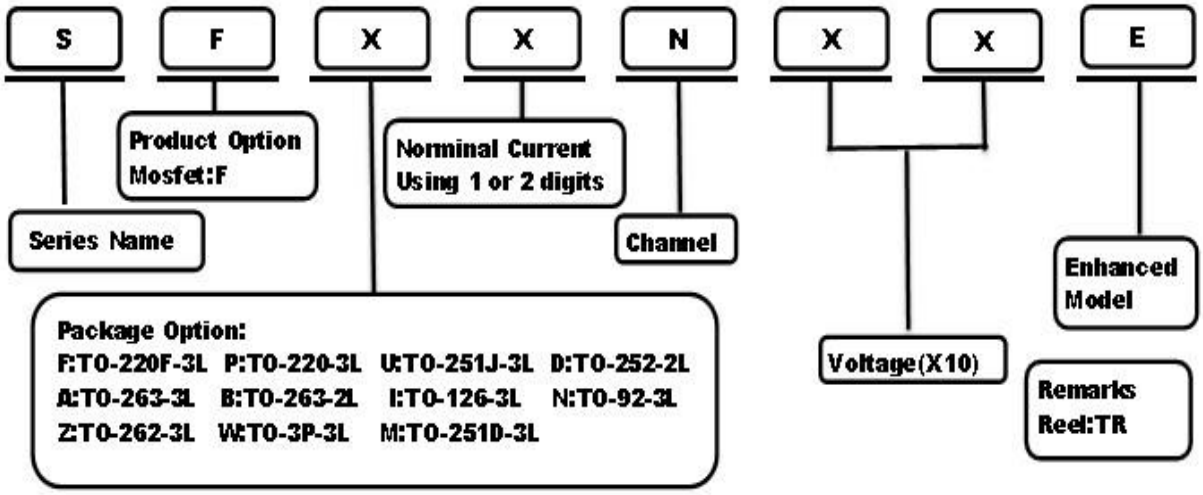
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies,active power factor correction,electronic lamp ballasts based on half bridge



FEATURES

- 18A,500V,$R_{DS(ON)(typ)}$=0.26Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFP18N50	TO-220-3L	SFP18N50	Pb free	Tube
SFF18N50	TO-220F-3L	SFF18N50	Pb free	Tube
SFW18N50	TO-3P	SFW18N50	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (TC=25°C unless otherwise noted)

Characteristics		Symbol	Rating			Unit
			SFF18N50	SFP18N50	SFW18N50	
Drain-Source Voltage		V_{DS}	500			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	18.0			A
	T_C=100°C		11.38			
Drain Current Pulsed		I_{DM}	72.0			A
Power Dissipation(T_C=25°C)		P_D	54	232	240	W
-Derate above 25°C			0.43	1.86	1.92	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	1502			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating			Unit
		SFF18N50	SFP18N50	SFW18N50	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.31	0.54	0.52	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	120	62.5	50	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=9.0A	--	0.26	0.31	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	2320	--	pF
Output Capacitance	C_{oss}		--	282	--	
Reverse Transfer Capacitance	C_{rss}		--	7.15	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=250V,I_D=18.0A, R_G=25Ω (Note 2,3)	--	60.0	--	ns
Turn-on Rise Time	t_r		--	131.3	--	
Turn-off Delay Time	$t_{d(off)}$		--	115.3	--	
Turn-off Fall Time	t_f		--	75.3	--	
Total Gate Charge	Q_g	V_{DS}=400V,I_D=18.0A, V_{GS}=10V (Note 2,3)	--	37.9	--	nC
Gate-Source Charge	Q_{gs}		--	12.44	--	
Gate-Drain Charge	Q_{gd}		--	12.05	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	18.0	A
Pulsed Source Current	I_{SM}		--	--	72.0	
Diode Forward Voltage	V_{SD}	I_S=18.0A,V_{GS}=0V	--	--	1.3	V
Reverse Recovery Time	T_{rr}	I_S=18.0A,V_{GS}=0V, dI_F/dt=100A/μs(Note 2)	--	582.93	--	ns
Reverse Recovery Charge	Q_{rr}		--	7.12	--	μC

Notes:

1. L=30mH, I_{AS}=8.60A,V_{DD}=140V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

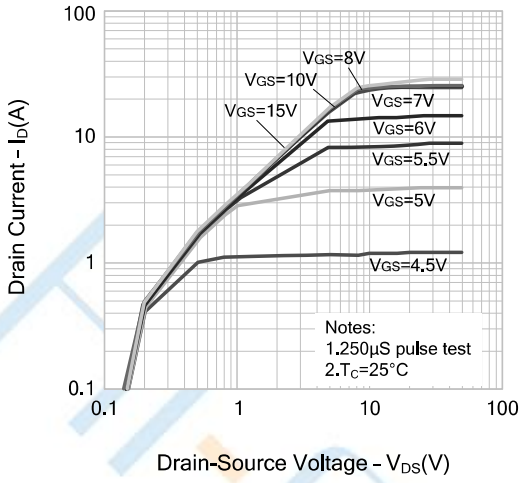


Figure 2. Transfer Characteristics

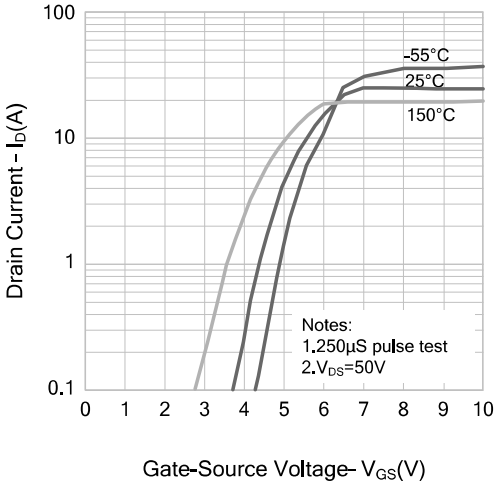


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

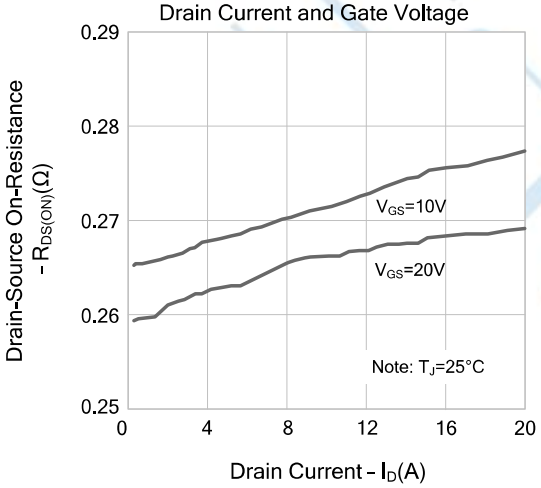


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

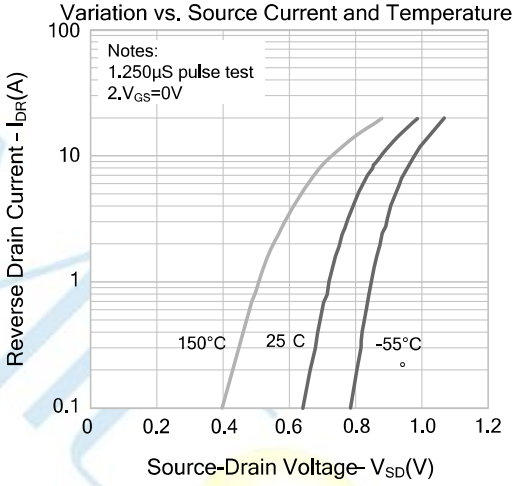


Figure 5. Capacitance Characteristics

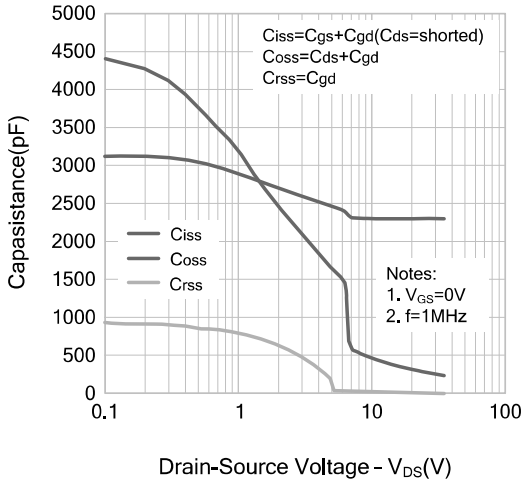
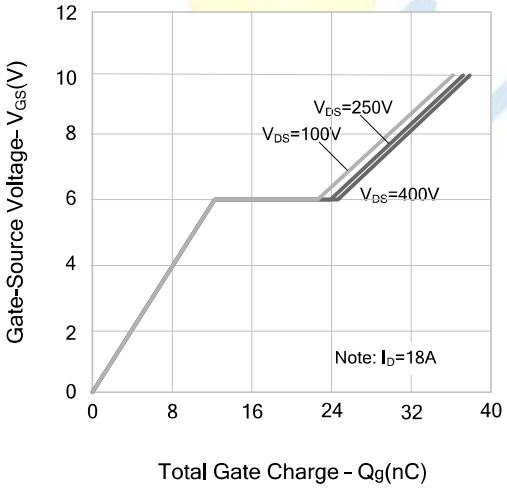


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

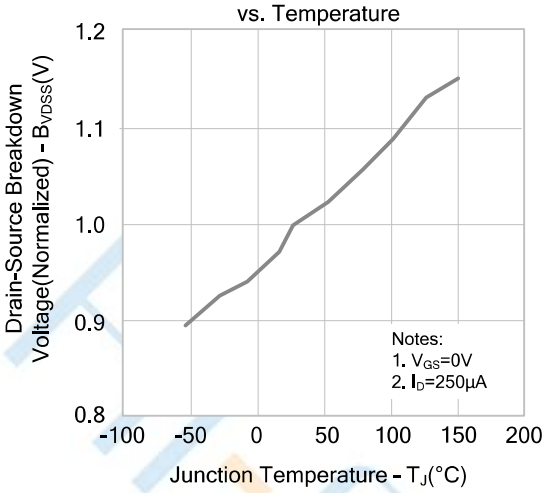


Figure 8. On-resistance Variation vs. Temperature

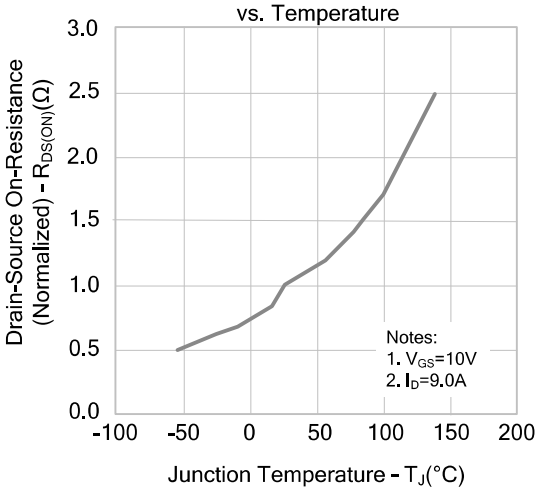


Figure 9-1. Max. Safe Operating Area(SFF18N50)

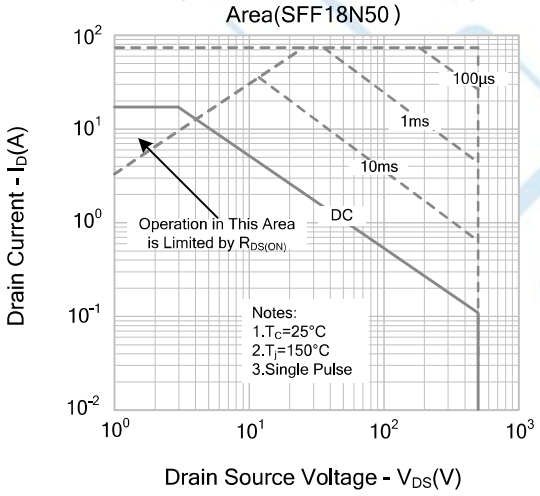


Figure 9-2. Max. Safe Operating Area(SFP18N50)

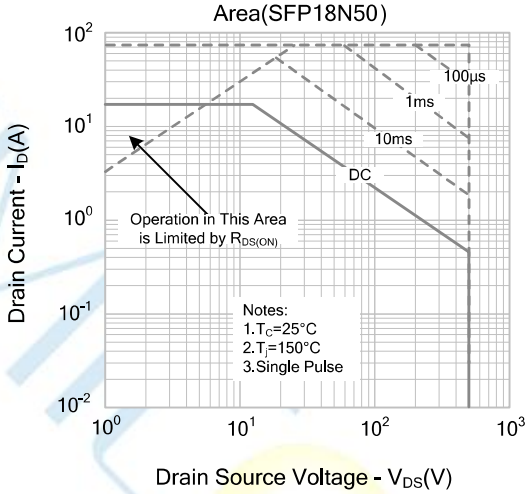


Figure 9-3. Max. Safe Operating Area(SFW18N50)

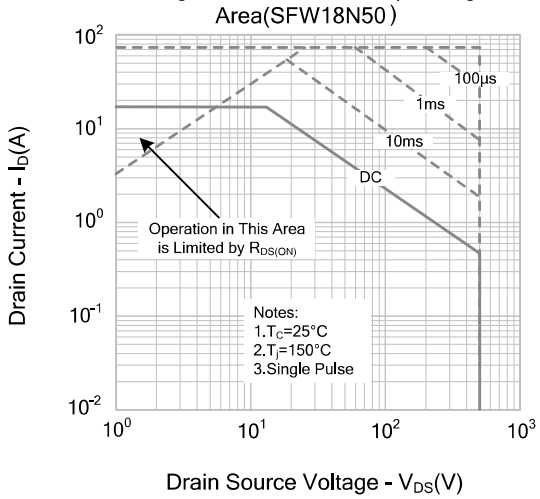
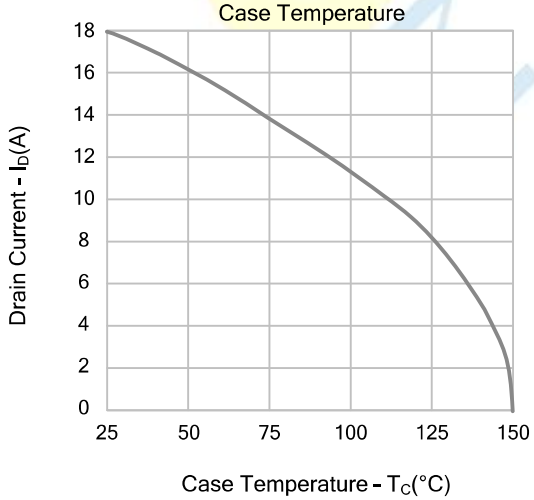
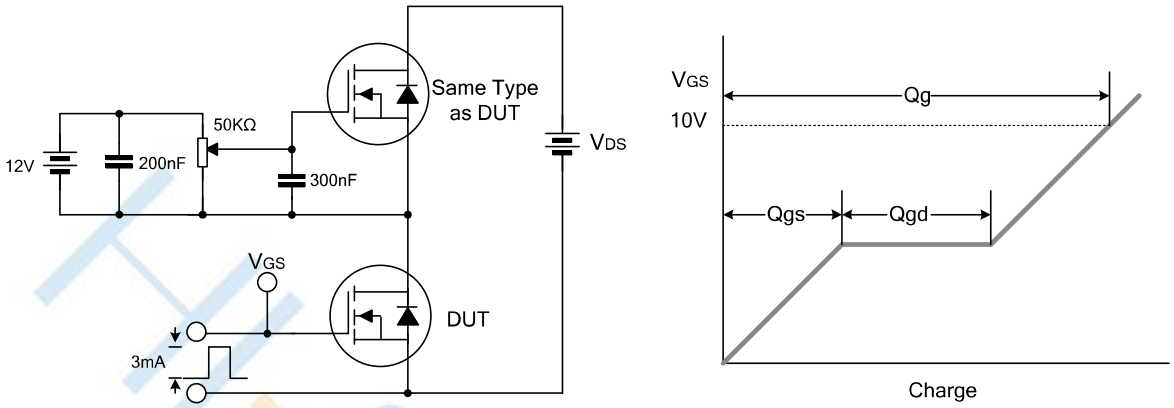


Figure 10. Maximum Drain Current vs. Case Temperature

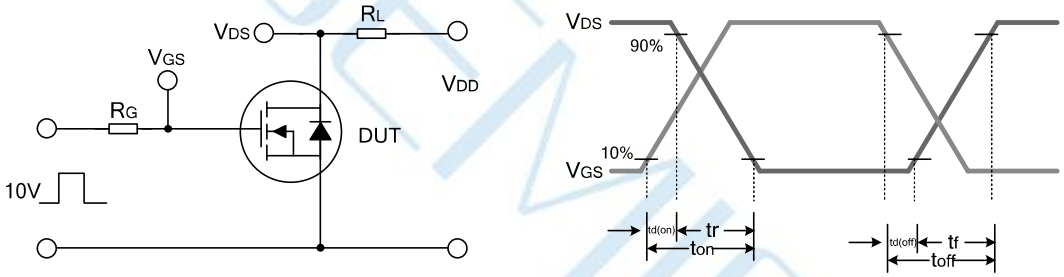


TYPICAL TEST CIRCUIT

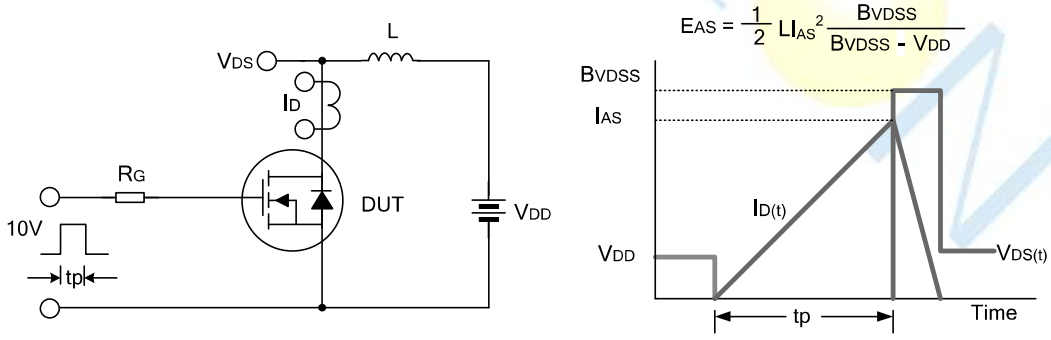
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

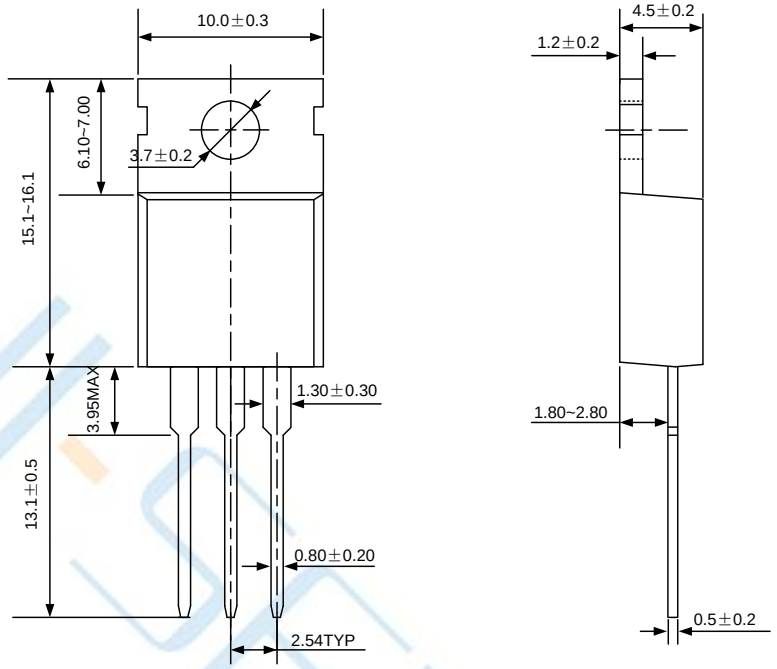


Unclamped Inductive Switching Test Circuit & Waveform

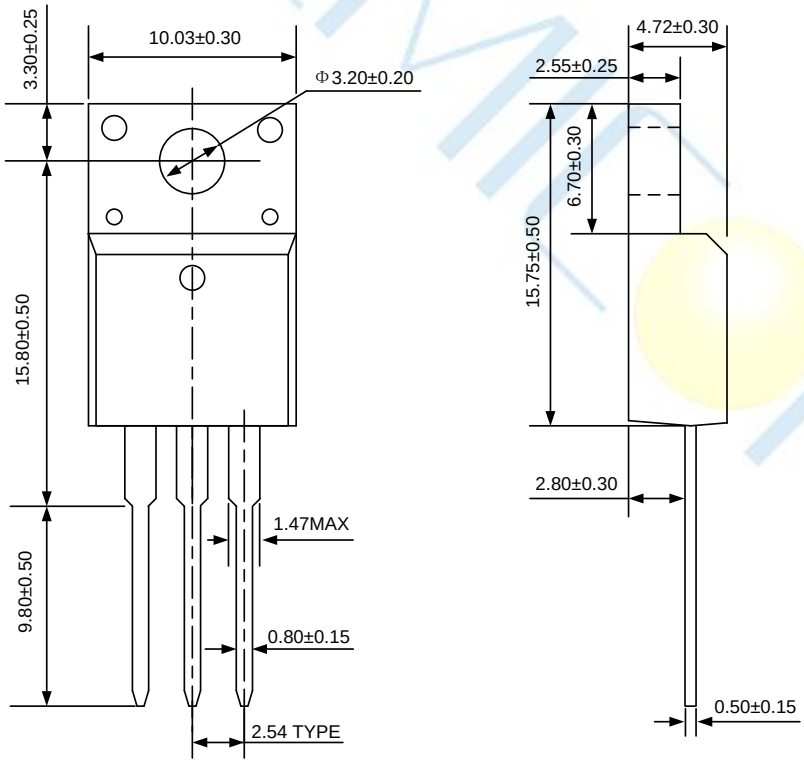


PACKAGE OUTLINE

TO-220-3L UNIT: mm



TO-220F-3L UNIT: mm



PACKAGE OUTLINE(continued)

TO-3PN UNIT: mm