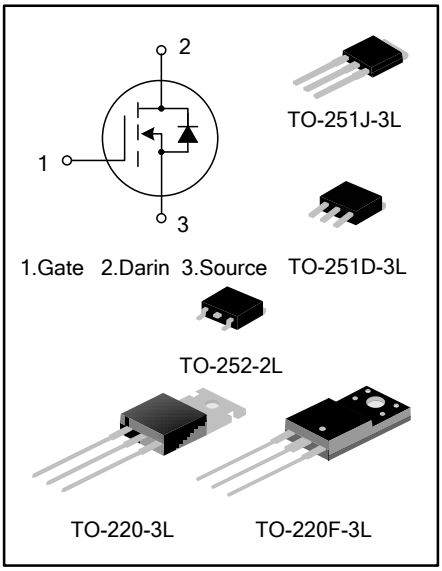
33A, 100V N-CHANNEL MOSFET

GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are produced using Hi-semicon's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies,active power factor correction, electronic lamp ballasts based on half bridge topology



FEATURES

- 33A,100V,$R_{DS(on)}$ (typ) =34mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFP33N10	TO-220-3L	SFP33N10	Pb free	Tube
SFF33N10	TO-220F-3L	SFF33N10	Pb free	Tube
SFD33N10TR	TO-252-2L	SFD33N10	Pb free	Tape & Reel
SFD33N10	TO-252-2L	SFD33N10	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (TC=25°C unless otherwise noted)

Characteristics		Symbol	Rating		Unit
			SFP/F33N10	SFD33N10	
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	±20		V
Drain Current	T_C=25°C	I_D	33		A
	T_C=100°C		23		
Drain Current Pulsed		I_{DM}	110		A
Power Dissipation(T_C=25°C)		P_D	130	98	W
-Derate above 25°C			1.04	0.78	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	695.22		mJ
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating		Unit
		SFP/F33N10	SFD33N10	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.96	1.28	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	110	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=Rated BV_{DSS}, V_{GS}=0V	--	--	25	μA
		V_{DS}=0.8 x Rated BV_{DSS}, V_{GS}=0V,T_C=125°C	--	--	250	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=16A	--	34	44	mΩ
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHZ	--	1239.00	--	pF
Output Capacitance	C_{oss}		--	247.30	--	
Reverse Transfer Capacitance	C_{rss}		--	43.70	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=16A, R_{GS}=5.1Ω, V_{GS}=10V	--	10.40	--	ns
Turn-on Rise Time	t_r		--	44.00	--	
Turn-off Delay Time	$t_{d(off)}$		--	45.80	--	
Turn-off Fall Time	t_f		--	12.67	--	
Total Gate Charge	Q_g	V_{DS}=80V, I_D=16A, V_{GS}=10V	--	37.01	--	nC
Gate-Source Charge	Q_{gs}		--	6.00	--	
Gate-Drain Charge	Q_{gd}		--	16.55	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	33	A
Pulsed Source Current	I_{SM}		--	--	110	
Diode Forward Voltage	V_{SD}	I_S=16A, V_{GS}=0V	--	--	1.2	V
Reverse Recovery Time	T_{rr}	I_S=33A, V_{GS}=0V	--	98.2	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs(Note 2)	--	0.37	--	nC

Notes:

1. L=1.5mH, I_{AS}=22.5A, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics(25°C)

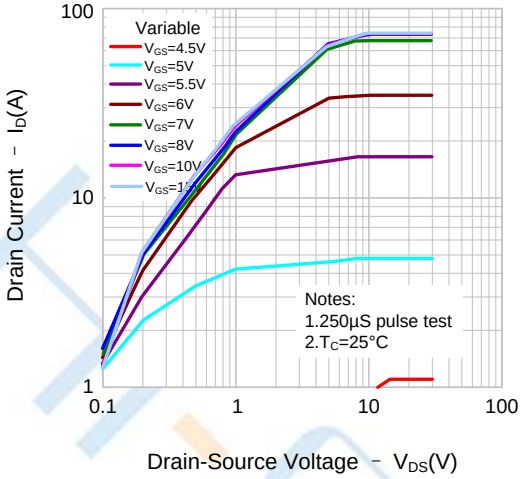


Figure 2. On-Region Characteristics(175°C)

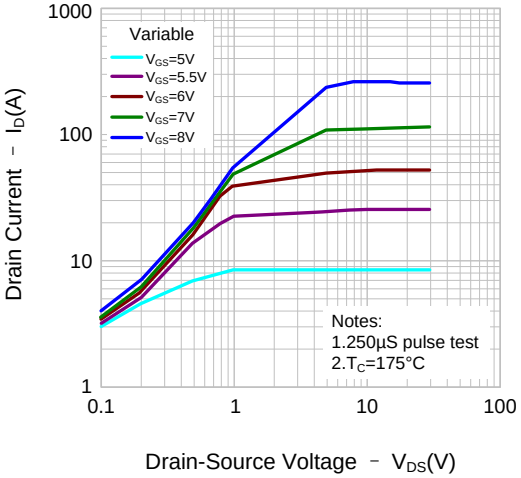


Figure 3. Transfer Characteristics

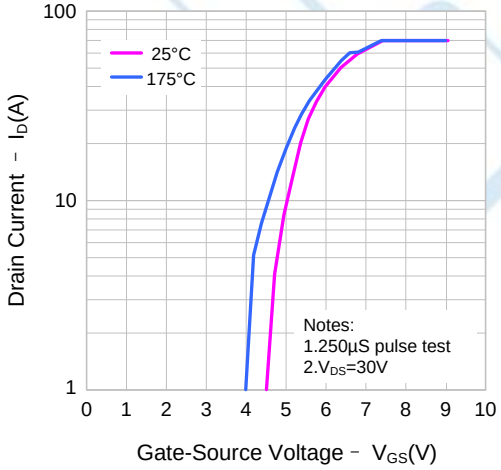


Figure 4. Source Drain Diode Forward Voltage Variation vs. Source Current and Temperature

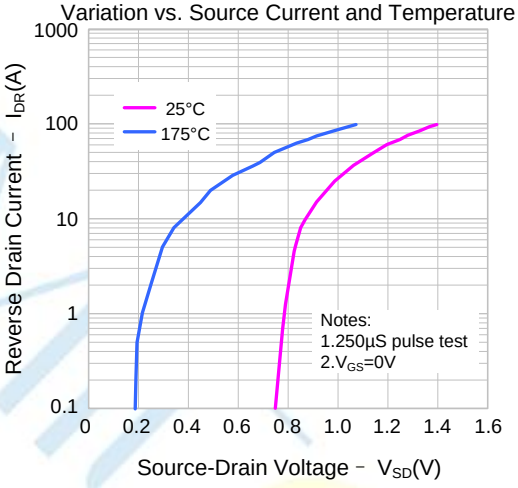


Figure 5. Capacitance Characteristics

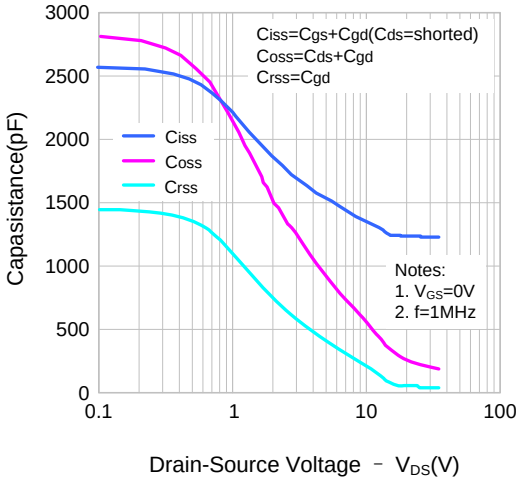
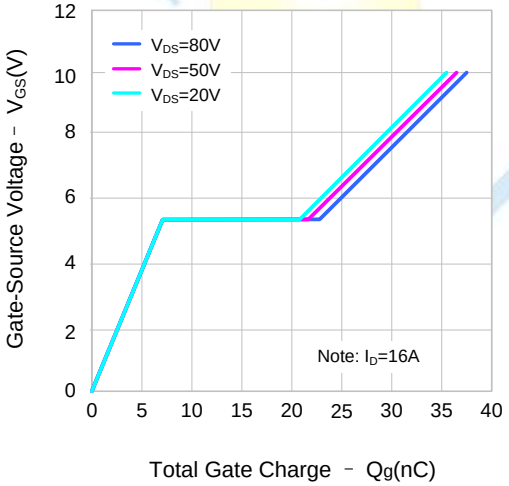


Figure 6. Gate Charge Characteristics



TYPICAL Characteristics

Figure 7. On-resistance Variation vs. Temperature

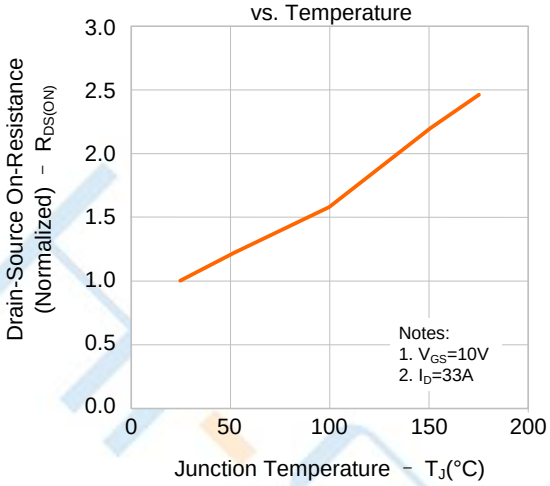


Figure 8-1 Max. Safe Operating Area (SFP/F33N10)

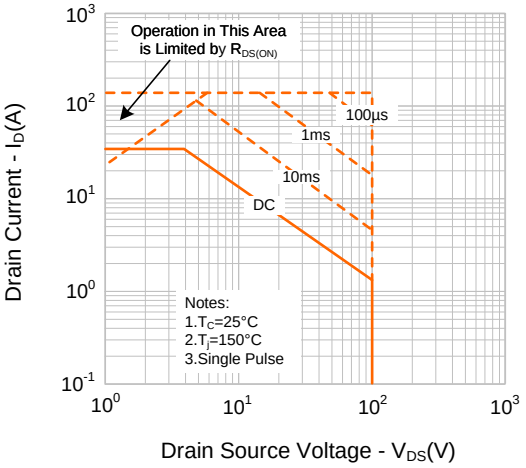


Figure 9. Maximum Drain Current vs. Case Temperature

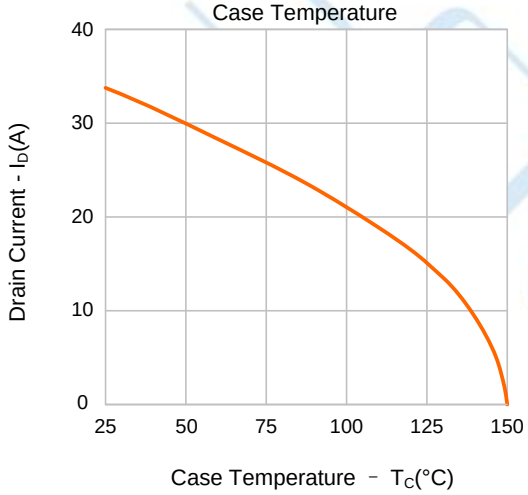
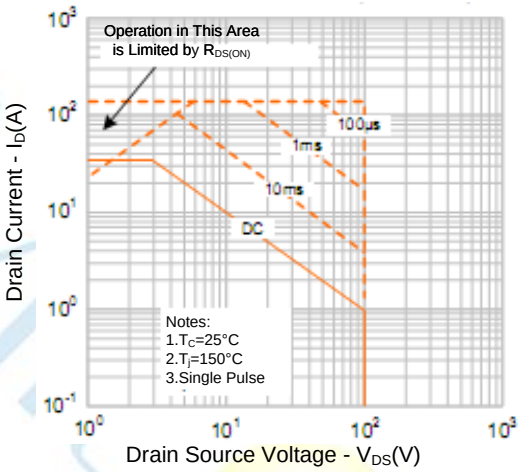
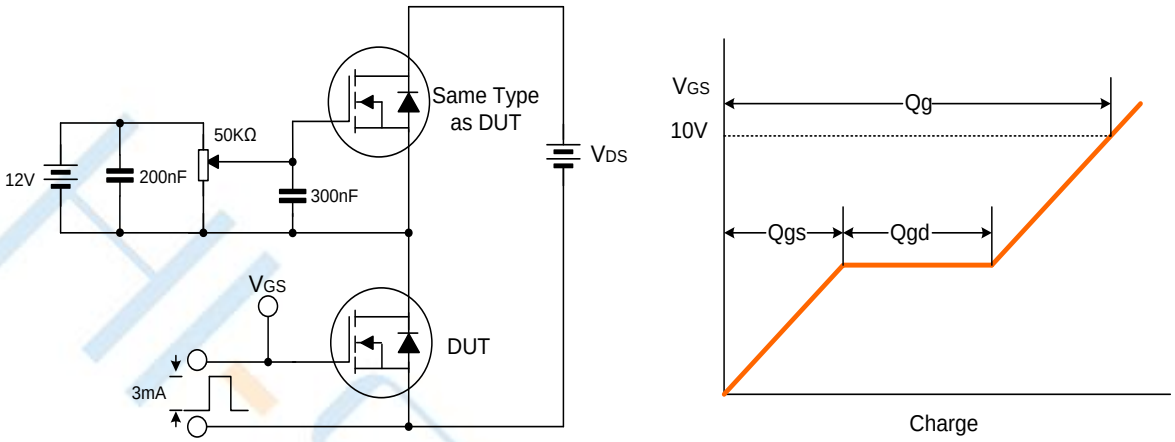


Figure 8-2 Max. Safe Operatin Area (SFD33N10)

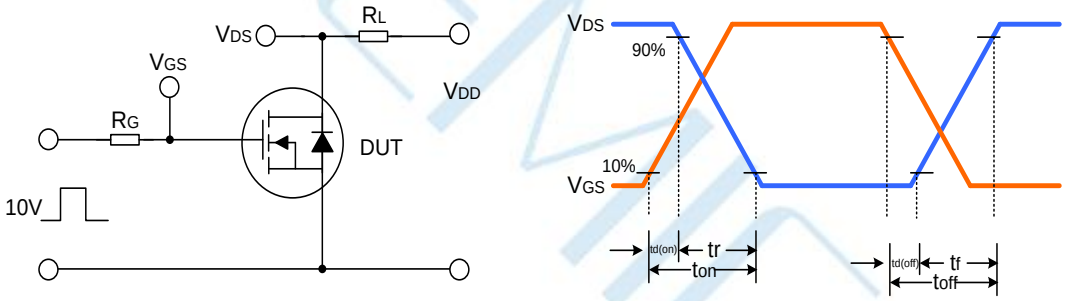


TYPICAL TEST CIRCUIT

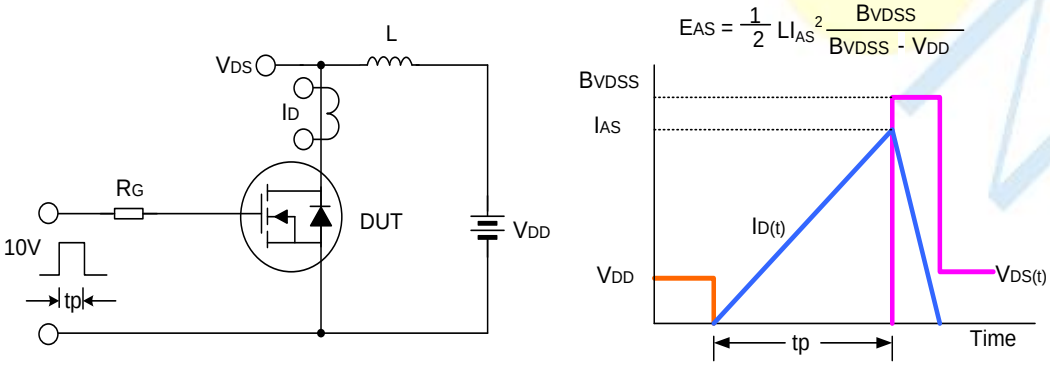
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

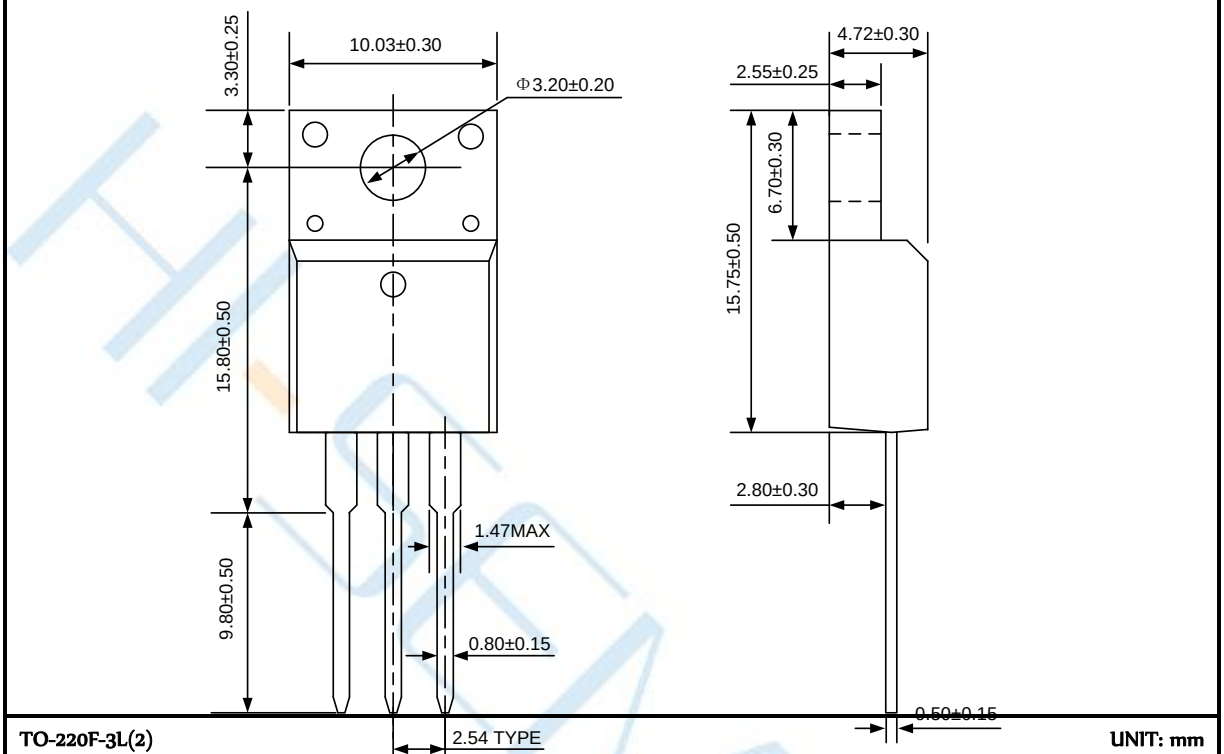


Unclamped Inductive Switching Test Circuit & Waveform

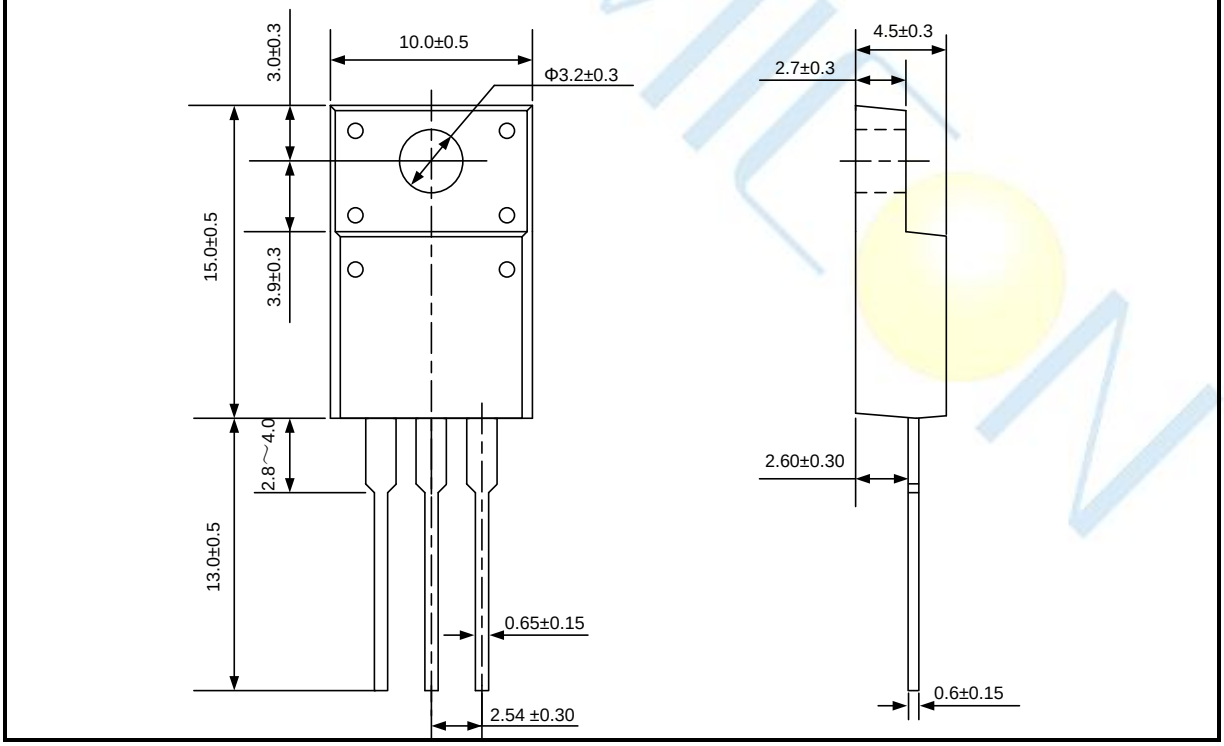


PACKAGE OUTLINE

TO-220F-3L(1) UNIT: mm

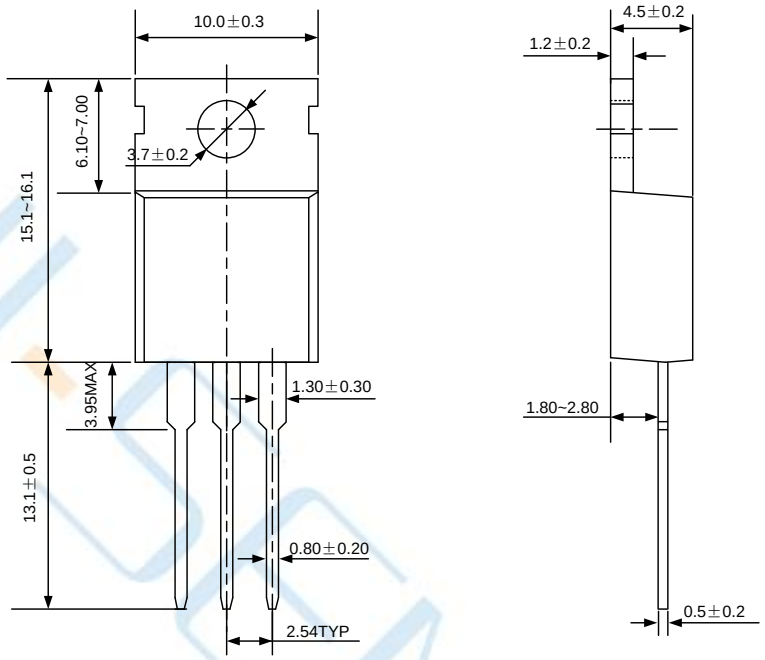


TO-220F-3L(2) UNIT: mm

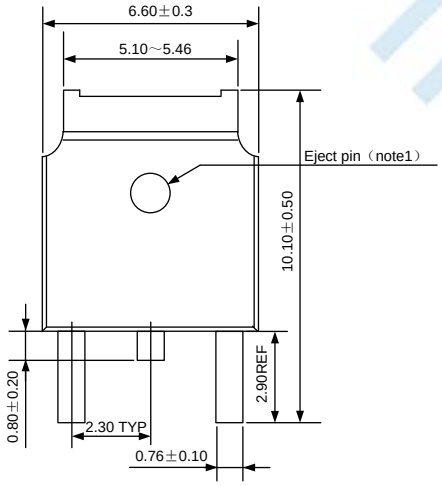


PACKAGE OUTLINE (continued)

TO-220-3L UNIT: mm



TO-252-2L UNIT: mm



NOTE1 There are two conditions for this position:has an eject pin or has no eject pin.