



SG12864H (128 DOTS X 64 DOTS)

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FEATURES

- ◆ BUILT-IN CONTROLLER (KS0107 OR EQUIVALENT)
- ◆ +5 V POWER SUPPLY
- ◆ 1/64 DUTY CYCLE
- ◆ 8-BIT PARALLEL INTERFACE
- ◆ 4.2 V LED FORWARD VOLTAGE

MECHANICAL DATA

ITEM	DIMENSIONS	UNIT
Module Size (W x H x T)	75.0 x 52.7 x 7.9 (9.2 LED)	mm
Viewing Area (W x H)	60.0 x 32.5	mm
Active Area (W x H)	55.01 x 27.49	mm
Dot Size (W x H)	0.40 x 0.40	mm
Dot Pitch (W x H)	0.43 x 0.43	mm

INTERFACE PIN CONNECTIONS

NO.	SYMBOL	LEVEL	FUNCTION
1	V _{DD}	5V	Power Supply Voltage
2	V _{SS}	0V	Power Supply Ground
3	V _O	-	Contrast Adjustment Voltage
4~11	DB0~DB7	H/L	Data Bus Line
12	CS1	H	Chip Select Signal For IC1
13	CS2	H	Chip Select Signal For IC2
14	/RES	L	Reset Signal
15	R/W	H/L	H : Read / L : Wrtie
16	D/I	H/L	H : Data, L : Instruction Code
17	E	H→L	Enable Signal
18	V _{out}	-	Power Supply Voltage For LCD
19	A	4.2V	LED Power (+)
20	K	0V	LED Power (-)

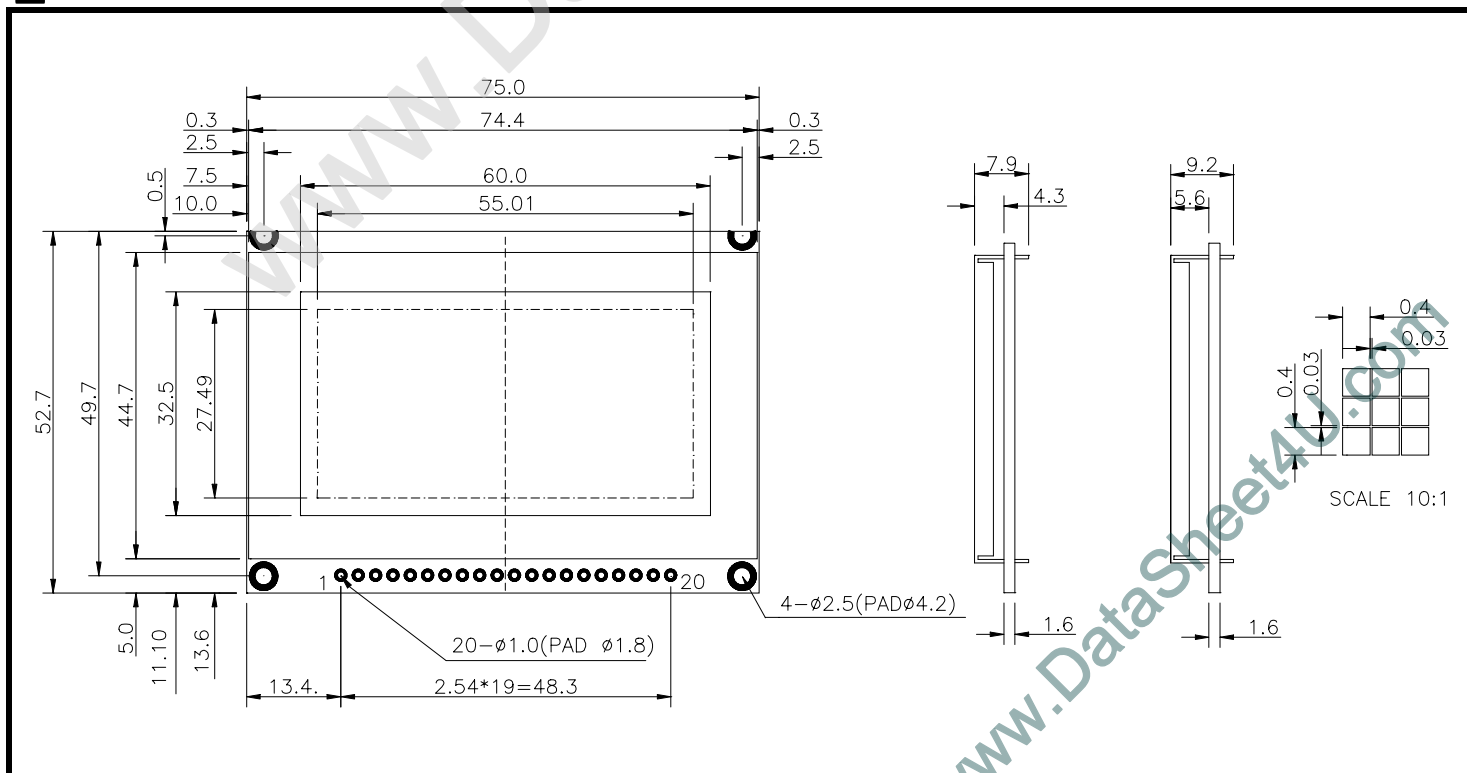
ABSOLUTE MAXIMUM RATINGS

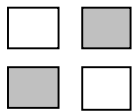
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V _{DD} -V _{SS}	0	-	7	V
Supply Voltage For LCD Drive	V _{DD} -V _O	0	-	18	V
Input Voltage	V _I	V _{SS}	-	V _{DD}	V

ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage For Logic	V _{DD} -V _{SS}	-	4.5	5	5.5	V
Supply Voltage For LCD	V _{DD} -V _O	V _{DD} =5V Ta=25°C	7.8	8.6	9.2	V
Supply Current	I _{DD}	V _{DD} =5V	-	6.2	10	mA
Input Voltage	"HIGH" Level	V _{IH}	-	2.2	-	V _{DD} V
Input Voltage	"LOW" Level	V _{IL}	-	-	-	0.6 V
Output Voltage	"HIGH" Level	V _{OH}	-	2.4	-	V
Output Voltage	"LOW" Level	V _{OL}	-	-	-	0.4 V

EXTERNAL DIMENSIONS





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TIMING CHARACTERISTICS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT.	FIG
E Cycle Time	t_{CYC}	1000	-	-	ns	1,2
E High Level Width	P_{WEH}	450	-	-	ns	1,2
E Low Level Width	P_{WEL}	450	-	-	ns	1,2
E Rise Time	t_r	-	-	25	ns	1,2
E Fall Time	t_f	-	-	25	ns	1,2
Address Setup Time	t_{AS}	140	-	-	ns	1,2
Address Hold Time	t_{AH}	10	-	-	ns	1,2
Data Setup Time	t_{DSW}	200	-	-	ns	1
Data Delay Time	t_{DDR}	-	-	320	ns	2
Data Hold Time	Write	t_{DHW}	10	-	ns	1
Data Hold Time	Read	t_{DHR}	20	-	ns	2

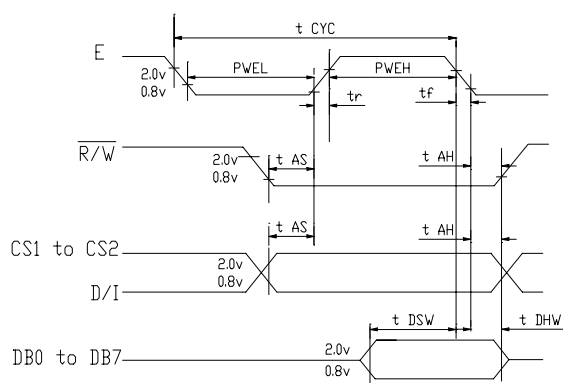


Fig1:CPU Write Timing

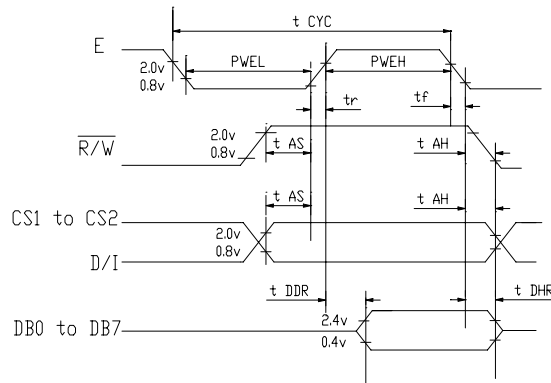


Fig2:CPU Read Timing

BLOCK DIAGRAM

