SG1524B/SG2524B/SG3524B Regulating Pulse Width Modulator

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1. Product Overview

The SG1524B is a pulse width modulator for switching power supplies, that gives improved performance over industry standards, like the SG1524. This is a direct pin-for-pin replacement for the earlier device, and combines advanced processing techniques and circuit design to provide improved reference accuracy, and extended common mode range at the error amplifier and current limit inputs. A DC-coupled flip-flop eliminates triggering and glitch problems, and a pulse width modulator data latch prevents edge oscillations. The circuit incorporates true digital shutdown for high speed response, while an under voltage lockout circuit prevents spurious outputs when the supply voltage is too low for stable operation. Full double-pulse suppression logic insures alternating output pulses when the shutdown pin is used for pulse-by-pulse current limiting. SG1524B is specified for operation over the full military ambient temperature range of –55 °C to 125 °C. SG2524B is characterized for the industrial range of –25 °C to 85 °C, and SG3524B is designed for the commercial range of 0 °C to 70 °C.

1.1 Features

The main features of SG1524B are as follows.

- 7 V to 40 V operation
- 5 V reference trimmed to ±1%
- 100 Hz to 400 kHz oscillator range
- Excellent external sync capability
- Dual 100 mA output transistors
- Wide current limit common mode range
- DC-coupled toggle flip-flop
- PWM data latch
- Undervoltage lockout
- Full double pulse suppression logic
- 60 V output collectors

1.2 High Reliability Features

The high reliability features of SG1524B are as follows.

- Available to MIL-STD-883, ¶ 1.2.1
- MSC-AMS level "S" processing available
- Available to DSCC-standard microcircuit drawing (SMD)

1.3 Block Diagram

The following figure shows the block diagram of SG1524B.

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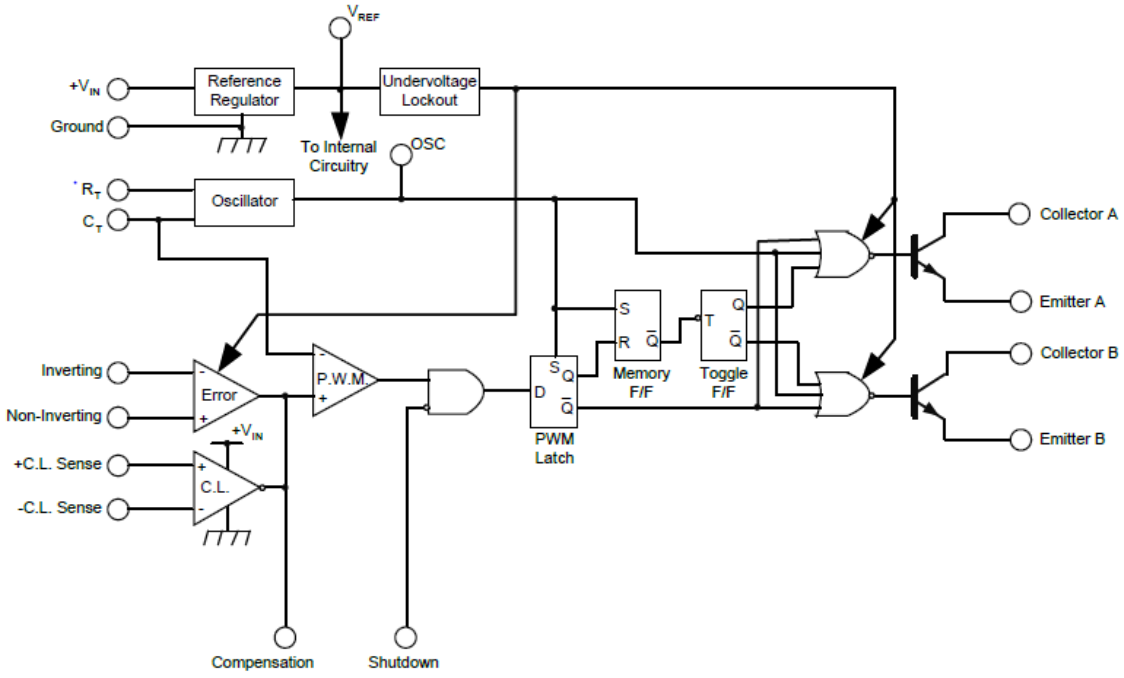
Figure 1-1. SG1524B Block Diagram



2. Electrical Specifications

This section shows the electrical characteristics of SG1524B/SG2524B/SG3524B. If not specified, these specifications apply over the operating ambient temperatures for SG1524B with –55 °C ≤ T_A ≤ 125 °C, SG2524B with –25 °C ≤ T_A ≤ 85 °C, SG3524B with 0 °C ≤ T_A ≤ 70 °C, and V_{IN} = 20 V. Low duty cycle pulse testing techniques are used, that maintain junction and case temperatures equal to the ambient temperature.

The following table shows the parameters and test conditions of SG1524B/SG2524B/SG3524B.

Table 2-1. Electrical Characteristics

Parameter	Test Conditions	SG1524B			SG2524B			SG3524B			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Section (I_L = 0 mA)											
Output voltage	T_J = 25 °C	4.95	5.00	5.05	4.95	5.00	5.05	4.90	5.00	5.10	V
Line regulation	V_{IN} = 7 V to 40 V		3	20		3	20		3	30	mV
Load regulation	I_L = 0 mA to 20 mA		5	30		5	30		5	50	mV
Temperature stability[1]	Over operating temperature range		15	50		15	50		15	50	mV
Total output voltage range	Over line, load and temperature	4.90		5.10	4.90		5.10	4.80		5.20	V
Short circuit current	V_{REF} = 0 V	25	50	120	25	50	120	25	50	120	mA
Undervoltage Lockout Section											
Threshold voltage		4.3	4.5	4.7	4.20	4.5	4.7	4.2	4.5	4.9	V
Oscillator Section (F_{OSC} = 45 kHz, R_T = 2700 Ω, C_T = 0.01 µF)											
Initial accuracy	T_J = 25 °C	42	45	48	42	45	48	40	45	50	kHz
Voltage stability	V_{IN} = 7 V to 40 V		0.1	1		0.1	1		0.1	1	%
Temperature stability[1]	Over operating range		1	2		1	2		1	2	%
Minimum frequency[1]	R_T = 150 kΩ, C_T = 0.1 µF		50	140		50	140		50	120	Hz
Maximum frequency	R_T = 2 kΩ, C_T = 470 pF	400	600		400	600		400	600		kHz
Sawtooth peak voltage	V_{IN} = 40 V		3.5	3.9		3.5	3.9		3.5	3.9	V
Sawtooth valley voltage	V_{IN} = 7 V	0.6	1		0.6	1		0.6	1		V

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Parameter	Test Conditions	SG1524B			SG2524B			SG3524B			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock amplitude		3.0	4.0		3.0	4.0		3.0	4.0		V
Clock pulse width		0.2	0.5	1.2	0.2	0.5	1.2	0.2	0.5	1.2	µs
Error Amplifier Section (V_{CM} = 2.3 V to V_{REF})											
Input offset voltage	$R_S \leq 2$ kΩ		0.5	5		0.5	5		2	10	mV
Input bias current			1	5		1	5		1	10	µA
Input offset current				1			1			1	µA
DC open loop gain	$R_L \geq 10$ MΩ	60	78		60	78		60	78		dB
Output low level	I_{SINK} = 100 µA $V_{PIN\ 1}$ - $V_{PIN\ 2}$ ≥ 150 mV		0.2	0.5		0.2	0.5		0.2	0.5	V
Output high level	I_{Source} = 100 µA $V_{PIN\ 2}$ - $V_{PIN\ 1}$ ≥ 150 mV	3.8	4.2		3.8	4.2		3.8	4.2		V
Common mode rejection	V_{CM} = 2.3 V to V_{REF}	70	90		70	90		70	90		dB
Supply voltage rejection	V_{IN} = 7 V to 40 V	76	100		76	100		76	100		dB
Gain-bandwidth product[1]	T_J = 25 °C	1	2		1	2		1	2		MHz
P.W.M. Comparator (F_{OSC} = 45 kHz, R_T = 2700 Ω, C_T = 0.01 µF)											
Minimum duty cycle	V_{COMP} = 0.5 V			0			0			0	%
Maximum duty cycle	V_{COMP} = 3.9 V	45	49		45	49		45	49		%
Current Limit Amplifier Section (V_{CM} = 0 V to 17.5 V)											
Sense voltage		180	200	220	180	200	220	170	200	230	mV
Input bias current			–3	–10		–3	–10		–3	–10	µA

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Parameter	Test Conditions	SG1524B			SG2524B			SG3524B			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Shutdown Input Section											
High input voltage		2.0			2.0			2.0			V
High input current	$V_{SHUTDOWN}$ = 5 V		0.10	1		0.10	1		0.10	1	mA
Low input voltage				0.6			0.6			0.6	V
Output Section for Each Transistor											
Collector leakage current	V_{CE} = 60 V			50			50			50	µA
Collector saturation voltage	I_C = 10 mA I_C = 100 mA		0.2 1.0	0.4 2.0		0.2 1.0	0.4 2.0		0.2 1.0	0.4 2.0	V
Emitter output voltage	I_E = 10 mA I_E = 100 mA	17.5 17	19 18		17.5 17	19 18		17.5 17	19 18		V
Emitter voltage rise time[1]	R_E = 2 kΩ, T_A = 25 °C		0.2	0.5		0.2	0.5		0.2	0.5	µs
Collector voltage fall time	R_C = 2 kΩ, T_A = 25 °C		0.1	0.2		0.1	0.2		0.1	0.2	µs
Power Consumption											
Standby current	V_{IN} = 40 V, $V_{SHUTDOWN}$ = 2.0 V		5	12		5	12		5	12	mA

1. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

2.1 Recommended Operating Conditions

The following table shows recommended operating conditions of SG1524B/SG2524B/SG3524B. Here, the operating conditions refer to ranges over which the device is functional.

Table 2-2. Recommended Operating Conditions

Parameter	Value	Unit
Input voltage (V_{IN})	7 to 40	V
Collector voltage	0 to 60	V
Error Amp common mode range	2.3 to V_{REF}	V
Current limit sense common mode range	0 to V_{IN} – 2.5 V	V

.....continued

Parameter	Value	Unit
Output current (each transistor)	0 to 100	mA
Reference load current	0 to 20	mA
Oscillator charging current	25 to 1.8	µA/mA
Oscillator frequency range	100 to 400	Hz/kHz
Oscillator timing resistor (R_T)	2 to 150	kΩ
Oscillator timing capacitor (C_T)	1 to 0.1	nF/µF
Operating Ambient Temperature Range		
SG1524B	–55 to 125	°C
SG2524B	–25 to 85	°C
SG3524B	0 to 70	°C

2.2 Typical Performance Curves

The following figures show characteristic curves of SG1524B. The conditions are, V_{IN} = 20 V, T_A = 25 °C.

Figure 2-1. Oscillator Frequency vs. Timing Resistor and Capacitor

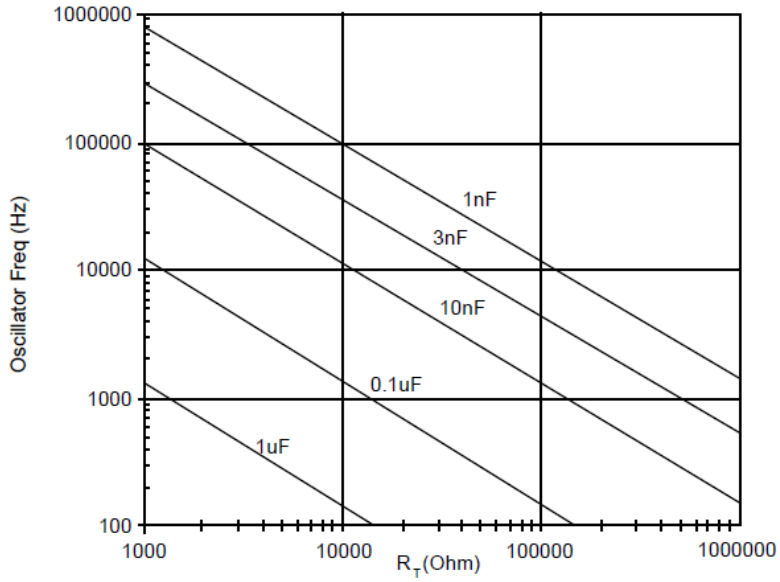


Figure 2-2. SG1524B Dead Times vs. Timing Capacitance (R_T = 2.7 kΩ)

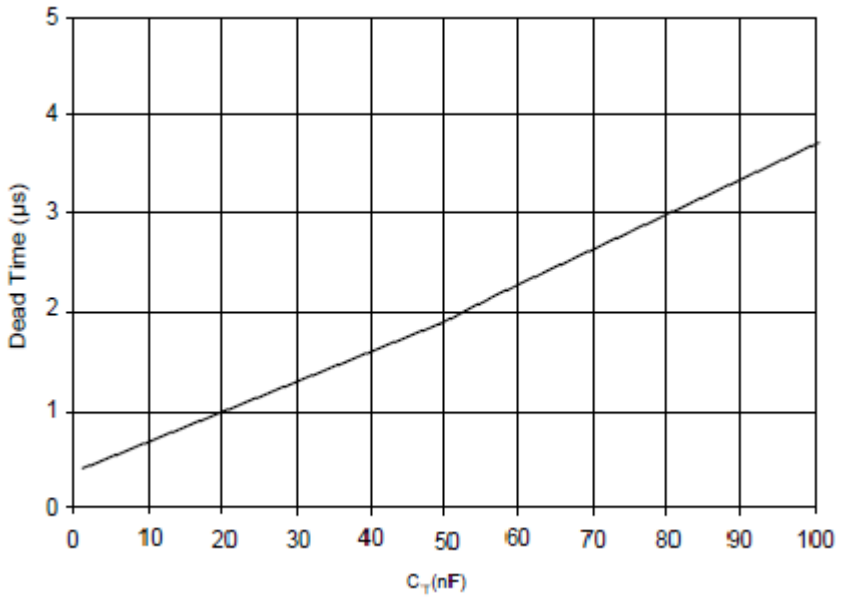
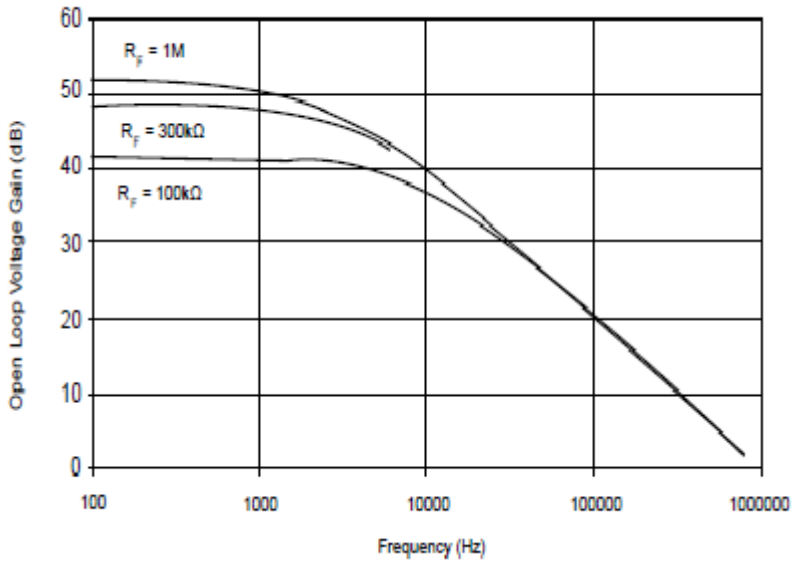


Figure 2-3. SG1524B Error Amplitude Voltage Gain vs. Frequency over R_F



2.3 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of SG1524B/SG2524B/SG3524B. The absolute maximum ratings refer to values beyond which damage may occur.

Table 2-3. Absolute Maximum Ratings

Parameter	Value	Units
Input voltage ($+V_{IN}$)	42	V

.....continued

Parameter	Value	Units
Collector voltage	60	V
Logic inputs	–0.3 to 5.5	V
Current limit sense inputs	–0.3 to V_{IN}	V
Output current (each transistor)	200	mA
Reference load current	50	mA
Oscillator charging current	5	mA
Operating Junction Temperature		
Hermetic (J and L Packages)	150	°C
Plastic (N and DW Packages)	150	°C
Storage temperature range	–65 to 150	°C
Lead temperature (soldering, 10 seconds)	300	°C
RoHS peak package solder reflow temperature (40 seconds maximum exposure)	260 (+0, –5)	°C

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3. Package Information

This section shows the package outline dimensions and thermal specifications of SG1524B/SG2524B/SG3524B. Controlling dimensions are in inches, and metric equivalents are shown for general information.

The following figure and table show DW 16-pin SOWB package and its dimensions. Dimensions do not include protrusions and should not exceed 0.155 mm (0.006 in.) on any side. Lead dimension should not include solder coverage.

Figure 3-1. DW 16-Pin SOWB Package

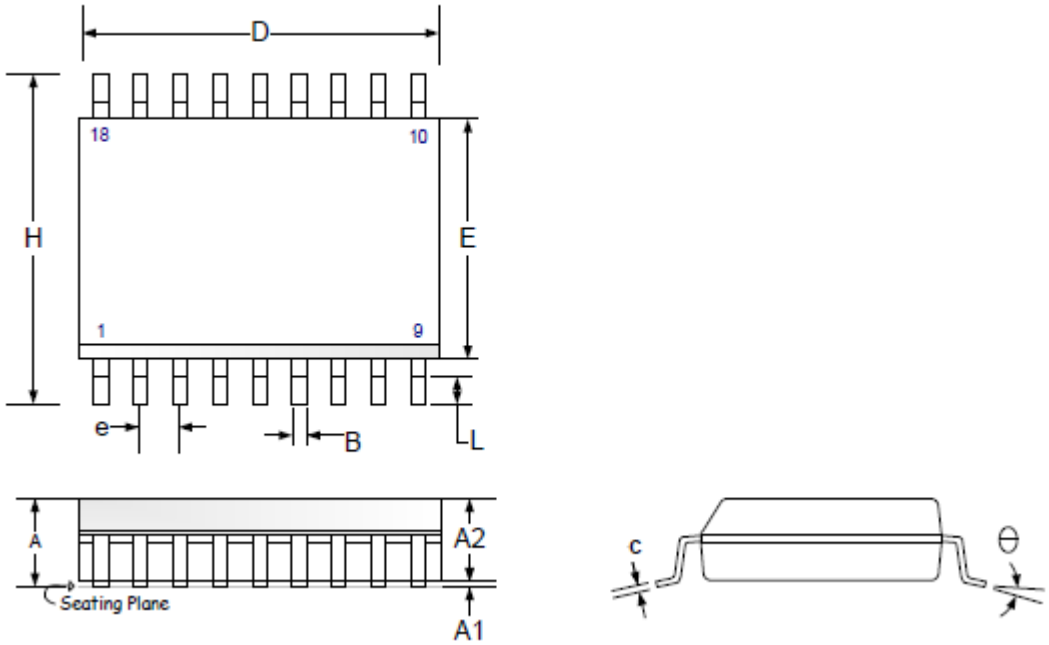

Table 3-1. DW 16-Pin SOWB Package Dimensions

Dimensions	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	9.78	10.01	0.385	0.394
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050

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Dimensions	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
Θ	0	8	0	8
Lead coplanarity		0.10		0.004

The following figure and table show N 16-pin plastic dual inline package and its dimensions. Dimensions do not include protrusions and should not exceed 0.155 mm (0.006 in.) on any side. Lead dimension should not include solder coverage.

Figure 3-2. N 16-Pin Plastic Dual Inline Package

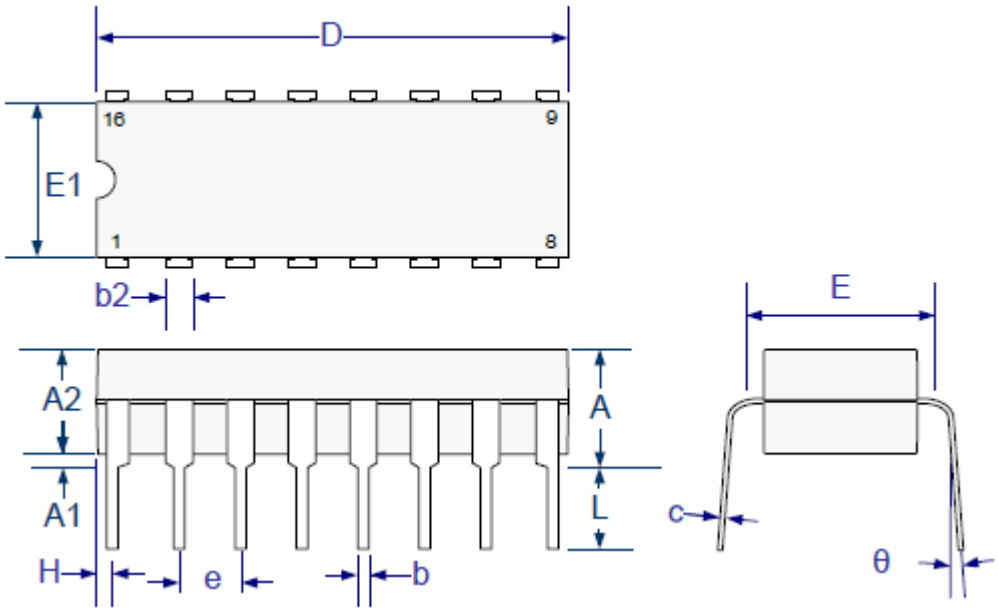


Table 3-2. N 16-Pin Plastic Dual Inline Package Dimensions

Dimensions	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	–	5.08	–	0.200
A1	0.38	0.51	0.015	0.040
A2	3.30 typical		0.130 typical	
b	0.38	0.51	0.015	0.020
b2	0.76	1.52	0.030	0.060
c	0.20	0.38	0.008	0.015
D	18.54	20.57	0.730	0.810
e	2.54 BSC		0.100 BSC	
E1	6.10	6.60	0.240	0.260

.....continued				
Dimensions	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
E	7.62 BSC		0.300 BSC	
L	3.05	-	0.120	-
θ	-	15°	-	15°

The following figure and table show J 16-pin ceramic dual inline package and its dimensions. Dimensions do not include protrusions and should not exceed 0.155 mm (0.006 in.) on any side. Lead dimension should not include solder coverage.

Figure 3-3. J 16-Pin Ceramic Dual Inline Package

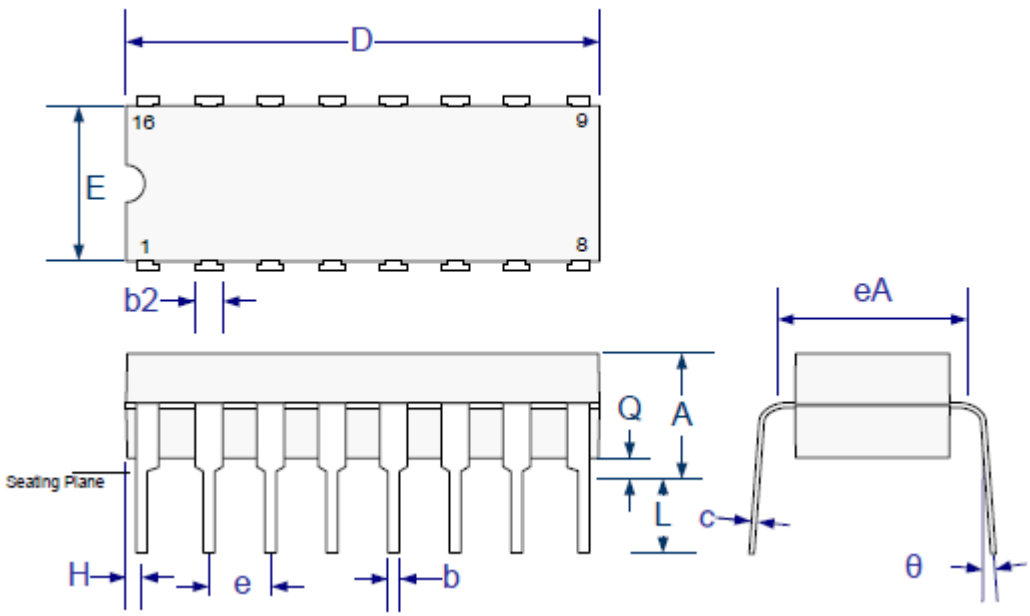


Table 3-3. J 16-Pin Ceramic Dual Inline Package Dimensions

Dimensions	Millimeters		Inches	
	Minimum	Maximum	Minimum	Maximum
A	-	5.08	-	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	

.....continued				
Dimensions	**Millimeters**		**Inches**	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	5.08	0.125	0.200
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

The following figure and table show L 20-pin ceramic leadless chip carrier (CLCC) package and its outline dimensions. All exposed metalized area should be gold plated, 60 micro-inch minimum thickness over nickel plated base, if not specified in purchase order.

Figure 3-4. L 20-Pin Ceramic Leadless Chip Carrier (CLCC) Package

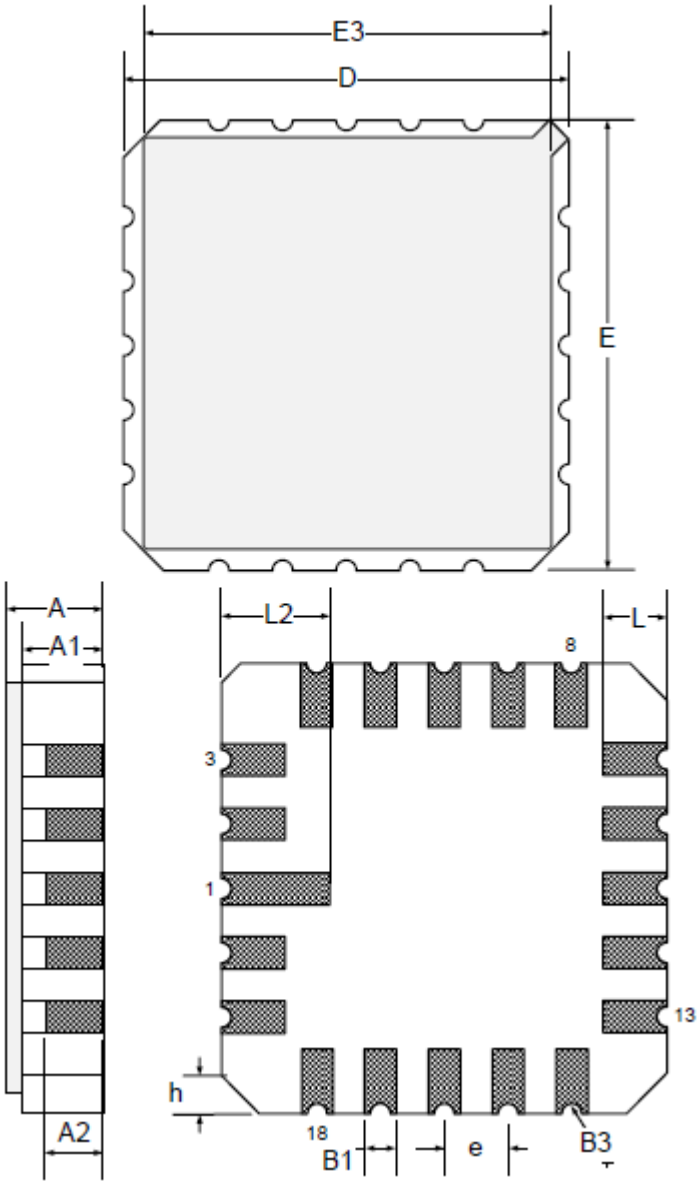


Table 3-4. L 20-Pin Ceramic Leadless Chip Carrier (CLCC) Package Outline Dimensions

DIM	Millimeters		Inches	
	Minimum	**Maximum**	**Minimum**	**Maximum**
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 typical		0.025 typical	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 typical		0.040 typical	
A1	1.372	1.68	0.054	0.066
A2	—	1.168	—	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203 R		0.008 R	

3.1 Thermal Data

The following table shows the thermal data specifications of SG1524B/SG2524B/SG3524B.

Table 3-5. Thermal Data Specifications

Parameter	Value	Units
J Package		
Thermal resistance-junction to case, θ_{JC}	30	°C/W
Thermal resistance-junction to ambient, θ_{JA}	80	°C/W
N Package		
Thermal resistance-junction to case, θ_{JC}	40	°C/W
Thermal resistance-junction to ambient, θ_{JA}	65	°C/W
DW Package		
Thermal resistance-junction to case, θ_{JC}	40	°C/W
Thermal resistance-junction to ambient, θ_{JA}	95	°C/W
L Package		
Thermal resistance-junction to case, θ_{JC}	35	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W

Note:

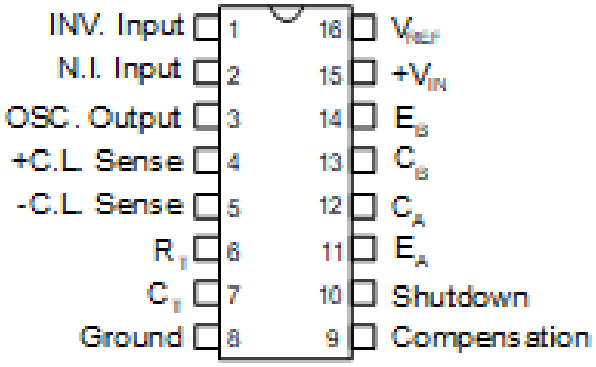
- Junction temperature calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

- The above numbers for θ_{JC} are maximum for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device or pc-board system. All of the above assume no ambient airflow.

4. Ordering Information

The following figures and tables show the connection diagrams and ordering information of SG1524B.

Figure 4-1. 16-Pin Dual Inline Package

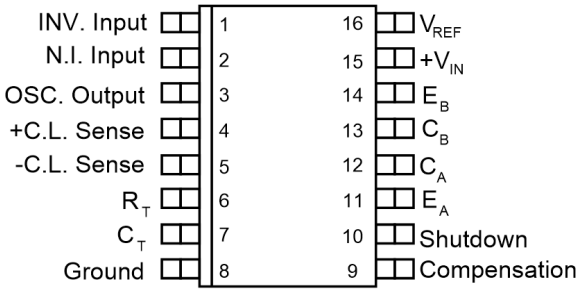


- N Package: RoHS complaint/Pb-free transition DC: 0503
- N Package: RoHS/Pb-free 100% matte tin lead finish

Table 4-1. Ordering Information of 16-Pin Dual Inline Package

Ambient Temperature	Type	Package	Part Number	Packaging Type
–55 °C to 125 °C	J	16-pin ceramic dual inline package	SG1524BJ	CERDIP (ceramic dual in-line package)
			SG1524BJ-883B	
			SG1524BJ-DESC	
–25 °C to 85 °C	N	16-pin dual inline plastic package	SG2524BN	PDIP (plastic dual in-line package)
0 °C to 70 °C			SG3524BN	

Figure 4-2. 16-Pin Small Outline Wide Body Package



- DW Package: RoHS complaint/Pb-free transition DC: 0516
- DW Package: RoHS/Pb-free 100% matte tin lead finish

Table 4-2. Ordering Information of 16-Pin Small Outline Wide Body Package

Ambient Temperature	Type	Package	Part Number	Packaging Type
–25 °C to 85 °C	DW	16-pin small outline wide body package	SG2524BDW	SOWB
0 °C to 70 °C			SG3524BDW	

Figure 4-3. 20-Pin Ceramic Leadless Chip Carrier

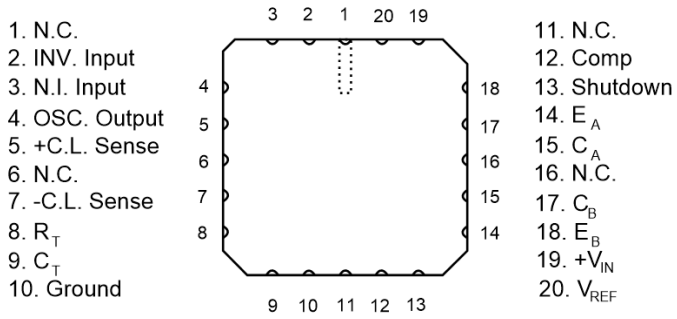


Table 4-3. Ordering Information of 20-Pin Ceramic Leadless Chip Carrier

Ambient Temperature	Type	Package	Part Number	Packaging Type
–55 °C to 125 °C	L	20-pin ceramic leadless chip carrier	SG1524BL-883B	CLCC
			SG1524BL	

Note:

- Contact your Microsemi representative for DESC product availability.
- All packages are viewed from the top.
- Hermetic packages, J and L use Sn63/Pb37 hot solder lead finish. Contact your Microsemi representative for availability of RoHS versions.
- Available in tape and reel. Append the letters "TR" to the part number (i.e., SG3524BDW-TR).

5. Revision History

Table 5-1. Revision History

Revision	Date	Description
A	08/2021	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00004165A,which replaces the previous Microsemi literature number SG1524B-2.00-0718.
2.0 (Microsemi)	07/2018	• Corrected typo in the title of the document. • Edited formatting.
1.4 (Microsemi)	12/2014	• Corrected typo in the Features section. • Corrected typo in the Ordering Information section.
1.1 (Microsemi)	02/1994	Document created.

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