SG521/22/24/28

Spread Spectrum Clock Generator

Approved Product

Features

- Generates Spread Spectrum Clock (SSC)
- Programmable Frequencies from 10 to 120 MHz
- 1.25% and 3.25% Down-Spread Options
- Separate Non-Modulated Clock
- Pin-Programmable Spread on/off Function
- 50% Output Clock Duty Cycle
- Power-Down Mode for Low Power Dissipation
- TTL or CMOS Compatible Outputs
- Low Cycle-to-Cycle Jitter of 250 ps-max
- External Clock or Crystal Oscillator Operation
- Glitch-Free Switching
- 3 to 5V Operation Supply Range
- 16-Pin Plastic SOIC Package

Applications

- CPU and μC Based Digital Systems
- Laser and Inkjet Printers
- Digital Copiers
- Multifunction Products (MFPs)
- Disk Drives
- CD-ROM
- Automotive
- Video and Imaging Applications

Benefits

- 12 to 20dB EMI Reduction
- Fast Time to Market
- Low System and Development Cost

General Description

IMI SG521/22/24/28 products are Spread Spectrum Clock Generators designed to reduce the high levels of Electromagnetic Interference (EMI) found in high-speed digital systems.

By using a modulated clock as the source for all system clocks and timing signals, the amount of radiated energy (EMI) throughout the system is greatly reduced. Energy reduction is related to the harmonic frequency, such that the higher the frequency the greater the energy reduction. The 5^{th} harmonic has greater energy reduction than the fundamental frequency.

The SG521/2/4/8 products produce a wide range of clock frequencies from 10 to 120 MHz, which are frequency modulated (PRCLK) by using a Spread Spectrum Clock (SSC) technique to reduce electromagnetic interference (EMI). In addition, a non-modulated clock output (MPCLK) with various standard clock frequencies is also provided for the part of the system that could be sensitive to a modulated clock. Refer to the Product Selection and Frequency Selection Truth Tables for the available modulated and non-modulated clock frequencies.

The spread function can be turned on or off using the SSON control line. When spread is enabled, the modulated output clock is down-spread at either 1.25% or 3.25% total spread.

These products are designed to be used with fixed frequency external clocks or crystal oscillators. The output clock frequencies are designed using a 14.318, 44.24 or 48 MHz reference clock.

The products operate from a 3 to 5 volt power supply and 0 to 70°C temperature range. The SG521/2/4/8 parts are available in 16-pin plastic SOIC packages and in die form.

Contact IMI for other packaging and Spread Spectrum Clock Generator (SSCG) products.

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Block Diagram

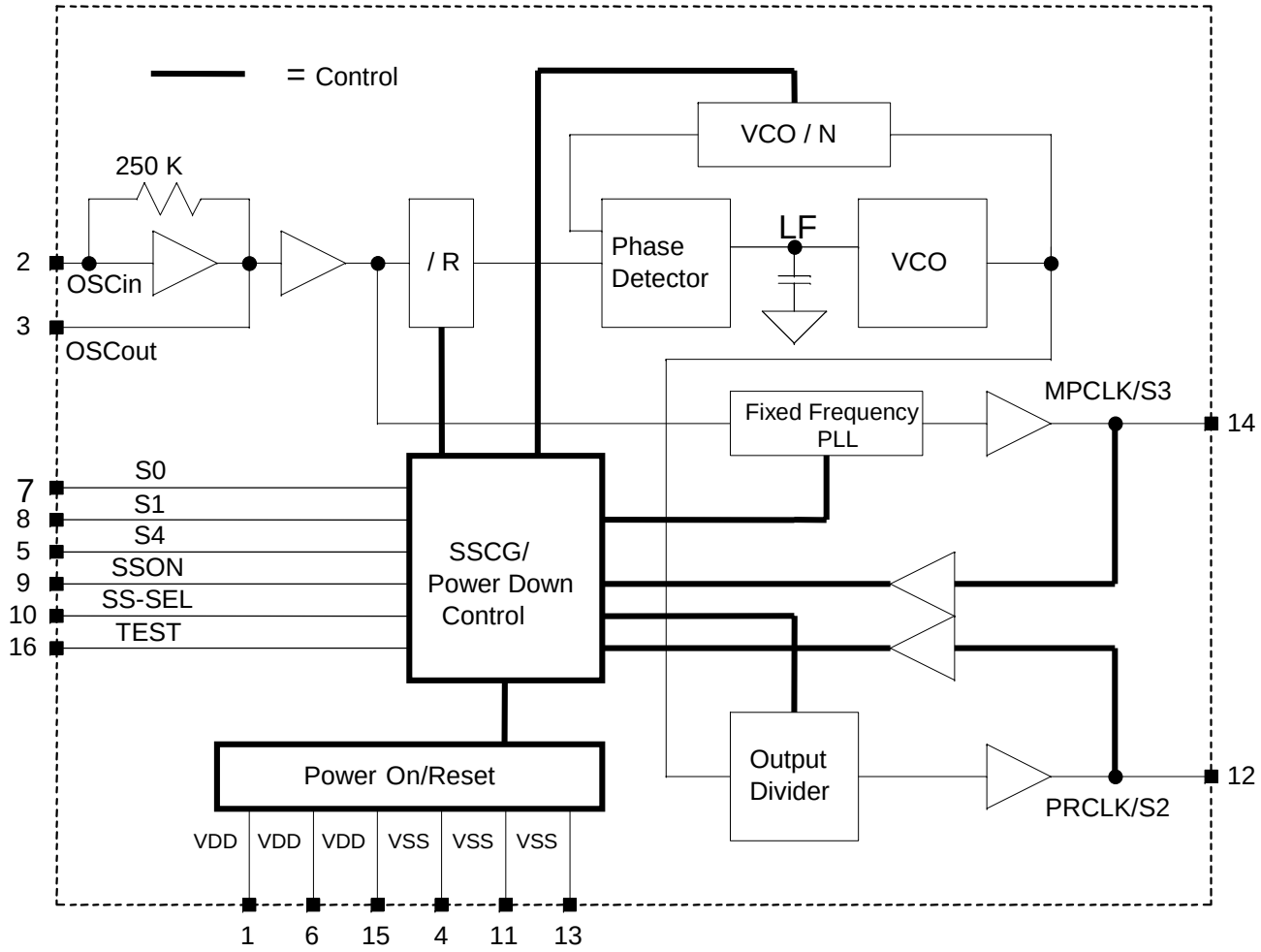

Figure 1. Block Diagram

Ordering Information

Part Number	Number of Pins and Package	Temperature Range
IMISG521BX	16-Pin SOIC	0 to 70°C
IMISG522BX	16-Pin SOIC	0 to 70°C
IMISG524BX	16-Pin SOIC	0 to 70°C
IMISG528BX	16-Pin SOIC	0 to 70°C

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Pin Configuration

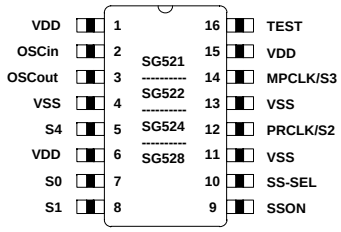

Figure 2. SG521/22/24/28 SOIC Package Pin Assignment

Pin Description

Pin #	Signal Name	I/O	Default State	Description
1	VDD	P	Power	Positive Power Supply.
2	OSCin	I	N/A	Input pin of on-chip reference oscillator.
3	OSCout	O	N/A	Output pin of on-chip reference oscillator. If Crystal Oscillator is used, this pin is left unconnected.
4	VSS	P	GND.	Power Supply Ground.
5	S4	I	1	Digital logic input used to select required crystal input frequency range, frequency spread clock (PRCLK) and non-spread clock MPCLK output frequencies. This pin has internal 150 K ohm pull-up resistor to VDD. Refer to Frequency Selection Tables for Truth Table.
6	VDD	P		Positive Power Supply
7	S0	I	0	Digital logic input used to select required crystal input frequency range, frequency spread clock (PRCLK) and non-spread clock MPCLK output frequencies. This pin has internal 150 K ohm pull-down resistor to GND. Refer to Frequency Selection Tables for Truth Table.
8	S1	I	0	Digital logic input used to select required crystal input frequency range, frequency spread clock (PRCLK) and non-spread clock MPCLK output frequencies. This pin has internal 150 K ohm pull-down resistor to GND. Refer to Frequency Selection Tables for Truth Table.
9	SSON	I	1	Input digital control pin used to enable or disable the frequency modulation function at PRCLK Output (Pin-12). When this pin is low (GND) spread function is on. When high (VDD), spread function is turned-off. This pin has 150 K ohm internal pulled-up to VDD.
10	SS-SEL	I	1	Used to select total Frequency Modulation (Spread) amount. The spread is either 1.25%(Narrow) or 3.25%(Wide). Both spreads are down-center with respect to output frequency at PRCLK (Pin-12). Refer to Frequency and Spread selection Tables for the Spread selection logic states. This pin has 150 K internal pull-up resistor to VDD.
11	VSS	P	GND.	Power Supply Ground
12	PRCLK/S2	I/O	1	Bi-directional pin used to share input control and output drive function. During power-on, this pin is a digital input and latches that state (High or Low) into an internal register as a valid S2 state. After power has reached a pre-determined level, pin 12 becomes the driver for the PRCLK modulated output clock. This pin has 150 K ohm internal pull-up resistor to VDD. For proper operation, an external 4.7 K ohm resistor connected to VDD or VSS is required. Refer to Frequency Selection Truth Tables for proper operation.
13	VSS	P	GND.	Power Supply Ground
14	MPCLK/S3	O/I	1	Bi-directional pin used to share input control and output drive function. During power-on, this pin is a digital input and latches that state (High or Low) into an internal register as a valid S3 state. After power has reached a pre-determined level, pin 14 becomes the driver for the MPCLK non-modulated output clock. This pin has 150 K ohm internal pull-up resistor to VDD. Refer to Frequency Selection Truth Tables for proper operation.
15	VDD	P	Power	Positive Power Supply
16	TEST	I	0	Provides Power-Down and Hi-Z function when used in conjunction with S0 and S1 digital inputs. This pin has internal pull-down to GND. Refer to Frequency Selection Truth Tables for proper operation.

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Absolute Maximum Ratings

Symbol	Parameter	Min.	Typical	Max.	Unit	Conditions
VDD	Supply Voltage	3.135	3.3/5.0	7.0	V	Measured from pin 1, 6 or 15 to VSS
Vimax	Input Voltage Relative to VSS	-0.3	-	VDD+0.3	V	Pins 5, 7, 8, 9, 10, 12, 14 and 16.
Vomax	Output Voltage Relative to VSS	-0.3	-	VDD+0.3	V	Pins 12 and 14
Top	Operating Temperature	0	-	70	°C	Refer to QA report.
Tst	Storage Temperature	-55	-	150	°C	Refer to QA report.
Tjc	Soldering Junction Temperature	-	-	300	°C	10 seconds soldering

Note: Operation at any Absolute Maximum Rating is not implied. Refer to DC Electrical Characteristics for proper Operating Range.

Test Conditions: VDD=3.3/5.0 V (+/-10%), CL=15pF, Operating Temperature = 0 to 70°C unless otherwise specified

DC Electrical Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit	Conditions
VDD	Power Supply Voltage, Operating	3.135	3.3/5.0	5.5	V	Measured from pin 1, 6 or 15 to VSS
OSCin-cl	Oscillator Input Load Capacitance		3		pF	Pin 2.
OSCout-cl	Oscillator Output Load Capacitance		5		pF	Pin 3.
Vinl	Input Voltage, Low	-	-	0.8	V	Pins 5, 7, 8, 9, 10, 12, 14 and 16.
Vinh	Input Voltage, High	2.0	-	-	V	Pins 5, 7, 8, 9, 10, 12, 14 and 16.
Iinl	Input Current, Low	-	-	50	µA	Pins 5, 7, 8, 9, 10, 12, 14 and 16.
Iinh	Input Current, High	-	-	50	µA	Pins 5, 7, 8, 9, 10, 12, 14 and 16.
VOL1	Output Low Voltage	-	-	0.4	Vdc	IL = 12mA, VDD = 5V
VOH1	Output High Voltage	VDD-1.0	-	-	Vdc	IL = 12mA, VDD = 5V
VOL2	Output Low Voltage	-	-	0.4	Vdc	IL = 10mA, VDD = 3.3V
VOH2	Output High Voltage	VDD-0.8	-	-	Vdc	IL = 10mA, VDD = 3.3V
Rpu/Rpd	Pull-up/down Resistors	100	150	250	KΩ	Pins 5, 7, 8, 9, 10, 12, 14 and 16.
Zo	Clock Output Impedance, PRCLK	-	12.5	-	Ohms	VDD = 5.00 VDC
Zo	Clock Output Impedance, MPCLK	-	23.0	-	Ohms	VDD = 5.00 VDC
Cin	Capacitance, Input		3		pF	Pins 2, 5, 7, 8, 9, 10, 12, 14 and 16
IDDt	Current, Leakage, Tri-State	-	-	5	µA	Pins 2, 5, 7, 8, 9, 10, 12, 14 and 16
IDDs	Current, Power Supply, Static	-	200	500	µA	Pins 2, 5, 7, 8, 9, 10, 12, 14 and 16
IDDd	Current, Power Supply, Dynamic	-	-	80	mA	Ref. = 48 MHz, PRCLK = 50.00 MHz, No Load.
IDDd	Current, Power Supply, Dynamic, VDD = 3.30 VDC	-	25.9	30.0	mA	SG528, Xin = 48 MHz, PRclk = 40 MHz, No Load
IDDd	Current, Power Supply, Dynamic, VDD = 3.30 VDC	-	38.5	45.0	mA	SG524, Xin = 48 MHz, PRclk – 120 MHz, No. Load
IDDd	Current, Power Supply, Dynamic, VDD = 5.00 VDC	-	47.8	55.0	mA	SG528, Xin = 48 MHz, PRclk = 40 MHz, No Load
IDDd	Current, Power Supply, Dynamic, VDD = 5.00 VDC	-	69.9	80.0	mA	SG524, Xin = 48 MHz, PRclk – 120 MHz, No. Load
IDDpd	Current, Power Supply, Power Down	-	-	25	µA	Test = 1.
Isco	Current, Output, Short Circuit	25	30	-	mA	PRCLK and MPCLK

Notes: Pins 5, 7, 8, 9, 10, 12, 14 and 16 have internal pull-up or pull-down resistors. These resistors define a default operating state for this part. Pins 12 and 14 require an external resistor for proper operation.

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Test Conditions: VDD=3.3/5.0 V (+/-10%) , CL=15pF and TA=0 to 70°C unless otherwise specified

Timing Electrical Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Find	Reference Frequency, delta	-10		+10	%	OSCin = 14.318, 44.24 and 48 MHz
Fout	Frequency, Output	10	-	120	MHz	PRCLK
Tr	Rise Time, PRCLK,	250	-	500	ps	Measured at 0.4 – 2.4V, @50.00 MHz
Tf	Fall Time, PRCLK	200	-	300	ps	Measured at 0.4 – 2.4V, @50.00 MHz
Tr	Rise Time, MPCLK	450	-	650	ps	Measured at 0.4 – 2.4V, @50.00 MHz
Tf	Fall Time, MPCLK	300	-	400	ps	Measured at 0.4 – 2.4V, @50.00 MHz
PRdty	Duty Cycle, PRCLK	45	50	55	%	Measured at 1.5 Volts
MPdty	Duty Cycle, MPCLK	45	50	55	%	Measured at 1.5 Volts
PRccj	Jitter, Cycle to Cycle, PRCLK	-	205	235	ps	3.30 VDC @ 50 MHz, Mod Off
PRccj	Jitter, Cycle to Cycle, PRCLK	-	215	250	ps	3.30 VDC @ 50 MHz, Mod On
PRccj	Jitter, Cycle to Cycle, PRCLK	-	216	250	ps	3.30 VDC @ 40 MHz, Mod Off
PRccj	Jitter, Cycle to Cycle, PRCLK	-	281	325	ps	3.30 VDC @ 40 MHz, Mod On
PRccj	Jitter, Cycle to Cycle, PRCLK	-	320	375	ps	5.0 VDC @ 50 MHz, Mod Off
PRccj	Jitter, Cycle to Cycle, PRCLK	-	324	375	ps	5.0 VDC @ 50 MHz, Mod On
PRccj	Jitter, Cycle to Cycle, PRCLK	-	191	225	ps	5.0 VDC @ 40 MHz, Mod Off
PRccj	Jitter, Cycle, to Cycle, PRCLK	-	351	400	ps	5.0 VDC @ 40 MHz, Mod On

Crystal Selection Truth Table

The SG521, 2, 4 and 8 uses one of three different reference frequencies. Determine the desired PRCLK frequency from the frequency selection tables in table 5 – 8. Determine the REQUIRED REFERENCE FREQUENCY, MPCLK and Product from table 1 and set S2, S3 and S4 control lines as indicated. Note that MPCLK/S3 and PRCLK/S2 are bi-directional signals and serve as an input control line during power up and an output after power is stable.

PRODUCT	REQUIRED REF. Input (MHz)	MPCLK OUT (MHz) (Pin 14)	S4 (Pin 5)	MPCLK/S3 (Pin 14)	PRCLK/S2 (Pin 12)
SG528	44.240	3.7 (44.24/12)	0	0	0
SG521/22/24	48.000	48.000	0	0	0
SG521/22/24/28	14.318	48.000	0	0	1
SG521/22/24/28	48.000	48.000	0	1	0
SG521/22/24/28	44.240	3.7 (44.24/12)	0	1	1
SG528	44.240	11.6 (44.24/4)	1	0	0
SG521/22/24	14.318	48.000	1	0	0
SG521/22/24/28	14.318	48.000	1	0	1
SG521/22/24/28	48.000	48.000	1	1	0
SG521/22/24/28	44.240	11.6 (44.24/4)	1	1	1

Table. 1

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Modulation Rate Calculation

The input frequency, Fin, at pin 2 (OSCin) and the correlating formula determine the modulation rate, Fmod, of the SG52x series. Refer to the formulae below:

If OSCin = 14.318 MHz, then;	Fmod = OSCin/(4 x 114) =	31.40kHz
If OSCin = 48.00 MHz, then;	Fmod = OSCin/(12 x 114) =	35.09kHz
If OSCin = 44.24 MHz, then;	Fmod = OSCin (48/44.24)/(12 x144) =	35.09kHz

SG521 Frequency and Spread Selection Truth Table

TEST "0" (pin 16)	MPCLK(S3) "1" (pin 14)	PRCLK(S2) "1" (pin 12)	SS_SEL "1" (pin 10)	S4 "1" (pin 5)	S1 "0" (pin 8)	S0 "0" (pin 7)	OSCin.(MHz) (pin 2)	PRCLK (MHz) (pin 12)	SPREAD 1.25%	SPREAD 3.25%
0	0	0	X	X	0	0	44.24	16.685345		•
0	0	0	X	X	0	1	44.24	40.044828		•
0	0	0	X	X	1	0	44.24	25.028017		•
0	0	0	X	X	1	1	44.24	30.033621		•
0	0	1	0	X	0	0	14.318	10.001544		•
0	0	1	0	X	0	1	14.318	20.003088		•
0	0	1	0	X	1	0	14.318	25.003860		•
0	0	1	0	X	1	1	14.318	50.007721		•
0	0	1	1	X	0	0	14.318	10.001544	•	
0	0	1	1	X	0	1	14.318	20.003088	•	
0	0	1	1	X	1	0	14.318	25.003860	•	
0	0	1	1	X	1	1	14.318	50.007721	•	
0	1	0	0	X	0	0	48	10.000000		•
0	1	0	0	X	0	1	48	20.000000		•
0	1	0	0	X	1	0	48	25.000000		•
0	1	0	0	X	1	1	48	50.000000		•
0	1	0	1	X	0	0	48	10.000000	•	
0	1	0	1	X	0	1	48	20.000000	•	
0	1	0	1	X	1	0	48	25.000000	•	
0	1	0	1	X	1	1	48	50.000000	•	
0	1	1	0	X	0	0	44.24	10.011207		•
0	1	1	0	X	0	1	44.24	20.022414		•
0	1	1	0	X	1	0	44.24	25.028017		•
0	1	1	0	X	1	1	44.24	50.056034		•
0	1	1	1	X	0	0	44.24	10.011207	•	
0	1	1	1	X	0	1	44.24	20.022414	•	
0	1	1	1	X	1	0	44.24	25.028017	•	
0	1	1	1	X	1	1	44.24	50.056034	•	
1	X	X	X	X	0	0	N/A	0 (PD)	N/A	
1	X	X	X	X	0	1	N/A	1 (PD)	N/A	
1	X	X	X	X	1	0	N/A	TEST	N/A	
1	X	X	X	X	1	1	N/A	Hi-Z	N/A	

Table 2.

Approved Product

SG522 Frequency and Spread Selection Truth Table

TEST "0" (pin 16)	MPCLK(S3) "1" (pin 14)	PRCLK(S2) "1" (pin 12)	SS_SEL "1" (pin 10)	S4 "1" (pin 5)	S1 "0" (pin 8)	S0 "0" (pin 7)	OSCin.(MHz) (pin 2)	PRCLK (MHz) (pin 12)	SPREAD 1.25%	SPREAD 3.25%
0	0	0	X	X	0	0	44.24	16.685345		•
0	0	0	X	X	0	1	44.24	40.044828		•
0	0	0	X	X	1	0	44.24	25.028017		•
0	0	0	X	X	1	1	44.24	30.033621		•
0	0	1	0	X	0	0	14.318	12.001853	•	
0	0	1	0	X	0	1	14.318	16.669240	•	
0	0	1	0	X	1	0	14.318	33.338480	•	
0	0	1	0	X	1	1	14.318	40.006176	•	
0	0	1	1	X	0	0	14.318	12.001853		•
0	0	1	1	X	0	1	14.318	16.669240		•
0	0	1	1	X	1	0	14.318	33.338480		•
0	0	1	1	X	1	1	14.318	40.006176		•
0	1	0	0	X	0	0	48	12.000000	•	
0	1	0	0	X	0	1	48	16.666667	•	
0	1	0	0	X	1	0	48	33.333333	•	
0	1	0	0	X	1	1	48	40.000000	•	
0	1	0	1	X	0	0	48	12.000000		•
0	1	0	1	X	0	1	48	16.666667		•
0	1	0	1	X	1	0	48	33.333333		•
0	1	0	1	X	1	1	48	40.000000		•
0	1	1	0	X	0	0	44.24	12.013448	•	
0	1	1	0	X	0	1	44.24	16.685345	•	
0	1	1	0	X	1	0	44.24	33.370690	•	
0	1	1	0	X	1	1	44.24	40.044828	•	
0	1	1	1	X	0	0	44.24	12.013448		•
0	1	1	1	X	0	1	44.24	16.685345		•
0	1	1	1	X	1	0	44.24	33.370690		•
0	1	1	1	X	1	1	44.24	40.044828		•
1	X	X	X	X	0	0	N/A	0 (PD)	N/A	
1	X	X	X	X	0	1	N/A	1 (PD)	N/A	
1	X	X	X	X	1	0	N/A	TEST	N/A	
1	X	X	X	X	1	1	N/A	Hi-Z	N/A	

Table 3.

Approved Product

SG524 Frequency and Spread Selection Truth Table

TEST "0" (pin 16)	MPCLK(S3) "1" (pin 14)	PRCLK(S2) "1" (pin 12)	SS_SEL "1" (pin 10)	S4 "1" (pin 5)	S1 "0" (pin 8)	S0 "0" (pin 7)	OSCin.(MHz) (pin 2)	PRCLK (MHz) (pin 12)	SPREAD 1.25%	SPREAD 3.25%
0	0	0	0	0	0	0	48	24.000000	•	
0	0	0	0	0	0	1	48	32.000000	•	
0	0	0	0	0	1	0	48	48.000000	•	
0	0	0	0	0	1	1	48	96.000000	•	
0	0	0	0	1	0	0	14.318	24.003706	•	
0	0	0	0	1	0	1	14.318	32.004941	•	
0	0	0	0	1	1	0	14.318	48.007412	•	
0	0	0	0	1	1	1	14.318	96.014824	•	
0	0	0	1	0	0	0	48	24.000000		•
0	0	0	1	0	0	1	48	32.000000		•
0	0	0	1	0	1	0	48	48.000000		•
0	0	0	1	0	1	1	48	96.000000		•
0	0	0	1	1	0	0	14.318	24.003706		•
0	0	0	1	1	0	1	14.318	32.004941		•
0	0	0	1	1	1	0	14.318	48.007412		•
0	0	0	1	1	1	1	14.318	96.014824		•
0	0	1	0	X	0	0	14.318	50.007721	•	
0	0	1	0	X	0	1	14.318	100.015441	•	
0	0	1	0	X	1	0	14.318	60.009265	•	
0	0	1	0	X	1	1	14.318	120.018529	•	
0	0	1	1	X	0	0	14.318	50.007721		•
0	0	1	1	X	0	1	14.318	100.015441		•
0	0	1	1	X	1	0	14.318	60.009265		•
0	0	1	1	X	1	1	14.318	120.018529		•
0	1	0	0	X	0	0	48	50.000000	•	
0	1	0	0	X	0	1	48	100.000000	•	
0	1	0	0	X	1	0	48	60.000000	•	
0	1	0	0	X	1	1	48	120.000000	•	
0	1	0	1	X	0	0	48	50.000000		•
0	1	0	1	X	0	1	48	100.000000		•
0	1	0	1	X	1	0	48	60.000000		•
0	1	0	1	X	1	1	48	120.000000		•
0	1	1	0	X	0	0	44.24	50.056034	•	
0	1	1	0	X	0	1	44.24	100.112069	•	
0	1	1	0	X	1	0	44.24	60.067241	•	
0	1	1	0	X	1	1	44.24	120.134483	•	
0	1	1	1	X	0	0	44.24	50.056034		•
0	1	1	1	X	0	1	44.24	100.112069		•
0	1	1	1	X	1	0	44.24	60.067241		•
0	1	1	1	X	1	1	44.24	120.134483		•
1	X	X	X	X	0	0	N/A	0 (PD)	N/A	
1	X	X	X	X	0	1	N/A	1 (PD)	N/A	
1	X	X	X	X	1	0	N/A	TEST	N/A	
1	X	X	X	X	1	1	N/A	Hi-Z	N/A	

Table 4.

Approved Product

SG528 Frequency and Spread Selection Truth Table

TEST "0" (pin 16)	MPCLK(S3) "1" (pin 14)	PRCLK(S2) "1" (pin 12)	SS_SEL "1" (pin 10)	S4 "1" (pin 5)	S1 "0" (pin 8)	S0 "0" (pin 7)	OSCin.(MHz) (pin 2)	PRCLK (MHz) (pin 12)	SPREAD 1.25%	SPREAD 3.25%
0	0	0	X	X	0	0	44.24	16.685345		•
0	0	0	X	X	0	1	44.24	40.044828		•
0	0	0	X	X	1	0	44.24	25.028017		•
0	0	0	X	X	1	1	44.24	30.033621		•
0	0	1	0	X	0	0	14.318	12.001853		•
0	0	1	0	X	0	1	14.318	16.669240		•
0	0	1	0	X	1	0	14.318	33.338480		•
0	0	1	0	X	1	1	14.318	40.006176		•
0	0	1	1	X	0	0	14.318	12.001853	•	
0	0	1	1	X	0	1	14.318	16.669240	•	
0	0	1	1	X	1	0	14.318	33.338480	•	
0	0	1	1	X	1	1	14.318	40.006176	•	
0	1	0	0	X	0	0	48	12.000000		•
0	1	0	0	X	0	1	48	16.666667		•
0	1	0	0	X	1	0	48	33.333333		•
0	1	0	0	X	1	1	48	40.000000		•
0	1	0	1	X	0	0	48	12.000000	•	
0	1	0	1	X	0	1	48	16.666667	•	
0	1	0	1	X	1	0	48	33.333333	•	
0	1	0	1	X	1	1	48	40.000000	•	
0	1	1	0	X	0	0	44.24	12.013448		•
0	1	1	0	X	0	1	44.24	16.685345		•
0	1	1	0	X	1	0	44.24	33.370690		•
0	1	1	0	X	1	1	44.24	40.044828		•
0	1	1	1	X	0	0	44.24	12.013448	•	
0	1	1	1	X	0	1	44.24	16.685345	•	
0	1	1	1	X	1	0	44.24	33.370690	•	
0	1	1	1	X	1	1	44.24	40.044828	•	
1	X	X	X	X	0	0	N/A	0 (PD)	N/A	
1	X	X	X	X	0	1	N/A	1 (PD)	N/A	
1	X	X	X	X	1	0	N/A	TEST	N/A	
1	X	X	X	X	1	1	N/A	Hi-Z	N/A	

Table 5.

Approved Product

SG521 Application Schematic

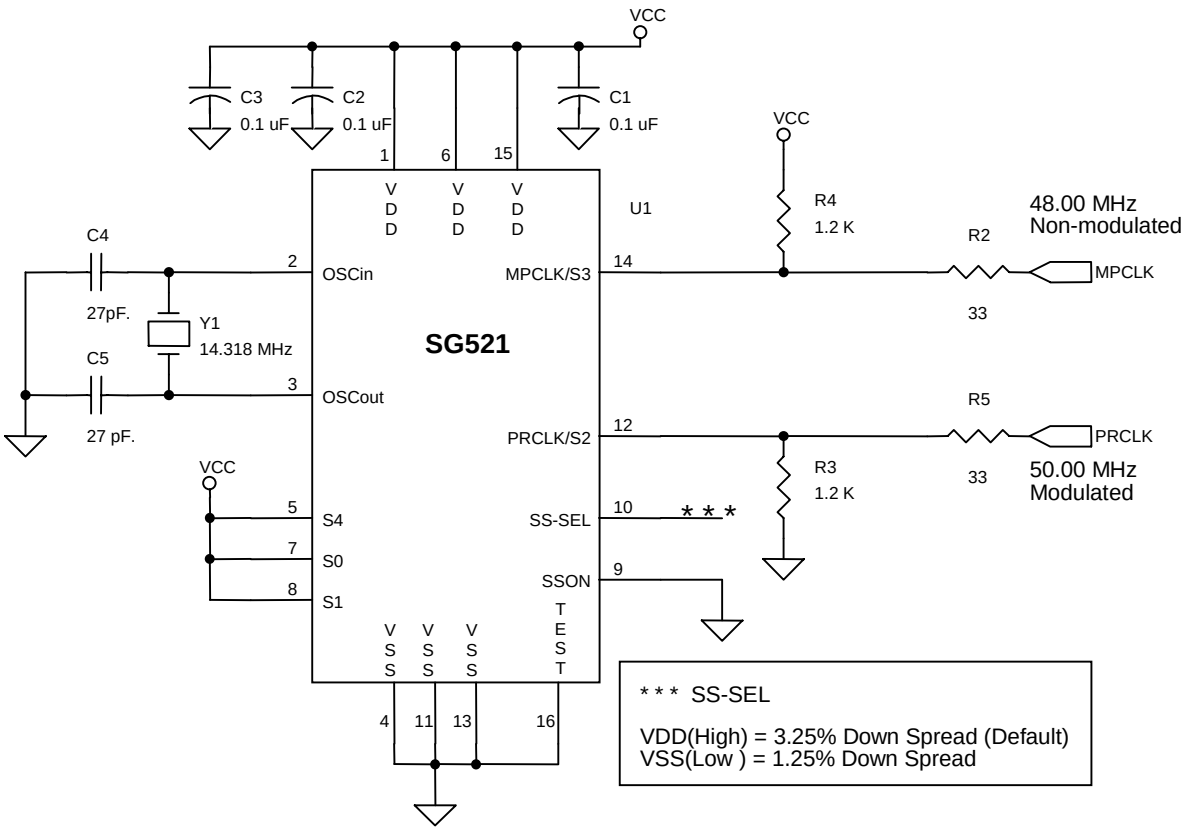

Figure 2.

Application Schematic Notes:

The application schematic shown in figure 2 above is a typical wiring diagram of the SG521. As depicted in this schematic, the SG521 will produce 48.00 MHz on the MPCLK output and a modulated 50.00 MHz on the PRCLK output. Pin 10 controls the amount of modulation on PRCLK, pin 12. When SS-SEL is high, modulation is 3.25% total spread and when SS-SEL is low, the total modulation is 1.25%.

Other considerations for this circuit is to insure that the power supply bypass capacitors, C2 and C3, are placed as closed to their respective pins as possible. Also, be sure that the oscillator components, X1, C4 and C5, are placed as close to pins 2 and 3 as possible.

Certain applications may require a separate island on the PCB for Power and Ground circuits for the SG521. This is not a requirement, but will improve the immunity, which can directly effect the Phase detector and VCO within the SG521.

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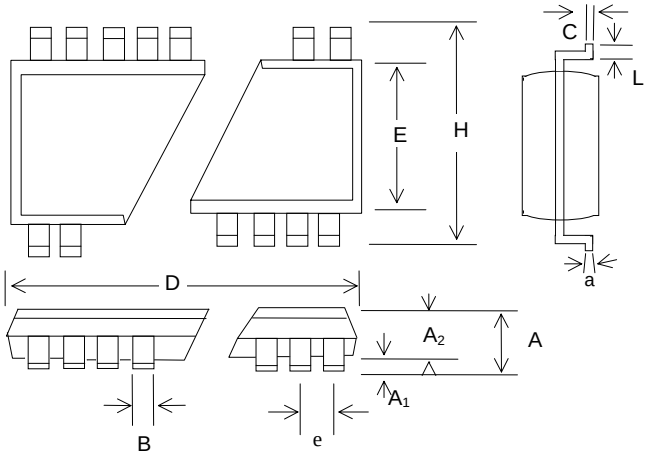
Package Drawing and Dimensions



16 Pin SOIC Outline Dimensions (300 mil)

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.093	-	0.104	2.35	-	2.65
A_1	0.004	-	0.012	0.10	-	0.30
A2	0.089		0.093	2.25		2.35
B	0.013	-	0.020	0.33	-	0.51
C	0.009	-	0.013	0.23	-	0.32
D	0.398	-	0.413	10.10	-	10.50
E	0.291	-	0.299	7.40	-	7.60
e	0.050 BSC			1.27 BSC		
H	0.394	-	0.419	10.00	-	10.65
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

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Notes:

NOTICE