

FEATURES

- Green-Mode PWM
- Supports the “Blue Angel” Norm
- Low Start-up Current (30uA)
- Low Operating Current (3mA)
- Leading-Edge Blanking
- Built-in Synchronized Slope Compensation
- Totem Pole Output with Soft Driving
- Improved EMI
- Constant Output Power Limit
- Current Mode Operation
- Cycle-by-cycle Current Limiting
- Under Voltage Lockout (UVLO)
- Programmable PWM Frequency
- GATE Output Maximum Voltage Clamped at 18V
- Short Circuit Protection
- Programmable Over Temperature Protection (OTP)
- Few External Components Required
- Low Cost

APPLICATIONS

- General-Purpose Switch Mode Power Supplies
- Flyback Power Converters
- Power Adapters
- Open-Frame SMPS
- Battery Charger Adapters

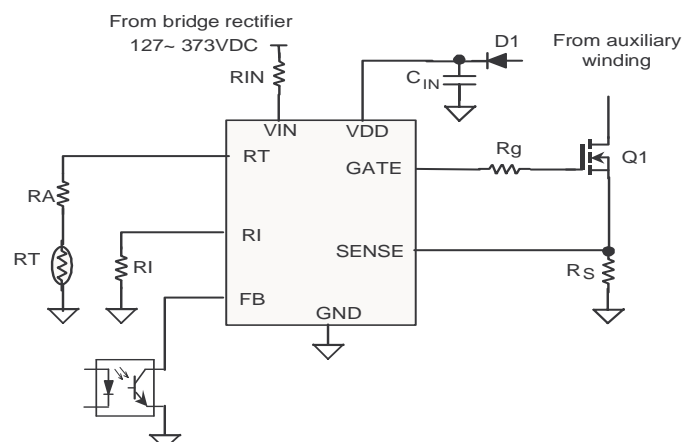
DESCRIPTION

This highly integrated PWM controller is enhanced to provide low standby-power and stronger protection features. In standby mode, the PWM frequency is linearly reduced to cut power consumption, and to provide a stable output voltage. The BiCMOS fabrication process enables reducing the start-up current to 30uA and the operating current to 3mA. This results in increased power conversion efficiency. During normal operation, the SG6840 acts as a fixed frequency PWM controller with a programmable PWM frequency. The PWM frequency can be controlled by changing an external resistor.

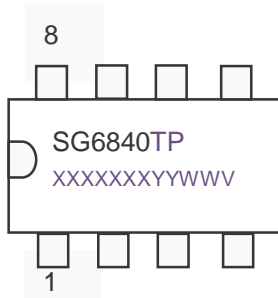
The patented green-mode function reduces the PWM frequency in response to decreases in the output load. This function dramatically cuts power losses under zero-load and light-load conditions, which helps the power supply meet even the most stringent international power conservation regulations. Proprietary synchronized slope compensation ensures the stability of the current loop under continuous-mode operation.

Built-in line-voltage compensation maintains a constant output power limit over a wide range of AC input voltages. An NTC thermistor is applied to sense the ambient temperature to provide over temperature protection. The SG6840 is available in 8-pin DIP and SO packages.

TYPICAL APPLICATION

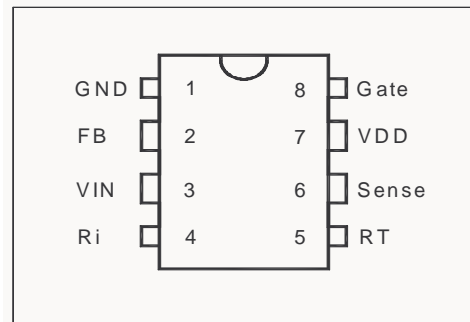


MARKING DIAGRAMS



T: D = DIP, S = SOP
 P: Z = Lead Free
 N = regular package
 XXXXXXX: Wafer Lot
 YY: Year; WW: Week
 V: Assembly Location

PIN CONFIGURATION



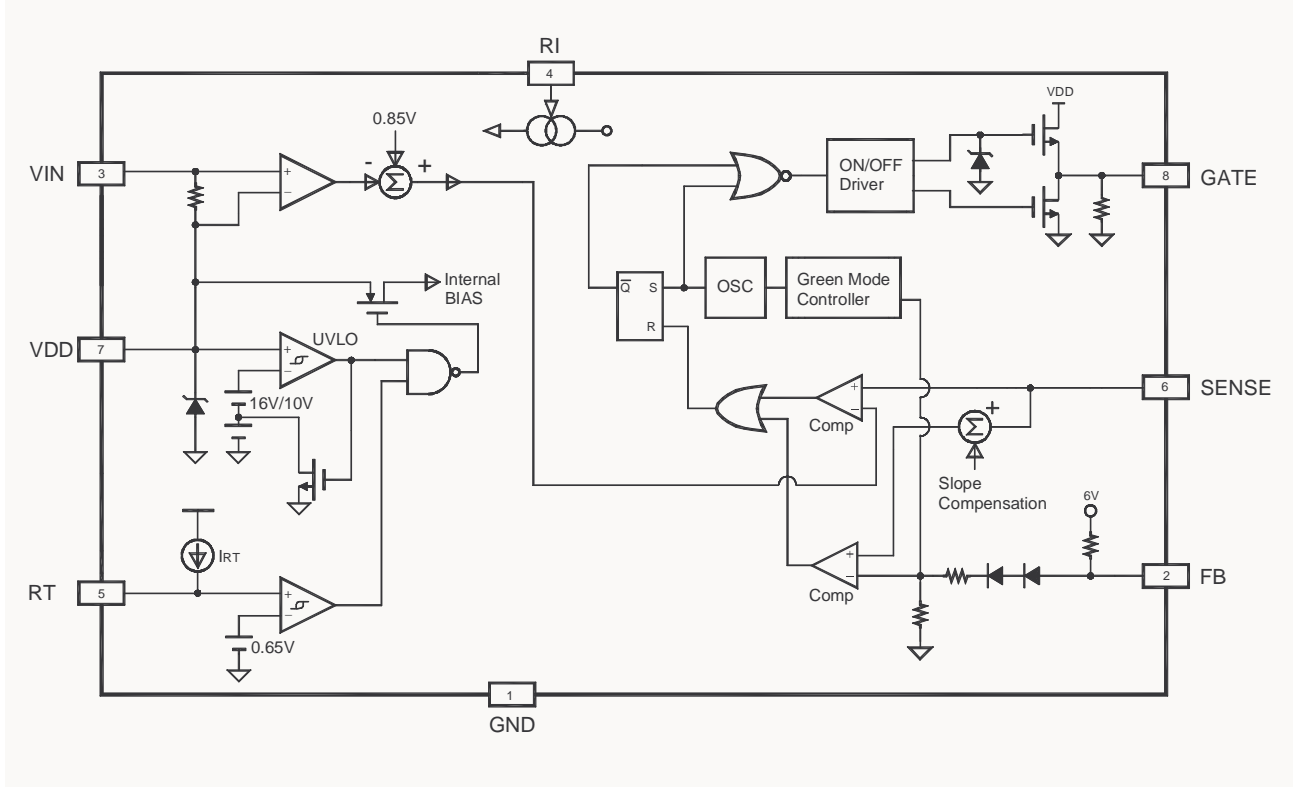
ORDERING INFORMATION

Part Number	Package
SG6840S	8-Pin SOP
SG6840D	8-Pin DIP
SG6840SZ	8-Pin SOP(Lead Free)
SG6840DZ	8-Pin DIP(Lead Free)

PIN DESCRIPTIONS

Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	Feedback. The FB pin provides the information used to regulate the power supply. The PWM duty cycle is controlled by the FB pin.
3	VIN	Start-up Current Input	The start-up current input. A start-up resistor is connected from the line-input to this pin. For an off-line converter, a typical resistance would be 1.5M. The start-up resistor can be adjusted to vary the line voltage compensation. The line voltage compensation is used to maintain a constant output power limit.
4	Ri	Reference Setting	Reference setting. The typical voltage is 1.3V. To generate a constant current for the SG6840, connecting a resistor to ground is suggested. Increasing the resistance will decrease the current and reduce the switching frequency. Typically, Ri = 26KΩ.
5	RT	Temperature Protection	Over temperature protection. A constant current is sourced out. An NTC thermistor is connected from this pin to ground to sense the temperature. When the voltage of this pin goes below the limit, over temperature protection will be enabled.
6	SENSE	Current Sense	Current sense. This pin senses the voltage across a sense resistor. When the voltage reaches the internal threshold, PWM output is disabled. In this manner, the controller provides over current protection.
7	VDD	Power Supply	Power supply.
8	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	30	V
	Zener Clamp	32	V
	Zener Current	10	mA
I _{out}	Gate Output Current	500	mA
V _{FB}	Input Voltage to FB Pin	-0.3 to 7V	V
V _{Sense}	Input Voltage to SENSE Pin	-0.3 to 7V	V
V _{RT}	Input Voltage to RT Pin	-0.3 to 7V	V
V _{RI}	Input Voltage to Ri Pin	-0.3 to 7V	V
P _d	Power Dissipation	1	W
R θ j-a	Thermal Resistance Junction-Air		
	DIP	82.5	°C/W
	SOP	141	
T _J	Junction Operating Temperature	150	°C
T _A	Ambient Operating Temperature	-25 to 85	°C
T _{stg}	Storage Temperature Range	-55 to +150	°C
	ESD Capability, HBM Model	3.0	kV
	ESD Capability, Machine model	300	V

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	<20	V
T _a	Operating Ambient Temperature	-20 to +85	°C
R _i	Current Source Setting	26	k Ω

ELECTRICAL CHARACTERISTICS
Feedback Input Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
A _V	Input Voltage to Current-Sense Attenuation		1/4.5	1/5	1/5.5	V/V
Z _{FB}	Input Impedance		3	4.5	6	k Ω
I _{FB}	Bias Current				2	mA
V _{oz}	Zero Duty-Cycle Input Voltage				1.2	V

Current Sense Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Zcs	Input Impedance		8	12	16	KΩ
T _{PD}	Delay to Output			150	200	nsec
V _{th}	Threshold Voltage for Current Limiting	I _{VIN} = 0 uA	0.8	0.85	0.9	V
ΔV _{TH @ I_{VIN}}	Threshold Voltage Change versus the Input Current of V _{IN}	I _{VIN} = 220 uA	-0.09	-0.15	-0.21	V
V _{SENSE0}	Threshold voltage for I _{VIN} = 80uA	I _{VIN} = 80 uA	0.73	0.81	0.89	V

Oscillator Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F _{OSC}	Frequency	R _I =26KΩ	60	65	70	KHz
F _{OSC-GREEN}	Green-Mode Frequency	R _I =26KΩ		10	15	KHz
V _G	Green-Mode Voltage (V _G = V _{FB} - V _D)			1.3		V
V _N	Normal-Mode Voltage (V _N = V _{FB} - V _D) (V _N = 4 V for a Maximum Duty Cycle)		1.7	2	2.3	V
S _G	Slope for Green-Mode Modulation	R _I =26KΩ	50	80	120	Hz/mV
F _{DV}	Frequency Variation versus V _{DD} Deviation	V _{DD} =10 to 20V			5	%
F _{DT}	Frequency Variation versus Temp. Deviation	T _A =-25 to 85 °C			5	%

PWM Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DC _(MAX)	Maximum Duty Cycle		75	80	90	%
DC _(MIN)	Minimum Duty Cycle		-	-	0	%
Bnk	Leading-Edge Blanking Time		200	270	350	nsec

Output Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{OL}	Output Voltage Low	V _{DD} = 12V, I _o = 150mA			1.5	V
V _{OH}	Output Voltage High	V _{DD} = 12V, I _o = 50mA	8V			V
t _r	Rising Time	V _{DD} =13V, C _L =1nF	150	250	350	nsec
t _f	Falling Time	V _{DD} =13V, C _L =1nF	30	50	90	nsec

Under-voltage Lockout Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{TH(ON)}	Start Threshold Voltage		15	16	17	V
V _{DD(min)}	Minimum Operating Voltage		9	10	11	V

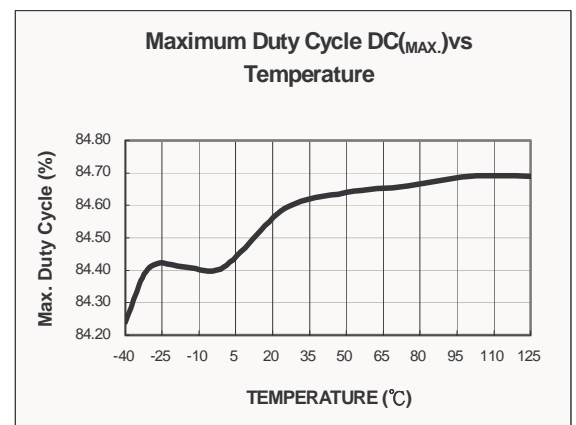
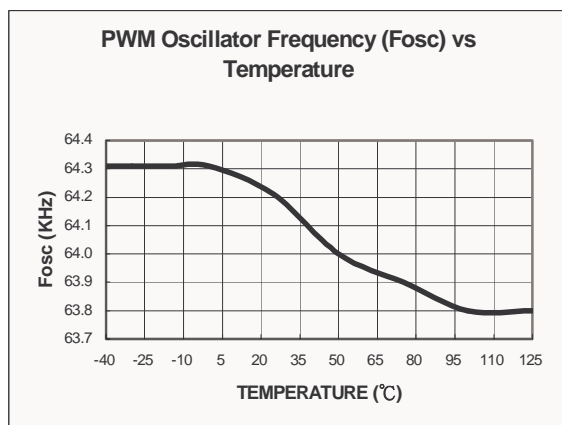
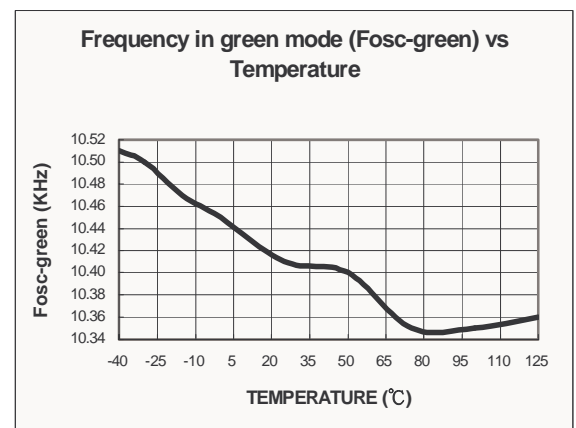
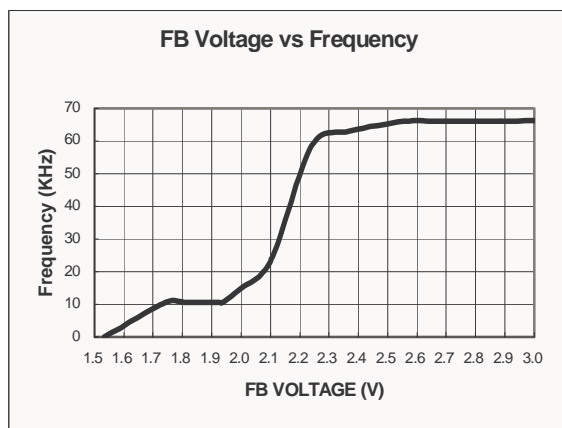
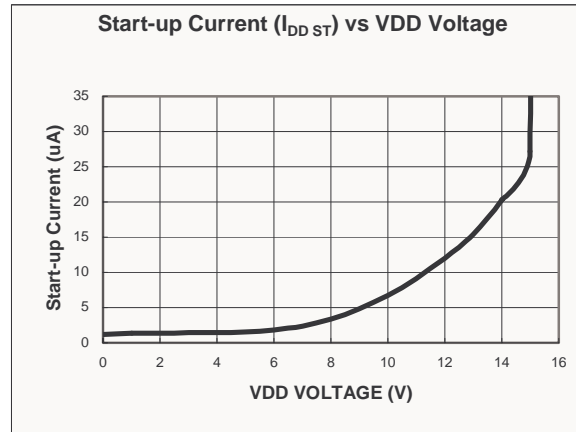
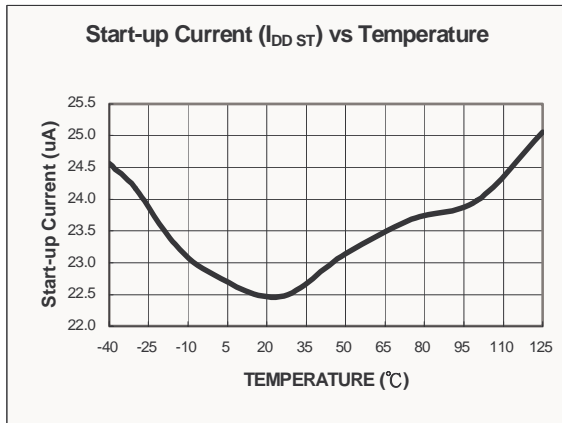
Over-Temperature Protection Section

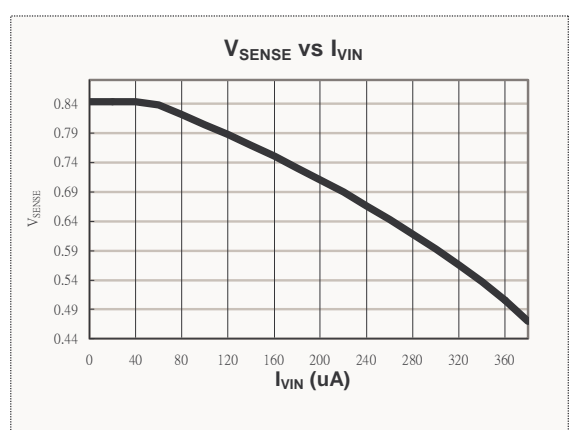
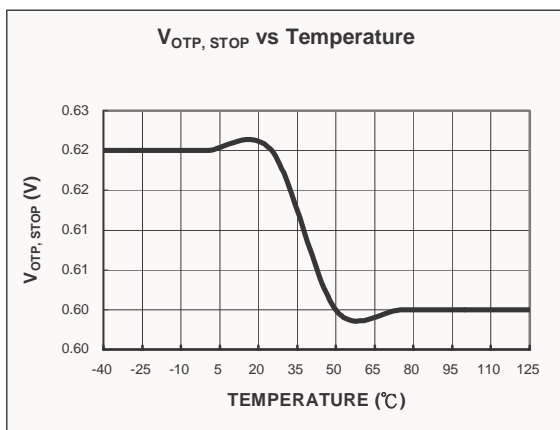
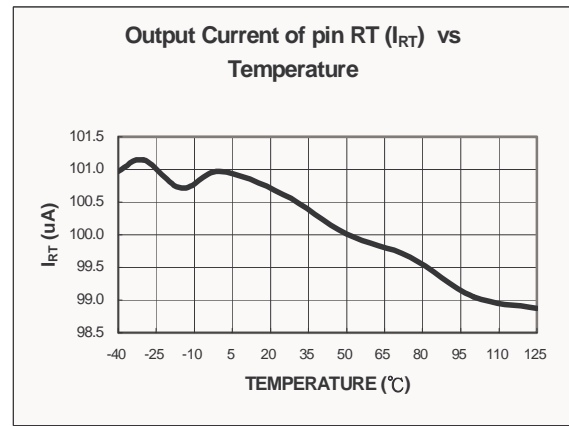
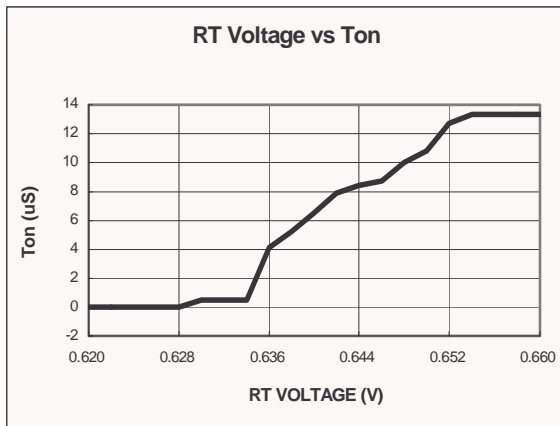
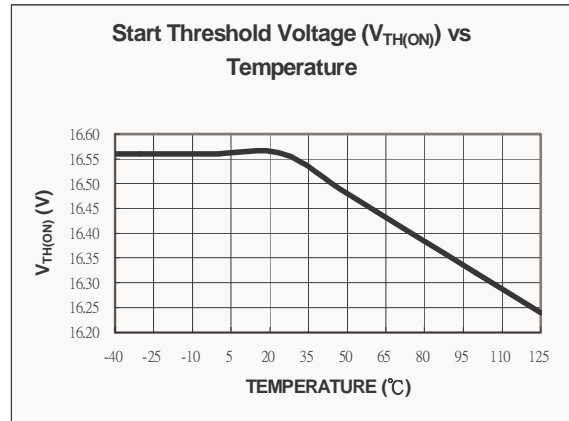
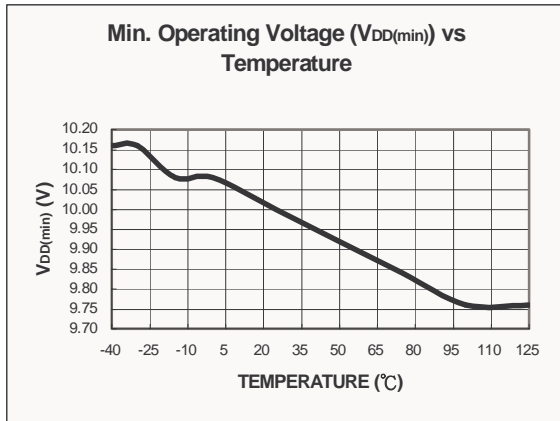
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{RT}	Output Current from the RT Pin	$R_T=26K\Omega$	92	100	108	μA
$V_{OTP,STOP}$	Over Temperature Protection Threshold Voltage Turn-Off Point. The Duty Cycle is Reduced to 0%		0.585	0.62	0.655	V
$V_{OTP,START}$	Over Temperature Protection Threshold Voltage. Starting point. The Duty Cycle Starts to Decrease			0.65		V

Total Standby Current Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{DD,ST}$	Start-up Current	$V_{DD}=14.5V$		30	40	μA
$I_{DD,OP}$	Operating Supply Current	$V_{FB} = SENSE = 0V$ $GATE = 1000pF$ $V_{DD} = 15.5V$	-	3	5	mA

TYPICAL CHARACTERISTICS





OPERATION DESCRIPTION

Start-up Current

The typical start-up current is only 30uA. This ultra-low start-up current allows users to use a high resistance, and low-wattage, start-up resistor to supply the start-up power required by the SG6840. A 1.5 MΩ, 0.25W, start-up resistor and a 10uF/25V V_{DD} hold-up capacitor would be sufficient for an AC-to-DC power adapter with a wide input range (100V_{AC} to 240V_{AC}).

Operating Current

The operating current has been reduced to 3mA. The low operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

The patented green-mode function provides off-time modulation to reduce the switching frequency under light-load and zero-load conditions. The feedback voltage, which is supplied by the voltage feedback loop, is compared to a reference voltage. Once the feedback voltage falls below the threshold voltage, the switching frequency will be linearly reduced until it reaches the minimum green-mode frequency (around 10kHz, if R_i=26kΩ).

Most of the power losses of the power supply are due to the switching loss of the transistor, the core loss of the transformer and inductors, and the power loss of the snubber, etc. The power losses from each of these sources are proportional to the switching frequency. Therefore, the off-time modulation of the PWM controller can significantly reduce the power consumption of the power supply under light-load and zero-load conditions. Under normal-load and high-load conditions, the PWM frequency is at its maximum (about 65kHz, with R_i=26kΩ), and it is not affected by off-time modulation.

Oscillator Operation

An external resistor R_i determines the PWM oscillation frequency. Using a 26kΩ resistor for R_i will result in a 50uA constant current I_i and a 65kHz switching frequency.

$$I_i \text{ (mA)} = 1.3V / R_i \text{ (k}\Omega\text{)}$$

$$f_{\text{PWM}} = \frac{1690}{R_i \text{ (k}\Omega\text{)}} \text{ (kHz)}$$

The SG6840 is designed to operate at PWM oscillation frequencies in the range of 50kHz ~ 100kHz.

Current Sensing and PWM Current

Limiting

The SG6840 has two feedback loops for the purposes of load regulation. The first feedback loop is used to regulate voltage, and the second feedback loop is used to regulate current. The SG6840's current-sense input is designed for current-mode control. A current-to-voltage conversion is done externally through a current-sense resistor R_s. Under normal operation, the FB voltage V_{FB} controls the peak voltage across the sense resistor R_s. The PWM duty cycle can be calculated according to the following equation:

$$I_{\text{pk}} = (V_{\text{FB}} - 1.4) / 5R_s$$

In the above equation, V_{FB} is the voltage of the FB pin and the dividing ratio of the external resistor is 5.

Under heavy-load conditions, the secondary-side DC output voltage will decrease. In response, the FB voltage V_{FB} will be increased so that the PWM duty cycle increases. The SG6840 will ensure that the response will be sufficient to regulate the output voltage of secondary-side back to its normal voltage. The inverting input of the SG6840's current-sense comparator is internally clamped to a variable voltage of around 0.85V (see the Constant Output Power Limit section). Current limiting occurs if the voltage of SENSE pin exceeds this 0.85V threshold value, such

Highly Integrated Green-Mode PWM Controller

SG6840

that $I_{pk}(\max) = 0.85V/R_s$. The magnitude of the resistance of the sense resistor R_s determines the maximum power limit. A larger resistance will result in a smaller I_{pk} and correspondingly, a lower power limit.

Leading Edge Blanking

Each time the power MOSFET is switched on, a leading spike occurs, due to the parasitic capacitance. To avoid premature termination of the switching pulse, this leading-edge spike is blanked out by a delay of 270 nsec. During this time period, the current-limit comparator is disabled and cannot switch off the gate drive regardless of how large the SENSE voltage is.

Under Voltage Lockout (UVLO)

The UVLO (Under Voltage Lockout) function ensures that the supply voltage V_{DD} will be adequate for the SG6840 to fully function before enabling the output stage. The turn-on and turn-off threshold voltages are fixed internally at 16V/10V. The hysteresis voltage between turn-on and turn-off prevents V_{DD} from being unstable during power on/off sequencing. The start-up current is typically 30uA. This enables efficient bootstrapping from the rectified input, for use with an offline converter. During normal operation, an auxiliary winding of the transformer supplies V_{DD} . At start-up, the V_{DD} hold-up capacitor C_{IN} must be charged-up to 16V through the start-up resistor R_{IN} , before enabling the output switch.

With an ultra-small start-up current of 30uA, R_{IN} can be as large as 1.5 M Ω and still be used to charge-up the hold-up capacitor C_{IN} , even when $V_{AC} = 90V_{rms}$. The power dissipation of this large resistance R_{IN} would then be less than 70mW (0.07W) even under high line ($V_{AC} = 240V_{rms}$) conditions. Under normal operation, the supply voltage V_{DD} is generated from the transformer's auxiliary winding after the IC starts up. The supply voltage V_{DD} is used to supply the operating current of the SG6840.

Gate Output / Soft Driving

The SG6840 BiCMOS output stage is a fast totem pole gate driver, which is designed to avoid cross-conduction currents. This minimizes heat dissipation, increases efficiency, and enhances

reliability. The output driver is clamped by an internal 18V Zener diode to improve control over the power MOSFET transistors, and to protect them against undesirable over-voltage gate signals. By controlling the rising time of the switch-on waveform and the falling shape of the switch-off waveform, the output stage is optimized to reduce switching noise, improve EMI, and to provide a stable MOSFET gate drive.

Built-in Slope Compensation

Current mode control regulates the peak transformer/inductor current via the current control loop. In continuous-mode operation, the current is the average current, and it is composed of both AC and DC components. Since the output is proportional to the average, not the peak current, this causes oscillations when the input voltage changes. Adding slope compensation to the current loop (reducing the current loop gain) to correct the problem is a simple approach. The SG6840 inserts a synchronized 0.33V positively-sloped ramp at every switching cycle to stabilize the current loop. The compensating voltage V_{s-comp} is equal to 0.33V.

Constant Output Power Limit

Whenever the SENSE voltage across the sense resistor R_s exceeds the threshold voltage (around 0.85V), the output GATE drive is turned off following a short propagation delay t_D . Since the propagation delay is constant regardless of the input line voltage V_{IN} , the output power will not be constant over the entire input voltage V_{IN} range (90Vrms to 265Vrms). To compensate for this, the internal threshold voltage is adjusted through the VIN pin. The adjustment depends on the input line voltage V_{IN} . The threshold voltage decreases from 0.85V to a smaller voltage when the input line voltage V_{IN} increases. A smaller threshold voltage at a higher input line voltage will force the output GATE drive to terminate earlier. This will reduce the total PWM turn-on time and make the output power equal to that at the low input line voltage.

Thermal Protection

A constant current I_{RT} is output from the RT pin. The resistor pin R_i determines the amplitude of the current I_{RT} .

$$I_{RT} = 2 \times (1.3V / R_i)$$

An NTC thermistor R_{ntc} in series with a resistor R_a can be connected from the RT pin to ground. Over temperature protection is enabled when the following condition occurs:

$$I_{RT} \times (R_{ntc} + R_a) < 0.65V$$

When the voltage of the RT pin is less than 0.65V ($V_{OTP,START}$) due to a high ambient temperature, the PWM duty cycle will start decreasing. Reducing the PWM duty cycle will also reduce the SMPS power output level, such that the temperature will start to decrease. If the over heating situation gets worse and the temperature continues climbing, the RT voltage will decrease still further to 0.62V ($V_{OTP,STOP}$). In that

case, the PWM duty cycle will drop to 0% and the SMPS will be completely turned off.

Noise immunity

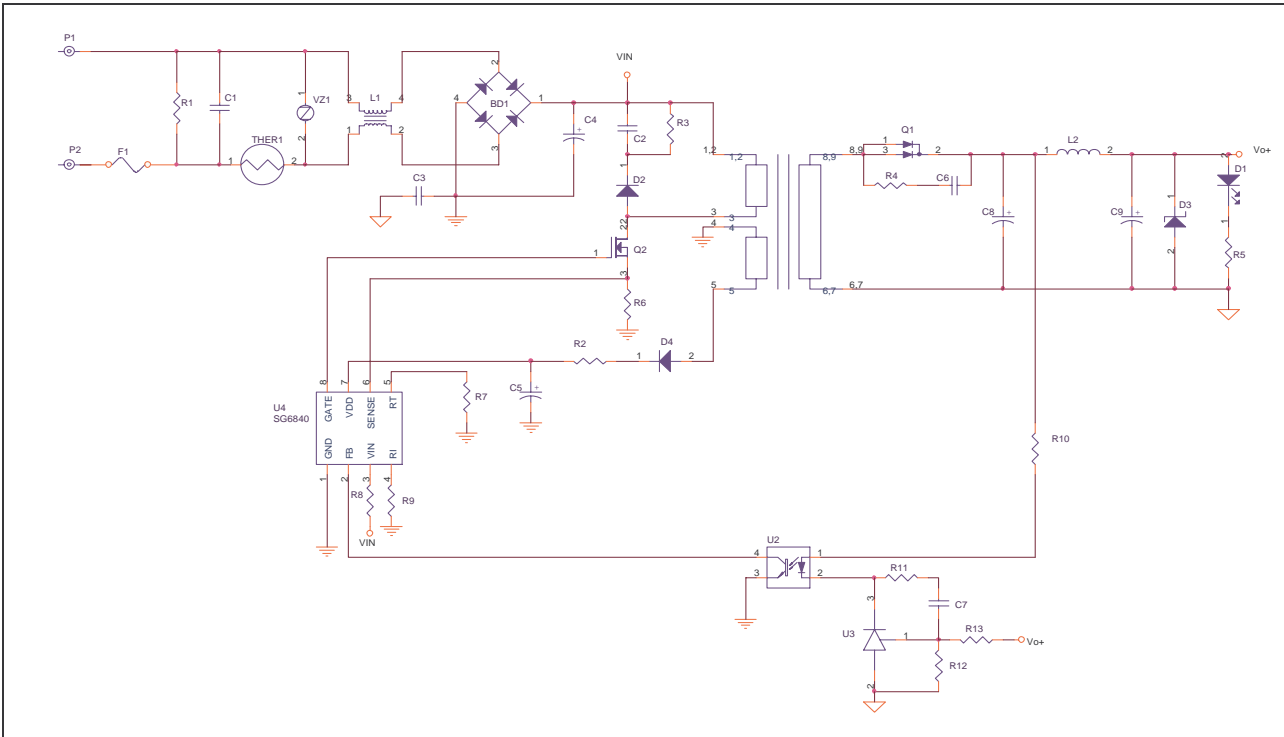
Noise from the current sense or the control signal can cause significant pulse width jitter, particularly in continuous-mode operation. While slope compensation helps alleviate these problems, further precautions should still be taken.

The SG6840 has a single ground pin. A high sink current from the output therefore cannot be returned separately. Good high frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate components such as R_i , R_s , and the VDD capacitor near the SG6840.

Most noise-related problems are due to the output (pin 8) being pulled below ground at turn-off by the external parasitic. This is particularly true when driving a MOSFET. A resistor ($10\Omega \sim 20\Omega$) connected in series from the output (pin 8) to the gate of the MOSFET will prevent such output noise.

REFERENCE CIRCUIT

Circuit

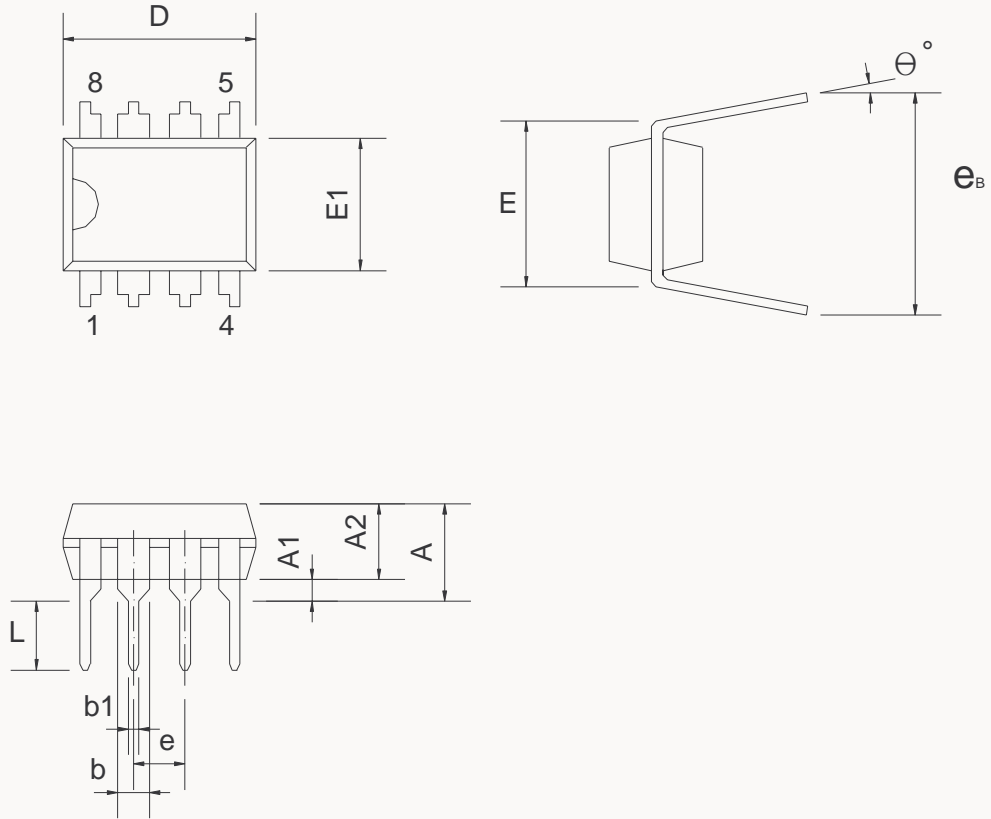


BOM

Reference	Component	Reference	Component
BD1	BD 1A/600V	Q2	MOS 2A/600V
C1	XC 0.22u	R1,R2	R 470KΩ 1/4W
C2	EC 0.1u 250V	R3	R 47Ω 1/4W
C3,C6,C7	YC 222p	R4	R 22Ω 1/4W
C4	EC 68u/400V	R5	R 4.7KΩ 1/4W
C5	CC 102p/1KV	R6	R 0.5Ω 1W
C8	EC 1200u/16V	R8,R12	R 510KΩ 1/4W
C9	EC 680u/16V	R9	R 20KΩ 1/8W 1%
C10	EC 10u/25V	R10	R 100Ω 1/8W
D1	LED	THER1	Thermistor SCK054
D3	ZD 12V	T1	Transformer EI28
F1	FUSE 2A/250V	U1	IC SG6840
L1	UU10.5	U2	IC 4N35D
L2	L04	U3	IC TL431
Q1	DIODE	VZ1	VZ 9G

PACKAGE INFORMATION

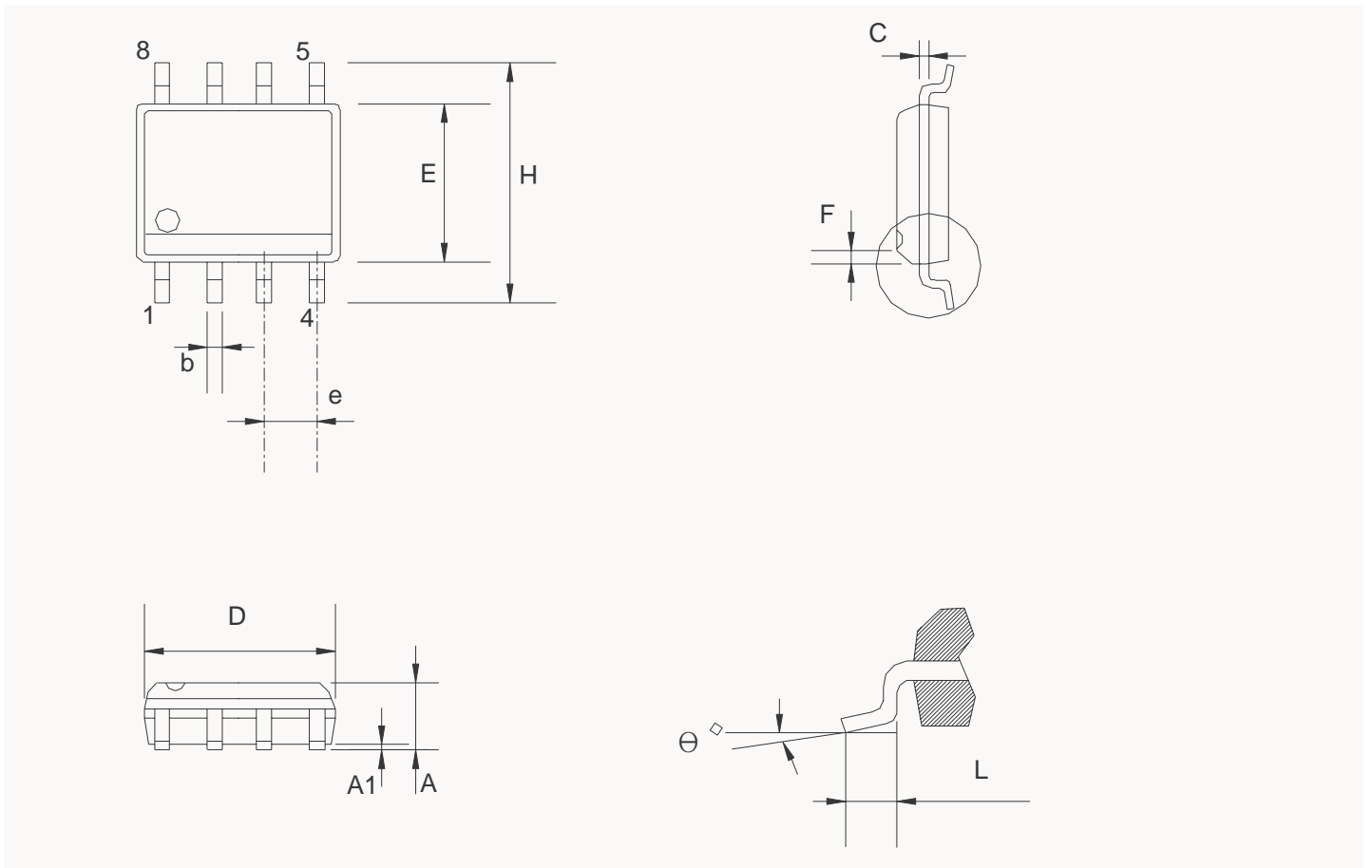
8 PINS-DIP(D)



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e _B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

8 PINS-SOP(S)



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	0.381		3.987	0.150		0.157
e		1.270			0.050	
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

DISCLAIMERS

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