Highly-Integrated Green-Mode PWM Controller **SG6842J**

FEATURES

- Green-mode PWM Controller
- Low Start-Up Current (8uA)
- Low Operating Current (4mA)
- Programmable PWM frequency with Jittering
- Peak-current-mode Operation
- Cycle-by-Cycle Current Limiting
- Synchronized Slope Compensation
- Leading-Edge Blanking
- Constant Output Power Limit (Full AC Input Range)
- VDD Over Voltage Protection (OVP)
- Programmable Over Temperature Protection (OTP)
- Internal Latch Circuit (OTP, OVP) Options
- Internal Open-loop Protection

APPLICATIONS

General-purpose switch mode power supplies and flyback power converters, including:

- Notebook Power Adapters
- Open-Frame SMPS

DESCRIPTION

The highly integrated SG6842J series of PWM controllers provides several features to enhance the performance of flyback converters.

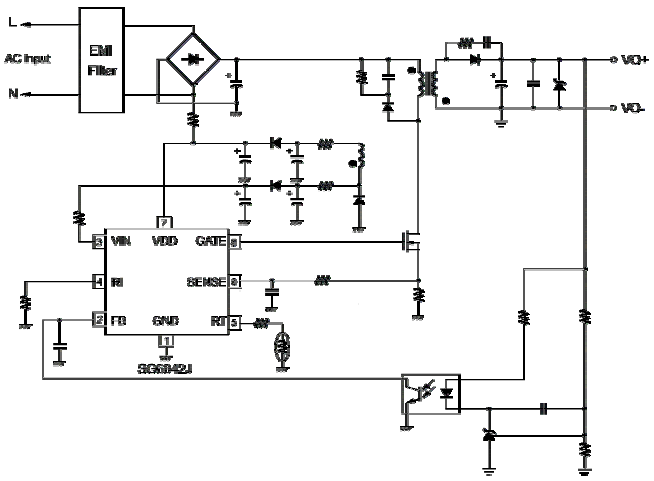
To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency at light-load conditions. To avoid acoustic-noise problem, the minimum PWM frequency set above 20kHz. This green-mode function enables the power supply to easily meet international power conservation requirements. To further reduce power consumption, SG6842J is manufactured by using the BiCMOS process. This allows the lowest start-up current around 8uA, and the operating current is only 4mA. As a result, large start-up resistance can be used.

SG6842J integrates frequency jittering function internally. The frequency jittering function helps reduce EMI emission of a power supply with minimum line filters. Also, its built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide AC input voltages, from 90VAC to 264VAC.

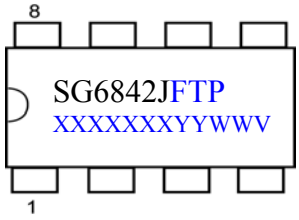
SG6842J provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open loop or output short-circuit failure occurs. PWM output is disabled till V_{DD} drops below the UVLO lower limit. Then, the controller starts up again. As long as V_{DD} exceeds about 24V, the internal OVP circuit is triggered. An external NTC thermistor can be applied for over-temperature protection. For OVP and OTP, the protection mode can be chosen to be latch off or auto recovery.

SG6842J is available in an 8-pin DIP or SOP package.

TYPICAL APPLICATION

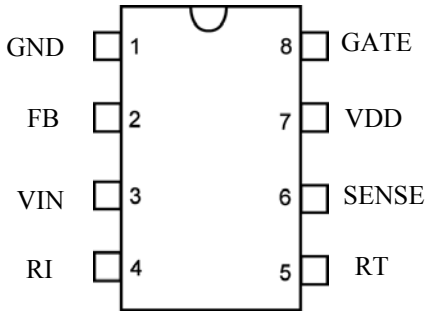


MARKING DIAGRAMS



F: L = OTP Latch, C = OTP auto-recovery
T: D = DIP, S = SOP
P : Z =Lead Free + ROHS Compatible
Null=regular package
XXXXXXX: Wafer Lot
YY: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



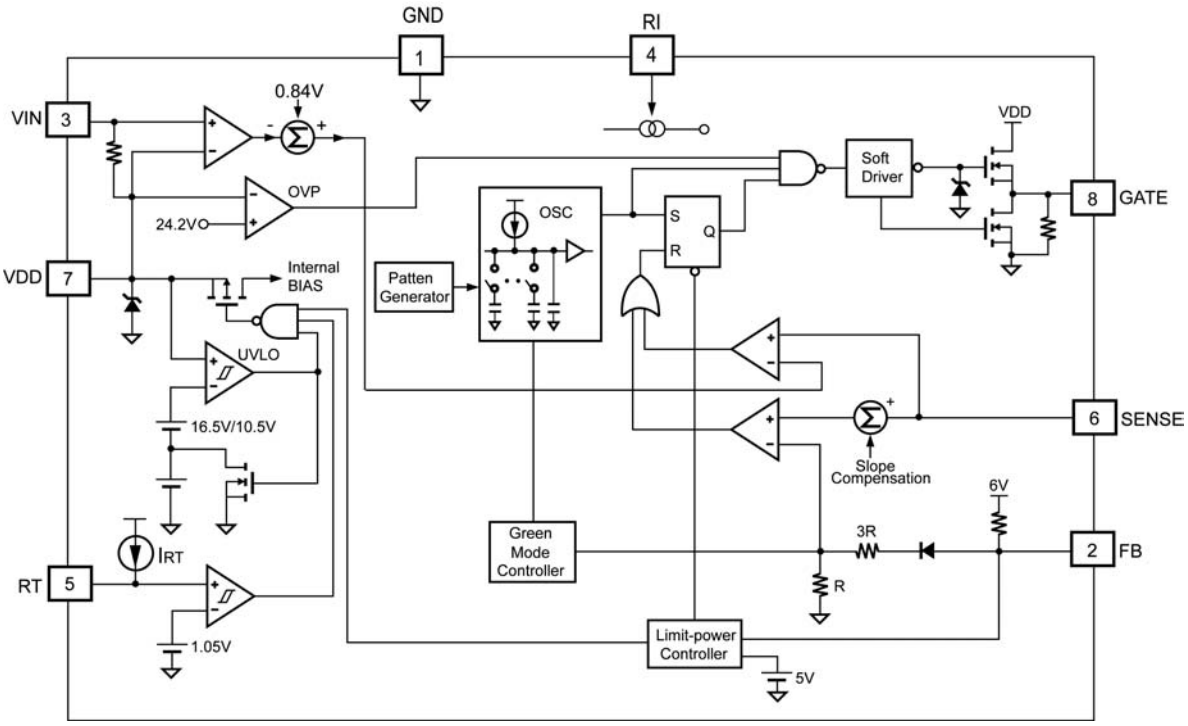
ORDERING INFORMATION

Part Number	OTP Latch	Package
SG6842JLSZ	Yes	8-Pin SOP (Lead Free)
SG6842JLDZ	Yes	8-Pin DIP (Lead Free)
SG6842JCSZ	No	8-Pin SOP (Lead Free)
SG6842JCDZ	No	8-Pin DIP (Lead Free)

PIN DESCRIPTIONS

Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2 FB		Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal from this pin and the current-sense signal from Pin 6. If FB voltage exceeds a threshold, the internal protection circuit will disable PWM output after a predetermined delay time.
3	VIN	Start-Up Input	For start-up, this pin is pulled high to the rectified line input via a resistor. Since the start-up current requirement of the SG6842J is very small, a large start-up resistance can be used to minimize power loss. Under normal operation, this pin is also used to detect the line voltage. As a result, constant output power limit over a universal AC input range can be achieved.
4	RI	Reference Setting	A resistor connected from the RI pin to GND pin will provide the SG6842J with a constant current source. This determines the center PWM frequency. Increasing the resistance will reduce PWM frequency. Using a 26kΩ resistor R_I results in a 65kHz center PWM frequency.
5	RT	Temperature Detection	For over-temperature protection. An external NTC thermistor is connected from this pin to GND pin. The impedance of the NTC will decrease at high temperatures. Once the voltage of the RT pin drops below a fixed limit , PWM output will be disabled.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power Supply	Power Supply. If VDD exceeds a threshold, the internal protection circuit will disable PWM output.
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET. It is internally clamped below 18V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Condition		Value	Unit
V_{DD}	Supply Voltage			25	V
V_{IN}	Input Terminal			30	V
V_{FB}	Input Voltage to FB Pin			-0.3 to 7V	V
V_{SENSE}	Input Voltage to SENSE Pin			-0.3 to 7V	V
V_{RT}	Input Voltage to RT Pin			-0.3 to 7V	V
V_{RI}	Input Voltage to RI Pin			-0.3 to 7V	V
P_D	Power Dissipation	at T_A < 50°C	DIP SOP	800 400	mW
$R_{\theta J-A}$	Thermal Resistance	Junction-Air	DIP SOP	82.5 141	°C/W
T_J	Operating Junction Temperature			-40 to +125	°C
T_{STG}	Storage Temperature Range			-55 to +150	°C
T_L	Lead Temperature (Soldering)	10 sec 10 sec	DIP SOP	260 230	°C

*All voltage values, except differential voltages, are given with respect to GND pin.

* Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING JUNCTION TEMPERATURE: -30°C ~ 85°C*

*For proper operation

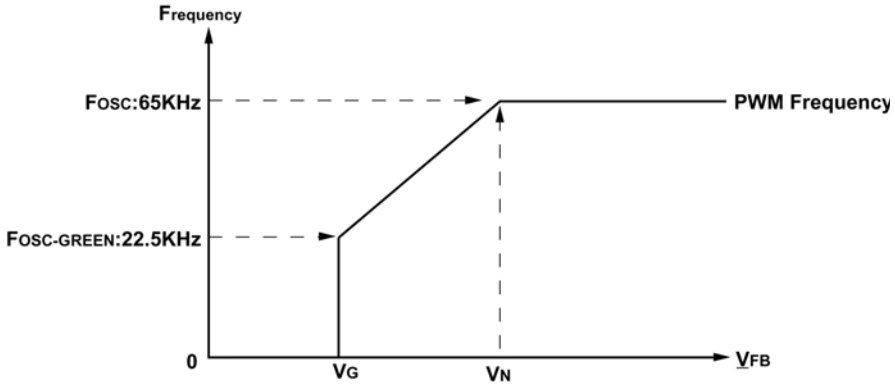
ELECTRICAL CHARACTERISTICS (VDD = 15V, T_A = 25°C, unless noted)

VDD Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OP}	Continuously Operating Voltage				22	V
V_{TH-ON}	Turn-on Threshold Voltage		15.5	16.5	17.5	V
V_{TH-OFF}	Turn-off Voltage		9.5	10.5 11.5	V	
I_{DD-ST}	Start-Up Current	V_{DD} = 15V, R_I = 26 kΩ GATE with 1nF to GND			30	uA
I_{DD-OP}	Operating Supply Current	GATE open		4	5	mA
V_{DD-OVP}	V_{DD} Over Voltage Protection		23.2	24.2	25.2	V
$T_{VDD-OVP}$	V_{DD} OVP Debounce Time	RI = 26kΩ		100		usec

RI Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
RI_{NOR}	R_I Operating Range		15.5		36	kΩ
RI_{MAX}	Max. R_I value for Protection			230		kΩ
RI_{MIN}	Min. R_I value for Protection			10		kΩ



Oscillator Section

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
F_{OSC}	Normal PWM Frequency	Center Frequency	R_I = 26kΩ	62	65	68	kHz
		Jitter Range		±3.7 ±4.2		±4.7	
T_{JTR} Jittering	Period		R_I = 26kΩ 3.9		4.4	4.9	mS
$F_{OSC-G-MIN}$	Green-Mode Min. Frequency		R_I = 26kΩ	18	22	25	kHz
F_{DV}	Frequency Variation Versus V_{DD} Deviation		VDD = 11.5V to 20V			5	%
F_{DT}	Frequency Variation Versus Temp. Deviation		T_A = -30 to 85 ℃			5	%

Feedback Input Section

Symbol Param eter		Test Condition	Min.	Typ.	Max.	Unit
A_V	FB Input to Current Comparator Attenuation	@Green mode	1/4.5	1/4	1/3.5	V/V
Z_{FB}	Input Impedance		4		7	kΩ
V_{HGH}	Output High Voltage	FB pin open	5.5			V
V_{FB-OL}	FB open-loop trigger level		5		5.4	V
T_{LPS}	FB open-loop Protection Delay	R_I = 26kΩ	50 56		62 mS	
V_N	Green-Mode Entry FB Voltage		1.9	2.1	2.3	V
V_G	Green-Mode Ending FB Voltage		V_N-0.6 V	$_N$-0.5 V	$_N$-0.4 V	
F_{G-TEST} Burst-Mode	test Frequency	V_G+20mV	$F_{OSC-G-MIN}$ +0.5			KHz
I_{ZERO}	PWM OFF FB Voltage				1.5	mA

Current Sense Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{CS}	Input Impedance		12			kΩ
V_{TH80}	Threshold voltage for current limit	I_{VIN} = 80uA, R_I = 26kΩ	0.81 0.84		0.87 V	
V_{TH160}	Threshold voltage for current limit	I_{VIN} = 160uA, R_I = 26kΩ	V_{TH80} -0.085	V_{TH80} -0.07	V_{TH80} -0.055	V
T_{PD}	Propagation Delay to GATE Output			100	200	nS
T_{LEB}	Leading Edge Blanking Time		260	360	460	nS
V_{SLOPE} Slope	Compensation	SENSE=2KΩ, Dut y = DCY_{MAX}	0.34 0.37		0.41 V	

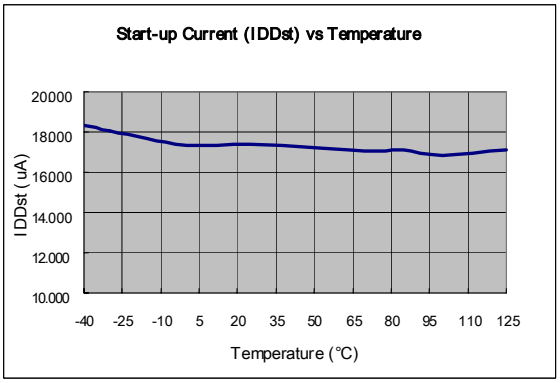
GATE Section

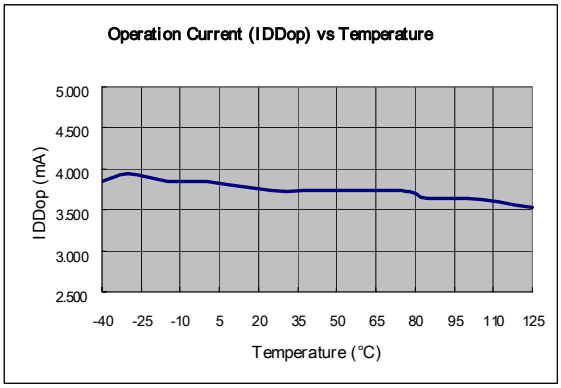
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DCY_{MAX}	Maximum Duty Cycle		80	85	90	%
V_{OL} Output	Voltage Low	V_{DD} =15V, I_O = 50mA			1.5	V
V_{OH} Output	Voltage High	V_{DD} =12V, I_O = 50mA	8V			V
T_R	Rising Time	V_{DD} =15V, C_L = 1nF	150	250	350	nS
T_F Fal	ling Time	V_{DD} =15V, C_L = 1nF	30	50	90	nS
I_O	Peak Output Current	V_{DD} =15V, GATE=6V	230			mA
V_{CLAMP}	Gate Output Clamping Voltage	VDD = 22V		18	19	V

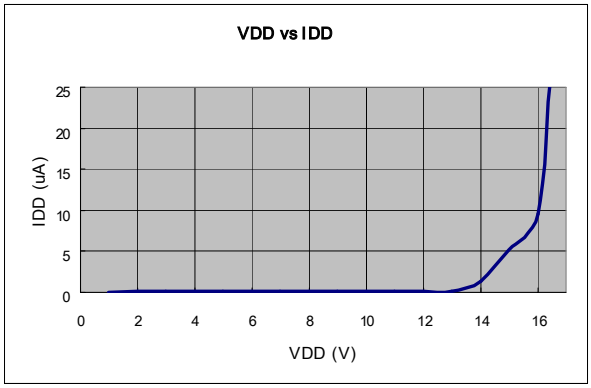
RT Section

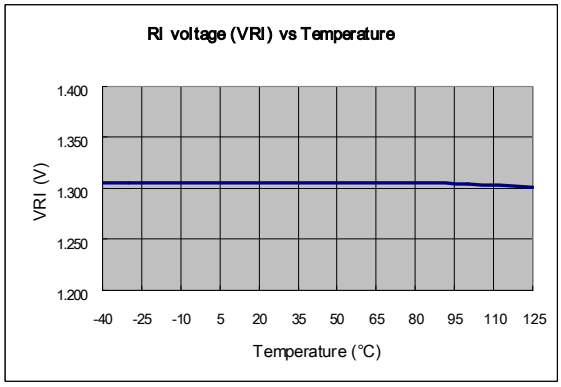
Symbol Param	eter	Test Condition	Min.	Typ.	Max.	Unit
I_{RT}	Output Current of RT pin	R_I = 26kΩ	67	70	73	uA
$V_{OTP-STOP}$	Trigger Voltage for Over-temperature Protection		1.015	1.05	1.085	V
$T_{OTP-LATCH}$	Over-temperature Latch-off Debounce.	R_I = 26kΩ, V_{RT}<0.7V 60		100	140	uS

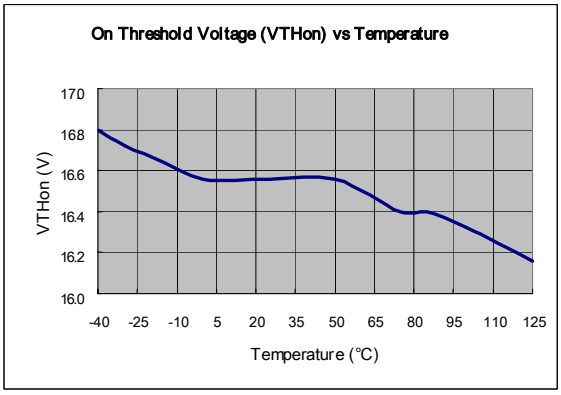
TYPICAL CHARACTERISTICS

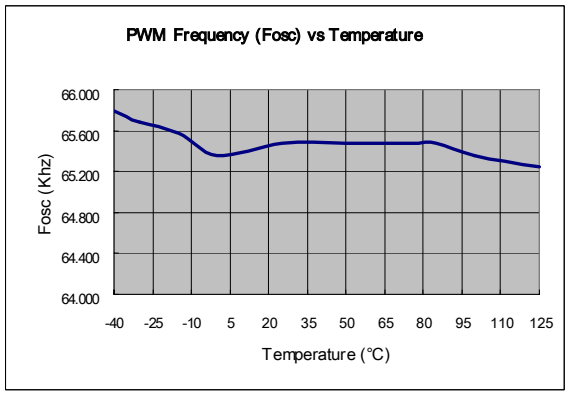


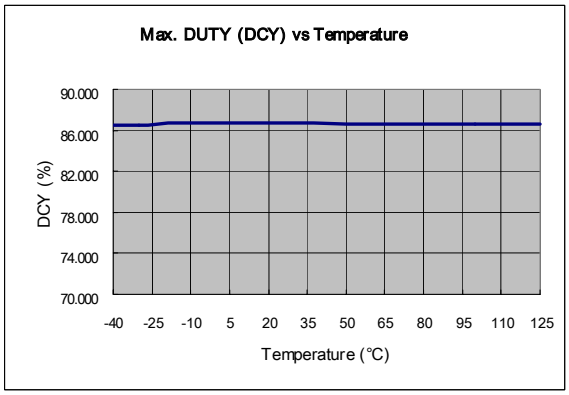


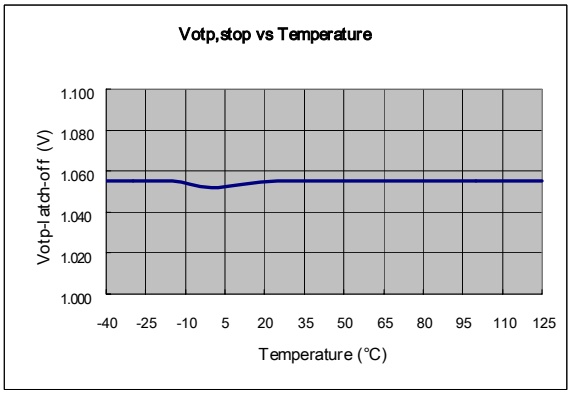


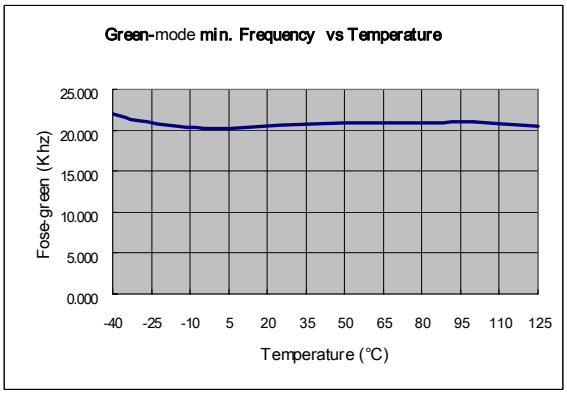


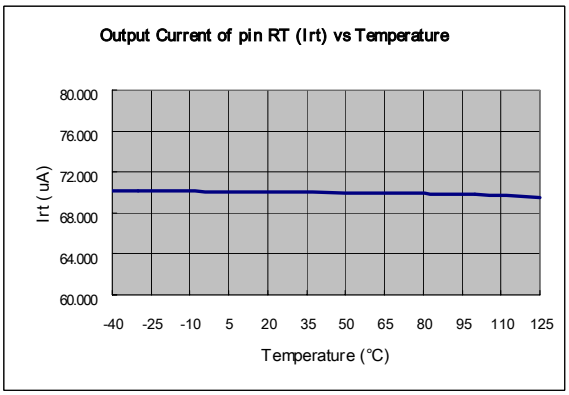


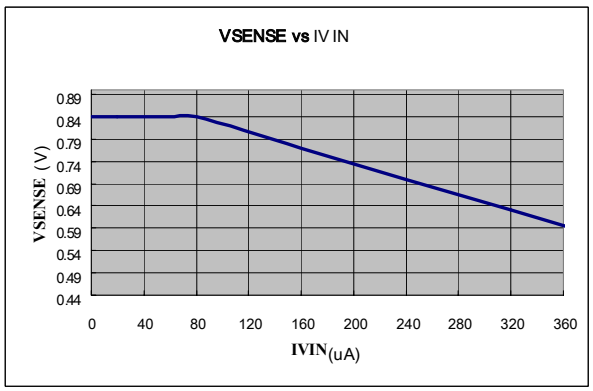


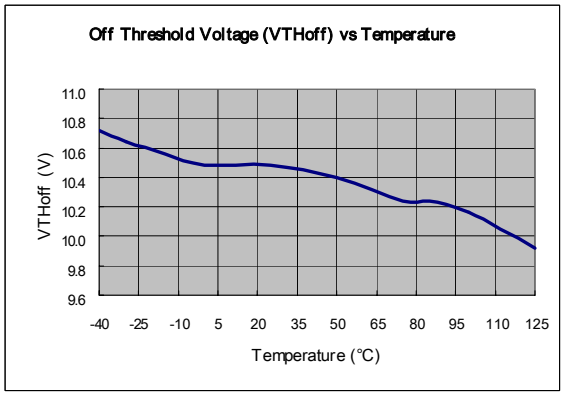

Max. DUTY (DCY) vs Temperature
DCY (%)
90.000
86.000
82.000
78.000
74.000
70.000
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)


Votp,stop vs Temperature
Votp-latch-off (V)
1.100
1.080
1.060
1.040
1.020
1.000
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)


Green-mode min. Frequency vs Temperature
Fose-green (Khz)
25.000
20.000
15.000
10.000
5.000
0.000
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)


Output Current of pin RT (Irt) vs Temperature
Irt (uA)
80.000
76.000
72.000
68.000
64.000
60.000
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)


VSENSE vs IV IN
VSENSE (V)
0.89
0.84
0.79
0.74
0.69
0.64
0.59
0.54
0.49
0.44
0 40 80 120 160 200 240 280 320 360
IVIN(uA)


Off Threshold Voltage (VTHoff) vs Temperature
VTHoff (V)
11.0
10.8
10.6
10.4
10.2
10.0
9.8
9.6
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (°C)

OPERATION DESCRIPTION

Start-Up Current

The typical start-up current is only 8uA. This allows a high resistance, low-wattage start-up resistor to be used, to minimize power loss. A 1.5 MΩ, 0.25W, start-up resistor and a 10uF/25V VDD hold-up capacitor would be sufficient for an AC/DC adapter with a universal input range.

Operating Current

The required operating current has been reduced to 4mA. This results in higher efficiency and reduces the VDD hold-up capacitance requirement.

Green-Mode Operation

The proprietary green-mode function provides off-time modulation to continuously decrease the PWM frequency under light-load conditions. To avoid acoustic-noise problem, the minimum PWM frequency set above 20kHz. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using a SG6842J controller can easily meet even the most restrictive international regulations regarding stand by power consumption.

Oscillator Operation

A resistor connected from the RI pin to GND pin generates a constant current source for the SG6842J controller. This current is used to determine the center PWM frequency. Increasing the resistance will reduce PWM frequency. Using a 26k Ω resistor R_I results in a corresponding 65kHz PWM frequency. The relationship between R_I and the switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (k\Omega)}(kHz) \quad \text{----------} \quad (1)$$

SG6842J also integrates frequency jittering function internally. The frequency variation ranges from around 61kHz to 69kHz for a center frequency 65kHz. The frequency jittering function helps reduce EMI emission of a power supply with minimum line filters.

$$I_{RT} = \frac{70uA}{R_I\ (k\Omega)} \bullet 26 \quad \text{----------} \quad (2)$$

Leading Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled, and it cannot switch off the gate drive.

Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 10.5V/16.5V. To enable a SG6842J controller during start-up, the hold-up capacitor must first be charged to 16.5V through the start-up resistor.

The hold-up capacitor will continue to supply VDD before energy can be delivered from the auxiliary winding of the main transformer. VDD must not drop below 10.5V during this start-up process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply VDD during start-up.

Gate Output / Soft Driving

The SG6842J BiCMOS output stage is a fast totem pole gate driver. Cross-conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET transistors from any harmful over-voltage gate signals. A soft driving waveform is implemented to minimize EMI.

Slope Compensation

The sensed voltage across the current sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. The built-in slope compensation

function improves power supply stability and prevents peak-current-mode control from causing sub-harmonic oscillations. Within every switching cycle, the SG6842J controller produces a positively sloped, synchronized ramp signal.

Constant Output Power Limit

When the SENSE voltage across the sense resistor R_S reaches the threshold voltage, the output GATE drive will be turned off following a small propagation delay T_{PD}. This propagation delay will result in an additional current proportional to $T_{PD}*V_{IN}/L_P$. The propagation delay is nearly constant regardless of the input line voltage V_{IN}. Higher input line voltages will result in larger additional currents. Thus, under high input-line voltages the output power limit will be higher than under low input-line voltages.

The output power limit variation can be significant over a wide range of AC input voltages. To compensate for this, the threshold voltage is adjusted by the current I_{IN}. Since the pin VIN is connected to the rectified input line voltage through the start-up resistor, a higher line voltage will result in a higher current I_{IN} through the pin VIN.

The threshold voltage decreases if the current I_{IN} increases. A small threshold voltage will force the output GATE drive to terminate earlier, thus reducing total PWM turn-on time, and making the output power equal to that of the low line input. This proprietary internal compensation feature ensures a constant output power limit over a wide range of AC input voltages (90VAC to 264VAC).

VDD Over-voltage Protection

VDD over-voltage protection has been built in to prevent damage due to over voltage conditions. When the voltage VDD exceeds the internal threshold due to abnormal conditions, PWM output will be turned off. Over-voltage conditions are usually caused by open feedback loops.

Limited Power Control

The FB voltage will increase every time the output of the power supply is shorted or over-loaded. If the FB voltage remains higher than a built-in threshold for longer than T_{LPS}, PWM output will then be turned off. As PWM output is turned off, the supply voltage VDD will also begin decreasing.

When VDD goes below the turn-off threshold (eg, 10.5V) the controller will be totally shut down. VDD will be charged up to the turn-on threshold voltage of 16.5V through the start-up resistor until PWM output is restarted. This protection feature will continue to be activated as long as the over-loading condition persists. This will prevent the power supply from overheating due to over loading conditions.

Protection Latch Circuit

For the SG6842J family, the built-in latch function provides a versatile protection feature that does not require external components. See ordering information for a detailed description. To reset the latch circuit, it is necessary to disconnect the AC line voltage of the power supply.

Thermal Protection

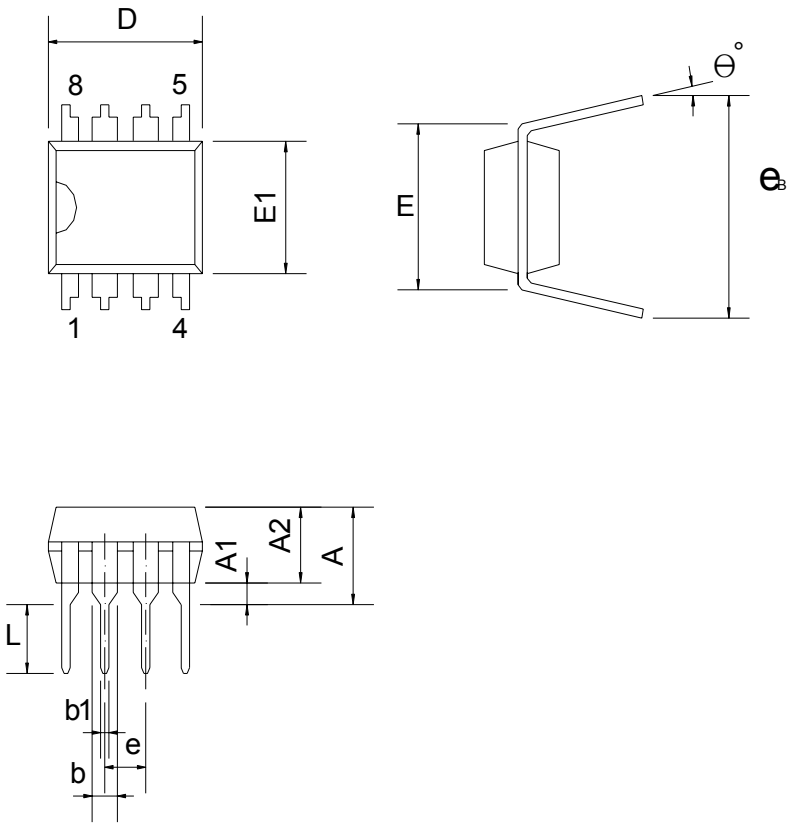
An external NTC thermistor can be connected from the RT pin to ground. A fixed current I_{RT} is sourced from the RT pin. Because the impedance of the NTC will decrease at high temperatures, when the voltage of the RT pin drops below 1.065V, PWM output will be disabled. The RT pin output current is related to the PWM frequency programming resistor R_I

Noise Immunity

Noise from the current sense or the control signal may cause significant pulse width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. The designer should avoiding long PCB traces and component leads. Compensation and filter components should be located near the SG6842J. Finally, increasing the power-MOS gate resistance is advised.

PACKAGE INFORMATION

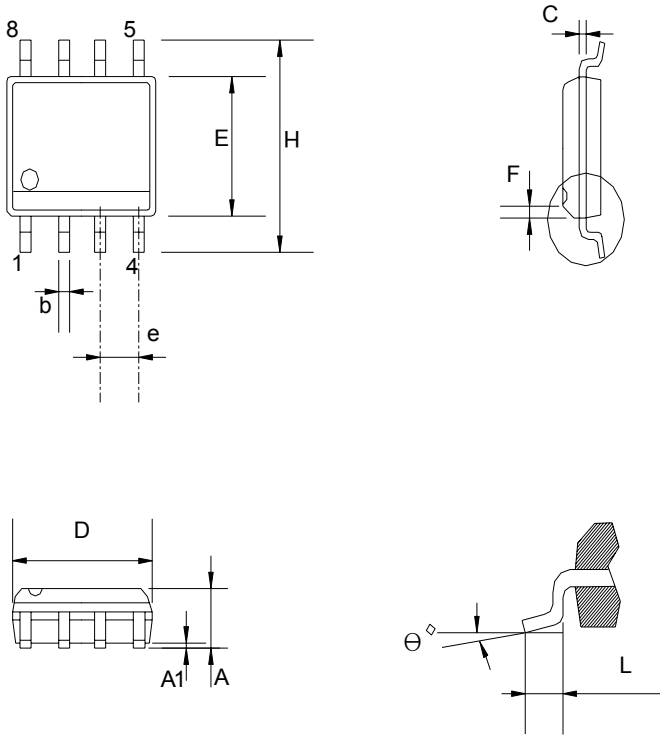
8PINS-DIP(D)



Dimensions

Symbol	Millimeters Inches					
	Min.	Typ. Max.		Min.	Typ. Max.	
A		5.334				0.210
A1	0.381	0.015				
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524	0.060			
b1		0.457	0.018			
D	9.017	9.271 10.160		0.355 0.365 0	400	
E		7.620	0.300			
E1	6.223	6.350 6.477 0	245 0.250 0.255			
e		2.540	0.100			
L	2.921	3.302 3.810 0	115 0.130 0.150			
eB	8.509	9.017 9.525 0	335 0.355 0.375			
θ°	0°	7° 15	°	0°	7° 15	°

8PINS-SOP(S)



Dimensions

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A 1.346			1.752	0.053		0.069
A1 0.101			0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D 4.648			4.978	0.183		0.196
E 3.810			3.987	0.150		0.157
e 1.016		1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H 5.791			6.197	0.228		0.244
L 0.406			1.270	0.016		0.050
θ°	0°	8	°	0°		8°

DISCLAIMERS

LIFE SUPPORT

System General's products are not designed to be used as components in devices intended to support or sustain human life. Use of System General's products in components intended for surgical implant into the body, or other applications in which failure of System General's products could create a situation where personal death or injury may occur, is not authorized without the express written approval of System General's Chief Executive Officer. System General will not be held liable for any damages or claims resulting from the use of its products in medical applications.

MILITARY

System General's products are not designed for use in military applications. Use of System General's products in military applications is not authorized without the express written approval of System General's Chief Executive Officer. System General will not be held liable for any damages or claims resulting from the use of its products in military applications.

RIGHT TO MAKE CHANGES

System General reserves the right to change this document and/or this product without notice. Customers are advised to consult their System General sales representative before ordering.