



SG6846

Highly Integrated Green-Mode PWM Controller

Features

- Low Startup Current: 8µA
- Low Operating Current: 3.7mA
- Peak-Current Mode of Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- V_{DD} Over-Voltage Protection (OVP)
- AC Input Brownout Protection with Hysteresis
- Constant Output-Power Limit (Full AC Input Range)
- Internal Latch Circuit for OVP, OTP, and OCP
- Two-level Over-Current Protection (OCP) with 96ms Delay Time
- Very Few External Components
- Programmable Over-Temperature Protection (OTP)

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output, such as for Printers, Scanners, Motor Drivers

Description

The highly integrated SG6846 series of PWM controllers provides several features to enhance the performance of flyback converters. To minimize standby-power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters burst-mode. This completely shuts off PWM output. The output restarts just before the supply voltage drops below the under-voltage lockout (UVLO) lower limit. This green-mode function enables power supplies to meet international power conservation requirements easily.

The SG6846 is designed especially for switch-mode power supply (SMPS) with surge-current output. It is incorporated with a two-level OCP function. Besides the cycle-by-cycle current limiting, if the switching current is higher than 2/3 of the peak-current threshold for a delay time, OCP is activated such that the SG6846 is totally shut down. Other protection functions include: AC-input brownout protection with hysteresis and V_{DD} OVP. For OTP, an external NTC thermistor can be applied to sense the ambient temperature. When OCP, V_{DD} OVP, or OTP are activated, an internal latch circuit is used to latch off the controller. The latch resets when the V_{DD} supply is removed.

Other features of this controller include built-in synchronized slope compensation and proprietary internal compensation for constant output-power limit over universal-AC-input range. Also, the gate output is clamped at 18V to protect the external MOSFET from over-voltage damage.

The SG6846 series controllers are available in both 8-pin dual in-line (DIP) and small outline (SOP) packages.

Ordering Information

Part Number	Operating Temperature Range	OTP Latch	Eco Status	Package	Packing Method
SG6846LSZ	-20 to +85°C	Yes	RoHS	8-Pin SOP	Tape & Reel
SG6846LSY	-20 to +85°C	Yes	Green	8-Pin SOP	Tape & Reel
SG6846LDZ	-20 to +85°C	Yes	RoHS	8-Pin DIP	Tube
SG6846LDY	-20 to +85°C	Yes	Green	8-Pin DIP	Tube

Typical Application

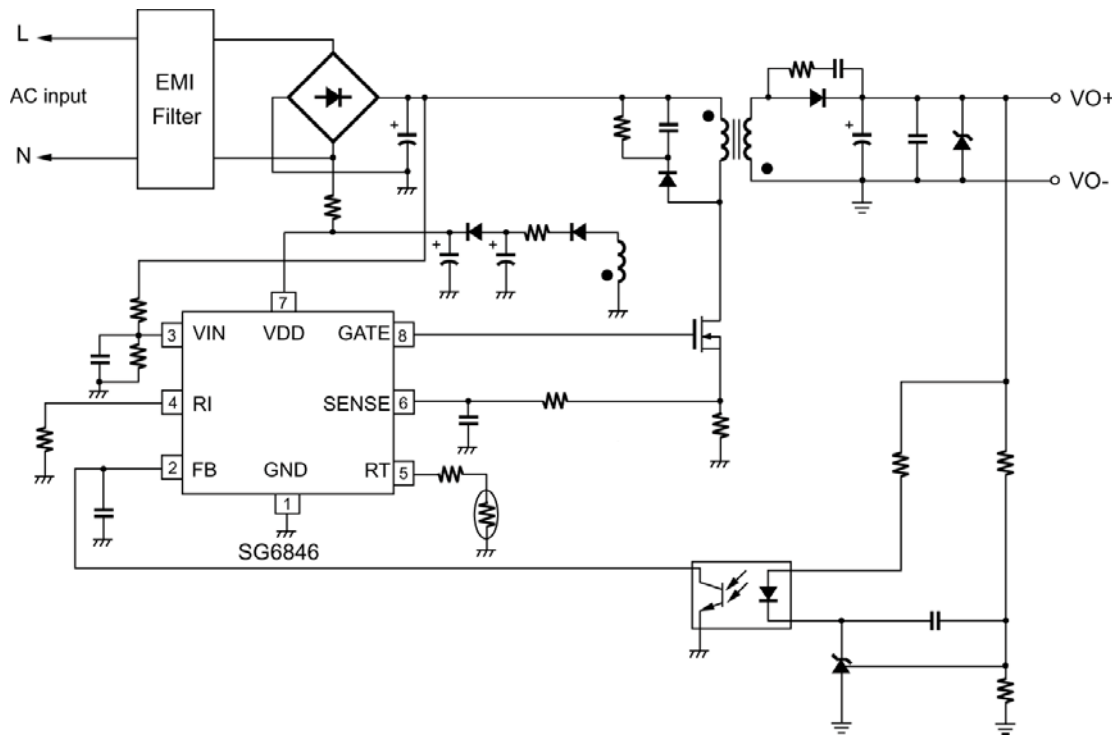


Figure 1. Typical Application

Block Diagram

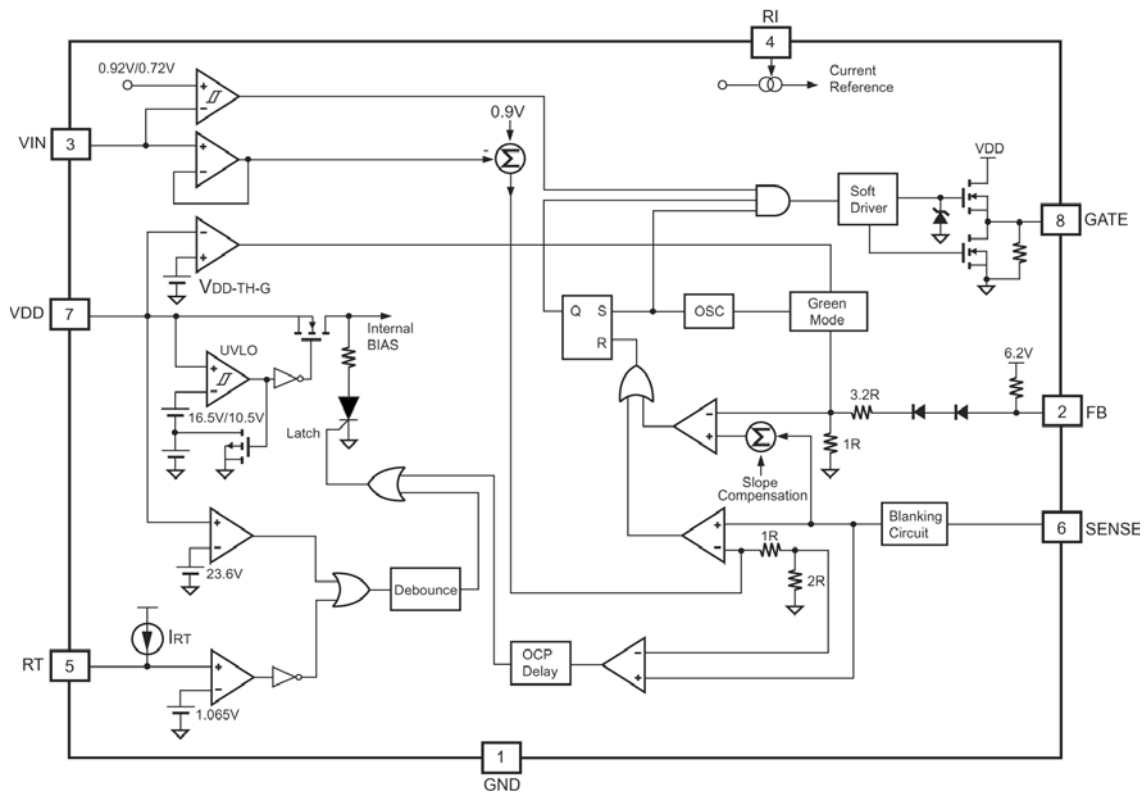
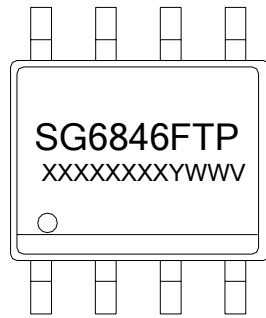


Figure 2. Block Diagram

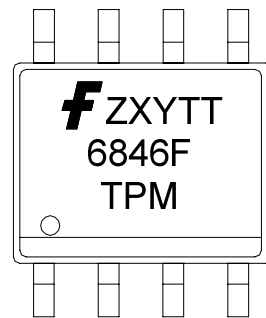
Marking Information



F: L = OTP Latch
T: D = DIP, S = SOP
P: Z = Lead Free + ROHS Compatible
 Null = Regular Package
XXXXXXXX: Wafer Lot
Y: Year; **WW**: Week
V: Assembly Location

※ Marking for SG6846LSZ (Pb-free)
 SG6846LDZ (Pb-free)

Figure 3. Top Mark 1



F: Fairchild logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
F: L = OCP Latch
T: Package Type (D = DIP, S = SOP)
P: Y = Green Package
M: Manufacturing Flow Code

※ Marking for SG6846LSY (Green-compound)
 SG6846LDY (Green-compound)

Figure 4. Top Mark 2

Pin Configuration

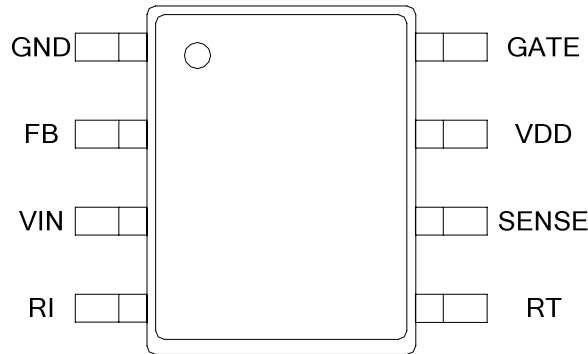


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The FB pin and the current-sense signal from Pin 6 determine the PWM duty cycle.
3	VIN	Line-Voltage Detection	Line-voltage detection. The line-voltage detection is used for brownout protection with hysteresis. Constant-output-power limit over universal-AC-input range is also achieved using the V_{IN} signal. It is suggested to add low-pass filter to filter out line ripple on bulk capacitor.
4	RI	Reference Setting	A resistor from the RI pin to ground generates a reference current source inside SG6846. This determines the switching frequency. Increasing the resistance reduces the switching frequency. Using a 26k Ω resistor RI results in a 65KHz switching frequency.
5	RT	Temperature Detection	For OTP. An external negative temperature coefficient (NTC) thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. Once the voltage of the RT pin drops below a threshold, PWM output is disabled.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting. If the switching current is higher than 2/3 of the peak-current threshold for longer than 96ms, OTP is activated. This two-level OCP feature is especially suitable for SMPS with surge current output.
7	VDD	Power Supply	Power Supply. The internal protection circuit disables PWM output in response to V_{DD} over voltage.
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET. A soft driving waveform is implemented for improved electromagnetic interference (EMI).

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Supply Voltage		25	V
V _L	Input Voltage to FB, SENSE, VIN, RT, RI Pins	-0.3	7.0	V
P _D	Power Dissipation	SOP	400	mW
		DIP	800	
R _{θJC}	Thermal Resistance Junction-to-Case)	SOP	41.2	°C/W
		DIP	67.1	
T _J	Operating Junction Temperature	-40	+125	°C
T _{STG}	Storage Temperature Range	-65	+150	°C
T _L	Lead Temperature, Wave Soldering, 10 Second		+260	°C
ESD	Human Body Model, JESD22-A114		2.0	kV
	Machine Model, JESD22-A115A		200	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T _A	Operating Ambient Temperature	-20	+85	°C

Electrical Characteristics

$V_{DD} = 15V$ and $T_A = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD} Section						
V_{DD-OP}	Continuously Operating Voltage				20	V
V_{DD-ON}	Turn-On Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Turn-Off Voltage		9.5	10.5	11.5	V
$V_{DD-TH-G}$	Low-Threshold Voltage for V_{DD} to Exit Green-OFF Mode			$V_{DD-OFF} + 1.25V$		V
V_{DD-LH}	Threshold Voltage for Latch-Off Release		3	4	5	V
I_{DD-ST}	Startup Current	$V_{DD-ON} - 0.16V$		8	30	μA
I_{DD-OP}	Operating Supply Current	GATE Open		3.7	5.0	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection (Latch Off)		22.6	23.6	24.6	V
$t_{D-VDDOVP}$	V_{DD} OVP Debounce Time	$R_I = 26k\Omega$		100		μs
I_{DD-H}	V_{DD} OVP Latch-Off Holding Current	$V_{DD} = 5V, T_A = 27^\circ C$		45		μA
V_{IN} Section						
V_{IN-OFF}	PWM Turn-Off Threshold Voltage		0.67	0.72	0.77	V
V_{IN-ON}	PWM Turn-On Threshold Voltage			$V_{IN-OFF} + 0.20$		V
Feedback Input Section						
A_V	Input-Voltage to Current-Sense Attenuation			1/4.2		V/V
Z_{FB}	Input Impedance		4.0	5.5	7.0	k Ω
V_{FBO}	FB-Pin Open Voltage			6.2		V
Current Sense Section						
Z_{SENSE}	Input Impedance			12		k Ω
t_{PD}	Delay to Output			100	200	ns
t_{LEB}	Leading-Edge Blanking Time			360		ns
V_{STH1V}	Threshold Voltage for Current Limit	$V_{IN} = 1V, R_I = 26k\Omega$	0.78	0.83	0.88	V
V_{STH3V}	Threshold Voltage for Current Limit	$V_{IN} = 3V, R_I = 26k\Omega$	0.65	0.70	0.75	V
$V_{STH1V-2/3}$	OCP Threshold Voltage for Current Limit	$V_{IN} = 1V, R_I = 26k\Omega$	0.56	0.61	0.66	V
$V_{STH3V-2/3}$	OCP Threshold Voltage for Current Limit	$V_{IN} = 3V, R_I = 26k\Omega$	0.46	0.51	0.56	V
t_{D-OCP}	Delay Time for OTP	$R_I = 26k\Omega$	82	96	110	ms

Continued on following page...

Electrical Characteristics (Continued)

$V_{DD} = 15V$ and $T_A = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator Section						
f_{OSC}	Normal PWM Frequency	$R_I = 26k\Omega$	60	65	70	KHz
f_{OSC-G}	Green-Mode Minimum Frequency	$R_I = 26k\Omega$	18.0	22.5	25.0	KHz
V_{FB-N}	FB-Pin Threshold for the Beginning of Green Mode			2.1		V
V_{FB-G}	Green-OFF-Mode Voltage at FB Pin			1.6		V
S_G	Slope for Green-Mode Modulation	$R_I = 26k\Omega$		85		Hz/mV
f_{DV}	Frequency Variation vs. V_{DD} Deviation	$V_{DD} = 11.5V$ to $20V$			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	$T_A = -20$ to $85^\circ C$		1.5	5.0	%

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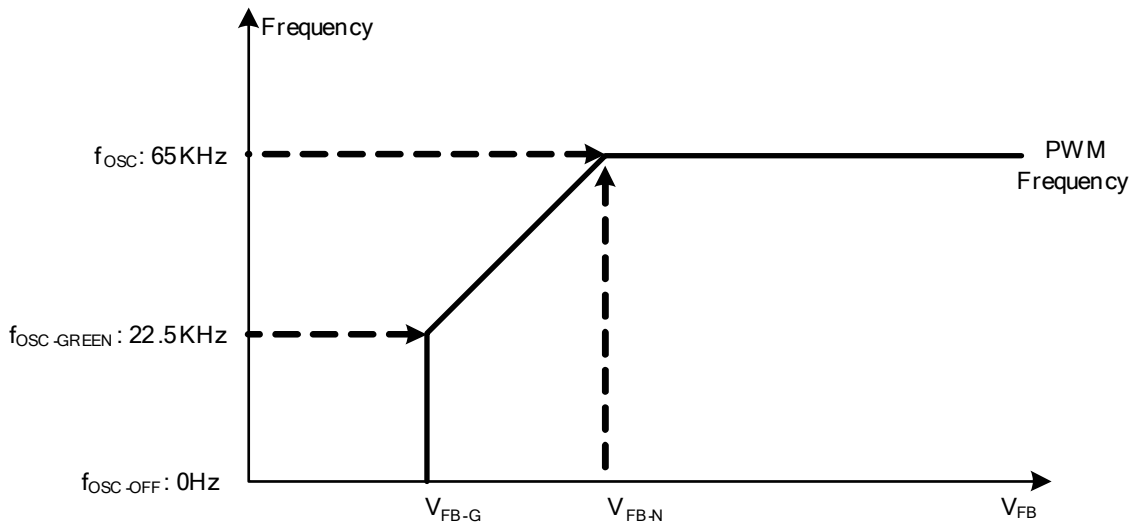


Figure 6. PWM Frequency

Electrical Characteristics (Continued) $V_{DD} = 15V$ and $T_A = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		80	85	90	%
V_{OL}	Output Voltage Low	$V_{DD} = 15V$, $I_{OUT} = 50mA$			1.5	V
V_{OH}	Output Voltage High	$V_{DD} = 12V$, $I_{OUT} = 50mA$	8			V
t_r	Rising Time	$V_{DD} = 15V$, GATE = 1nF		350		ns
t_f	Falling Time	$V_{DD} = 15V$, GATE = 1nF		50		ns
V_{CLAMP}	Gate Output Clamping Voltage	$V_{DD} = 20V$		18		V
OTP Section						
I_{RT}	Output Current of RT Pin	$R_I = 26k\Omega$	64	70	76	μA
V_{RTTH}	Threshold Voltage for OTP		1.015	1.065	1.115	V
$t_{DOTP-LATCH}$	Over-Temperature Latch-Off Debounce	$R_I = 26k\Omega$		100		μs
V_{RT-RLS}	OTP Release Voltage (for Non-Latch-Off Version)			$V_{RTTH} + 0.1$		V
R_I Section						
R_{I-NOR}	R_I Operating Range		15.5		36.0	k Ω
R_{I-MAX}	Maximum R_I Value for Protection			216		k Ω
R_{I-MIN}	Minimum R_I Value for Protection			6		k Ω

Typical Performance Characteristics

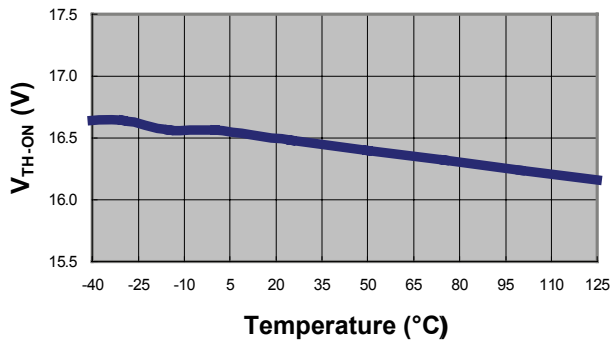


Figure 7. Startup Threshold vs. Temperature

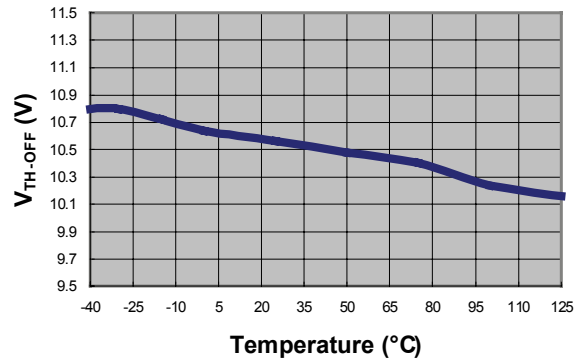


Figure 8. Minimum Operating Voltage vs. Temperature

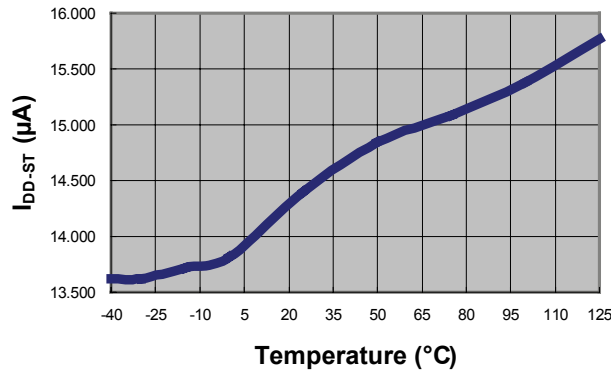


Figure 9. Startup Current vs. Temperature

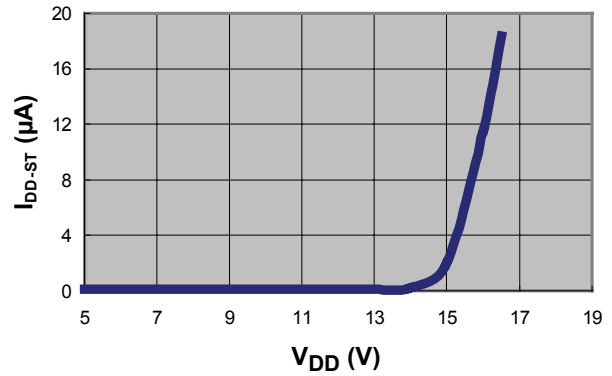


Figure 10. Startup Current vs. V_{DD} Voltage

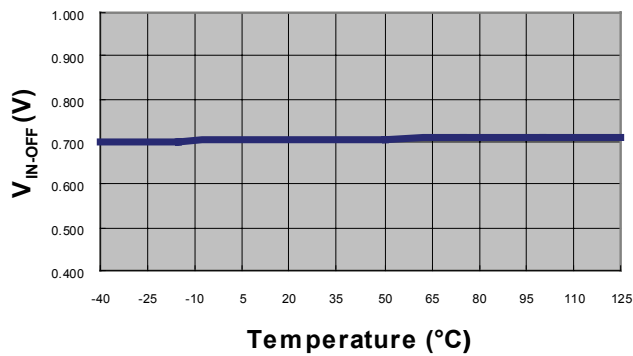


Figure 11. PWM Turn-Off Threshold Voltage vs. Temperature

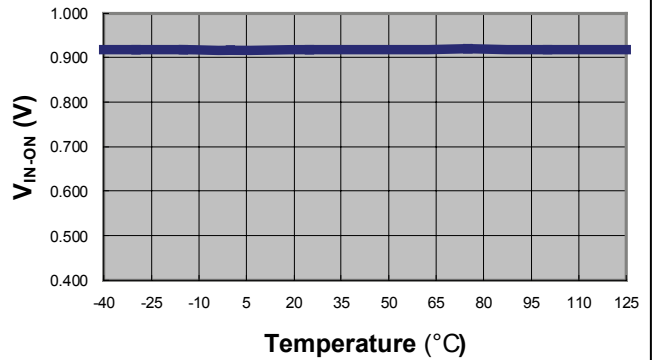


Figure 12. PWM Turn-On Threshold Voltage vs. Temperature

Typical Performance Characteristics (Continued)

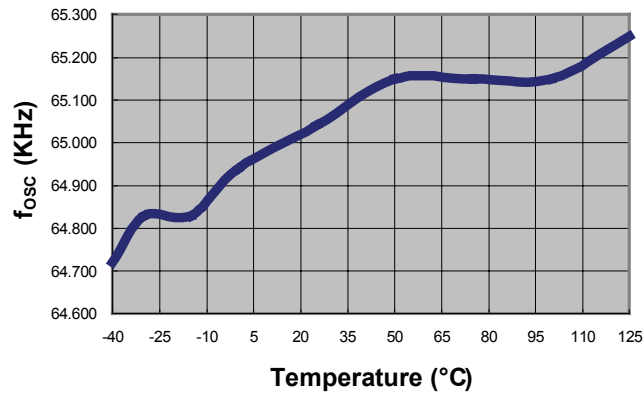


Figure 13. PWM Frequency vs. Temperature

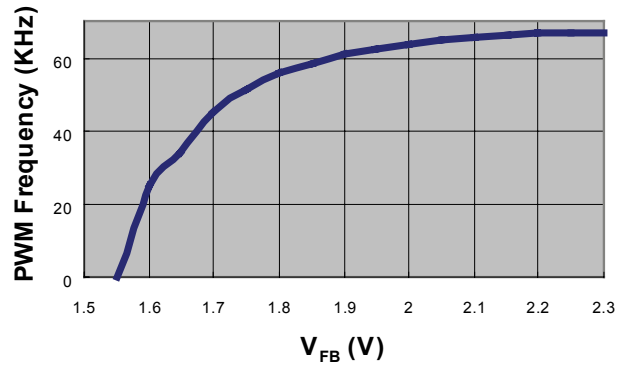


Figure 14. PWM Frequency vs. FB Voltage (R_f=26kΩ)

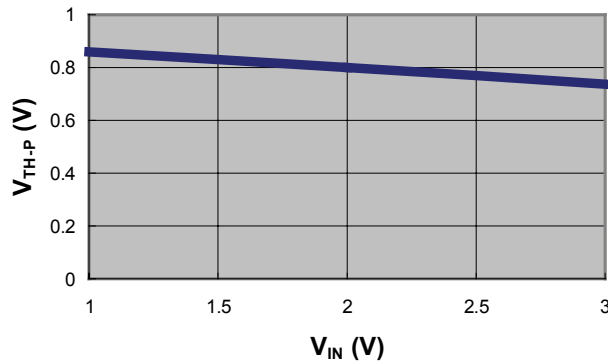


Figure 15. Current-Limit Threshold vs. V_{IN} Voltage

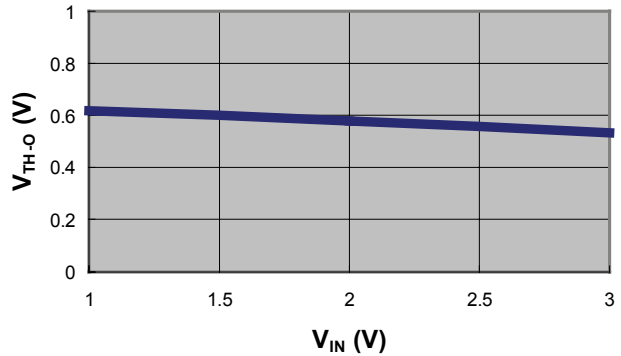


Figure 16. 2/3 Current-Limit Threshold vs. V_{IN} Voltage

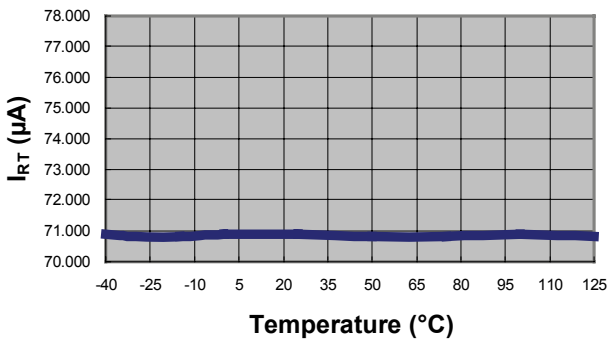


Figure 17. Output Current of RT Pin (I_{RT}) vs. Temperature

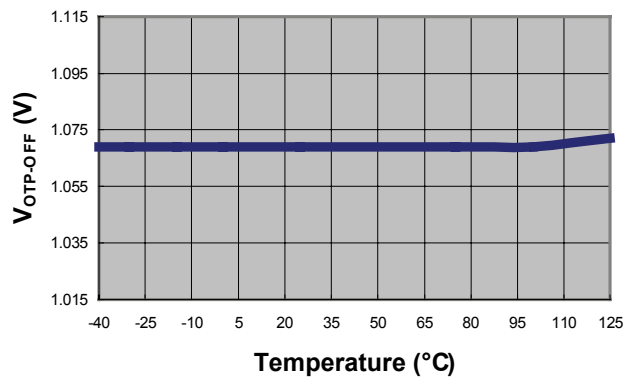


Figure 18. OTP Threshold Voltage vs. Temperature

Operation Description

Startup Operation

The turn-on/turn-off thresholds are fixed internally at 16.5V/10.5V. To enable the SG6846 during startup, the hold-up capacitor must first be charged to 16.5V through the startup resistor.

The hold-up capacitor continues to supply V_{DD} before energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 10.5V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply V_{DD} during startup.

The typical startup current is only 8 μ A. This allows a high resistance, low-wattage startup resistor to be used to minimize power loss. A 1.5M Ω /0.25W, startup resistor and a 10 μ F/25V V_{DD} hold-up capacitor is sufficient for a universal input range.

The required operating current has been reduced to 3.7mA. This enables higher efficiency and reduces the V_{DD} hold-up capacitance requirement.

Green-Mode Operation

Power supplies using the SG6846 can easily meet even the most restrictive international regulations regarding standby power consumption. The proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Maximum on time is limited to provide protection against abnormal conditions. To further reduce power consumption under zero-load condition, the PWM oscillator is completely turned off and the power supply enters burst-mode. After the PWM oscillator is turned off, the IC's supply voltage V_{DD} drops gradually. Before the V_{DD} voltage drops below the UVLO threshold, the PWM oscillator is turned on again. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions.

Oscillator Operation

A resistor connected from the RI pin to GND generates a reference-current source inside the SG6846. This current is used to determine the PWM frequency. Increasing the resistance decreases the amplitude of the current source and reduces the PWM frequency. Using a 26k Ω resistor RI results in a corresponding 65KHz switching frequency. The relationship between RI and the switching frequency is:

$$f_{PWM}(\text{KHz}) = \frac{1690}{R_I (\text{k}\Omega)} \quad (1)$$

If an open circuit or short circuit to ground occurs at the RI pin, the internal protection circuit immediately shuts down the controller.

Two-Level Over-Current Protection (OCP)

Cycle-by-cycle current limiting shuts down the PWM immediately when the switching current is over the peak-current threshold. Additionally, when the switching current is higher than 2/3 of the peak-current threshold, the internal counter starts counting up. When the switching current is lower than 2/3 of the peak current threshold, the internal counter counts down. When the total accumulated counting time is more than about 96ms ($R_I = 26\text{k}\Omega$), the controller is latched off.

The two-level OCP protection and up/down counter are especially designed for SMPS with surge current output such as those for printers, scanners, and motor drivers.

Constant-Output-Power Limit

For constant-output-power limit over universal input-voltage range, the peak-current threshold is adjusted by the voltage of the VIN pin. Since the VIN pin is connected to the rectified AC-input line voltage through the resistive divider, a higher line voltage generates a higher V_{IN} voltage. The threshold voltage decreases as the V_{IN} voltage increases, making the maximum output power at high-line input voltage equal to that at low-line input.

Brownout Protection

Since the VIN pin is connected through a resistive divider to the rectified AC input line voltage, it can also be used for brownout protection. If the V_{IN} voltage is less than 0.72V, the PWM output is shut off. If the V_{IN} voltage is over 0.92V, the PWM output is turned on again. The hysteresis window for ON/OFF is around 0.2V.

V_{DD} Over-Voltage Protection (OVP)

V_{DD} OVP is built in to prevent damage. If V_{DD} is over 23.6V, SG6846 is latched off.

Over-Temperature Protection (OTP)

An external NTC thermistor can be connected from the RT pin to GND. The impedance of the NTC decreases at high temperatures. When the voltage of the RT pin drops below 1.05V, the SG6846 is turned off. *For protection-mode options, see Ordering Information.*

Operation Description (Continued)

Noise Immunity

Noise from the current sense or the control signal may cause significant pulse-width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. Avoid long PCB traces and component leads. Compensation and filter components should be located near the SG6846.

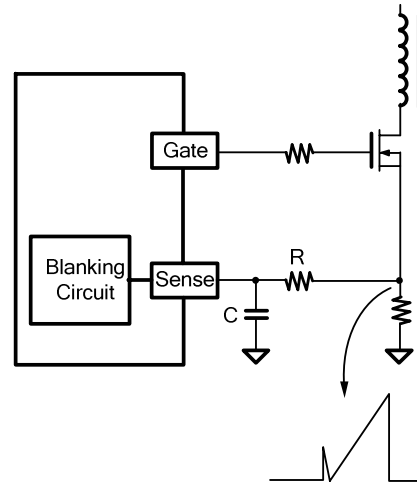


Figure 19. Current Sense R-C Filter

Reference Circuit

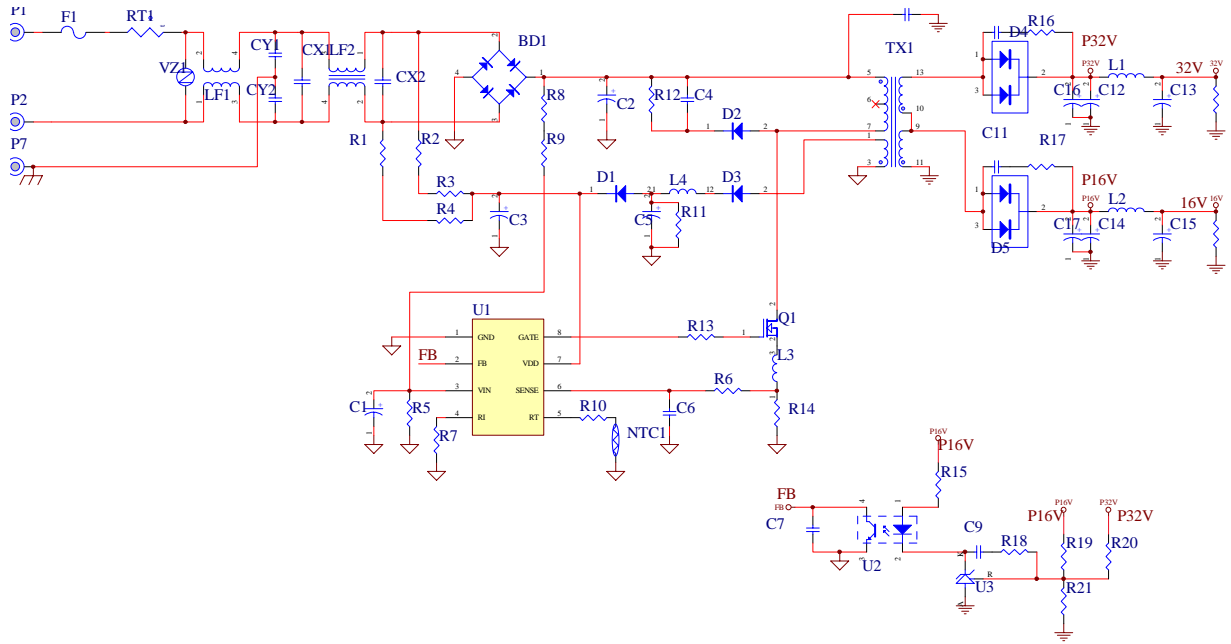
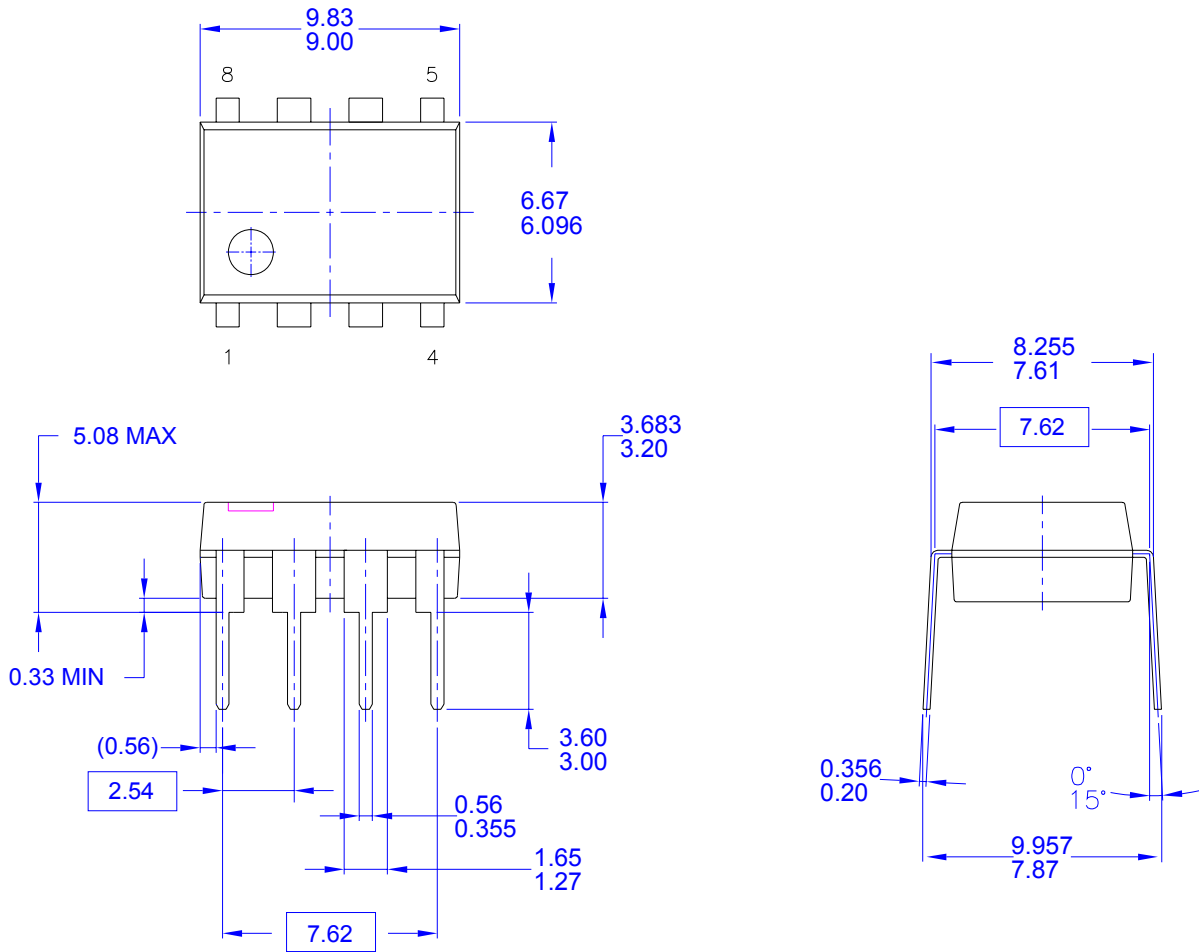


Figure 20. Application Circuit for 32V / 16V Output

BOM

Part No.	Value	Part No.	Value	Part No.	Value
R1, R2, R3, R4	470KΩ +/-5%	C4	103 P 630V	D3	FR103 1.0A 200V
R8, R9	51MΩ +/-1%	C10,C11	102 P 1KV	BD1	DBL406G
R5	16K2Ω +/-1%	C6,C7	102 P 50V	D4	BYT28-300
R15	1K5Ω +/-5%	C9	222 P 50V	D5	BYV32-150
R13	10Ω +/-5%	C14,C17	470μ 25V	F1	250V4A QUICK
R18	4K7Ω +/-5%	C15	220μ 25V	L1,L2	1.8μH
R21	15KΩ +/-1%	C13,C16	220μ 50V	L4	10μH
R7	27KΩ +/-5%	C2	150μ 400V	U3	TL431 +/-1%
R6	330Ω +/-1%	C1	4.7μ 50V	U1	SG 6846
R19	102KΩ +/-1%	C3	10μ 50V	U2	PC817
R14	0Ω22 +/-5%	CX1	X1 0.47μ 275V	Q1	7NB60
R16, R17	1W 20Ω +/-5%	C8	Y2 222P 250V	TX1	EI-33
R11	20KΩ +/-5%	C5	100μ 50V	RT1	SCK053
R12	100KΩ +/-5%	CX2	X2 0.1μF 275V	VZ1	14ψ 470V
R20	887KΩ +/-1%	D1	1N4148		
R22	10KΩ +/-1%	D2	BYV95C		

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994
- E) DRAWING FILENAME AND REVISION: MKT-N08FREV2.

Figure 21. 8-Pin Dual In-Line Package (DIP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Physical Dimensions

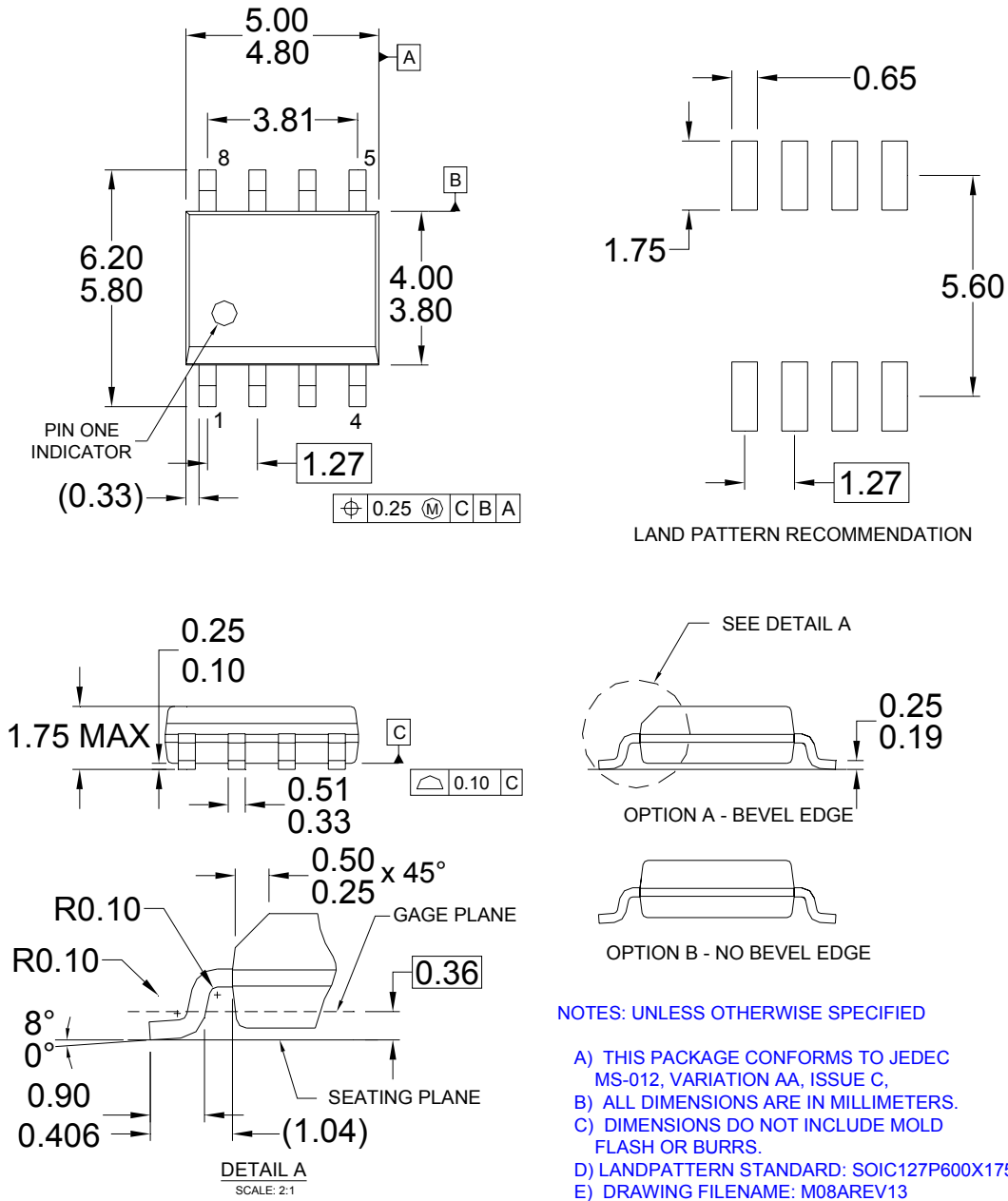


Figure 22. 8-Pin Small Outline Package (SOP)

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