Green mode PFC/Flyback-PWM Controller

SG6905

FEATURES

- Interleaved PFC/PWM switching
- Green mode PWM operation
- Low start-up and operating current
- Innovative switching charge multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode control for PFC
- PFC over-voltage and under-voltage protections
- PFC remote on/off Control
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Constant power limit for PWM
- Power-on sequence control
- Brownout protection
- Over temperature protection

APPLICATIONS

- Switching Power Suppliers with Active PFC
- High-Power Adaptors

DESCRIPTION

The highly integrated SG6905 is specially designed for power supplies with boost PFC and flyback PWM. It requires very few external components to achieve versatile protections. It is available in a 20-pin SOP package.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise.

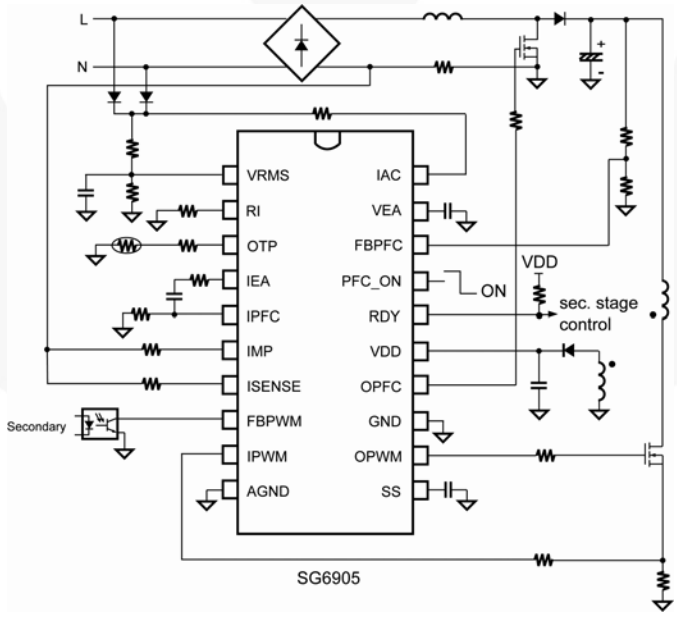
For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6905 will shut off PFC to prevent extra-high voltage on output.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

During start-up, the RDY pin will be pulled low until the PFC output voltage reaches to the setting level. This signal can be used to control the second power stage for proper power on sequence.

SG6905 provides complete protection functions such as brownout protection and RI pin open/short.

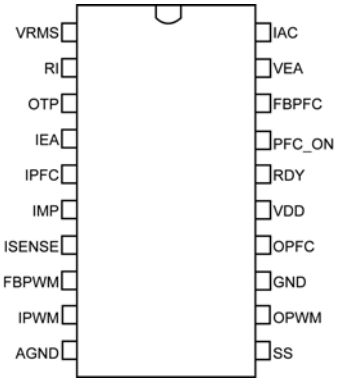
TYPICAL APPLICATION



MARKING DIAGRAMS

T: S = SOP
P : Z =Lead Free
Null=regular package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



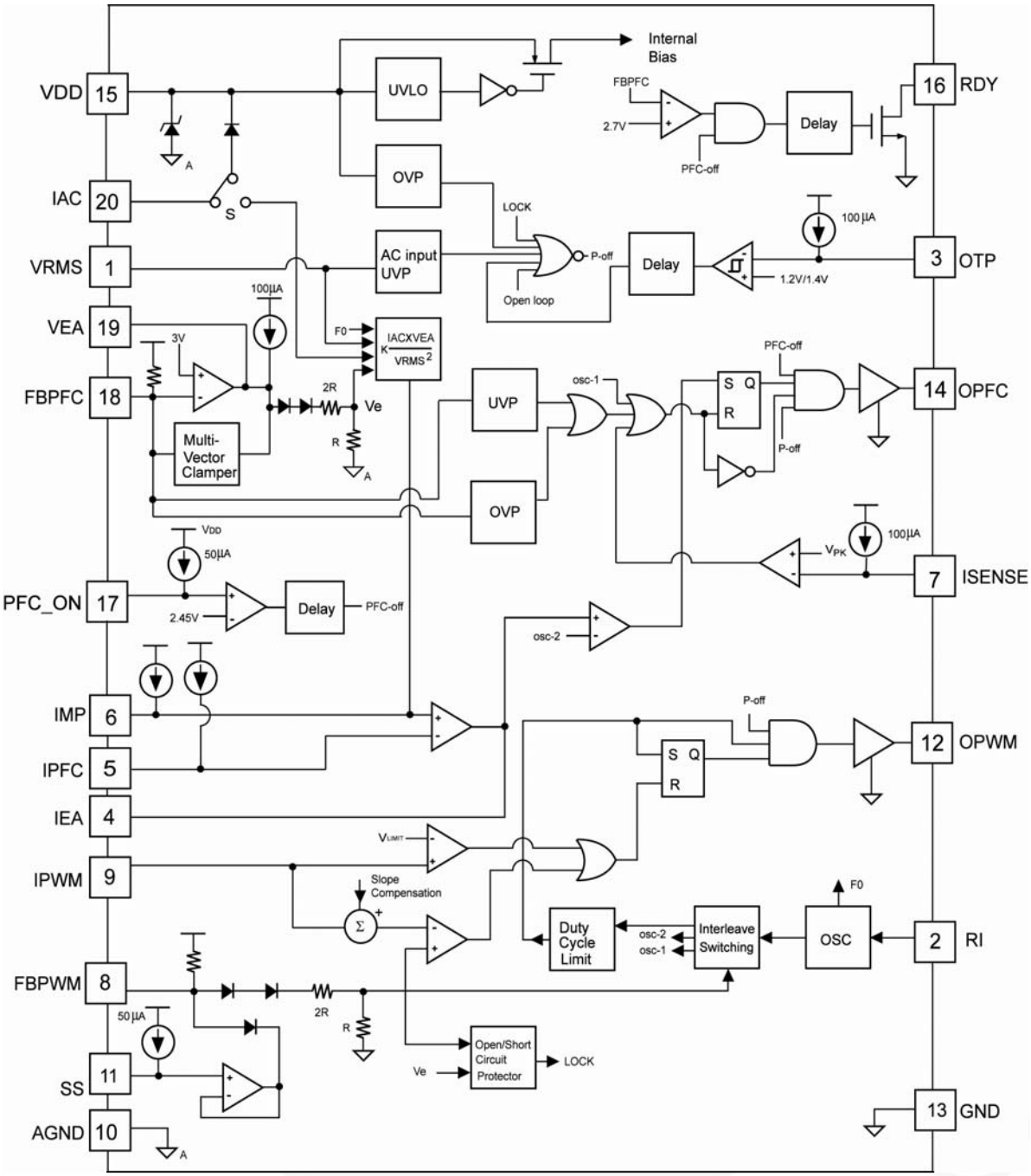
ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6905SZ		20-pin SOP

PIN DESCRIPTIONS

Name	Pin No.	Type	Function
VRMS	1	Line-Voltage Detection	Line voltage detection. The pin is used for PFC multiplier, brownout protection .For brownout protection; the controller will be disabled after a delay time when the VRMS voltage drops below a threshold voltage.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / RI] kHz, where RI is in kΩ. For example, if RI is equal to 24kΩ, then the switching frequency will be 65 kHz.
OTP	3	Over Temperature Protection	This pin supplies an over temperature protection signal. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6905 will be disabled.
IEA	4	Output for PFC Current Amplifier	This is the output of the PFC current amplifier. The signal from this pin will be compared with an internal saw-tooth and hence determine the pulse width for PFC gate drive.
IPFC	5	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current amplifier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
IMP	6	Non-inverting Input for PFC Current Amplifier	The non-inverting input of the PFC current amplifier and also the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average- current- mode control.
ISENSE	7	Peak Current Limit Setting for PFC	The peak-current setting for PFC.
FBPWM	8	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a 6.5kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
IPWM	9	PWM Current Sense	The current-sense input for the Flyback PWM. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
AGND	10	Ground	Signal Ground
SS	11	PWM Soft Start	During startup, the SS pin will charge an external capacitor with a 50μA (RI=24kΩ) constant current source. The voltage on FBPWM will be clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.
OPWM	12	PWM Gate Drive	The totem-pole output drive for the Flyback PWM MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
GND	13	Ground	Power Ground
OPFC	14	PFC Gate Drive	The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
VDD	15	Supply	The power supply pin.
RDY	16	Ready signal output	This pin outputs a ready signal to control the power on sequence. Once the SG6905 is turned on and the FBPFC(PFC Feedback input)voltage is higher than 2.7V, will lock this pin to high impedance. Disable the SG6905 Will reset this pin to the low.
PFC_ON	17	Remote On/Off	The PFC stage will disabled whenever the voltage at this pin is exceed 2.45V.
FBPFC	18	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amp. This pin is connected to the PFC output through a divider network.
VEA	19	Error-Amp Output for PFC voltage feedback loop	The error-amp output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value will result in a narrow bandwidth and hence improve the power factor.
IAC	20	Input AC Current	Before start-up, this input is used to provide startup current for VDD. For normal operation, this input is used to provide current reference for the multiplier.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{VDD}	DC Supply Voltage*	25	V
I_{AC}	Input AC Current	2	mA
V_{High}	OPWM, OPFC, IAC	-0.3 to +25	V
V_{Low}	Others	-0.3 to +7	V
P_D	Power Dissipation At T_A < 50°C	0.8	W
T_J	Operating Junction Temperature	-40 to +125	°C
T_{STG}	Storage Temperature Range	-55 to +150	°C
$R_{\theta j\text{-}C}$	Thermal resistance (Junction to Case)	23.64	°C/W
T_L	Lead Temperature (Wave soldering or IR, 10 seconds)	260	°C
$V_{ESD,HBM}$	ESD capability, HBM model	4.5	KV
$V_{ESD,MM}$	ESD capability, Machine model	250	V

*All voltage values, except differential voltages, are given with respect to GND pin.
*Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Operating Ambient Temperature*	-20 to +85	°C

*For proper operation

ELECTRICAL CHARACTERISTICS (V_{DD}=15V, T_A=25°C UNLESS NOTED)

VDD section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$I_{DD\text{-}ST}$	Start-up Current	$V_{DD\text{-}ON}$-0.16V		10	25	µA
$I_{DD\text{-}OP}$	Operating Current	V_{DD}= 15V; RI= 24KΩ OPFC, OPWM open		6	10	mA
$V_{DD\text{-}ON}$	Start Threshold Voltage		15	16	17	V
$V_{DD\text{-}OFF}$	Min. Operating Voltage		9	10	11	V
$V_{DD\text{-}OVP}$	VDD OVP Threshold		23.5	24.5	25.5	V
$t_{D\text{-}VDDOVP}$	Debounce Time of VDD OVP	RI= 24KΩ	8		25	µs
$V_{DD\text{-}TH\text{-}G}$	VDD Low-Threshold Voltage to Exit Green-OFF Mode		$V_{DD\text{-}OFF}$ +0.9	$V_{DD\text{-}OFF}$ +1.5	$V_{DD\text{-}OFF}$ +2.1	V

VRMS for UVP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under Voltage Protection Threshold (with T_{UVP} delay)		0.75	0.8	0.85	V
$V_{RMS-UVP-2}$	Recovery level on VRMS		$V_{RMS-UVP-1}$+0.17	$V_{RMS-UVP-1}$+0.19	$V_{RMS-UVP-1}$+0.21	V
t_{D-PWM}	When UVP occurs, the interval from OPFC off to OPWM off	RI= 24KΩ	$t_{UVP-Min}$ +9		$t_{UVP-Min}$ +14	ms
t_{UVP}	Under Voltage Protection Delay Time (No delay for startup)	RI= 24KΩ	150	195	240	ms

PFC stage

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3	3.05	V
Av	Open-loop Gain			60		dB
Z_o	Output Impedance			110		KΩ
OVP_{FBPFC}	PFC Over-Voltage-Protection on FBPFC		3.2	3.25	3.3	V
□OVP_{PFC}	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$t_{OVP-PFC}$	Debounce Time of PFC OVP	RI= 24KΩ	40	70	120	μs
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.1	3.15	3.2	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		μA/mV
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.9	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		μA
UVP_{FBPFC}	PFC Feedback Under Voltage Protection		0.35	0.4	0.45	V
$t_{UVP-PFC}$	Debounce Time of PFC UVP	RI= 24KΩ	40	70	120	μs

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common-mode Rejection Ratio	V_{CM}= 0~1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	RI= 24 KΩ (I_{MR}=20+I_{RI}*0.8)	50		70	μA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	RI= 24KΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	VRMS= 1.05V	0.15	0.2	0.25	V
		VRMS= 3V	0.35	0.4	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading Edge Blanking Time		70	120	170	ns

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output;	RI= 24KΩ		250		μA
I_{MO-1}	Multiplier Current Output (low-line, high-power)	V_{RMS}= 1.05V; I_{AC}= 90μA; VEA= 7.5V;RI= 24 KΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (high-line, high-power)	V_{RMS}= 3V; I_{AC}= 264μA; V_{EA}= 7.5V;RI= 24 KΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Oscillator

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC}	PFC Frequency	RI= 24KΩ	62	65	68	KHz
F_{DV}	Frequency Variation versus V_{DD} Deviation	V_{DD}= 11 to 20V			2	%
F_{DT}	Frequency Variation versus Temp. Deviation	T_A= -20 to 85°C			2	%

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_Z	Output Voltage Maximum (Clamp)	V_{DD}= 20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}= 15V; I_O= 100mA			1.5	V
t_{PFC}	The interval of OPFC lags behind OPWM at startup		8	11	13.5	ms
V_{OH-PFC}	Output Voltage High	V_{DD}= 13V; I_O= 100mA	8			V
t_{R-PFC}	Rising Time	V_{DD}= 15V; C_L= 5nF; O/P= 2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}= 15V;C_L= 5nF; O/P= 9V to 2V	40	60	110	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%

PFC On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{ON/OFF}$	Constant Current Output for PFC_ON pin	RI= 24KΩ	44	50	56	μA
V_{OFF}	Turn-off Threshold Voltage		2	2.45	2.9	V
t_{PFC_ON}	Debounce Time of PFC_On/Off	RI= 24KΩ	40	70	120	μs

PWM Stage

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$A_{v\text{-}PWM}$	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN\text{-}LOOP}$	PWM Open Loop Protection voltage		4.2	4.5	4.8	V
$t_{OPEN\text{-}PWM}$	PWM Open Loop Protection Delay Time	RI= 24KΩ	45	56	70	ms
$t_{OFF\text{-}PWM\text{-}DLY}$	PWM off to turn on delay time		450	600	750	ms
$V_{FB\text{-}N}$	Frequency Reduction Threshold on FBPWM	PFC_ON > V_{OFF}	1.8	2.0	2.2	V
S_G	Green-Mode Modulation Slope	PFC_ON > V_{OFF}	80	100	120	Hz/V
$V_{FB\text{-}G}$	Voltage on FBPWM at Fs = $F_{OSC\text{-}MINFREQ}$	PFC_ON > V_{OFF}	1.35	1.6	1.75	V

PWM-Current Sense

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{PD\text{-}PWM}$	Propagation Delay to Output		50		120	ns
V_{LIMIT}	Peak Current Limit Threshold Voltage		0.85	0.9	0.95	V
$t_{LEB\text{-}PWM}$	Leading-Edge Blanking Time		170	250	350	ns
□V_{SLOPE}	Slope Compensation □V_S = □V_{SLOPE} x (T_{on}/T) □V_S : Compensation Voltage Added to Current Sense		0.3	0.33	0.36	V

PWM Oscillator

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC}	PWM Frequency	RI= 24KΩ	62	65	68	KHz
$F_{OSC\text{-}MIN}$	Minimum Frequency	RI= 24KΩ; FBPWM= $V_{FB\text{-}G}$; PFC_ON > V_{OFF}	19	21	23.5	KHz
F_{DV}	Frequency Variation versus V_{DD} Deviation	V_{DD}= 11V to 20V			2	%
F_{DT}	Frequency Variation versus Temp. Deviation	T_A= -20 to 85°C			2	%

PWM Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{Z\text{-}PWM}$	Output Voltage Maximum (Clamp)	V_{DD}= 20V		16	18	V
$V_{OL\text{-}PWM}$	Output Voltage Low	V_{DD}= 15V; I_O= 100mA			1.5	V
$V_{OH\text{-}PWM}$	Output Voltage High	V_{DD}= 13V; I_O= 100mA	8			V
$t_{R\text{-}PWM}$	Rising Time	V_{DD}= 15V; C_L= 5nF; O/P= 2V to 9V	30	60	120	ns
$t_{F\text{-}PWM}$	Falling Time	V_{DD}= 15V; C_L= 5nF; O/P= 9V to 2V	30	50	110	ns
DCY_{MAXPWM}	PWM Maximum Duty Cycle		73	78	83	%

RDY section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{FB-RDY-HIGH}$	Threshold voltage of FBPFC for RDY high impedance		2.65	2.7	2.75	V
$I_{FB-RDY-HIGH}$	The leakage current of RDY is a high impedance at the voltage of FBPFC	FBPFC= 2V			10	μA
V_{OL}	Output Voltage Low for RDY is failed	I_{SINK}= 1mA			0.5	V
t_{RDY}	The interval between FBPFC exceeds $V_{FB-RDY-HIGH}$ and RDY is high impedance			4	6	ms

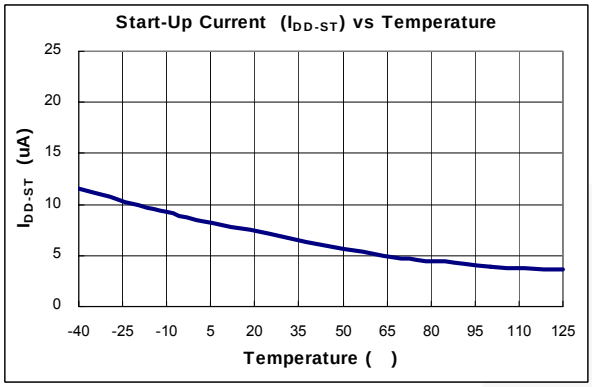
OTP section

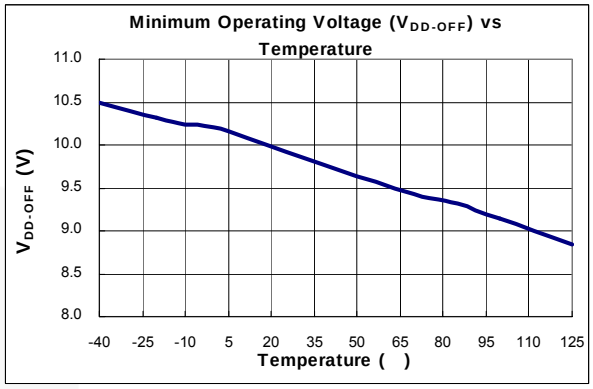
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OTP}	OTP Pin Output Current	RI= 24KΩ	90	100	110	μA
V_{OTP-ON}	Recovery level on OTP		1.35	1.4	1.45	V
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.2	1.25	V
t_{OTP}	OTP Debounce Time	RI= 24KΩ	8		25	μs

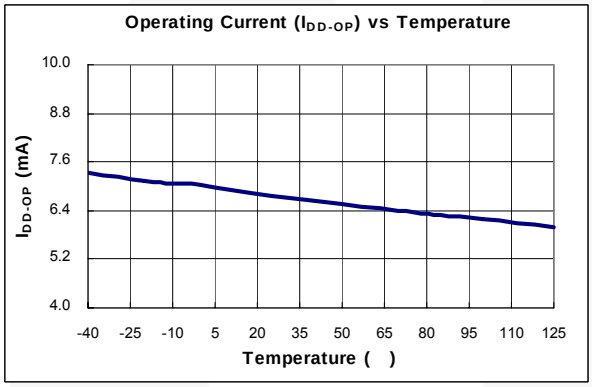
Soft-Start Section

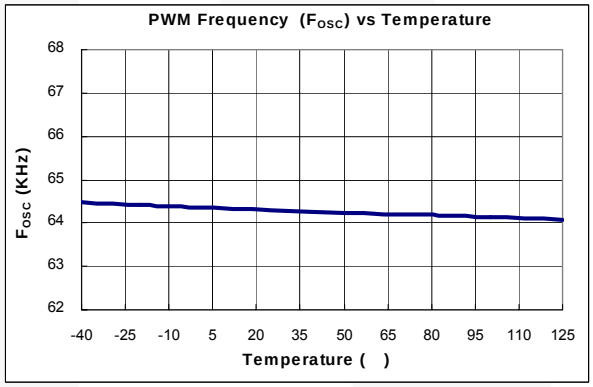
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Constant Current Output for Soft Start	RT= 24KΩ	44	50	56	μA
R_D	Discharge R_{DSON}			470		Ω

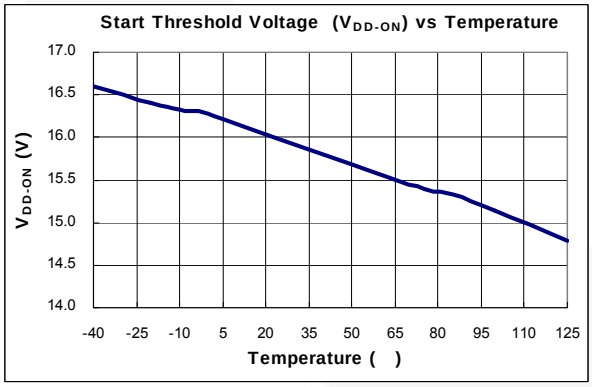
TYPICAL CHARACTERISTICS

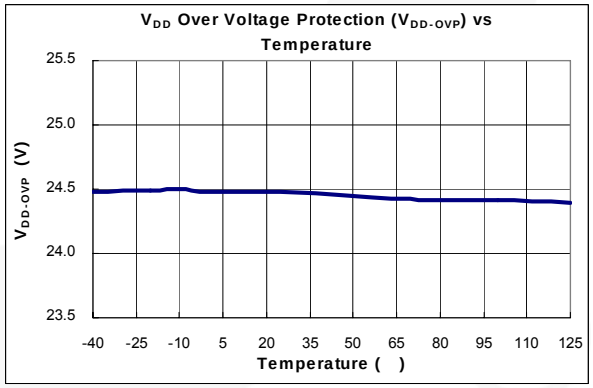


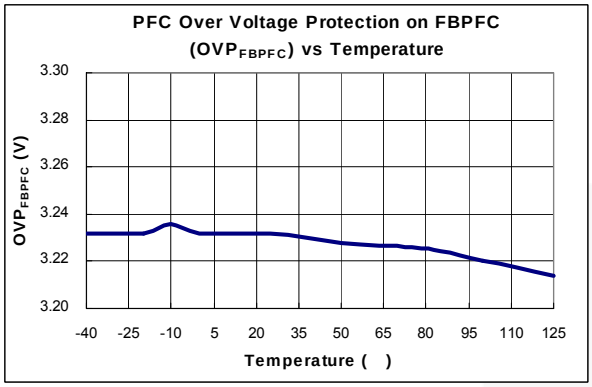


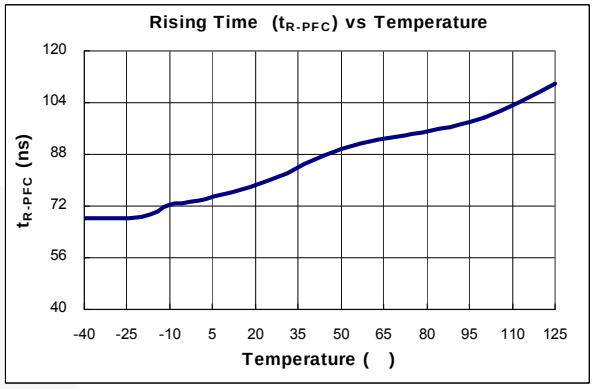


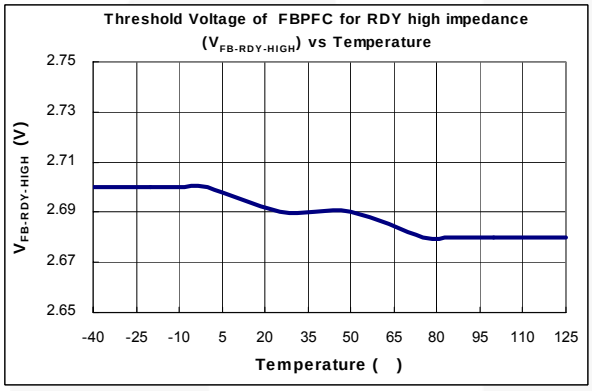


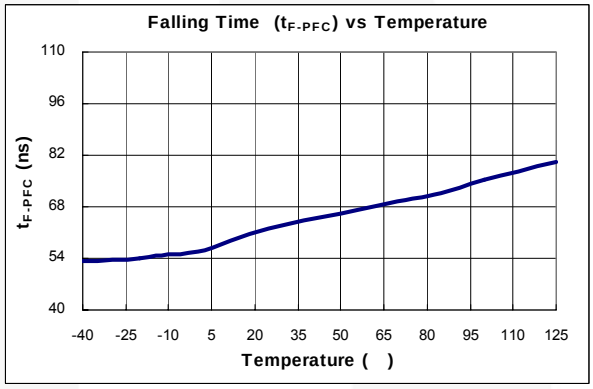


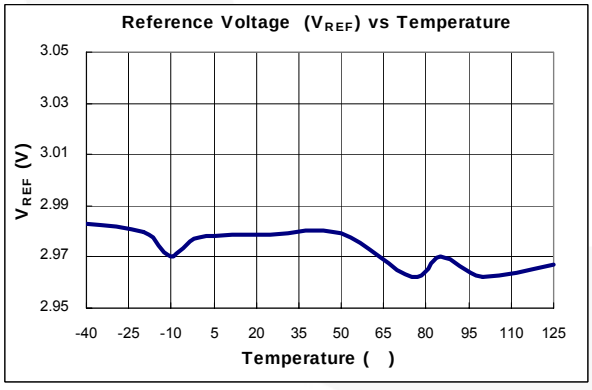


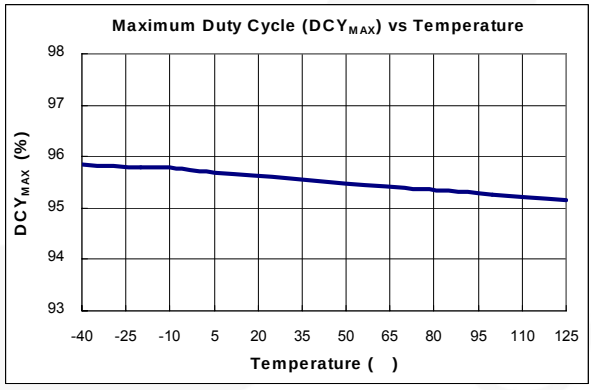


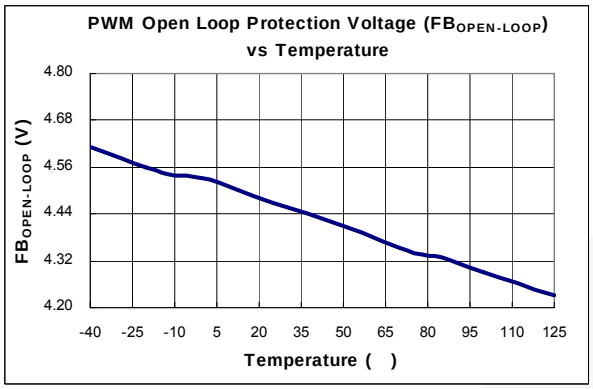


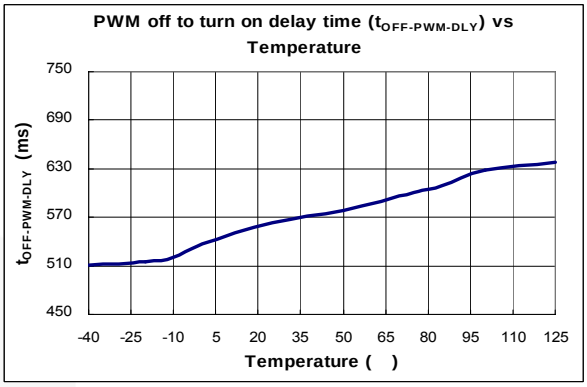


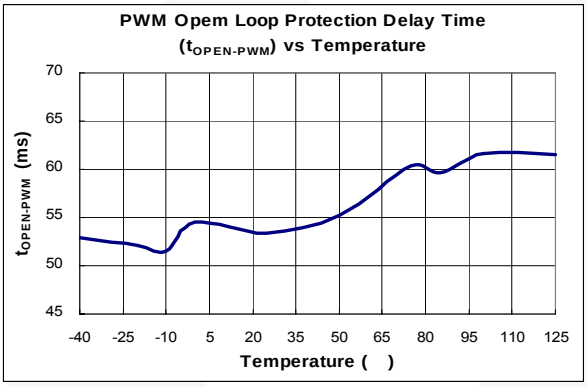


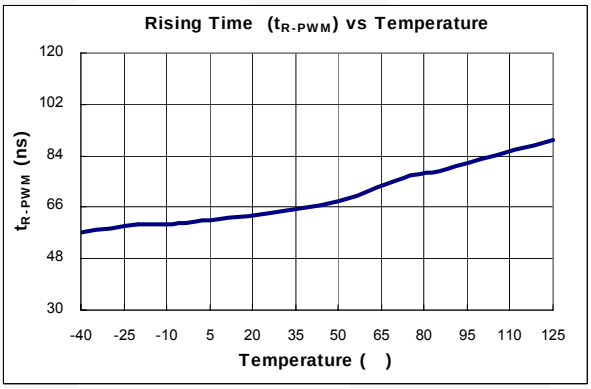


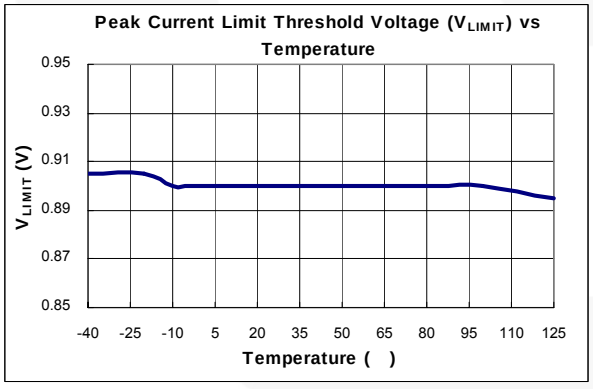


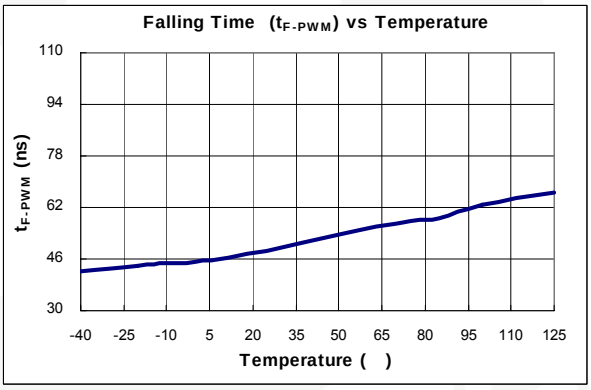


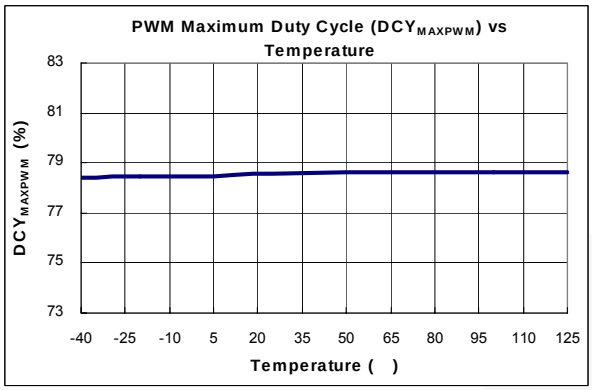


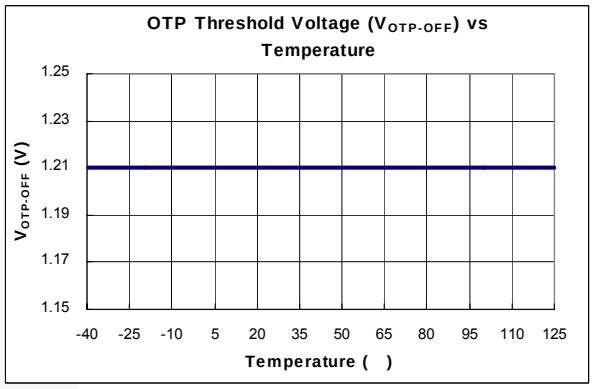












OPERATION DESCRIPTION

The highly integrated SG6905 is specially designed for power supplies consist of boost PFC and flyback PWM. It requires very few external components to achieve green-mode operation and versatile protections. It is available in 20-pin SOP package.

The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise. At light loads, the switching frequency is continuously decreased to reduce power consumption.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6905 will shut off PFC to prevent extra-high voltage on output.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

During start-up, the RDY pin will be pulled low until the PFC output voltage reaches to the setting level. This signal can be used to control the second power stage for proper power on sequence.

SG6905 provides complete protection functions such as brownout protection and RI pin open/short.

Start Up

Figure 1 shows the start up circuit of the SG6905. A resistor R_{AC} is utilized to charge V_{DD} capacitor through S1. The turn-on and turn-off threshold of SG6905 are fixed internally at 16V/10V. During start-up, the hold-up capacitor must be charged to 16V through the start-up resistor so that SG6905 will be enabled. The hold-up capacitor will continue to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer flyback converter. V_{DD} must not drop below 10V during this start-up process. This UVLO hysteresis window ensures that hold-up capacitor is adequate to supply V_{DD} during start-up. Since SG6905 consumes less than 25μA startup current, the value of R_{AC} can be large to reduce power consumption. One 10uF capacitor should hold enough energy for successful start-up. After start-up, S1 will switch so that the current I_{AC} will be the input for PFC multiplier. This helps reduce circuit complexity and power consumption.

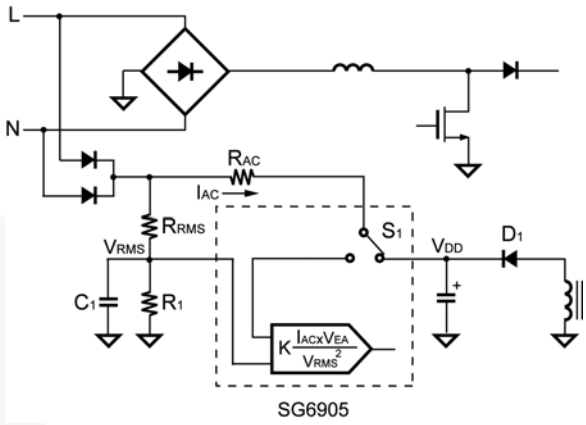


FIG.1 Start up circuit of the SG6905

PFC ON/OFF Control and RDY Signal for Power ON Sequence Control

A PFC on/off control function is built-in to control the power on and power off of PFC controller. Once the voltage on this pin is pulled below 2.45V, the OPFC will be enabled. Once the OPFC is enabled, the output voltage of the PFC converter will gradually increase to the regulated voltage. To provide a proper power on sequence control, a RDY pin will be pulled high after the PFC voltage reach 90% (FBPFC>$V_{FB\text{-}RDY\text{-}HIGH}$) of its regulated voltage.

Switching Frequency and Current Sources

The switching frequency of SG6905 can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$F_{OSC} = \frac{1560}{R_I\ (k\Omega)}(kHz) \text{ ---------- (1)}$$

For example, a 24KΩ resistor R_I results in a 65 KHz switching frequency. Accordingly, a constant Current I_T will flow through R_I.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \text{ ---------- (2)}$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 2 shows a resistive divider with low-pass filtering for line-voltage detection on VRMS pin. The V_{RMS} voltage is used for the PFC multiplier and brownout protection.

For brownout protection, the SG6905 is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier, please refer to below section for more details.

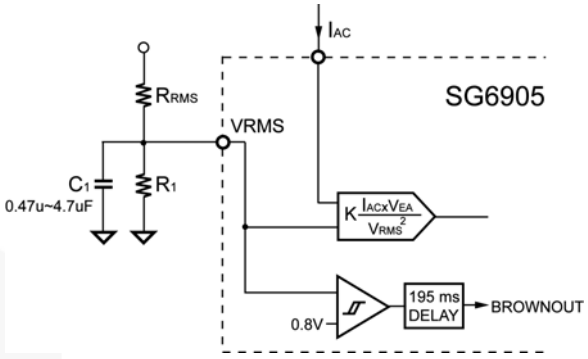


FIG.2 Line voltage detection circuit

Interleave Switching

The SG6905 uses interleaved switching to synchronize the PFC and Flyback stages. This reduces switching noise and spreads the EMI emissions. Figure 3 shows that an off-time T_{OFF} is inserted in between the turn-off of the PFC gate drive and the turn-on of the PWM.

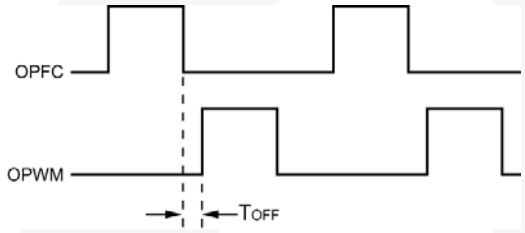


FIG.3 Interleaved switching pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase will follow that of the input voltage. Using SG6905, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier/divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 4 shows the total control loop for the average-current-mode control circuit of SG6905.

The current source output from the switching charge multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (uA) \text{ ----------} \quad (3)$$

Refer to Fig. 3, the current output from IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed current sources. They are used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. The constant current sources I_{MR1} and I_{MR2} are typically 60μA.

Through the differential amplification of the signal across Rs, better noise immunity is achieved. The output of IEA will be compared with an internal sawtooth and hence the pulse width for PFC is determined. Through the average current-mode control loop, the input current Is will be proportional to I_{MO}.

$$I_{MO} \times R2 = Is \times Rs \text{ ----------} \quad (4)$$

According to equation (4), the minimum value of R2 and maximum of Rs can be determined since I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor Rs. The value of Rs should be small to reduce power consumption, but it should be large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as constant as possible according to Equation 3. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The trans-conductance error amplifier has output impedance Z_O and a capacitor C_{EA} (1μF ~ 10μF) should be connected to ground. This establishes a dominant pole f1 for the voltage loop.

$$f_1 = \frac{1}{2\pi \times Z_O \times C_{EA}} \text{ ----------} \quad (5)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= Vin(rms) \times Iin(rms) \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{2}} \qquad \text{----------} \quad (6) \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^{2}} \\ &= \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned}$$

From Equation 6, V_{EA}, the output of the voltage error amplifier, actually controls the total input power and hence the power delivered to the load.

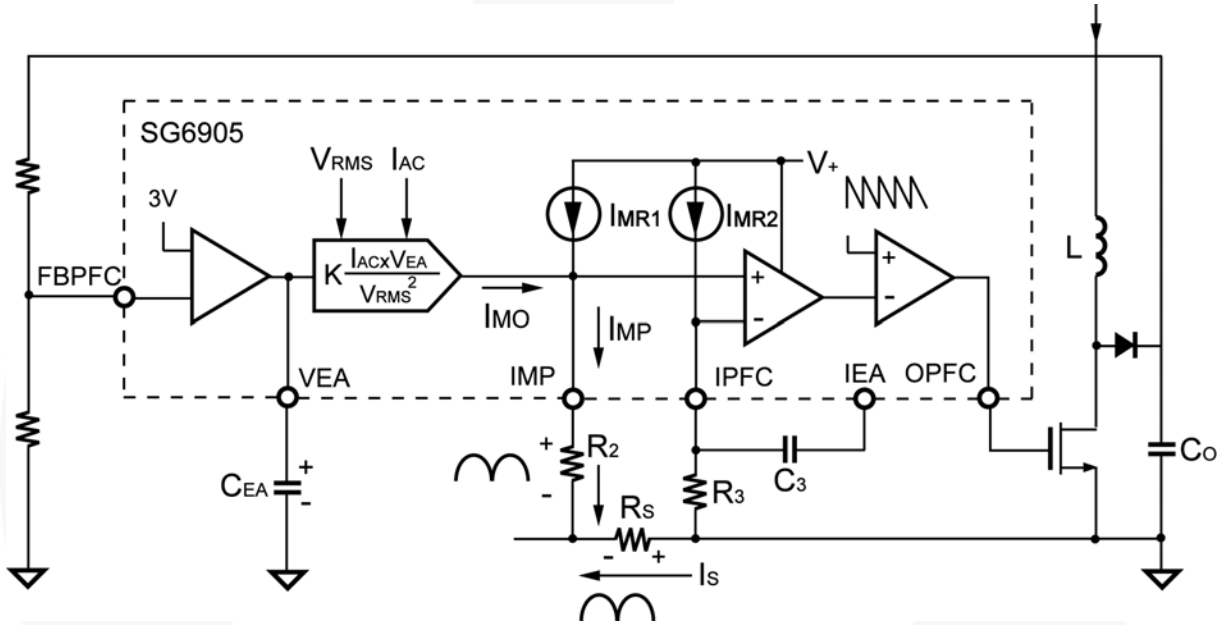


FIG.4 Average current mode control loop

Multi-vector Error Amplifier

Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative *Multi-Vector Error Amplifier* provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 5 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ± 5% of the reference voltage, the trans-conductance error amplifier will adjust its output impedance to increase the loop response. Either R_A or R_B is opened, OPFC of SG6905 will shut off immediately to prevent extra-high voltage on the output capacitor.

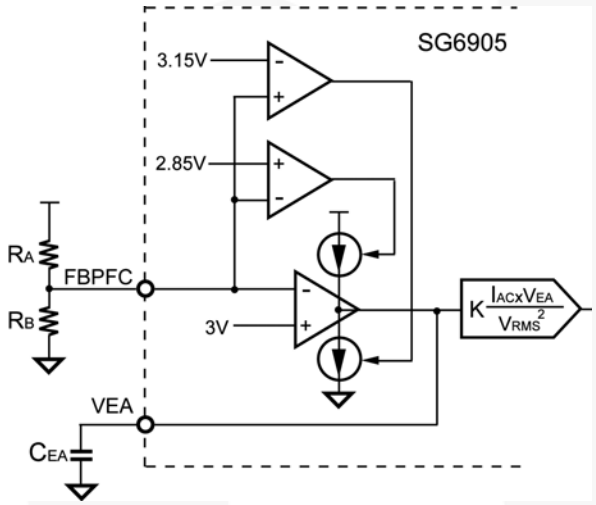


FIG. 5 Multi-vector error amplifier

Cycle-by-Cycle Current Limiting

SG6905 provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 6 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and V_{RMS} is also shown in Figure 6.

The amplitude of the constant current I_P is determined by the internal current reference according to the following equation:

$$I_P = 2 \times \frac{1.2V}{R_I} \quad \text{----------} \quad (7)$$

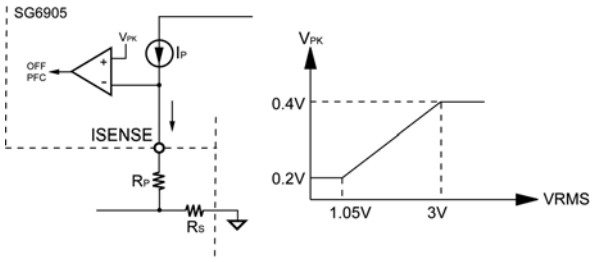


FIG. 6 VRMS controlled current limiting

The peak current of the I_{SENSE} is given by (V_{RMS}<1.05V):

$$I_{SENSE\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{----------} \quad (8)$$

Flyback PWM and Slope Compensation

As shown in Figure 7, peak-current-mode control is utilized for Flyback PWM. The SG6905 inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous current-mode operation.

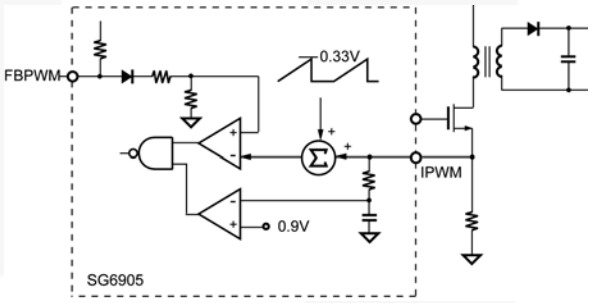


FIG. 7 Peak current control loop

When the IPWM voltage, across the sense resistor, reaches the threshold voltage (0.9V), the OPWM will be turned off after a small propagation delay t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp in inserted at every switching cycle.

Limited Power Control

Every time when the output of power supply is shorted or over loaded, the FBPWM voltage will increase. If the FBPWM voltage is higher than a designed threshold, $FB_{OPEN-LOOP}$ (4.5V), for longer than $t_{OPEN-PWM}$ (56ms), the OPWM will then be turned off. As OPWM is turned off, the supply voltage VDD will also begin decreasing.

When V_{DD} is lower than the turn-off threshold, V_{DD-OFF} (10V), SG6905 will be totally shut down. Due to the start up resistor, V_{DD} will be charged up to the turn-on threshold voltage, V_{DD-ON} (16V), until SG6905 is enabled again. If the over loading condition still exists, the protection will take place repeatedly. This will prevent the power supply from being overheated under over loading condition.

Over-Temperature Protection (OTP)

SG6905 provides an OTP pin for over-temperature protection. A constant current is output from this pin. If RI is equal to 24KΩ, then the magnitude of the constant current will be 100μA. An external NTC thermistor must be connected from this pin to ground shown as Figure 8. When the OTP voltage drops below $V_{OTP-OFF}$ (1.2V), SG6905 will be disabled, and will not recovery until OTP voltage exceeds V_{OTP-ON} (1.4V).

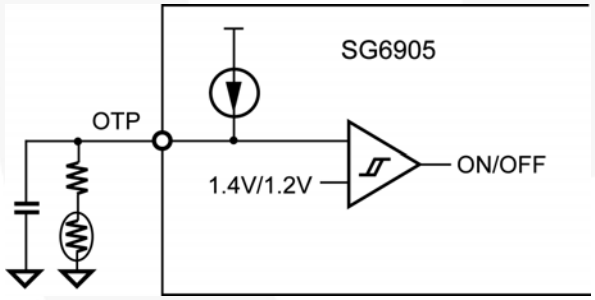


Fig. 8 OTP function

Soft-Start

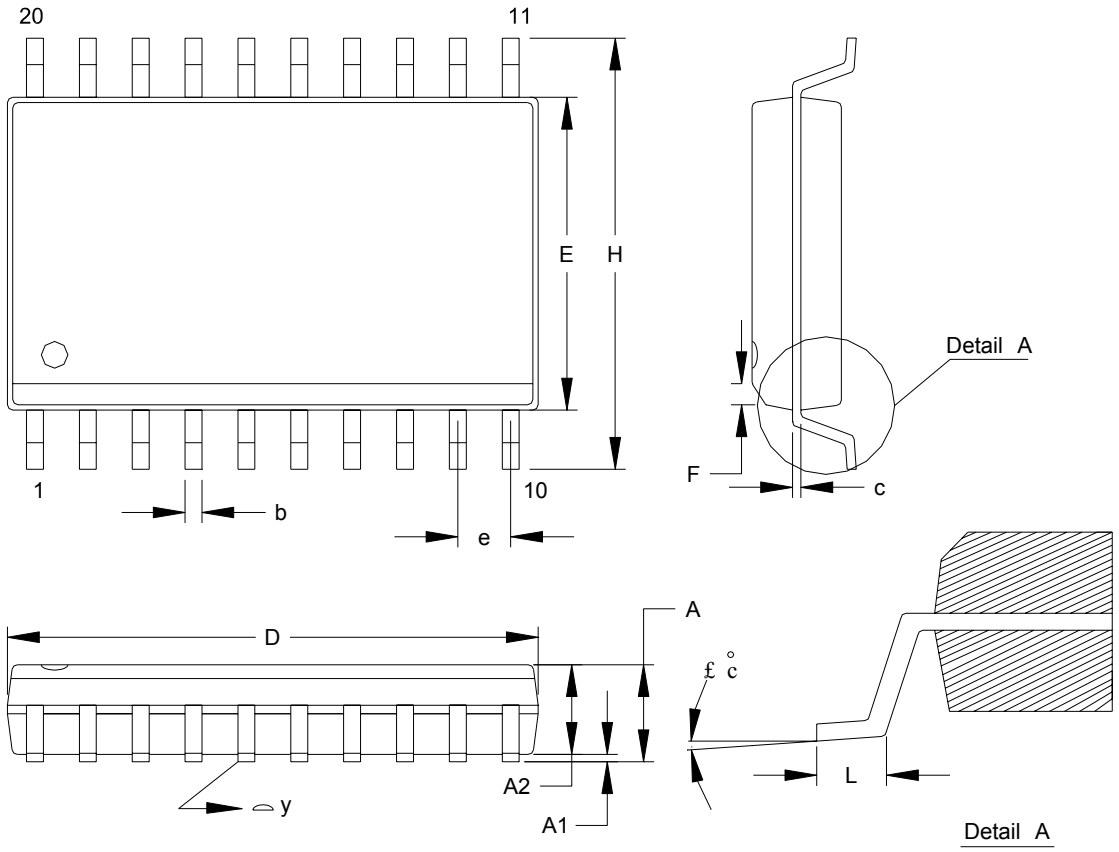
During startup of PWM stage, the SS pin will charge an external capacitor with a constant current source. The voltage on FBPWM will be clamped by SS voltage during startup. In the event of a protected condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.

Gate Drivers

SG6905 output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode to protect the external power MOSFET.

PACKAGE INFORMATION

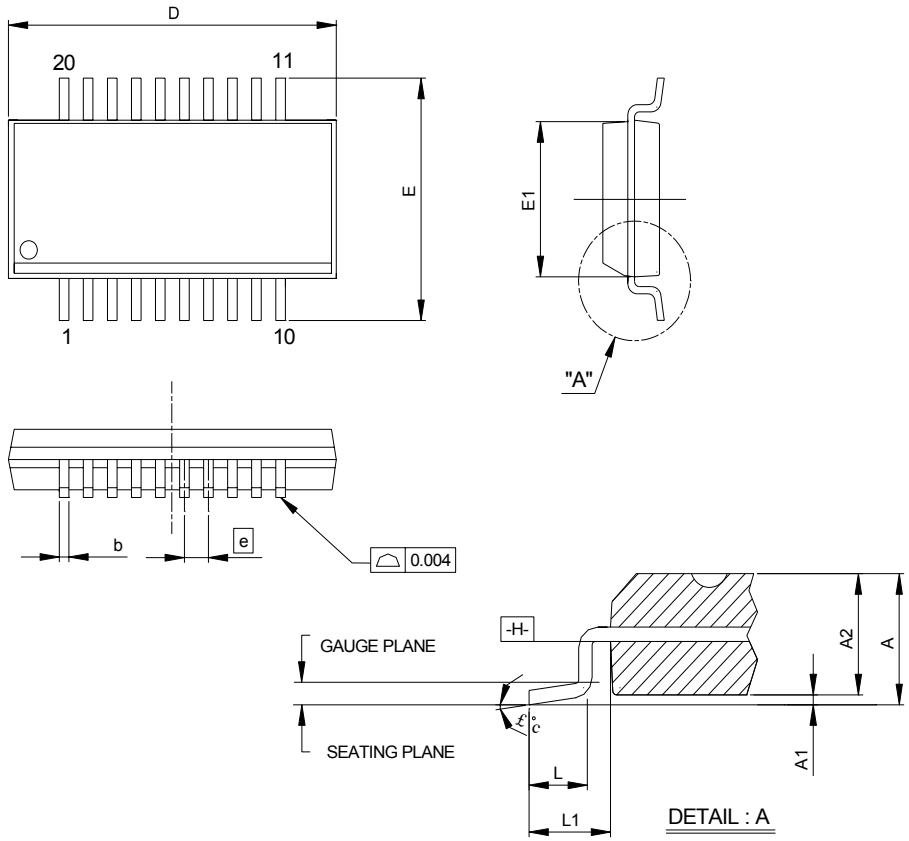
20 PINS – PLASTIC SOP (S)



Dimension:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362		2.642	0.093		0.104
A1	0.101		0.305	0.004		0.012
A2	2.260		2.337	0.089		0.092
b		0.406			0.016	
c		0.203			0.008	
D	12.598		12.903	0.496		0.508
E	7.391		7.595	0.291		0.299
e		1.270			0.050	
H	10.007		10.643	0.394		0.419
L	0.406		1.270	0.016		0.050
F		0.508X45°			0.020X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

20 PINS – PLASTIC SSOP (R)



Dimension:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053	0.064	0.069
A1	0.102		0.254	0.004	0.006	0.010
A2			1.499			0.059
b	0.203		0.305	0.008		0.012
C	0.178		0.254	0.007		0.010
D	8.560	8.661	8.738	0.337	0.341	0.344
E	5.791	5.994	6.198	0.228	0.236	0.244
E1	3.810	3.912	3.988	0.150	0.154	0.157
e		0.635 BASIC			0.025 BASIC	
L	0.406	0.635	1.270	0.016	0.025	0.050
L1		1.041 BASIC			0.041 BASIC	
θ°	0°		8°	0°		8°

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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