PRELIMINARY

SG901-1071 Miniature Wi-Fi Radio

Overview

The SG901-1071 Module is a single chip based 802.11b/g/n WLAN radio for embedded, low-power and extremely small form factor mobile applications. The product conforms to the IEEE 802.11b, g, and n protocols operating in the 2.45GHz ISM frequency band supporting 802.11n modulations up to 72.2Mbps, all OFDM modulations, and all mandatory 802.11b modulations.

The SG901-1071 is a fully integrated wireless radio including RF Synthesizer/VCO, high-speed data converters, digital baseband processor, onboard MAC and PHY processors, Power Management, Power Amplifier, and LNA.

An on-board EEPROM stores calibration data for alignment-free integration.

Bluetooth integration features of the radio are made available.

An on-board crystal and filter simplify system integration. Just add one 1.8V regulator, 3.3V Power, Antenna, and host communications. For maximum flexibility, the SG901-1071 can optionally accept a wide range of external reference clock frequencies.

Host control is provided by either an SDIO or SPI interface.

Features

- Very Small Footprint (12.7x10.3mm)
- RoHs compliant
- Fully integrated 802.11 System Solution
- Ultra Low Current consumption
- Fully compliant with the IEEE 802.11bg, and n WLAN standards
- Support for 802.11n modulations up to 72.2Mbps, and all 802.11g and mandatory 802.11b modulations
- Intelligent Power Control, Including 802.11 Power Save Mode
- Supports SPI interface
- Supports SDIO interface

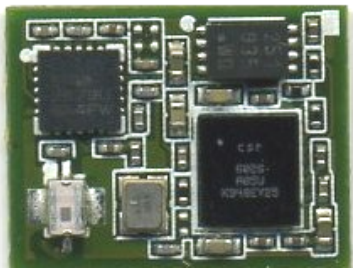
Applications

- Personal Digital Assistants (PDA)
- Portable Computers
- Hand-held Data Transfer Devices
- Cameras
- Computer Peripherals
- Cable Replacement
- Cellular Phones

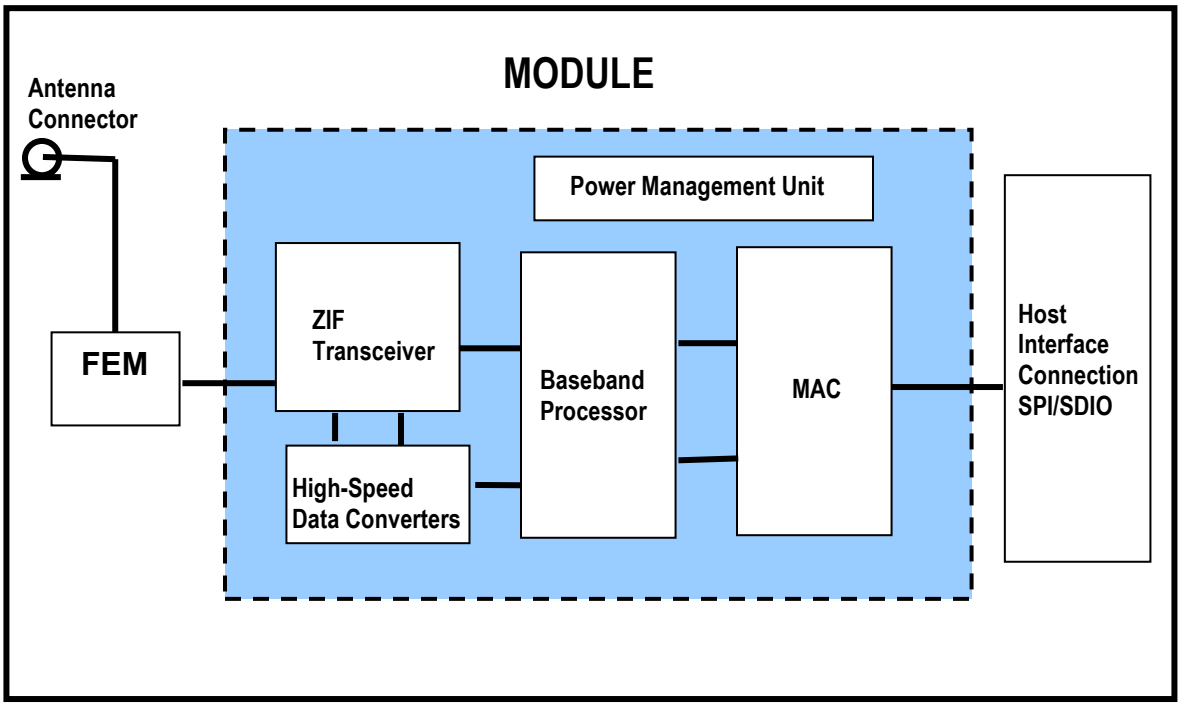
Ordering Information

Tape and Reel	SG901-1071-TR
Bulk	SG901-1071-BLK

Evaluation Kit Available



Block Diagram



General Electrical Specifications

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Absolute Maximum Ratings						
3.0V Supply			-0.3		3.6	V
VLDO Supply			-0.3		2.5	V
Operating Conditions and Input Power Specifications						
Operating Temperature Range			-30		85	°C
3.3V Supply	Input Supply Voltage	3.3V Supply input	2.7	3.3	3.6	V
	Standby Mode Current	32.768kHz Mode		270		uA
	Power Save Mode Current	DTIM = 1		2.5		mA
	Peak TX Current			270		mA
	Peak RX Current	Processing Packets		82		mA
Power Save Mode Settling Times	Wake up Time	From 32.768KHz Mode		5		mS
	Ramp up	To Processing Beacons		360		uS
	Ramp Down	To Stand By 32.768KHz mode		760		uS
VHIO Supply	Input Supply Voltage	VHIO input supply determines Host CMOS logic levels	1.7		3.3	V
	Input Supply Current	VHIO = 1.8V		TBD		mA
	Standby Mode Current	VHIO = 1.8V		TBD		uA
VLDO Supply	Input Supply Voltage	Required Internal regulator supply input	1.45		2.0	V
Input Voltage Levels	VIL		-0.3		0.25VHIO	V
	VIH		0.625VHIO		VHIO+0.3	V
Output Voltage Levels	VOL	IOL = 8.0mA			0.4	V
	VOH	IOH = -8.0mA	0.75VHIO		VHIO	V
Input Capacitance			1.0		5.0	pF

RF Characteristics

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Antenna Port Impedance				50		Ohms
Antenna Input Return Loss		CH1 to CH14	-9.5		-14	dB
RX Sensitivity	11b, 1Mbps		-97	-96.3	-93	dBm
	11b, 2 Mbps		-94	-92.5	-91	dBm
	11b, 5.5 Mbps		-92	-91	-89	dBm
	11b, 11 Mbps		-88	-86.7	-84	dBm
	11g, 9Mbps		-91	-89.6	-88	dBm
	11g, 18Mbps		-86	-84.9	-87	dBm
	11g, 36Mbps		-80	-78.6	-76	dBm
	11g, 54Mbps		-73	-71.4	-69	dBm
	11n, MCS1			-86		dBm
	11n, MCS3			-80		dBm
	11n, MCS5			-72		dBm
	11n, MCS7			-68		dBm
Channel to Channel De-sensitivity	CH1 to 14	11g, 54Mbps 10% PER	-0.7		0.7	dB
Maximum Input Signal	CH7	11g, 54Mbps	-19		-16	dBm
Adjacent Channel Rejection	1Mbps			50		
	11Mbps			47		
	9Mbps			25		dB
	54Mbps			13		dB
	MCS1			24		dB
	MCS7			5		dB
TX Output Power	11b, 1Mbps	@802.11b spectral mask	17	18.2	19	dBm
	11b, 11Mbps		17	18.2	19	dBm
	11g, 9Mbps	@802.11g spectral mask	17	17.9	19	dBm
	11g, 54Mbps	EVM = -27dB	12	13.4	15	dBm
	802.11n MCS1	@802.11n spectral mask		17		dBm
	802.11n MCS7	EVM = -27dB		13		dBm

Pinout List

SIGNAL NAME	PIN NUMBER	DESCRIPTION		NOTES
Reference Clock Pins				
OSC_EN	4	Oscillator Enable Output		not normally used – Contact Sagrad for options
REF_CLK	19	Reference Oscillator Input		normally not connected - Contact Sagrad for options
RF Pins				
BTH	13	Bluetooth RF Switched Interface		Input - Output
2G4_RF	16	Wi-Fi / Bluetooth Antenna Port, 50 ohms		
Serial Interface Pins (VHIO Domain, logic levels compatible with the VHIO (Pin 32) input voltage)				
SDCMD	25	SPI MOSI (input)	SDIO CMD	
SDCLK	26	SPI Clock Input	SDIO CLK	
SDD0	24	SPI MISO (output)	SDIO Data 0	
SDD1	23	SPI: Interrupt Output	SDIO Data 1	
SDD2	22		SDIO Data 2	
SDD3	21	SPI Chip Select Input	SDIO Data 3	
Control Pins				
POWERUP	5	Power Up Enable (from Host)		VLDO Domain with internal pull up High = operating, Low = off
RSTn	31	Reset Input		VHIO Domain – Active Low reset
SLEEPCLK	33	32.768 kHz Sleep Clock Input		VHIO Domain
DBG_SPI_CSn	27	Debug SPI Chip Select Input		VHIO Domain
DBG_SPI_CLK	30	Debug SPI Clock Input		VHIO Domain
DBG_SPI_MISO	28	Debug SPI Data Output		VHIO Domain
DBG_SPI_MOSI	29	Debug SPI Data Input		VHIO Domain
Bluetooth Coexistence Pins (VHIO Domain)				
WLAN_DENY	1	Bluetooth Coexistence		
BT_ACTIVE	3	Bluetooth Coexistence		
BT_PERIODIC	2	Bluetooth Coexistence		
BT_STATUS	34	Bluetooth Coexistence		
Power and Ground Pins				
VHIO	32	Supply Voltage for I/O's		1.7 to 3.3V, Internally decoupled with a 0.1uF capacitor
VLDO	6	External regulator supply input		1.45 to 2.0V, Internally decoupled with a 2.4uF capacitor
3.0V	8	RF supply		2.7 to 3.3V, Internally decoupled with a 0.2uF capacitor
GND	7, 9, 10, 11, 12, 14, 15, 17, 18, 20, 35	Ground Connections		

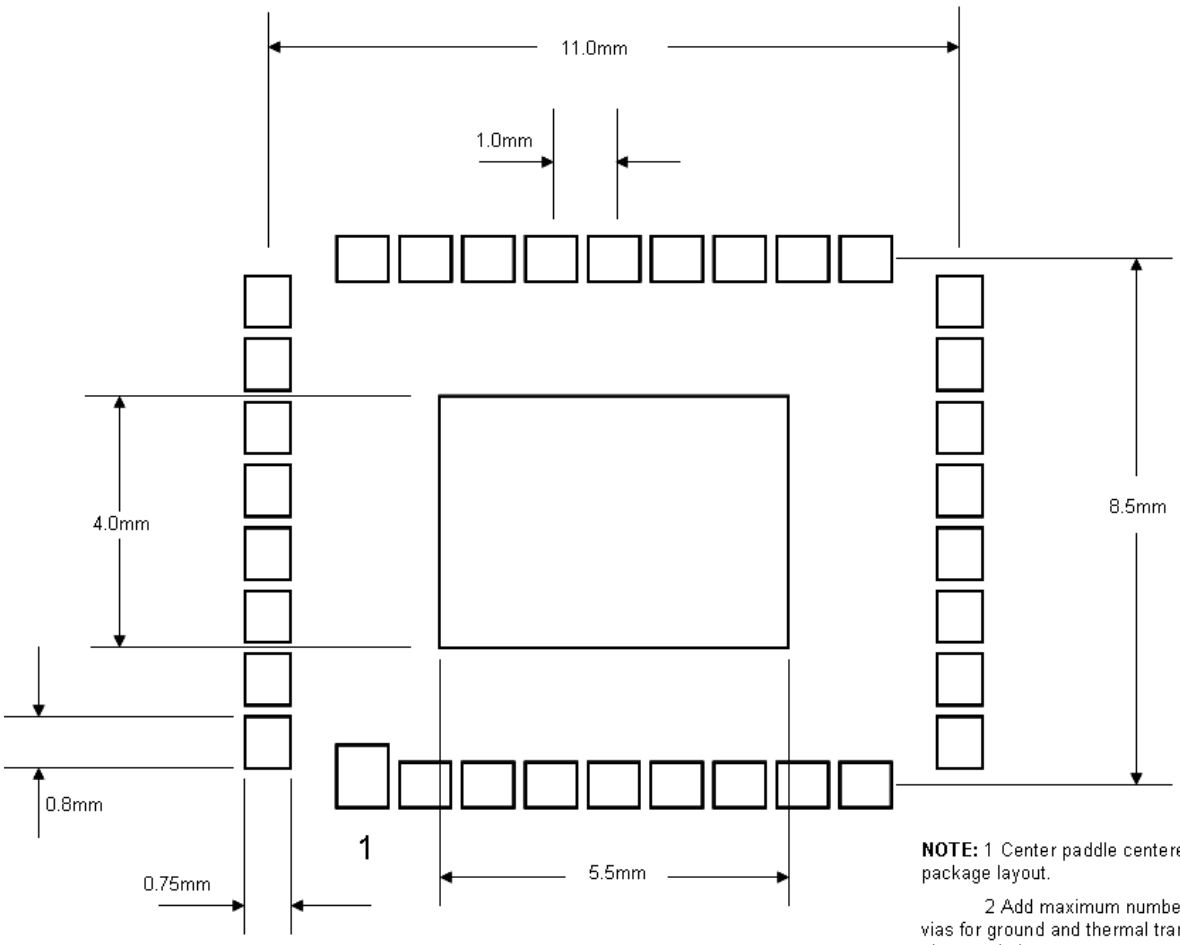
Software Support

Linux
2.6 Kernel

Encryption Support

Feature	Linux
Security	
WEP 40/64, 104/128	Yes
TKIP	Yes
AES/CCMP	Yes
WPA	Yes
WPA2	Yes
BIP	Yes
QoS	
WMM	Yes
Cisco Standards	
CCX v1	Yes
CCX v2	Yes
Bluetooth Coexistence	
PTA (802.15.2)	Yes
802.11/BT on same Antenna	Yes
Data and Voice Simultaneously	Yes
Data and Data Simultaneously	Yes
Voice and Voice Simultaneously	Yes

Recommended Layout



NOTE: 1 Center paddle centered on package layout.

2 Add maximum number of vias for ground and thermal transfer characteristics.