SGM2101
Five-Channel, High Efficiency, DC/DC Power Management Unit

GENERAL DESCRIPTION

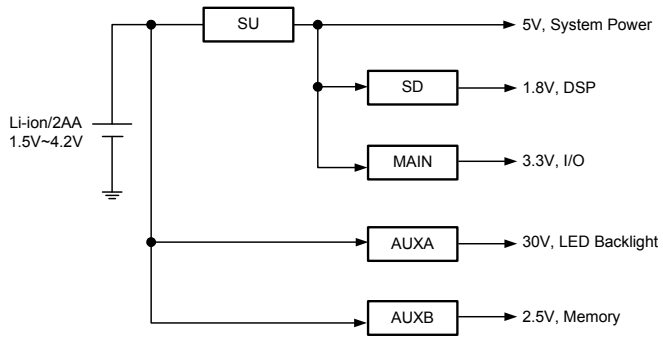
The SGM2101 is a single chip power management unit for a wide range of portable applications. It incorporates three synchronous switching regulators and two switching regulator controllers in a space saving thin QFN package. High efficiency, compact size and flexible configuration make SGM2101 the ideal power supply solution for two AA cells or single Li-ion battery powered equipments.

Synchronous switching regulators, SU, SD, & MAIN, provide the core powers for CPU, DSP and I/O. Switching regulator controllers, AUXA and AUXB, coupled with external MOSFETs provide versatile auxiliary powers for LCD panel bias, LED backlight, stepping motor, or memory module.

All channels operate at the same programmable constant switching frequency, ranging from 100kHz to 1MHz. Each channel, with built-in digital soft-start, can be individually selected, and programmed to the desired output voltage with two external resistors. Power OK, short-circuit flag and thermal protection features provide the system status and extra level of fault protection.

The SGM2101 is available in Green TQFN-7×7-48L package and is rated over the -40°C to +85°C temperature range.

TYPICAL APPLICATION IN DIGITAL CAMERAS



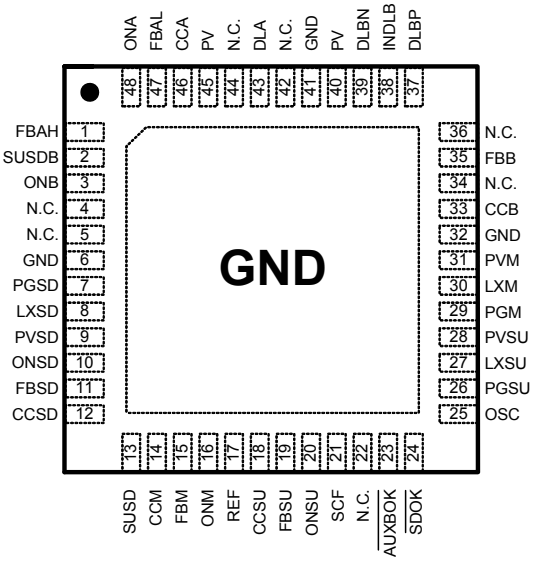
FEATURES

- **2A, Step-Up Synchronous Switching Regulator with 1.1V Start-Up Voltage, 90% Efficiency**
- **1A, Step-Down Synchronous Switching Regulator, 90% Efficiency**
- **1A, Pin Selectable Step-Up or Step-Down, Synchronous Switching Regulator, 90% Efficiency**
- **Constant Current Step-Up Switching Regulator Controller, LED Driver, with Output Open Protection**
- **Pin Selectable Step-Up or Step-Down Switching Regulator Controller, with Power OK Indicator**
- **Operates from 100kHz to 1MHz Switching Frequency**
- **Individual Enable, Digital Soft-Start and Overload Protection**
- **1μA Quiescent Current in Shutdown Mode**
- **Available in Green TQFN-7×7-48L Package**

APPLICATIONS

Digital still Cameras, Camcorders
Smart Mobile Phones, PDAs
Portable GPS Equipments
Handheld Multi-Media Equipments

PIN CONFIGURATION (TOP VIEW)



PACKAGE/ORDERING INFORMATION

ORDER NUMBER	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	MARKING INFORMATION	PACKAGE OPTION
SGM2101YTQC48/TR	TQFN-7×7-48L	-40°C to +85°C	SGM2101YTQ48	Tape and Reel, 2500

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range.....-65℃ to +125℃
Junction Temperature.....150℃
Operating Temperature Range.....-40℃ to +85℃
Lead Temperature (Soldering 10 sec)
.....260℃
ESD Susceptibility
HBM.....3000V
MM.....200V

NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	FBAH	Voltage Feedback Input of AUXA Controller. Connect a resistive voltage-divider from the boost converter output to FBAH to set the output voltage. The feedback threshold is 0.8V. This pin is high impedance in shutdown. FBAH provide conventional voltage.
2	SUSDB	Configures AUXB as a Boost or a Buck. This function must be hardwired. On-the-fly changes are not allowed. Connected it to PV for Step-up mode, and connect it to GND for Step-down mode.
3	ONB	AUXB Controller ON/OFF Input. Logic high = ON; however, turn-on is locked out until 1024 OSC cycles after the boost has reached regulation. This pin has an internal 475kΩ pull-down resistance to GND.
4	N.C.	No internal connection.
5	N.C.	No internal connection.
6	GND	Analog Ground. Connect all PGxx_ pins to GND with short wide traces as close to the IC as possible.

PIN DESCRIPTION

PIN	NAME	FUNCTION
7	PGSD	Power Ground. Connect all PGxx_ pins to GND with short wide traces as close to the IC as possible.
8	LXSD	Buck Converter Switching Node. Connect to the inductor of the buck converter. LXSD is high impedance in shutdown.
9	PVSD	Buck Converter Supply Input. Bypass to GND with a 1μF ceramic capacitor. The efficiency of this channel is measured from this pin.
10	ONSD	Buck Converter ON/OFF Control Input. Logic high = ON; however, turn-on is locked out until 1024 OSC cycles after the boost has reached regulation. This pin has an internal 475kΩ pull-down resistance to GND.
11	FBSD	Buck Converter Feedback Input. The feedback threshold is 0.8V. This pin is high impedance in shutdown.
12	CCSD	Buck Converter Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the control loop of the converter. This pin is actively driven to GND in shutdown, overload and thermal limit.
13	SUSD	Configures the Main Converter as a Boost or a Buck. This function must be hardwired. On-the-fly changes are not allowed. With SUSD connected to PV, the main is configured as a boost and PVM is the converter's output. With SUSD connected to GND, this channel is configured as a buck; PVM is the Power Source Input Pin of Main Converter.
14	CCM	Main Converter Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the control loop of the converter. This pin is actively driven to GND in shutdown, overload, and thermal limit.
15	FBM	Main Converter Feedback Input. The feedback threshold is 0.8V. This pin is high impedance in shutdown. The output voltage must not be set higher than the boost output.
16	ONM	Main ON/OFF Input. Logic high = ON; however, turn-on is lock out until 1024 OSC cycles after the boost has reached regulation. This pin has an internal 475kΩ pull-down resistance to GND.
17	REF	Reference Output. Bypass REF to GND with a 0.1μF or greater capacitor. The maximum allowed REF load is 200μA. REF is actively pulled to GND when the boost is shutdown.
18	CCSU	Boost Converter Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the control loop of the converter. This pin is actively driven to GND in shutdown, overload, and thermal limit.
19	FBSU	Boost Converter Feedback Input. The feedback threshold is 0.8V. This pin is high impedance in shutdown.
20	ONSU	Boost Converter ON/OFF Input. Logic high = ON; however, turn-on is lock out until 1024 OSC cycles after the boost has reached regulation. This pin has an internal 475kΩ pull-down resistance to GND.
21	SCF	Open-Drain, Active-Low, Short-Circuit Flag Output. SCF goes open when overload protection occurs and during startup. SCF can drive high-side PMOS switches connected to one or more outputs to completely disconnect the load when the channel turns off in response to a logic command or an overload.
22	N.C.	No internal connection.

PIN DESCRIPTION

PIN	NAME	FUNCTION
23	$\overline{\text{AUXBOK}}$	Open-Drain, Active-Low, Power-OK Signal of AUXB. $\overline{\text{AUXBOK}}$ goes low when the AUXB controller has successfully completed soft-start. $\overline{\text{AUXBOK}}$ goes high impedance in shutdown, overload, and thermal limit.
24	$\overline{\text{SDOK}}$	Open-Drain, Active-Low, Power-OK Signal of Buck Converter. $\overline{\text{SDOK}}$ goes low when the buck has successfully completed soft-start. $\overline{\text{SDOK}}$ goes high impedance in shutdown, overload and thermal limit.
25	OSC	Oscillator Control. Connect a timing capacitor from OSC to GND and a timing resistor from OSC to PVSU (or other DC voltage) to set the oscillator frequency between 100kHz and 1MHz. This pin is high impedance in shutdown.
26	PGSU	Power Ground. Connect all PGxx_ pins to GND with short wide traces as close to the IC as possible.
27	LXSU	Boost Converter Switching Node. Connect to the inductor of the boost converter. LXSU is high impedance in shutdown.
28	PVSU	Power Output of the Boost Converter regulator. PVSU can also power other converter channels. Connect PVSU and PV together.
29	PGM	Power Ground. Connect all PGxx_ pins to GND with short wide traces as close to the IC as possible.
30	LXM	Main Converter Switching Node. Connect to the inductor of the main converter (can be configured as a boost or a buck by SUSD). LXM is high impedance in shutdown.
31	PVM	When SUSD = PVSU, the main converter channel is configured as a boost and PVM is the main output. When SUSD = GND, main channel is configured as a buck and PVM is the power input.
32	GND	Analog Ground. Connect all PGxx_ pins to GND with short wide traces as close to the IC as possible.
33	CCB	AUXB Controller Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the control loop of the converter. This pin is actively driven to GND in shutdown, overload, and thermal limit.
34	N.C.	No internal connection.
35	FBB	AUXB Controller Feedback Input. The feedback threshold is 0.8V. This pin is high impedance in shutdown.
36	N.C.	No internal connection.
37	DLBP	AUXB Controller Gate-Drive Output. DLBP drives between INDLB and GND. The PMIC configures DLBP to drive a PMOS. DLBP is driven high in shutdown, overload and thermal limit.
38	INDLB	Voltage Input of AUXB Controller Gate-Drive. The voltage at INDLB sets the high gate-drive voltage. PMIC connect INDLB to the external PMOS source terminal to ensure the PMOS is completely off when DLBP swing high.
39	DLBN	AUXB Controller Gate-Drive Output. DLBN drives between INDLB and GND. The PMIC configures DLBN to drive an NMOS. DLBN is driven high in shutdown, overload and thermal limit.

PIN DESCRIPTION

PIN	NAME	FUNCTION
40	PV	IC Power Input. Connect pin 40 and pin 45 two PV pins together in application.
41	GND	Analog Ground. Connect all PGxx_ pins to GND with short wide traces as close to the IC as possible.
42	N.C.	No internal connection.
43	DLA	AUXA Controller Gate-Drive Output. Connect to the gate of an NMOS. DLA drives between PVSU and GND and supplies up to 500mA. This pin is actively driven to GND in shutdown, overload, and thermal limit.
44	N.C.	No internal connection.
45	PV	IC Power Input. Connect PVSU and PV together.
46	CCA	AUXA Controller Compensation Node. Connect a series resistor-capacitor from this pin to GND to compensate the control loop of the converter. This pin is actively driven to GND in shutdown, overload, and thermal limit.
47	FBAL	AUXA Controller Current-Feedback Input. Connect a resistor from FBAL to GND to set LED current in LED boost-drive circuits. The feedback threshold is 0.2V. Connecting this pin to GND if just use the FBAH feedback. This pin is high impedance in shutdown.
48	ONA	AUXA Controller ON/OFF Input. Logic high = ON; however, turn-on is locked out until 1024 OSC cycles after the boost has reached regulation. This pin has an internal 475kΩ pull-down resistance to GND.

ELECTRICAL CHARACTERISTICS

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDLB} = +3.6V, T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
Input Voltage Range		1.1		5.5	V
Boost Minimum Startup Voltage	I_{LOAD} < 1mA		1.2		V
Shutdown Supply Current into PV	PV = 3.6V		0.1	10	μA
Shutdown Supply Current into PV with Boost Enabled	ONSU = 3.6V, FBSU = 0.9V (does not include switching losses)		450	550	μA
Shutdown Supply Current into PV with Boost and Buck Enabled	ONSU = ONSD = 3.6V, FBSU = FBSD = 0.9V (does not include switching losses)		700	800	μA
Shutdown Supply Current into PV with Boost and Main Enabled	ONSU = ONM = 3.6V, FBSU = FBM = 0.9V (does not include switching losses)		700	800	μA
Shutdown Supply Current from PV and PVSU with Boost and One AUX Enabled	ONSU = ONA = 3.6V, FBSU = 0.9V (does not include switching losses)		650	750	μA
REFERENCE					
Reference Output Voltage	I_{REF} = 20μA	1.23	1.25	1.27	V
Reference Load Regulation	10μA < I_{REF} < 200μA		0.3	2	mV
Reference Line Regulation	2.7V < PVSU < 5.5V		0.2	2	mV
OSCILLATOR					
OSC Discharge Trip Level	Rising edge		1.2		V
OSC Discharge Resistance	OSC = 1.5V		86		Ω
OSC Discharge Pulse Width			200		ns
OSC Frequency	R_{OSC} = 47kΩ, C_{OSC} = 100pF		500		kHz
OVERLOAD PROTECTION					
Overload Protection Fault Delay			100,000		OSC cycles
SCF Leakage Current			0.1	1	μA
SCF Output Low Voltage			0.01	0.1	V
THERMAL LIMIT PROTECTION					
Thermal Shutdown			160		℃
Thermal Hysteresis			20		℃
LOGIC INPUTS (ONx, SUSD, SUSDB)					
ONSU Input Low Level	PVSU = 3.6V			0.4	V
ONSU Input High Level	PVSU = 3.6V	1.6			V
ONM, ONSD, ONA, ONB, SUSD and SUSDB Input Low Level	2.7V < PVSU < 5.5V			0.4	V
ONM, ONSD, ONA, ONB, SUSD and SUSDB Input High Level	2.7V < PVSU < 5.5V	1.6			V
SUSD Input Leakage			0.01	1	μA
ONx Impedance to GND			475		kΩ

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SU (BOOST REGULATOR)					
Boost Startup-to-Normal Operating Threshold	Rising edge or falling edge		2		V
Boost Startup-to-Normal Operating Threshold Hysteresis			80		mV
Boost Voltage Adjust Range		3.0		5.5	V
Start Delay of ONSD, ONM, ONA and ONB after SU in Regulation			1024		OSC cycles
FBSU Regulation Voltage		0.788	0.8	0.812	V
FBSU to CCSU Transconductance	FBSU = CCSU	80	120	160	μS
FBSU Input Leakage Current	FBSU = 0.8V	-100	0.01	100	nA
Skip Mode Trip Level			200		mA
Current-Sense Amplifier Transresistance			0.275		V/A
Boost Maximum Duty Cycle	FBSU = 0.75V	80	85	90	%
PVSU Leakage Current	V_{LX} = 0V, PVSU = 3.6V		0.1		μA
LXSU Leakage Current	V_{LX} = V_{OUT} = 3.6V		0.1	5	μA
Switch On-Resistance	N-Channel		150	300	mΩ
	P-Channel		200	300	
N-Channel Current Limit		1.8	2.1	2.4	A
P-Channel Turn-Off Current			75		mA
Startup Current Limit	PVSU = 1.8V		450		mA
Startup t_{OFF}	PVSU = 1.8V		800		ns
Startup Frequency	PVSU = 1.8V		200		kHz

ELECTRICAL CHARACTERISTICS

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDLB} = +3.6V, T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN (BOOST/BUCK REGULATOR)					
Main Boost Voltage Adjust Range	SUSD = PVSU	3.0		5.5	V
Main Buck Voltage Adjust Range	SUSD = GND, PVM must be greater than output	2.45		5.00	V
PVM Under-Voltage Lockout in Buck Mode	SUSD = GND	2.4	2.45	2.5	V
FBM Regulation Voltage		0.788	0.8	0.812	V
FBM to CCM Transconductance	FBM = CCM	80	120	160	μS
FBM Input Leakage Current	FBM =0.8V	-100	0.01	100	nA
Skip Mode Trip Level	Boost Mode (SUSD = PVSU)		200		mA
	Buck Mode (SUSD = GND)		150		
Current-Sense Amplifier Transresistance	Boost Mode (SUSD = PVSU)		0.25		V/A
	Buck Mode (SUSD = GND)		0.5		
Maximum Duty Cycle	Boost Mode (SUSD = PVSU)	80	85	90	%
	Buck Mode (SUSD = GND)		95		
LXM Leakage Current	V_{LXM} = 0V to 3.6V, PVSU = 3.6V		0.1	5	μA
Switch On-Resistance	N-Channel		150	300	mΩ
	P-Channel		200	300	
Synchronous Rectifier Turn-Off Current	Boost Mode (SUSD = PVSU)		75		mA
	Buck Mode (SUSD = GND)		100		
Soft-Start Interval			4096		OSC cycles

ELECTRICAL CHARACTERISTICS

(V_{PVSU} = V_{PV} = V_{PVM} = V_{PVSD} = V_{INDLB} = +3.6V, T_A = +25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SD (BUCK REGULATOR)					
Buck Output-Voltage Adjust Range	PVSD must be greater than output	1.25		5	V
FBSD Regulation Voltage		0.788	0.8	0.812	V
FBSD to CCSD Transconductance	FBSD = CCSD	80	120	160	μS
FBSD Input Leakage Current	FBSD = 0.8V	-100	0.01	100	nA
Skip Mode Trip Level			150		mA
Current-Sense Amplifier Transresistance			0.5		V/A
LXSD Leakage Current	V_{LXSD} = 0V to 3.6V, PVSU = 3.6V		0.1	5	μA
Switch On-Resistance	N-Channel		150	300	mΩ
	P-Channel		200	300	
P-Channel Current Limit		0.6	0.9	1.2	A
N-Channel Turn-Off Current			100		mA
Soft-Start Interval			2048		OSC cycles
$\overline{SDOK}$ Output Low Voltage	0.1mA into $\overline{SDOK}$		0.01	0.1	V
$\overline{SDOK}$ Leakage Current	ONSU = GND		0.01	1	μA

ELECTRICAL CHARACTERISTICS

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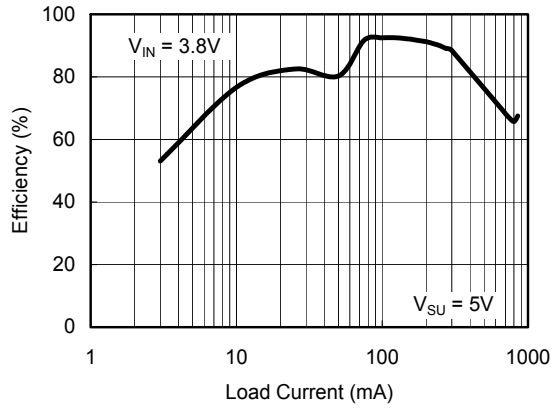
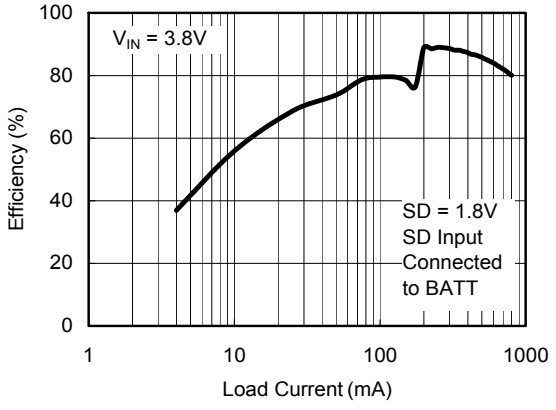
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AUXA and AUXB DC/DC CONTROLLERS					
Maximum Duty Cycle	FB_ = 0.75V	80	85	90	%
FBAH, FBB Regulation Voltage		0.788	0.8	0.812	V
FBAL Regulation Voltage			0.2		V
AUXB FB to CC Transconductance		80	120	160	μS
AUXA FBAL or FBAH to CC Transconductance		40	80	120	μS
FBx Input Leakage Current		-100	0.1	100	nA
DLx Driver Resistance	Output high or low		2.5		Ω
DLx Drive Current	Sourcing or sinking		0.5		A
Soft-Start Interval			4096		OSC cycles
$\overline{\text{AUXBOK}}$ Output Low Voltage	0.1mA into $\overline{\text{AUXBOK}}$		0.01	0.1	V
$\overline{\text{AUXBOK}}$ Leakage Current	ONB = GND		0.01	1	μA

TYPICAL PERFORMANCE CHARACTERISTICS

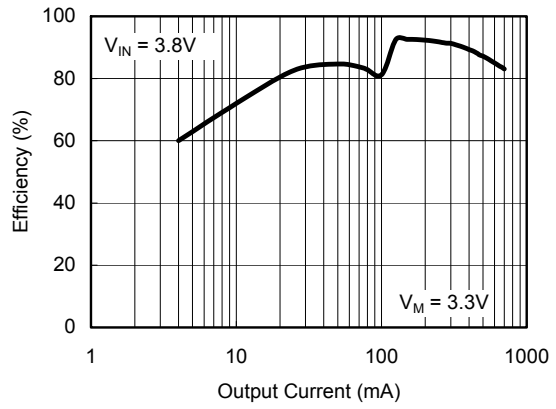
Step-Up Efficiency vs. Load Current



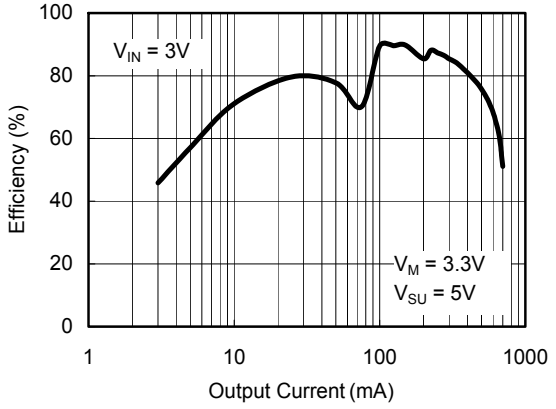
Step-Down Efficiency vs. Load Current



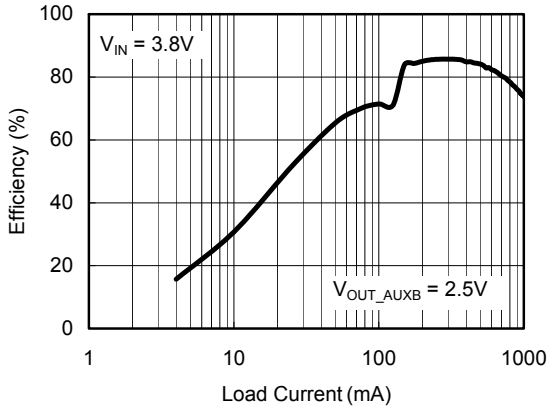
Main(Step-Down) Efficiency vs. Load Current



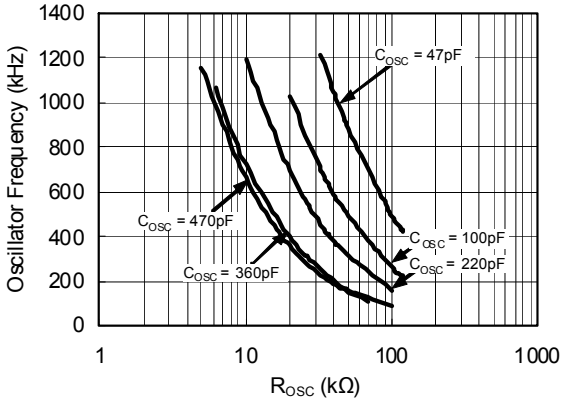
Main (Step-Up) Efficiency vs.Load Current



AUXB Efficiency vs. Load Current

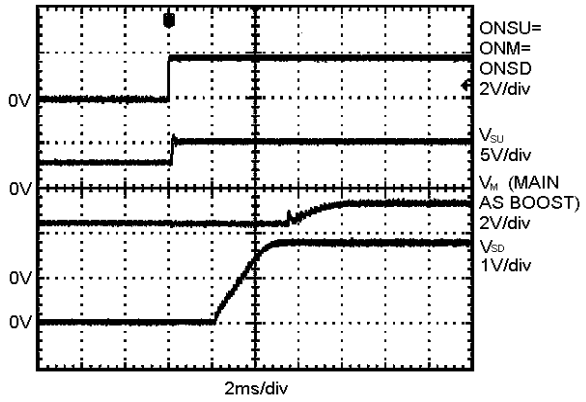


Oscillator Frequency vs. R_{OSC}

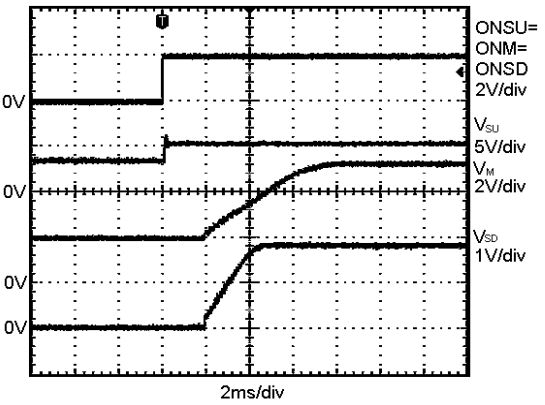


TYPICAL PERFORMANCE CHARACTERISTICS

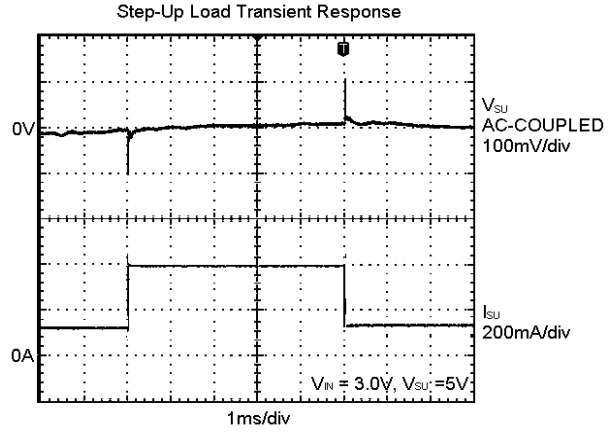
Main (Step-Up Mode) and Step-Down Startup Waveforms



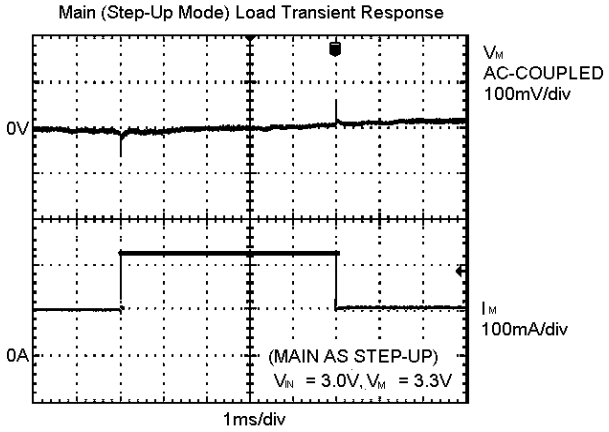
Main (Step-Down Mode) and Step-Down Startup Waveforms



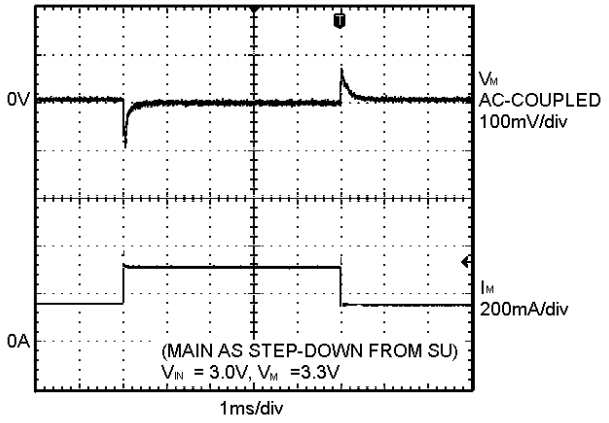
Step-Up Load Transient Response



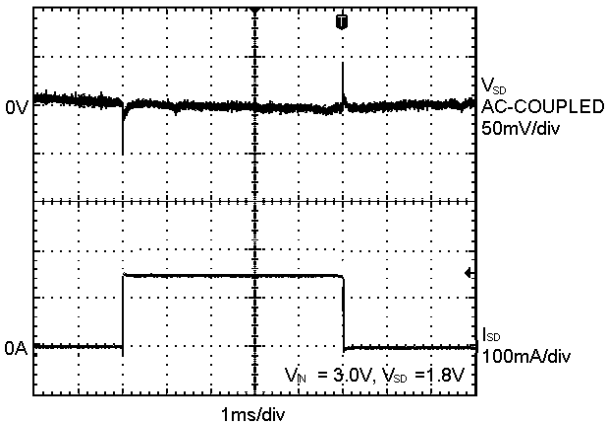
Main (Step-Up Mode) Load Transient Response



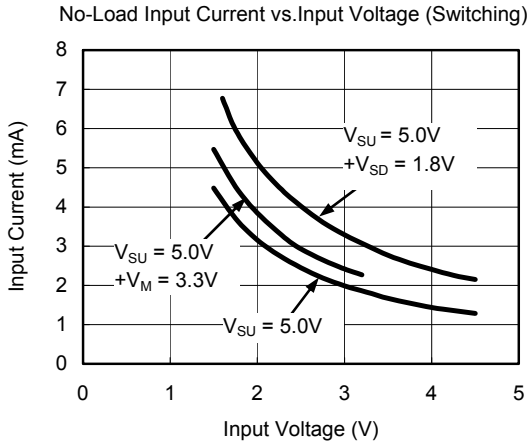
Main (Step-Down Mode) Load Transient Response

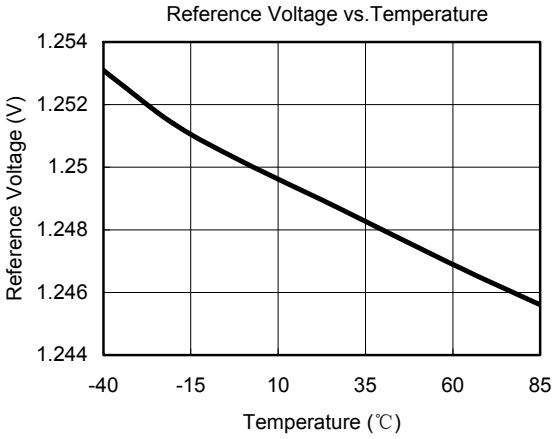


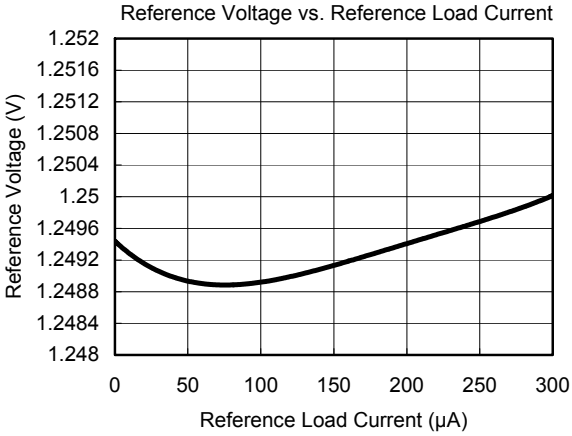
Step-Down Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS







DETAILED DESCRIPTION

The SGM2101 includes the following blocks to build a multiple-output power management unit for portable equipments. It can accept inputs from a variety of sources including 1-cell Li+ batteries, 2-cell alkaline or NiMH batteries, and even systems designed to accept both battery types. The SGM2101 includes five DC/DC converter channels to generate all required voltages:

• SU, boost DC/DC switching regulator, with on-chip power FETs.
• MAIN, pin selectable boost or buck DC/DC switching regulator with on-chip power FETs.
• SD, buck DC/DC switching regulator with on-chip power FETs.
• AUXA, DC/DC switching regulator controller for white LED as well as conventional boost applications; includes open LED overvoltage protection.
• AUXB, pin selectable boost or buck DC/DC switching regulator controller.

SU, Boost DC/DC Switching Regulator

The boost DC/DC switching converter typically is used to generate a 5V output voltage from a 1.5V to 4.5V battery input, but any output voltage from V_{IN} to 5V can be set. An internal NFET switch and external synchronous rectifier allow conversion efficiencies as high as 90%. For heavy loading case, the converter operates in a low-noise PWM mode with constant frequency. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. Efficiency is enhanced under light (<75mA TYP) loading by a Power Saving Mode that switches the boost only as needed to service the load. In this mode, the maximum inductor current is 200mA for each pulse.

MAIN, Boost or Buck DC/DC Switching Regulator

The main converter can be configured as a boost (Figure 2) or a buck converter (Figure 1) under the control of SUSD pin. The main DC/DC converter is typically used to generate 3.3V, but any voltage from 2.7V to 5V can be set; however, the main output must not be set higher than the boost output (PVSU).

An internal MOSFET switch and synchronous rectifier allow conversion efficiencies as high as 90%. Under moderate to heavy loading, the converter operates in a low-noise PWM mode with constant frequency. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. Efficiency is enhanced under light loading (<200mA typical for boost mode, <150mA typical for buck mode) by assuming a power saving mode during which the converter switches only as needed to service the load.

Buck operation can be direct from a Li+ cell if the minimum input voltage exceeds the desired output by approximately 200mV. Note that if the main DC/DC, operating as a buck, operates in dropout, the overload protection circuit senses an out-of-regulation condition and turns off all channels.

Li+ Battery to 3.3V Boost-Buck Operation

When generating 3.3V from an Li+ cell, boost-buck operation may be needed, so a regulated output can be maintained for input voltages above and below 3.3V. In this case, it may be best to configure the main converter as a buck (SUSD = GND) and to connect its input, PVM, to the boost output (PVSU), set to a voltage at or above 4.2V (Figures 1 and 3). The compound efficiency with this connection is typically up to 90%. This connection is also suitable for designs that must operate from both 1-cell Li+ and 2 AA cells.

Note that the boost output supplies both the boost load and the main buck input current when the main is powered from the boost. The main input current reduces the available boost output current for other loads.

2 AA to 3.3V Operation

In designs that operate only from 2 AA cells, the main DC/DC can be configured as a boost converter (SUSD = PVSU) to maximize the 3.3V efficiency (Figure 2).

SD, Buck DC/DC Switching Regulator

The buck DC/DC is optimized for generating low output voltages (down to 0.8V) at high efficiency. It runs from the power source from PVSD pin. PVSD pin can be connected directly to the battery if sufficient headroom exists to avoid dropout; otherwise, PVSD can be powered from the output of another converter. This Buck can also operate with the boost (main converter in boost mode) for boost- buck operation.

For heavy loading, the converter operates in a low-noise PWM mode with constant frequency and modulated pulse width. Efficiency is enhanced under light (<75mA TYP) loading by assuming a Power Saving Mode during which the buck switches only as needed to service the load. In this mode, the maximum inductor current is 150mA for each pulse. The buck DC/DC is inactive until the boost DC/DC is in regulation.

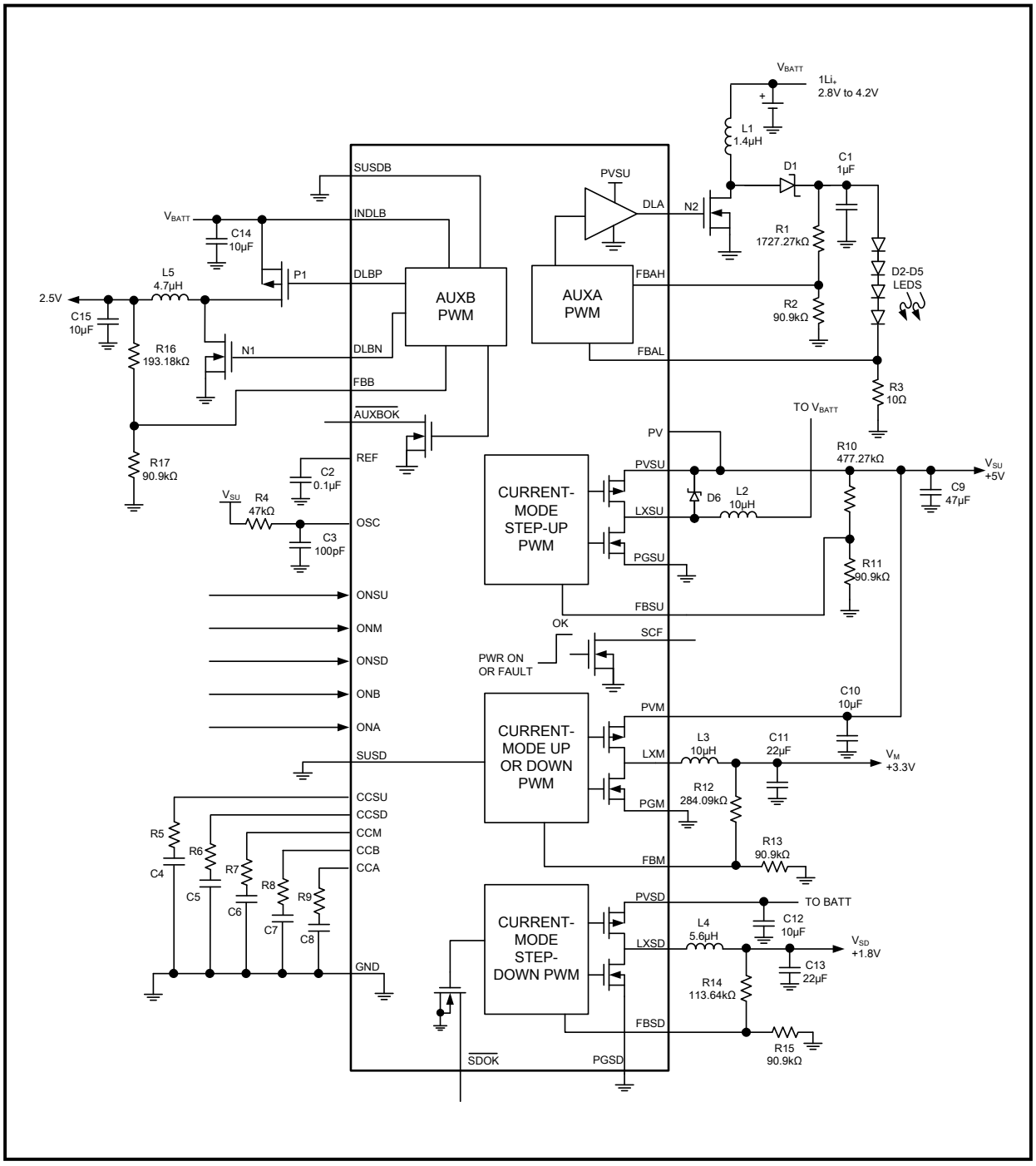


Figure 1. Typical 1-Cell Li+ Powered System (3.3V logic is stepped down from +5V or Battery, and 1.8V core is stepped down directly from the battery. Alternate connections are shown in the following Figures.)

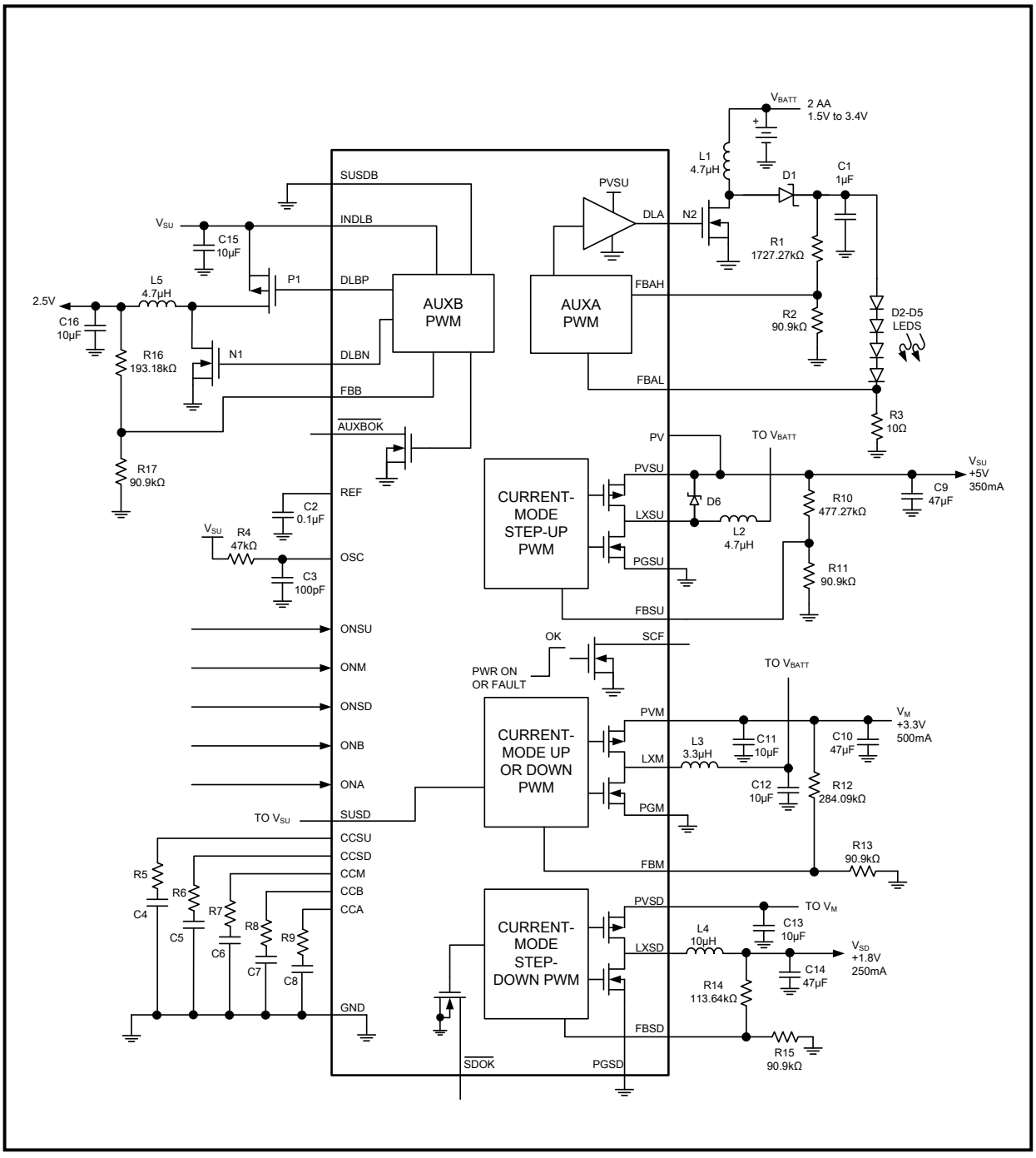


Figure 2. Typical 2-Cell AA-Powered System (3.3V is boosted from the battery and 1.8V is stepped down from V_M (3.3V).)

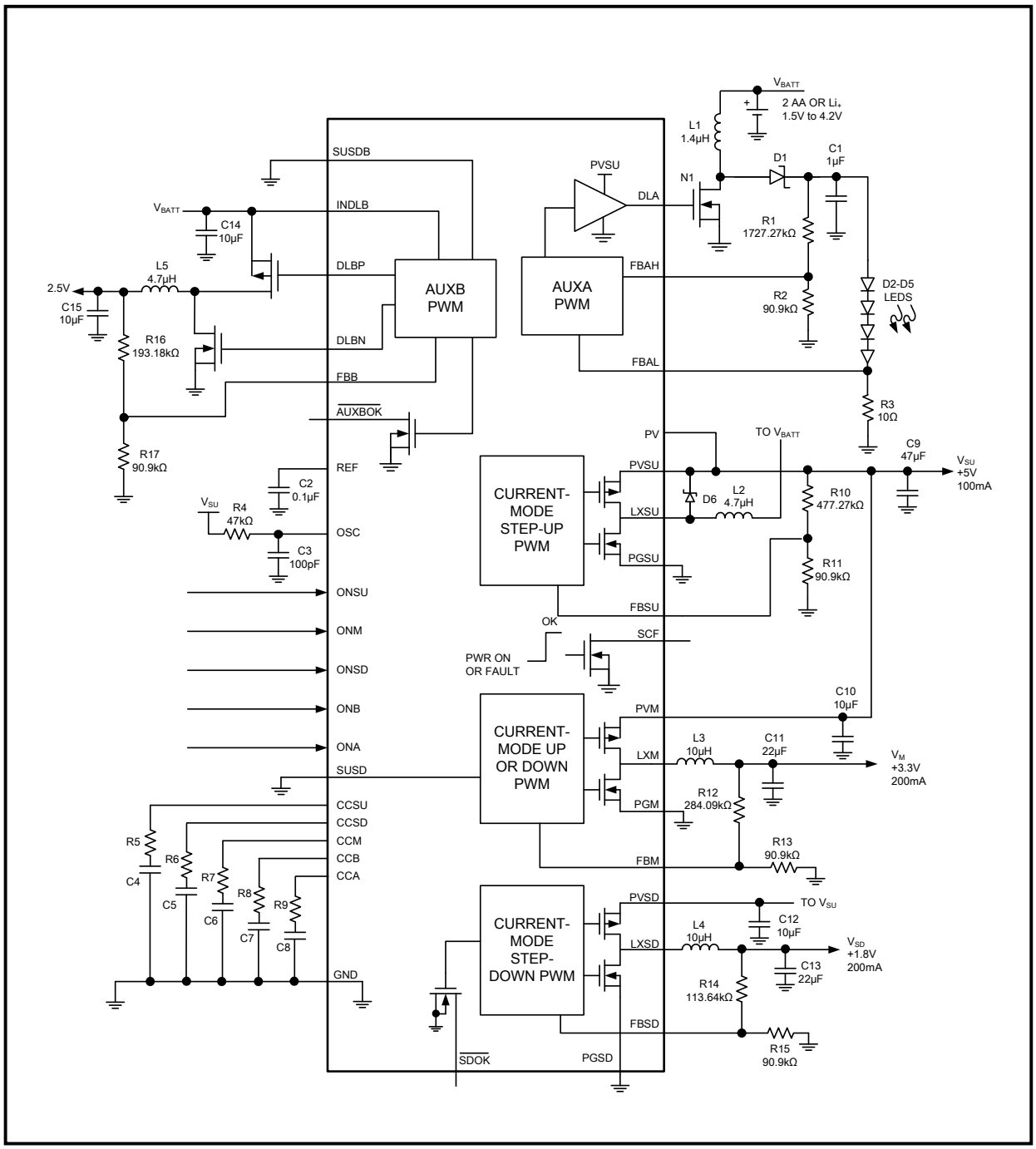


Figure 3. Li+ or Multi-battery Input (This power supply accepts inputs from 1.5V to 4.2V, so it can operate from either 2 AA cells or 1 Li+ cell. The 3.3V logic supply and the 1.8V core supply are both stepped down from 5V for true boost-buck operation.)

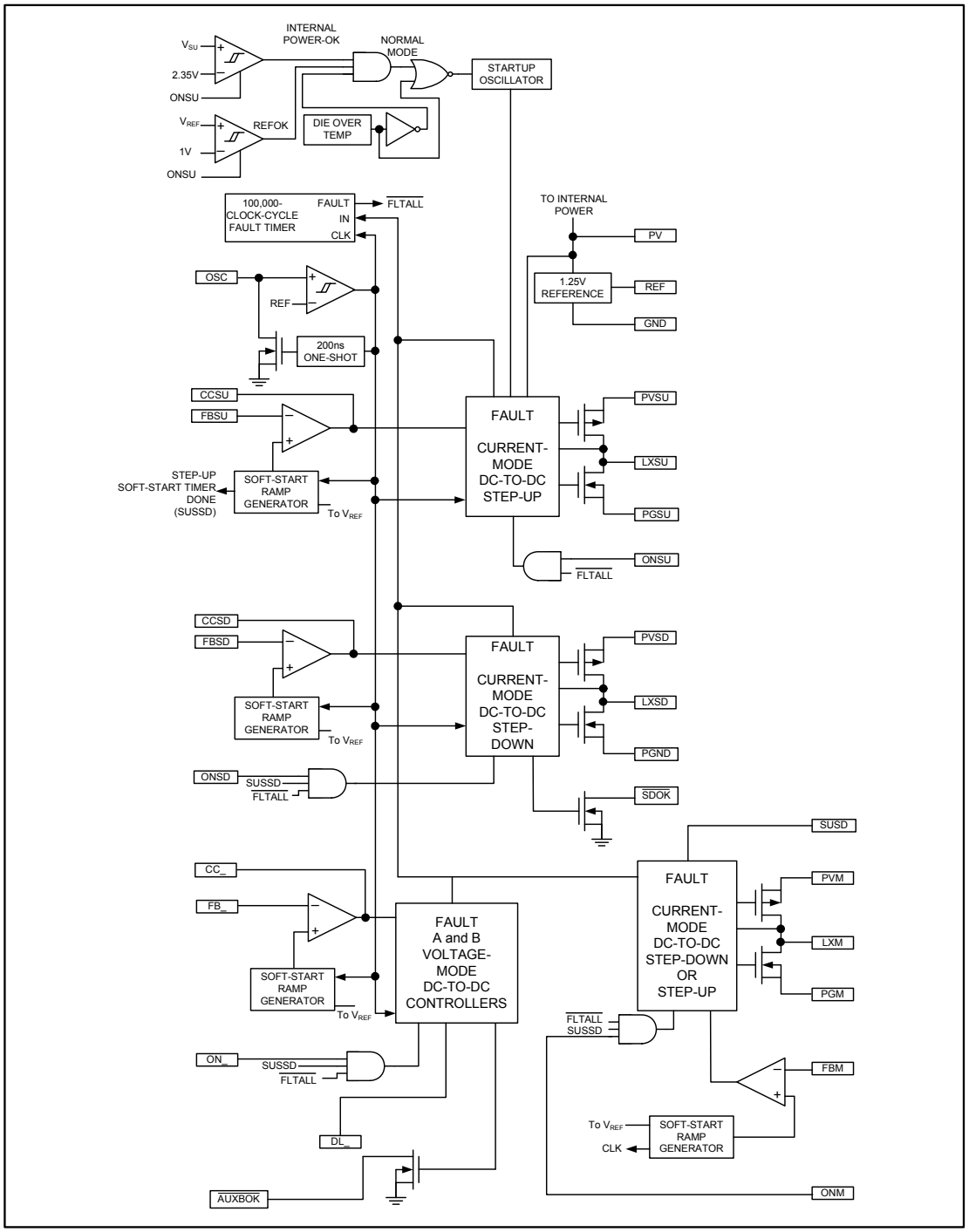


Figure 4. SGM2101 Functional Diagram

The buck also features an open-drain $\overline{SDOK}$ output that goes low when the buck output is in regulation. $\overline{SDOK}$ can be used to drive an external MOSFET switch that gates 3.3V power to the processor after the core voltage is in regulation. This connection is shown in Figure 9.

AUXA and AUXB DC/DC Controllers

The two auxiliary controllers operate as fixed-frequency voltage-mode PWM controllers. They do not have any internal MOSFETs, so output power is determined by external components. The controllers regulate output voltage by modulating the pulse width of the DL_ driver.
On the SGM2101, AUXB is PWM controller. AUXA is a boost/flyback controller that can be connected to regulate output voltage and/or current (for white-LED drive). AUXB can be configured to buck or boost DC/DC by SUSDB pin, the output power is dependent on external MOSFETs.

Maximum Duty Cycle

The AUX PWM controllers have a guaranteed maximum duty cycle of 80%: all controllers can achieve at least 80% and typically reach 85%. In boost designs that employ continuous current, the maximum duty cycle limits the boost ratio so:

$$1 - V_{IN} / V_{OUT} \leq 80\%$$

With discontinuous inductor current, no such limit exists for the input/output ratio since the inductor has time to fully discharge before the next cycle begins.

AUXA DC/DC Controller or LED Driver

The AUXA boost DC/DC controller has two feedback inputs, FBAL and FBAH, with feedback thresholds of 0.2V (FBAL) and 0.8V (FBAH). If used as a conventional voltage-output boost, FBAL is grounded and FBAH is used as the feedback input.
If AUXA is used as a switch-mode boost current source for white LEDs, FBAL provides current-sensing feedback, while FBAH provides (optional) open-LED overvoltage protection (Figure 5). In this application, the member of white-LED can be 3, 4 or more; it's dependent on the power Source Voltage.

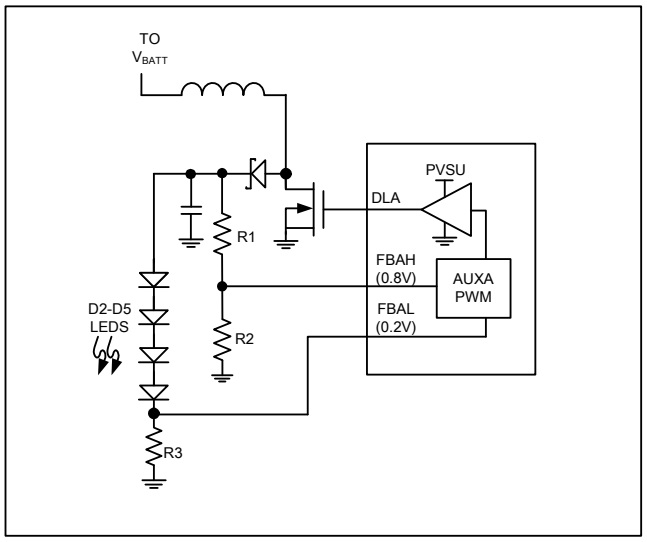


Figure 5. White LED drive with open LED overvoltage protection is provided by the additional voltage feedback input to FBAH

AUXB Boost or Buck DC/DC Controller

AUXB can be configured to Sync. or general buck controller, by connecting SUSDB pin to GND, Figure 6 is Sync. Buck DC/DC. This Sync. Buck can provide big current for heavy loading, customer can select different external MOSFETs to provide different output current.

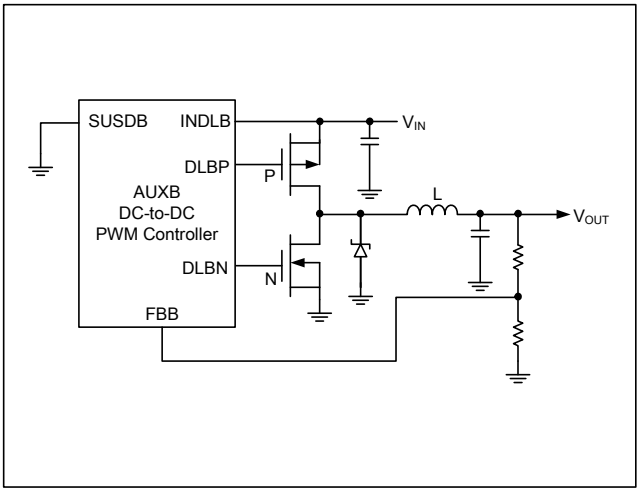


Figure 6. Sync. Buck DC/DC realized by AUXB Controller

Status Outputs ($\overline{SDOK}$, $\overline{AUXBOK}$, SCF)

The SGM2101 includes three versatile status outputs that can provide information to the system. All are open-drain outputs and can directly drive MOSFET switches to facilitate sequencing, disconnect loads during overloads, or perform other hardware-based functions.

$\overline{SDOK}$ pulls low when the buck has successfully completed soft-start. $\overline{SDOK}$ goes high impedance in shutdown, overload, and thermal limit. A typical use for $\overline{SDOK}$ is to drive a P-channel MOSFET that connects 3.3V power to the CPU I/O after the CPU core is powered up (Figure 9), thus providing safe sequencing in hardware without system intervention.

$\overline{AUXBOK}$ is Power good output of AUXB DC/DC controller.

SCF goes high (high impedance, open drain) when overload protection occurs. Under normal operation, SCF pulls low. SCF can drive a high-side P-channel MOSFET switch that can disconnect a load during power-up or when a channel turns off in response to a logic command or an overload. Several connections are possible for SCF. One is shown in Figure 11 where SCF provides load disconnect for the boost on fault and power-up.

Soft-Start

The SGM2101 channels feature a soft-start function that limits inrush current and prevents excessive battery loading at startup by ramping the output voltage of each channel up to the regulation voltage. This is accomplished by ramping the internal reference inputs to each channel error amplifier from 0V to the 0.8V reference voltage over a period of 4096 oscillator cycles (16ms at 500kHz) when initial power is applied or when a channel is enabled.

The buck soft-start ramp takes half the time (2048 clock cycles) of the other channel ramps. This allows the buck and main outputs to track each other and rise at nearly the same dV/dt rate on power-up. Once the buck output reaches its regulation point (1.5V or 1.8V TYP), the main output (3.3V TYP) continues to rise at the same ramp rate. See the Typical Performance Characteristics Main and Buck Startup Waveforms graphs.

Soft-start is not included in the SU channel to avoid limiting startup capability with loading.

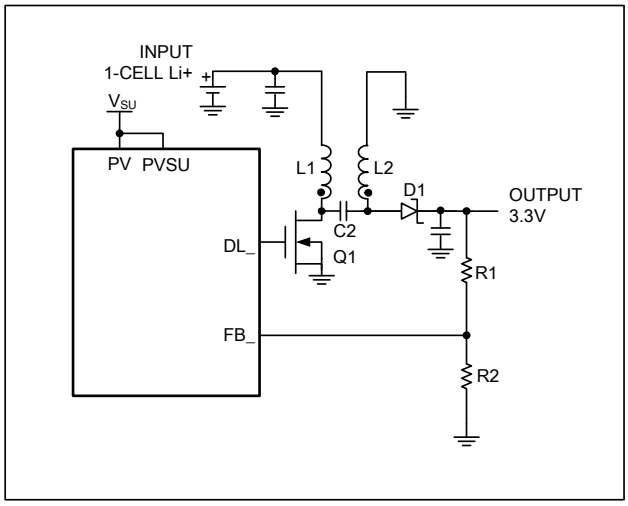


Figure 7. SEPIC Converter Additional Boost-Buck Channel

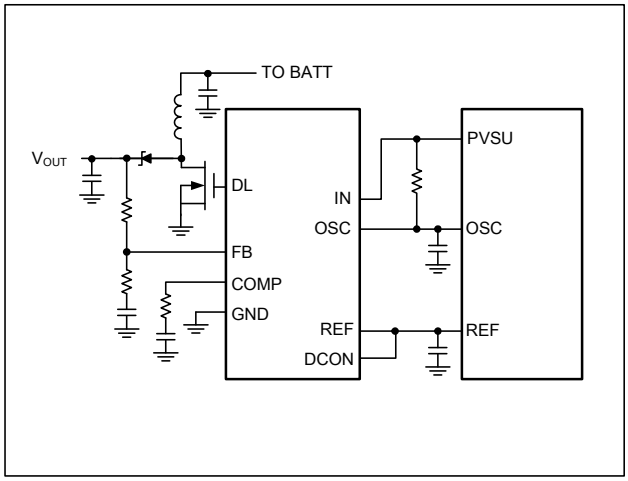


Figure 8. Adding a PWM Channel with an External Slave Controller

Fault Protection

The SGM2101 has robust fault and overload protection. After power-up, the device is set to detect an out-of-regulation state that could be caused by an overload or short. If any DC/DC converter channel (boost, main, buck, or any of the auxiliary controllers) remains faulted for 100,000 clock cycles (200ms at 500kHz), then all outputs latch off until the SU Channel is reinitialized by the ONSU pin or by cycling the input power. The fault detection circuitry for any channel is disabled during its initial turn-on soft-start sequence.

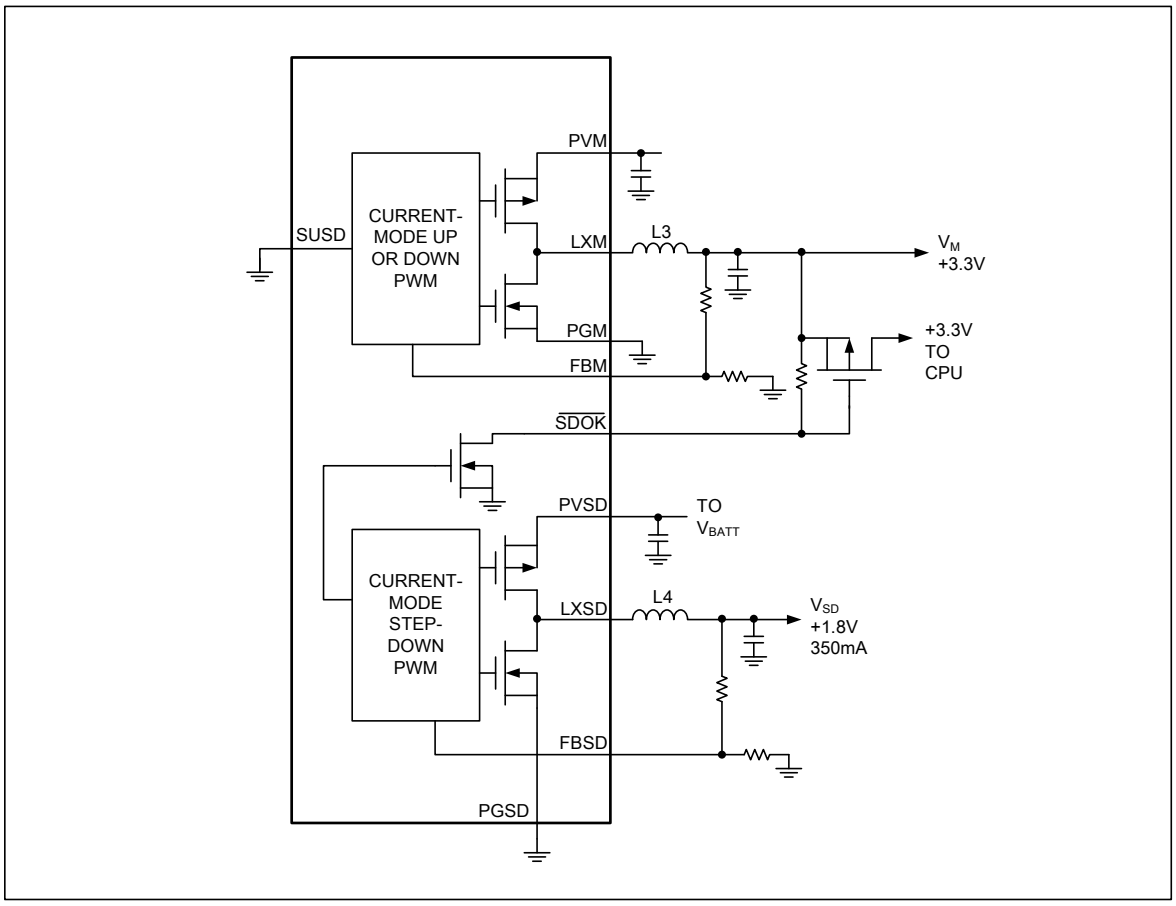


Figure 9. Using $\overline{\text{SDOK}}$ to Drive External PFET that Gates 3.3V Power to CPU after 1.8V Core Voltage Is in Regulation

An exception to the standard fault behavior is that there is no 100,000 clock cycle delay in entering the fault state if the boost output (PVSU) is dragged below its 2.5V UVLO threshold or is shorted. In this case, the boost UVLO immediately triggers and shuts down all channels. The boost then continues to attempt starting. If the boost output short remains, these attempts cannot succeed since PVSU remains near ground.

If a soft-short or overload remains on PVSU, the startup oscillator switches the internal N-channel MOSFET, but fault is retriggered if regulation is not achieved by the end of the soft-start interval. If PVSU is dragged below the input, the overload is supplied by the body diode of the internal synchronous rectifier, or by a Schottky diode connected from the battery to PVSU. If desired, this overload current can be interrupted by a P-channel MOSFET controlled by SCF, as shown in Figure 11.

Reference

The SGM2101 has a precise 1.25V reference. Connect a 0.1μF ceramic bypass capacitor from REF to GND within 0.2in (5mm) of the REF pin. REF can source up to 200μA and is enabled whenever ONSU is high and PVSU is above 2.5V. If the 200μA REF load limit must be exceeded, buffer REF with an external op amp.

Shutdown

The boost converter is activated with a high input at ONSU. The main converter (boost or buck) is activated by a high input on ONM. The buck and auxiliary DC/DC converters A and B activate with high inputs at ONSD, ONA and ONB respectively. The buck, main, and AUX_ converters cannot be activated until PVSU is in regulation. For automatic startup, connect ON_ to PVSU or a logic level greater than 1.6V.

Oscillator

All DC/DC converter channels employ fixed- frequency PWM operation. The operating frequency is set by an RC network at the OSC pin. The range of usable settings is 100kHz to 1MHz. Figure 10 is the function diagram of oscillator.

The oscillator uses a comparator, a 200ns one-shot, and an internal NFET switch in conjunction with an external timing resistor and capacitor (Figure 10). When the switch is open, the capacitor voltage exponentially approaches the boost output voltage from zero with a time constant given by the product of R_{OSC} and C_{OSC}. The comparator output switches high when the capacitor voltage reaches V_{REF} (1.25V). In turn, the one-shot activates the internal MOSFET switch to discharge the capacitor for 200ns, and the cycle repeats. The oscillation frequency changes as the main output voltage ramps upward following startup. The oscillation frequency is then constant once the main output is in regulation.

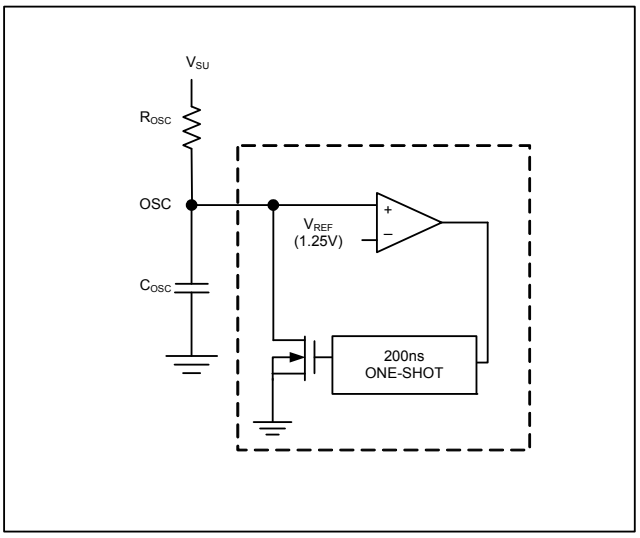


Figure 10. Oscillator Function Diagram

Low-Voltage Startup Oscillator

The SGM2101 internal control and reference voltage circuitry receive power from PVSU and do not function when PVSU is less than 2.5V. To ensure low voltage startup, the boost employs a low-voltage startup oscillator that activates at 1.2V if a Schottky rectifier is connected from V_{BATT} to PVSU (1.1V with no Schottky rectifier). The startup oscillator drives the internal N-channel MOSFET at LXSU until PVSU reaches 2.5V, at which point voltage control is passed to the current-mode PWM circuitry.

Once in regulation, the SGM2101 operates with inputs as low as 1.1V since internal power for the IC is supplied by PVSU. At low input voltages, the boost may have difficulty starting into heavy loads. However, this can be remedied by connecting an external P-channel load switch driven by SCF so the load is not connected until the PVSU is in regulation (Figure 11).

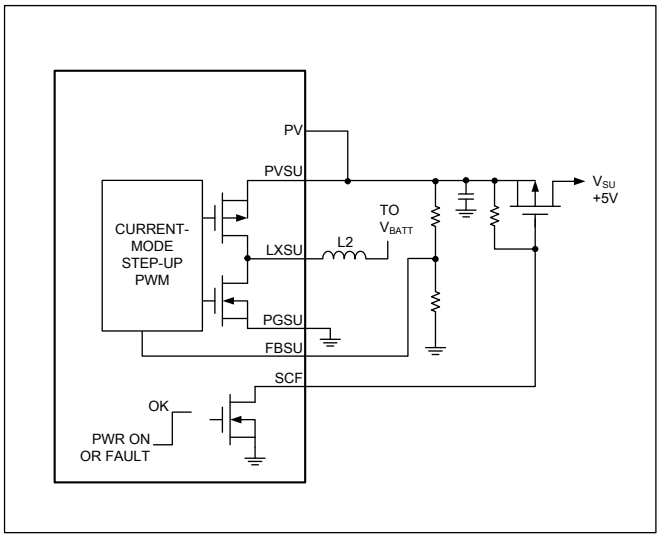


Figure 11. SCF Drives PFET Load Switch on 5V to Disconnect Load on Fault and Allow Full-Load Startup

DESIGN GUIDE

Setting the Switching Frequency

Choose a switching frequency to optimize external component size or circuit efficiency for the particular application. Typically, switching frequencies between 400kHz and 500kHz offer a good balance between component size and circuit efficiency—higher frequencies generally allow smaller components, and lower frequencies give better conversion efficiency. The switching frequency is set with an external timing resistor (R_{OSC}) and capacitor (C_{OSC}). At the beginning of a cycle, the timing capacitor charges through the resistor until it reaches V_{REF}. The charge time, t_1, is as follows:

$$t_1 = -R_{OSC} \times (C_{OSC} + C_{par}) \times \ln [1 – (1.25 / V_{PVSU})]$$

where C_{par} (15pF TYP) is the parasitic capacitance at the OSC pin due to internal ESD protection structure and the die-to-package capacitance.

The internal comparator that compares the capacitor C_{OSC} voltage to the reference has a delay td of 50ns (TYP). The capacitor voltage then decays to zero over time, t_2 = 200ns. The oscillator frequency is as follows:

$$f_{OSC} = 1 / (t_1 + t_d + t_2)$$

f_{OSC} can be set from 100kHz to 1MHz. Choose C_{OSC} between 22pF and 470pF. Determine R_{OSC}:

$$R_{OSC} = (200ns + 50ns - 1/ f_{OSC}) / ([C_{OSC} + C_{par}] \ln[1 - 1.25 / V_{PVSU}])$$

See the Typical Performance Characteristics for f_{OSC} vs. R_{OSC} using different values of C_{OSC}.

Setting Output Voltages

All SGM2101 output voltages are resistor set. The FB_ threshold is 0.8V for all channels except for FBAL (0.2V). When setting the voltage for any channel, connect a resistive voltage-divider from the channel output to the corresponding FB_ input and then to GND. The FB_ input bias current is less than 100nA, so choose the bottom-side (FB_-to-GND) resistor to be 100kΩ or less. Then calculate the top-side (output-to-FB_) resistor:

$$R_{TOP} = R_{BOTTOM}[(V_{OUT} / 0.8) - 1]$$

When using AUXA to drive white LEDs (Figure 5), select the LED current-setting resistor R_3 (Figure 5) using the following formula:

$$R_3 = 0.2V / I_{LED}$$

General Filter Capacitor Selection

The input capacitor in a DC/DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. One 4.7μF to10.0μF and one 0.01μF ceramic capacitors are recommended to be used as decoupling capacitors.

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance.

Output ripple with a ceramic output capacitor is approximately as follows:

$$V_{RIPPLE} = I_{L(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$$V_{RIPPLE(ESR)} = I_{L(PEAK)} \times ESR$$

Output capacitor specifics are also discussed in each converter's *Compensation* section.

Boost Component Selection

This section describes component selection for the boost, as well as for the main, if SUSD = PV.

The external components required for the boost are an inductor, an input and output filter capacitor, and a compensation RC.

The inductor is typically selected to operate with continuous current for best efficiency. An exception might be if the boost ratio, (V_{OUT} / V_{IN}), is greater than 1/ (1 - D_{MAX}), where D_{MAX} is the maximum PWM duty factor of 80%.

When using the boost channel to boost from a low input voltage, loaded startup is aided by connecting a Schottky diode from the battery to PVSU.

Boost Inductor

In most boost designs, a reasonable inductor value (L_{IDEAL}) can be derived from the following equation, which sets continuous peak-to-peak inductor current at 1/2 the DC inductor current:

$$L_{IDEAL} = [2V_{IN(MAX)} \times D(1 - D)] / (I_{OUT} \times f_{OSC})$$

where D is the duty factor given by:

$$D = 1 - (V_{IN} / V_{OUT})$$

Given L_{IDEAL}, the consistent peak-to-peak inductor current is 0.5 I_{OUT} / (1 - D). The peak inductor current, $I_{IND(PK)}$ = I_{OUT} / (1 - D).
Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises and a larger output capacitance may be required to suppress output ripple.

Boost Compensation
The inductor and output capacitor are usually chosen first in consideration of performance, size, and cost. The compensation resistor and capacitor are then chosen to optimize control-loop stability. In some cases, it may help to re-adjust the inductor or output-capacitor value to get optimum results. For typical designs, the component values in the circuit of Figure 1 yield good results.
The boost converter employs current-mode control, thereby simplifying the control-loop compensation. When the converter operates with continuous inductor current (typically the case), a right-half-plane zero appears in the loop-gain frequency response. To ensure stability, the control-loop gain should cross over (drop below unity gain) at a frequency (f_C) much less than that of the right-half-plane zero.
The relevant characteristics for boost channel compensation are as follows:
• Transconductance (from FB to CC), gm_{EA} (135μS)
• Current-sense amplifier transresistance, R_{CS} (0.3V/A)
• Feedback regulation voltage, V_{FB} (0.8V)
• Boost output voltage, V_{SU}, in V
• Output load equivalent resistance, R_{LOAD}, in Ω =V_{OUT}/ I_{LOAD}

The key steps for boost compensation are as follows:
1) Place f_C sufficiently below the right-half-plane zero (RHPZ) and calculate C_C.
2) Select R_C based on the allowed load-step transient. R_C sets a voltage delta on the C_C pin that corresponds to load-current step.
3) Calculate the output-filter capacitor (C_{OUT}) required to allow the R_C and C_C selected.
4) Determine if C_P is required (if calculated to be >10pF).
For continuous conduction, the right-half-plane zero frequency (f_{RHPZ}) is given by the following:

$$f_{RHPZ} = V_{OUT}(1 - D)^2 / (2\pi \times L \times I_{LOAD})$$

where D = the duty cycle = 1 - (V_{IN} / V_{OUT}), L is the inductor value, and I_{LOAD} is the maximum output current. Typically target crossover (f_C) for 1/6 of the RHPZ. For example, if we assume f_{OSC} = 500kHz, V_{IN} = 2.5V, V_{OUT} = 5V, and I_{OUT} = 0.5A, then R_{LOAD} = 10Ω. If we select L = 4.7μH, then:

$$f_{RHPZ} = 5 (2.5 / 5)^2 / (2\pi \times 4.7 \times 10^{-6} \times 0.5) = 84.65kHz$$

Choose f_C = 14kHz. Calculate C_C:
$C_C = (V_{FB} / V_{OUT})(R_{LOAD} / R_{CS})(g_M / 2\pi \times f_C)(1 - D)$
= (0.8 / 5)(10 / 0.3) x [135μS / (6.28 x 14kHz)] (2/5)
= 4.1nF

Choose 4.1nF.
Now select R_C so transient-droop requirements are met. As an example, if 4% transient droop is allowed, the input to the error amplifier moves 0.04 x 0.8V, or 32mV. The error-amp output drives 32mV x 135μS, or 4.32μA, across R_C to provide transient gain. Since the current-sense transresistance is 0.3V/A, the value of R_C that allows the required load-step swing is as follows:

$$R_C = 0.3 I_{IND(PK)} / 4.32\mu A$$

In a boost DC/DC converter, if L_{IDEAL} is used, output current relates to inductor current by:

$$I_{IND(PK)} = I_{OUT} / (1 - D) = I_{OUT} \times V_{OUT} / V_{IN}$$

So, for a 500mA output load step with V_{IN} = 2.5V and V_{OUT} = 5V:

$$R_C = [(0.3 \times 0.5 \times 5) / 2)] /4.32\mu A = 86.8k\Omega$$

Note that the inductor does not limit the response in this case since it can ramp at 2.5V / 4.7μH, or 530mA/μs.
The output filter capacitor is then chosen so the C_{OUT} R_{LOAD} pole cancels the R_C C_C zero:

$$C_{OUT} \times R_{LOAD} = R_C \times C_C$$

For the example:

$$C_{OUT} = 86.8k\Omega \times 6.8nF / 10\Omega = 59\mu F$$

Choose 59μF for C_{OUT}. If the available C_{OUT} is substantially different from the calculated value, insert the available C_{OUT} value into the above equation and recalculate R_C. Higher substituted C_{OUT} values allow a higher R_C, which provides higher transient gain and consequently less transient droop.

If the output filter capacitor has significant ESR, a zero occurs at the following:

$$Z_{ESR} = 1 / (2\pi \times C_{OUT} \times R_{ESR})$$

If $Z_{ESR} > f_C$, it can be ignored, as is typically the case with ceramic output capacitors. If Z_{ESR} is less than f_C, it should be cancelled with a pole set by capacitor C_P connected from C_C to GND:

$$C_P = C_{OUT} \times R_{ESR} / R_C$$

If C_P is calculated to be <10pF, it can be omitted.

Buck Component Selection

This section describes component selection for the buck converter, and for the main converter if used in buck mode (SUSD = GND).

Buck Inductor

The external components required for the buck are an inductor, input and output filter capacitors, and compensation RC network.

The SGM2101 buck converter provides best efficiency with continuous inductor current. A reasonable inductor value (L_{IDEAL}) can be derived from the following:

$$L_{IDEAL} = [2(V_{IN}) \times D(1 - D)] / I_{OUT} \times f_{OSC}$$

This sets the peak-to-peak inductor current at 1/2 the DC inductor current. D is the duty cycle:

$$D = V_{OUT} / V_{IN}$$

Given L_{IDEAL}, the peak-to-peak inductor current is 0.5 I_{OUT}. The absolute-peak inductor current is 1.25 I_{OUT}. Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, inductor current rises, and a larger output capacitance may be required to suppress output ripple. Larger values than L_{IDEAL} can be used to obtain higher output current, but typically with larger inductor size.

Buck Compensation

The relevant characteristics for buck compensation are as follows:

- Transconductance (from FB to C_C), gm_{EA} (135μS)
- Buck slope-compensation pole, $P_{SLOPE} = V_{IN} /(\pi L)$
- Current-sense amplifier transresistance, R_{CS} (0.6V/A)
- Feedback-regulation voltage, V_{FB} (0.8V)
- Buck output voltage, V_{SD}, in V
- Output-load equivalent resistance, R_{LOAD}, in Ω = V_{OUT} / I_{LOAD}

The key steps for buck compensation are as follows:

1) Set the compensation R_C to zero to cancel the R_{LOAD} C_{OUT} pole.

2) Set the loop crossover below the lower of 1/5 the slope compensation pole or 1/5 the switching frequency.

If we assume V_{IN} = 2.5V, V_{OUT} = 1.8V, and I_{OUT} = 350mA, then R_{LOAD} = 5.14Ω.

If we select f_{OSC} = 500kHz and L = 5.6μH.

$P_{SLOPE} = V_{IN} / (\pi L)$ = 142kHz, so choose f_C = 24kHz and calculate C_C:

$C_C = (V_{FB} / V_{OUT})(R_{LOAD} / R_{CS})(g_M / 2\pi \times f_C)$
= (0.8 / 1.8)(5.14 / 0.6) x [135μS / (6.28 x 24kHz)]
= 4.1nF

Choose 4.1nF.

Now select R_C so transient-droop requirements are met. As an example, if 4% transient droop is allowed, the input to the error amplifier moves 0.04 x 0.8V, or 32mV. The error-amp output drives 32mV x 135μS, or 4.32μA across R_C to provide transient gain. Since the current-sense transresistance is 0.6V/A, the value of R_C that allows the required load-step swing is as follows:

$$R_C = 0.6\ I_{IND(PK)} / 4.32\mu A$$

In a buck DC/DC converter, if L_{IDEAL} is used, output current relates to inductor current by the following:

$$I_{IND(PK)} = 1.25\ I_{OUT}$$

So for a 250mA output load step with V_{IN} = 2.5V and V_{OUT} = 1.8V:

$$R_C = (1.25 \times 0.6 \times 0.25) / 4.32\mu A = 43.4k\Omega$$

Choose 43.4kΩ.

Note that the inductor does somewhat limit the response in this case since it ramps at (V_{IN} - V_{OUT}) / 5.6μH, or (2.5 - 1.8) / 5.6μH = 125mA/μs.

The output filter capacitor is then chosen so the C_{OUT} R_{LOAD} pole cancels the R_C C_C zero:

$$C_{OUT} \times R_{LOAD} = R_C \times C_C$$

For the example:

$$C_{OUT} = 43.4k\Omega \times 6.8nF / 5.14\Omega = 57.4\mu F$$

Since ceramic capacitors are common in either 22μF or 47μF values, 22μF is within a factor of two of the ideal value and still provides adequate phase margin for stability. If the output filter capacitor has significant ESR, a zero occurs at the following:

$$Z_{ESR} = 1 / (2\pi \times C_{OUT} \times R_{ESR})$$

If $Z_{ESR} > f_C$, it can be ignored, as is typically the case with ceramic output capacitors. If $Z_{ESR} < f_C$, it should be cancelled with a pole set by capacitor C_P connected from C_C to GND:

$$C_P = C_{OUT} \times R_{ESR} / R_C$$

If C_P is calculated to be <10pF, it can be omitted.

AUX Controller Component Selection
External MOSFET
All SGM2101 AUX controllers drive external logic- level MOSFETs. Significant MOSFET selection parameters are as follows:
• On-resistance ($R_{DS(ON)}$)
• Maximum drain-to-source voltage ($V_{DS(MAX)}$)
• Total gate charge (Q_G)
• Reverse transfer capacitance (C_{RSS})

Use a MOSFET with on-resistance specified with gate drive at or below the main output voltage. The gate charge, Q_G, includes all capacitance associated with charging the gate and helps to predict MOSFET transition time between on and off states. MOSFET power dissipation is a combination of on-resistance and transition losses. The on-resistance loss is as follows:

$$P_{RDSON} = D \times I_L^2 \times R_{DS(ON)}$$

where D is the duty cycle, I_L is the average inductor current, and $R_{DS(ON)}$ is MOSFET on-resistance. The transition loss is approximately as follows:

$$P_{TRANS} = (V_{OUT} \times I_L \times f_{OSC} \times t_T) / 3$$

where V_{OUT} is the output voltage, I_L is the average inductor current, f_{OSC} is the switching frequency, and t_T is the transition time. The transition time is approximately Q_G / I_G, where Q_G is the total gate charge, and I_G is the gate-drive current (0.5A TYP).
The total power dissipation in the MOSFET is as follows:

$$P_{MOSFET} = P_{RDSON} + P_{TRANS}$$

Diode
For most AUX applications, a Schottky diode rectifies the output voltage. Schottky low forward voltage and fast recovery time provide the best performance in most applications. Silicon signal diodes (such as 1N4148) are sometimes adequate in low-current (<10mA), high-voltage (>10V) output circuits where the output voltage is large compared to the diode forward voltage.

AUXA Compensation
The auxiliary controllers employ voltage-mode control to regulate their output voltage. Optimum compensation depends on whether the design uses continuous or discontinuous inductor current.

AUXA Boost, Discontinuous Inductor Current
When the inductor current falls to zero on each switching cycle, it is described as discontinuous. The inductor is not utilized as efficiently as with continuous current, but in light-load applications this often has little negative impact since the coil losses may already be low compared to other losses. A benefit of discontinuous inductor current is more flexible loop compensation, and no maximum duty-cycle restriction on boost ratio.
To ensure discontinuous operation, the inductor must have a sufficiently low inductance to fully discharge on each cycle. This occurs when:

$$L < [V_{IN}^2 (V_{OUT} - V_{IN}) / V_{OUT}^3] [R_{LOAD} / (2f_{OSC})]$$

A discontinuous current boost has a single pole at the following:

$$f_P = (2V_{OUT} - V_{IN}) / (2\pi \times R_{LOAD} \times C_{OUT} \times V_{OUT})$$

Choose the integrator cap so the unity-gain crossover, f_C, occurs at f_{OSC} / 10 or lower. Note that for many AUX circuits, such as those powering motors, LEDs, or other loads that do not require fast transient response, it is often acceptable to overcompensate by setting f_C at f_{OSC} / 20 or lower.
C_C is then determined by the following:

$$C_C = [2V_{OUT} \times V_{IN} / ((2V_{OUT} - V_{IN}) \times V_{RAMP})] [V_{OUT} / (K(V_{OUT} - V_{IN}))]^{1/2} [(V_{FB} / V_{OUT})(g_M / (2\pi \times f_C))]$$

where:

$$K = 2L \times f_{OSC} / R_{LOAD}$$

and V_{RAMP} is the internal slope-compensation voltage ramp of 1.25V.
The $C_C R_C$ zero is then used to cancel the f_P pole, so:

$$R_C = R_{LOAD} \times C_{OUT} \times V_{OUT} / [(2V_{OUT} - V_{IN}) \times C_C]$$

AUXA Boost, Continuous Inductor Current

Continuous inductor current can sometimes improve boost efficiency by lowering the ratio between peak inductor current and output current. It does this at the expense of a larger inductance value that requires larger size for a given current rating. With continuous inductor current boost operation, there is a right-half-plane zero, Z_{RHP}, at the following:

$$Z_{RHP} = (1 - D)^2 \times R_{LOAD} / (2\pi \times L)$$

where $(1 - D) = V_{IN} / V_{OUT}$ (in a boost converter).
There is a complex pole pair at the following:

$$f_0 = V_{OUT} / [2\pi \times V_{IN} (L \times C_{OUT})^{1/2}]$$

If the zero due to the output capacitance and ESR is less than 1/10 the right-half-plane zero:

$$Z_{COUT} = 1 / (2\pi \times C_{OUT} \times R_{ESR}) < Z_{RHP} / 10$$

Then choose C_C so the crossover frequency f_C occurs at Z_{COUT}. The ESR zero provides a phase boost at crossover:

$$C_C = (V_{IN} / V_{RAMP}) (V_{FB} / V_{OUT}) [g_M / (2\pi \times Z_{COUT})]$$

Choose R_C to place the integrator zero, $1 / (2\pi \times R_C \times C_C)$, at f_0 to cancel one of the pole pairs:

$$R_C = V_{IN}(L \times C_{OUT})^{1/2} / (V_{OUT} \times C_C)$$

If Z_{COUT} is not less than Z_{RHP} / 10 (as is typical with ceramic output capacitors) and continuous conduction is required, then cross the loop over before Z_{RHP} and f_0:

$$f_C < f_0 / 10, \text{ and } f_C < Z_{RHP} / 10$$

In that case:

$$C_C = (V_{IN} / V_{RAMP}) (V_{FB} / V_{OUT}) (g_M / (2\pi \times f_C))$$

Place:

$1 / (2\pi \times R_C \times C_C) = 1 / (2\pi \times R_{LOAD} \times C_{OUT})$, so that

$$R_C = R_{LOAD} \times C_{OUT} / C_C$$

Or, reduce the inductor value for discontinuous operation.

APPLICATION INFORMATION

Typical Operating Circuits

Figure 1, 2 and 3 show connections for AA and Li+ battery arrangements. Figures 5-8 show various connections for the AUXA and AUXB controllers. Figures 9 and 11 show various connections for the $\overline{SDOK}$ and SCF outputs.

Figure 1. Typical Operating Circuit for One Li+ Cell

In this connection, the main converter is operated as a buck (SUSD = GND) and is powered from PVSU. This provides boost-buck operation for the main 3.3V output, So a regulated output is maintained over the Li+ 2.8V to 4.2V cell voltage range. The compound efficiency from the battery to the 3.3V output reaches 90%.

The buck 1.8V (core) output is powered directly from V_{BATT}.

The AUXA controller generates a regulated current for a series network of four white LEDs that backlight the LCD.

Figure 2. Typical Operating Circuit for 2 AA Cells

Figure 2 is optimized for 2-cell AA inputs (1.5V to 3.4V) by connecting the buck input (PVSD) to the main output (PVM). The main 3.3V output operates directly from the battery as a boost (SUSD = PVSU). The 1.8V core output now operates as a boost-buck with efficiency up to 90%. The rest of the circuit is unchanged from Figure 1.

Figure 3. Typical Operating Circuit for 2 AA Cells and 1-Cell Li+

The SGM2101 can also allow either 1-cell Li+ or 2 AA cells to power the same design. If the buck and main inputs are both connected to PVSU, then both the 3.3V and 1.8V outputs operate as buck-boost converters. There is an efficiency penalty compared to stepping down VSD directly from the battery, but that is not possible with a 1.5V input. Furthermore, the cascaded boost-buck efficiency compares favorably with other boost-buck techniques.

LED Backlight, LCD Bias and Other Boost Applications

Any AUX channel can be used for a wide variety of boost applications. These include generating 5V or some other voltage for motor or actuator drive, generating 15V or a similar voltage for LCD bias, or generating a boost current source to efficiently drive a series array of white LEDs for LCD panel backlight. Figures 5 and 6 show examples of these applications.

SEPIC Buck-Boost

The SGM2101s' internal switch boost, main, and buck converters can be cascaded to make a high-efficiency boost-buck converter, but it is sometimes desirable to build a second boost-buck converter with an AUX_ controller.

One type of boost/buck converter is the SEPIC, shown in Figure 7. Inductors L1 and L2 can be separate inductors or can be wound on a single core and coupled like a transformer. Typically, a coupled inductor improves efficiency since some power is transferred through the coupling so less power passes through the coupling capacitor (C2). Likewise, C2 should have low ESR to improve efficiency. The ripple-current rating must be greater than the larger of the input and output currents. The MOSFET (Q1) drain-source voltage rating and the rectifier (D1) reverse-voltage rating must exceed the sum of the input and output voltages. Other types of boost/buck circuits are a flyback converter and a boost converter followed by a linear regulator.

Applications for Status Outputs

The SGM2101 has three status outputs: $\overline{SDOK}$, $\overline{AUXBOK}$ and SCF. These monitor the output of the buck channel, the AUXB channel, and the status of the overload-short-circuit protection. Each output is open drain to allow the greatest flexibility. Figures 9 and 11 show some possible connections for these outputs.

Using $\overline{SDOK}$ for Power Sequencing

$\overline{SDOK}$ goes low when the buck reaches regulation. Some microcontrollers with low-voltage cores require that the high-voltage (3.3V) I/O rail not be powered up until the core has a valid supply. The circuit in Figure 9 accomplishes this by driving the gate of a PFET connected between the 3.3V output and the processor I/O supply.

Using SCF for Full-Load Startup

The SCF output goes low only after the boost reaches regulation. It can be used to drive a P-channel MOSFET switch that turns off the load of a selected supply in the event of an overload. Or, it can remove the load until the supply reaches regulation, effectively allowing fullload start-up. Figure 11 shows such a connection for the boost output.

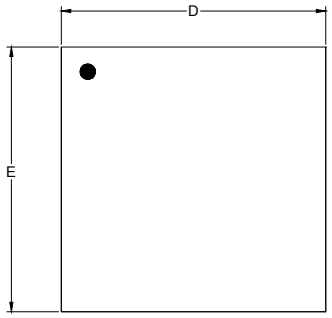
Designing a PC Board

Good PC board layout is important to achieve optimal performance from the SGM2101. Poor design can cause excessive conducted and/or radiated noise. Conductors carrying discontinuous currents and any high-current path should be made as short and wide as possible. A separate low-noise ground plane containing the reference and signal grounds should connect to the power-ground plane at only one point to minimize the effects of power-ground currents. Typically, the ground planes are best joined right at the IC.

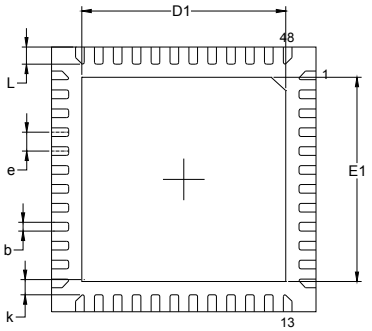
Keep the voltage-feedback network very close to the IC, preferably within 0.2in (5mm) of the FB_ pin. Nodes with high dV/dt (switching nodes) should be kept as small as possible and should be routed away from high-impedance nodes such as FB_. Refer to the SGM2101 EV kit data sheet for a full PC board example.

PACKAGE OUTLINE DIMENSIONS

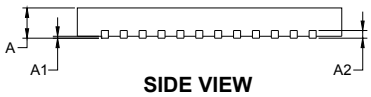
TQFN-7×7-48L



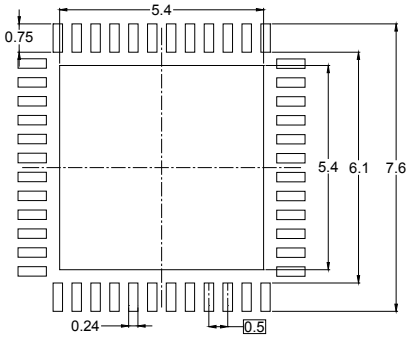
TOP VIEW



BOTTOM VIEW



SIDE VIEW

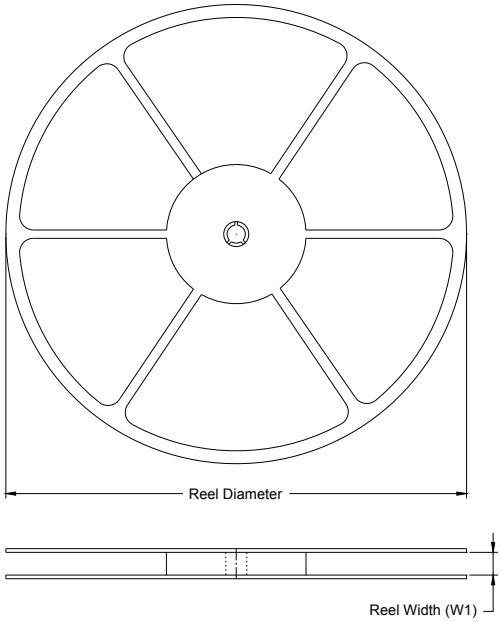


RECOMMENDED LAND PATTERN (Unit: mm)

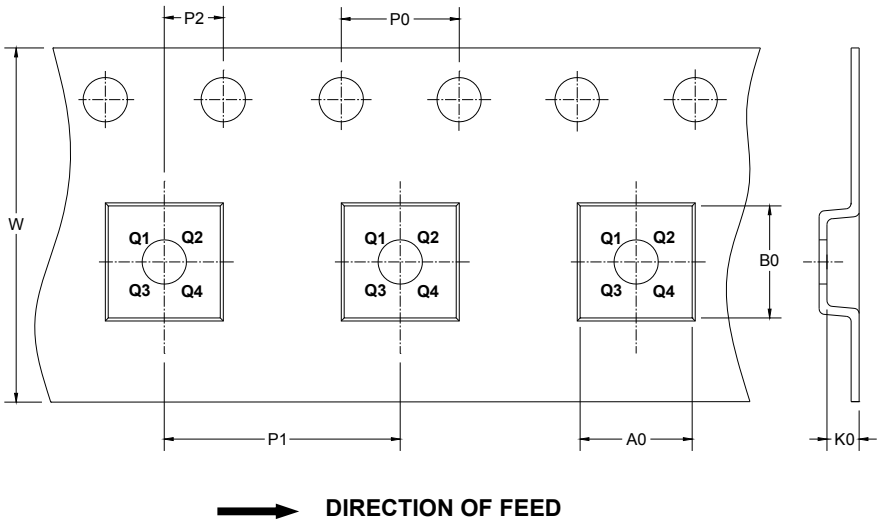
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	6.900	7.100	0.272	0.280
D1	5.300	5.500	0.209	0.217
E	6.900	7.100	0.272	0.280
E1	5.300	5.500	0.209	0.217
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.350	0.550	0.014	0.022

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

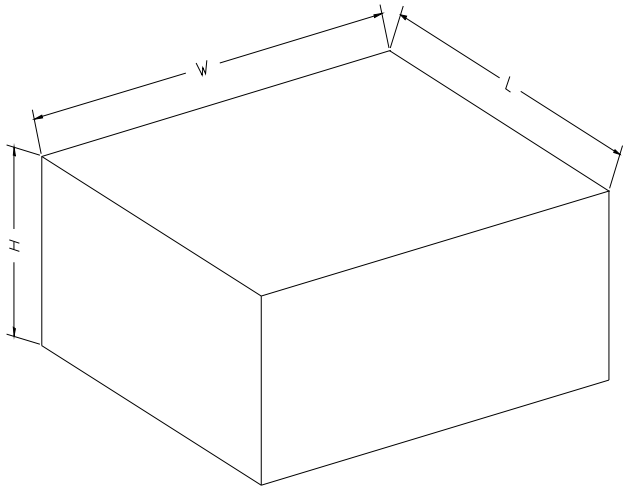


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-7×7-48L	13″	16.4	7.3	7.3	1.2	4.0	12.0	2.0	16.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

REVISION HISTORY

VERSION	DATE	PAGE	LOCATION	REMARK
SGM2101 REV.A.1_20130218	20130218	30	Recommended Land Pattern	Added
		31, 32	TAPE AND REEL INFORMATION	Added