

GENERAL DESCRIPTION

The SGM41296 is an I²C programmable monolithic driver with integrated power MOSFETs for thermoelectric cooling devices (TEC). It can deliver 1.5A to the TEC continuously, from a 2.7V to 5.5V source over the TEC operating voltage range. The TEC voltage is linearly controlled by an analog input voltage (CTL).

The voltage and current limits for protecting the TEC and the device can be adjusted, activated or deactivated on the fly by the 1Mbps I²C serial interface. A full suite of protection features such as over-current, over-voltage and over-temperature, and an internal 2 stage soft-start circuit are also provided by this device.

Requiring a minimal number of external components and with a tiny TQFN package, the SGM41296 offers the minimum solution size for TEC applications. It is an ideal choice for applications such as optical laser diode and fiber communication networks.

FEATURES

- Wide 2.7V to 5.5V Input Voltage Range
- Up to 1.5A Output Current for TEC
- TEC Voltage and Current Monitoring
- 2.5V Reference Output with 1% Accuracy
- Fixed 1MHz Switching Frequency for the Buck
- I²C Programmable Soft-Start Time
- TEC Voltage/Current Limits for Heating/Cooling
- LDO/Buck Current Limits for Heating/Cooling
- Input Over-Voltage and UVLO Protection
- Hiccup Mode Protection
- Die Temperature Warning
- Die Over-Temperature Protection
- EN and SD Pins for Power Sequencing
- Available in a Green TQFN-2×3-16L Package

APPLICATIONS

- Optical Laser Diode Modules
- Fiber Communication Networks

TYPICAL APPLICATION

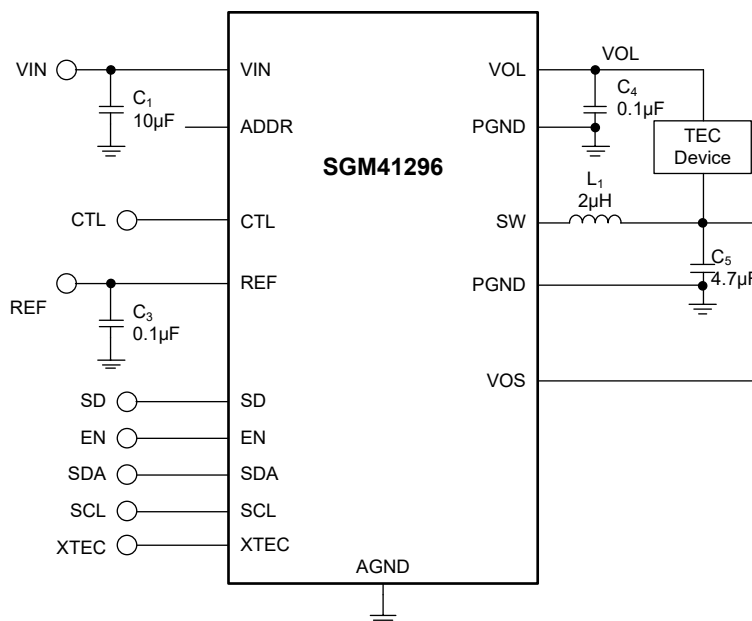


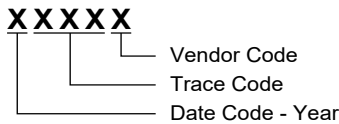
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|----------|---------------------|-----------------------------|----------------------|-----------------|---------------------|
| SGM41296 | TQFN-2x3-16L | -40°C to +125°C | SGM41296XTRJ16G/TR | 41296 XXXXXX | Tape and Reel, 3000 |
| SGM41296 | TQFN-2x3-16L | -40°C to +125°C | SGM41296XTRJ16G-K/TR | 41296 XXXXXX | Tape and Reel, 5000 |

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage..... -0.3V to 6V
- V_{SW}-0.3V (-2V for < 10ns) to 6V
- CTL, REF, EN, SD, VOS, XTEC, ADDR...-0.3V to V_{IN} + 0.3V
- AGND to PGND -0.3V to 0.3V
- All Other Pins..... -0.3V to 6V
- Package Thermal Resistance
 - TQFN-2x3-16L, θ_{JA}..... 62.6°C/W
 - TQFN-2x3-16L, θ_{JB}..... 9°C/W
 - TQFN-2x3-16L, θ_{JC}..... 31.8°C/W
- Junction Temperature.....+150°C
- Storage Temperature Range-65°C to +150°C
- Lead Temperature (Soldering, 10s).....+260°C
- ESD Susceptibility
 - HBM..... 4000V
 - CDM 1000V

RECOMMENDED OPERATING CONDITIONS

- Supply Voltage Range2.7V to 5.5V
- Operating Ambient Temperature Range-40°C to +125°C
- Operating Junction Temperature Range.....-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

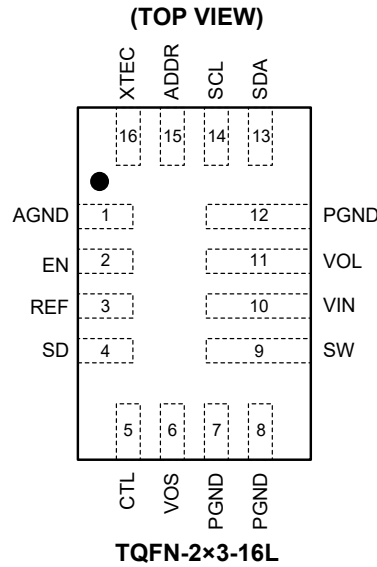
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

| PIN NUMBER | PIN NAME | TYPE ⁽¹⁾ | FUNCTION |
|------------|----------|---------------------|---|
| 1 | AGND | P | Analog ground. |
| 2 | EN | DI | The effective-high enable input, to enable the power stage starting with soft-start procedure. When pulling low, stop power stage and force both outputs into Hi-Z state. |
| 3 | REF | AO | 2.5V internal reference output. Decouple this pin with at least 0.1µF, X5R or better ceramic capacitor to AGND. |
| 4 | SD | DI | The effective-low power stage shutdown control input. Pull this pin low to shutdown both the switch regulator and linear regulator and force both outputs into Hi-Z floating state. When pulling high, start output with the soft-start procedure. |
| 5 | CTL | AI | Voltage control input. CTL voltage controls the TEC voltage (regulated between the VOS and VOL pins). |
| 6 | VOS | AI | Voltage sensing for the switch regulator. |
| 7, 8, 12 | PGND | P | Ground return path of internal power switches and linear regulator bypass MOSFETs. Place decouple/storage caps closely between those pins and the VIN pin. |
| 9 | SW | P | Chopper switch node, connect to one end of the power inductor. |
| 10 | VIN | P | Power input to all circuit inside the chip. Closely placed decouple caps between this pin and those PGND pins is highly recommended. |
| 11 | VOL | P | Linear regulator output, which sinks or sources to drive one end of the TEC device. |
| 13 | SDA | DIO | Data IO of the I ² C compatible serial interface. |
| 14 | SCL | DI | Clock IO of the I ² C compatible serial interface. |
| 15 | ADDR | DI | I ² C slave address programming. Pull ADDR pin down (< 50kΩ) or short it to GND to select 0x21 I ² C slave address. Leave it floating or connect it to a capacitor (< 150nF) to choose 0x60 address. Pin state detection for addressing is executed within 20ms after power-up UVLO releases. |
| 16 | XTEC | AO | TEC current or voltage monitor output. The output voltage is proportional to VOL current or the differential voltage across the VOL and VOS (selected by XTEC bit). |

NOTE:

1. P = Power, AI = Analog Input, AO = Analog Output, DI = Digital Input, DIO = Digital Input/Output.

ELECTRICAL CHARACTERISTICS

($V_{IN} = 3.3V$, $T_J = -40^\circ C$ to $+125^\circ C$, typical values tested at $T_J = +25^\circ C$, over-temperature limits are guaranteed by characterization, unless otherwise noted).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|----------------|---|---------------------------------------|-------|-------|------------|---|
| Input Voltage Range | V_{IN} | | 2.7 | | 5.5 | V | |
| Under-Voltage Lockout Threshold Rising | | | 2.5 | 2.6 | 2.66 | V | |
| Under-Voltage Lockout Threshold Hysteresis | | | | 60 | | mV | |
| Reference Voltage | V_{REF} | $2.7V \leq V_{IN} \leq 5.5V$, $I_{REF} = 10mA$ | $T_J = +25^\circ C$ | 2.485 | 2.5 | 2.515 | V |
| | | | $T_J = -40^\circ C$ to $+125^\circ C$ | 2.475 | 2.5 | 2.525 | |
| Shutdown Current | | $V_{EN} = 0V$, $V_{IN} = 5.5V$ | | 160 | 300 | μA | |
| Quiescent Current | | No switching, $V_{IN} = 5.5V$ | | 0.83 | 1.3 | mA | |
| Power MOSFETs | | | | | | | |
| VOL PFET Switch On-Resistance | R_{DSON_P1} | $V_{IN} = 5V$ | | 44 | 75 | m Ω | |
| | | $V_{IN} = 3.3V$ | | 58 | 95 | | |
| VOL NFET Switch On-Resistance | R_{DSON_N1} | $V_{IN} = 5V$ | | 27 | 55 | m Ω | |
| | | $V_{IN} = 3.3V$ | | 34 | 65 | | |
| Buck PFET Switch On-Resistance | R_{DSON_P2} | $V_{IN} = 5V$ | | 44 | 75 | m Ω | |
| | | $V_{IN} = 3.3V$ | | 58 | 95 | | |
| Buck NFET Switch On-Resistance | R_{DSON_N2} | $V_{IN} = 5V$ | | 27 | 55 | m Ω | |
| | | $V_{IN} = 3.3V$ | | 34 | 65 | | |
| VOL Pin Leakage | | $V_{EN} = 0V$, $V_{IN} = 6V$, $V_{VOL} = 0V$ | | 0.1 | 2 | μA | |
| | | $V_{EN} = 0V$, $V_{IN} = 6V$, $V_{VOL} = 6V$ | | 100 | 200 | | |
| Buck SW Pin Leakage | | $V_{EN} = 0V$, $V_{IN} = 5.5V$, $V_{SW} = 0V$ or $5.5V$ | | 0.1 | 5 | μA | |
| Maximum VOL PFET Source Current 1 st Limit Range | | Set by I^2C | 0.039 | | 2.028 | A | |
| Maximum VOL NFET Sink Current 1 st Limit Range | | Set by I^2C | 0.039 | | 2.028 | A | |
| Maximum VOL PFET Source Current 2 nd Limit Range | | Set by I^2C | 2 | | 3.5 | A | |
| Maximum VOL NFET Sink Current 2 nd Limit Range | | Set by I^2C | 2 | | 3.5 | A | |
| Maximum Buck PFET Source Current 2 nd Limit Range | | Set by I^2C | 2.5 | | 4 | A | |
| Maximum Buck NFET Sink Current 2 nd Limit Range | | Set by I^2C | 2.5 | | 4 | A | |
| Hiccup Cycle Time | | | | 15 | | ms | |
| TEC to CTL Voltage Gain | | | | 5 | | V/V | |
| Frequency Setting | | | | | | | |
| Buck Duty Cycle Range | | 1MHz switching frequency | 0 | | 100 | % | |
| Switching Frequency | f_{SW} | | 990 | 1120 | 1250 | kHz | |
| EN Input Logic Low Voltage | V_{ENL} | | | | 0.4 | V | |
| EN Input Logic High Voltage | V_{ENH} | | 1.2 | | | V | |
| EN Input Current | I_{EN} | $V_{EN} = 5.5V$ | | 0.36 | 1.5 | μA | |
| | | $V_{EN} = 0V$ | | 0.01 | 1 | μA | |
| SD Input Logic Low Voltage | V_{SD_ENL} | | | | 0.4 | V | |
| SD Input Logic High Voltage | V_{SD_ENH} | | 1.2 | | | V | |
| SD Pull-Down Resistor | | | | 1.3 | | M Ω | |
| SD Turn-On Delay | | Turn-on IC | | 30 | | ms | |

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 3.3V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, typical values tested at $T_J = +25^{\circ}C$, over-temperature limits are guaranteed by characterization, unless otherwise noted).

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------------|---|---------------------|------|------|-------------|
| TEC Current Measurement (XTEC Outputs ITEC) | | | | | | |
| ITEC Initial (Offset Bias) Voltage | | $I_{VOL} = 0A$, XTEC bit = 1 | 1.23 | 1.25 | 1.27 | V |
| ITEC Current Gain | | 1.5A TEC current | | 0.5 | | V/A |
| ITEC Current Monitor Accuracy | | I_{VOL} sink (or source) > 500mA | -6.4 | | 6.4 | % |
| ITEC Current Limit Setting Accuracy | | I_{VOL} sink (or source) > 700mA | -20 | | 20 | % |
| XTEC Output Resistance | | | | 80 | | Ω |
| TEC Voltage Measurement (XTEC Outputs VTEC) | | | | | | |
| Voltage Sense Gain | | | 0.19 | 0.2 | 0.21 | V/V |
| Voltage Measurement (XTEC Outputs VTEC) | $V_{VTEC_AT_1.0_V}$ | $V_{VOL} - V_{VOS} = 1.0V$ | 1.43 | 1.45 | 1.47 | V |
| VTEC Initial (Offset Bias) Voltage | | $V_{VOL} = V_{VOS}$ | 1.23 | 1.25 | 1.27 | V |
| VTEC Voltage Limit Accuracy | | VTEC voltage limit > 700mV | -16 | | 16 | % |
| Heating Mode Threshold | | Condition for set MODE[1:0] /REG09[7:6] | | 30 | | mV |
| Cooling Mode Threshold | | | $V_{VOL} - V_{VOS}$ | | 30 | |
| LDO Analog Output (VOL) | | | | | | |
| Discharge Period before Startup | | DIS_TIME | | 18 | | ms |
| Discharge Resistance | | | | 500 | | Ω |
| I²C | | | | | | |
| SCL, SDA Input Logic High Voltage | | | 1.2 | | | V |
| SCL, SDA Input Logic Low Voltage | | | | | 0.4 | V |
| Output Low Voltage | V_{OL} | $I_{SINK} = 200\mu A$ | | | 0.4 | V |
| Internal ADDR Pull-Up Resistor | | | | 260 | | k Ω |
| I ² C Clock Frequency | | | | 1 | | MHz |
| Protection | | | | | | |
| Thermal Shutdown ⁽¹⁾ | | | | 165 | | $^{\circ}C$ |
| Thermal Hysteresis ⁽¹⁾ | | | | 20 | | $^{\circ}C$ |
| Temperature Warning Threshold ⁽¹⁾ | t_{OTW} | | | 125 | | $^{\circ}C$ |
| OTW Hysteresis ⁽¹⁾ | t_{OTW_H} | | | 20 | | $^{\circ}C$ |
| Input Over-Voltage Threshold | | I ² C enable | 5.6 | 5.75 | 5.9 | V |
| Input Over-Voltage Hysteresis | | I ² C enable | | 0.25 | | V |
| VTEC Over-Voltage Threshold ⁽²⁾ | | $ V_{VOL} - V_{VOS} $, excessive over the programmed threshold | | 1 | | V |
| External Component Selections ⁽³⁾ | | | | | | |
| Recommended Input Capacitance | | | 10 | 22 | | μF |
| Recommended Inductance | | | 1 | 2.2 | 3.3 | μH |
| VOS Recommended Output Capacitance | | | 4.7 | | | μF |
| VOL Recommended Output Capacitance | | | 0.1 | 1 | 2 | μF |

NOTES:

1. Guaranteed by production characterization.
2. Guaranteed by design and verified with bench test.
3. Guaranteed by design and production characterization, verified with bench test.

I²C INTERFACE TIMING CHARACTERISTICS ⁽¹⁾

| PARAMETER | SYMBOL | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS |
|---|---------------------|----------------|-------|------------------------|-----|------|-------|
| SCL Clock Frequency | f _{SCL} | Standard mode | +25°C | | | 100 | kHz |
| | | Fast mode | +25°C | | | 400 | kHz |
| | | Fast mode plus | +25°C | | | 1 | MHz |
| LOW Period of the SCL Clock | t _{LOW} | Standard mode | +25°C | 4.7 | | | μs |
| | | Fast mode | +25°C | 1.3 | | | μs |
| | | Fast mode plus | +25°C | 0.5 | | | μs |
| HIGH Period of the SCL Clock | t _{HIGH} | Standard mode | +25°C | 4.0 | | | μs |
| | | Fast mode | +25°C | 600 | | | ns |
| | | Fast mode plus | +25°C | 260 | | | ns |
| Bus Free Time between a STOP and a START Conditions | t _{BUF} | Standard mode | +25°C | 4.7 | | | μs |
| | | Fast mode | +25°C | 1.3 | | | μs |
| | | Fast mode plus | +25°C | 0.5 | | | μs |
| Hold Time for a Repeated START Condition | t _{hd,STA} | Standard mode | +25°C | 4.0 | | | μs |
| | | Fast mode | +25°C | 600 | | | ns |
| | | Fast mode plus | +25°C | 260 | | | ns |
| Setup Time for a Repeated START Condition | t _{su,STA} | Standard mode | +25°C | 4.7 | | | μs |
| | | Fast mode | +25°C | 600 | | | ns |
| | | Fast mode plus | +25°C | 260 | | | ns |
| Data Setup Time | t _{su,DAT} | Standard mode | +25°C | 250 | | | ns |
| | | Fast mode | +25°C | 100 | | | ns |
| | | Fast mode plus | +25°C | 50 | | | ns |
| Data Hold Time | t _{hd,DAT} | Standard mode | +25°C | 0.05 | | 3.45 | μs |
| | | Fast mode | +25°C | 0.05 | | 0.9 | μs |
| | | Fast mode plus | +25°C | 0 | | | μs |
| Rise Time of SCL Signal after a Repeated START Condition and after an Acknowledge Bit | t _{rCL1} | Standard mode | +25°C | 20 + 0.1C _B | | 1000 | ns |
| | | Fast mode | +25°C | 20 + 0.1C _B | | 1000 | ns |
| | | Fast mode plus | +25°C | | | 120 | ns |
| Rise Time of SCL Signal | t _{rCL} | Standard mode | +25°C | 20 + 0.1C _B | | 1000 | ns |
| | | Fast mode | +25°C | 20 + 0.1C _B | | 300 | ns |
| | | Fast mode plus | +25°C | | | 120 | ns |
| Fall Time of SCL Signal | t _{fCL} | Standard mode | +25°C | 20 + 0.1C _B | | 300 | ns |
| | | Fast mode | +25°C | 20 + 0.1C _B | | 300 | ns |
| | | Fast mode plus | +25°C | | | 120 | ns |
| Rise Time of SDA Signal | t _{rDA} | Standard mode | +25°C | 20 + 0.1C _B | | 1000 | ns |
| | | Fast mode | +25°C | 20 + 0.1C _B | | 300 | ns |
| | | Fast mode plus | +25°C | | | 120 | ns |
| Fall Time of SDA Signal | t _{fDA} | Standard mode | +25°C | 20 + 0.1C _B | | 300 | ns |
| | | Fast mode | +25°C | 20 + 0.1C _B | | 300 | ns |
| | | Fast mode plus | +25°C | | | 120 | ns |

I²C INTERFACE TIMING CHARACTERISTICS ⁽¹⁾ (continued)

| PARAMETER | SYMBOL | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS |
|---------------------------------|---------------------|----------------|-------|-----|-----|-----|-------|
| Setup Time for STOP Condition | t _{su,STO} | Standard mode | +25°C | 4.0 | | | µs |
| | | Fast mode | +25°C | 600 | | | ns |
| | | Fast mode plus | +25°C | 260 | | | ns |
| Capacitive Load for SDA and SCL | C _B | | +25°C | | | 0.4 | nF |

NOTE:

1. Industry standard I²C timing characteristics according to I²C-Bus Specification. Not tested in production.

I²C INTERFACE TIMING DIAGRAM

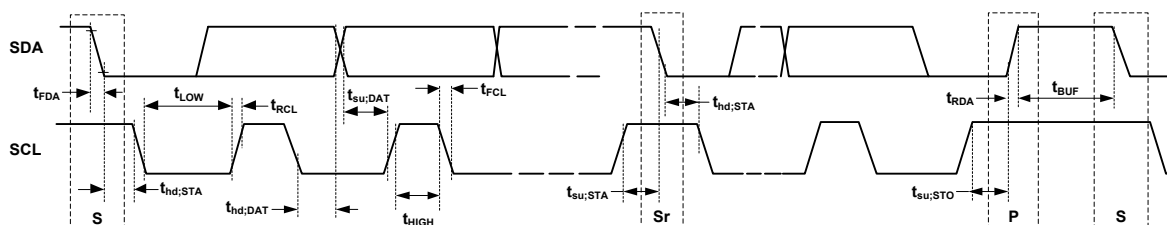
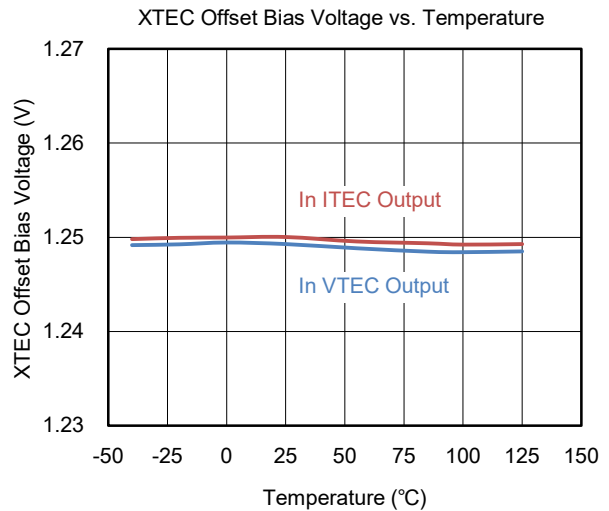
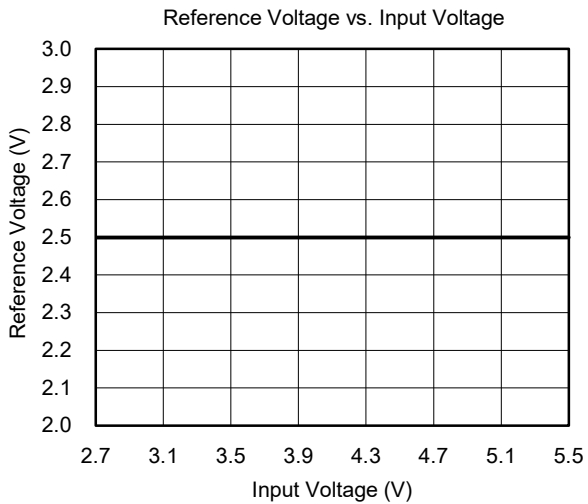
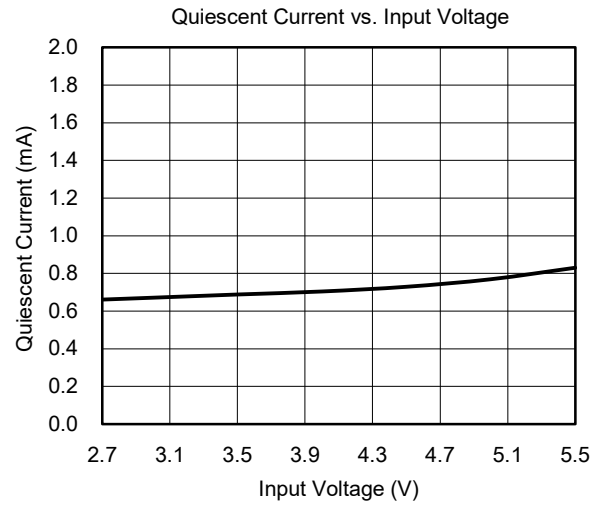
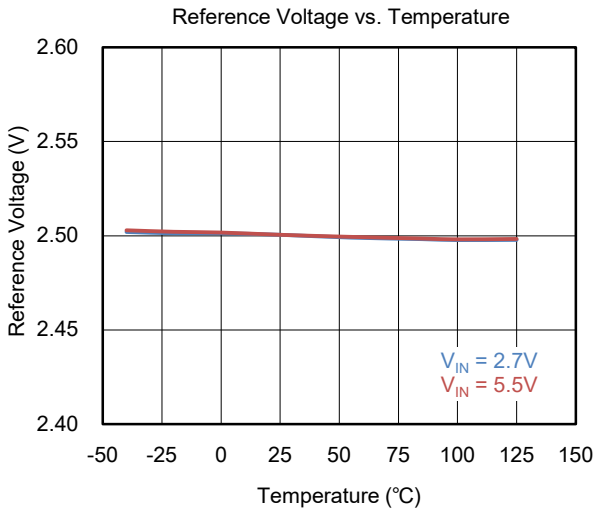
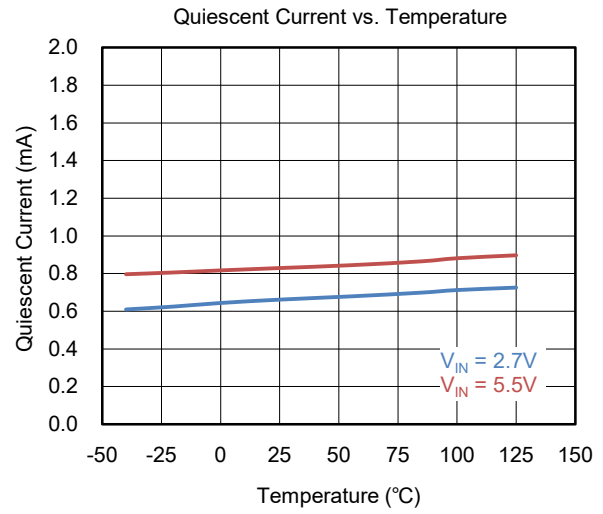
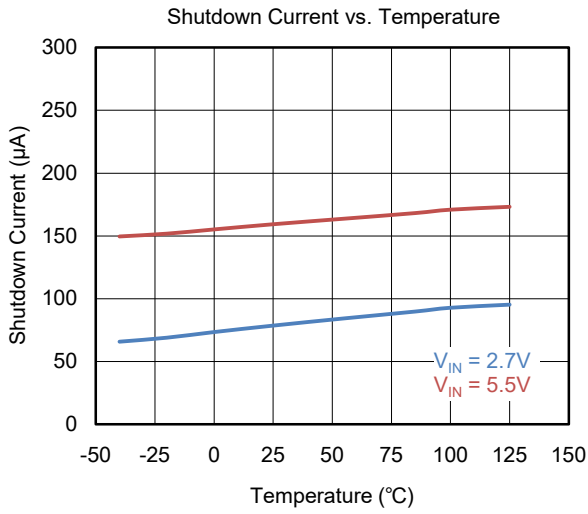


Figure 2. Serial Interface Timing for F/S-Mode

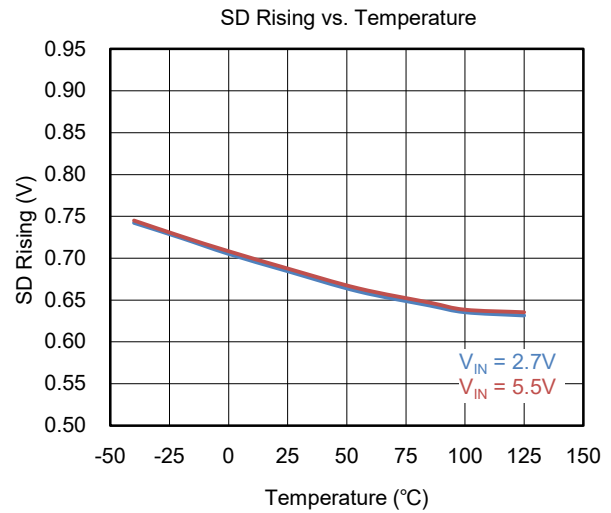
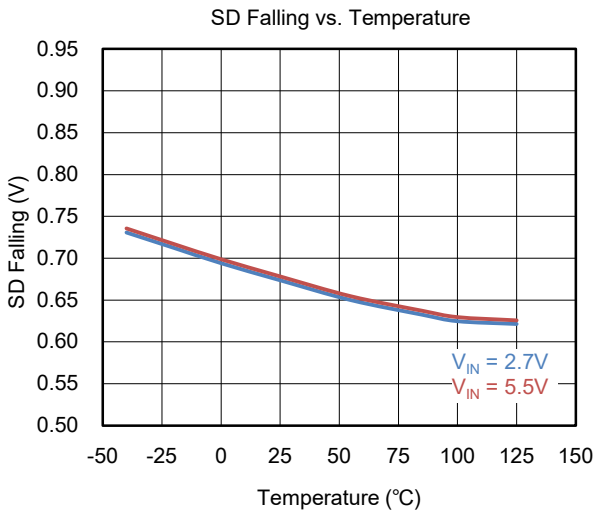
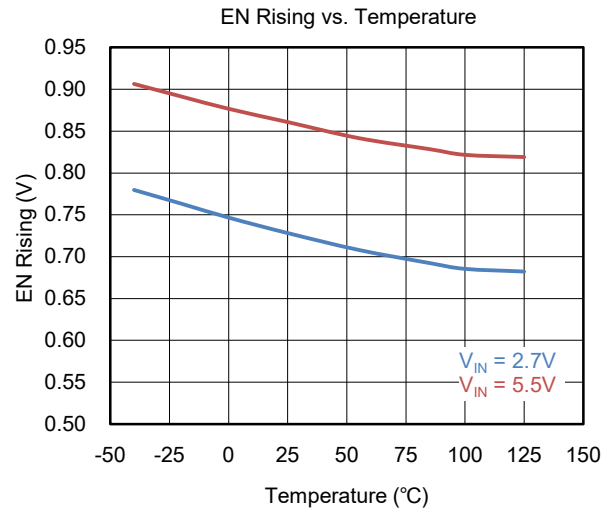
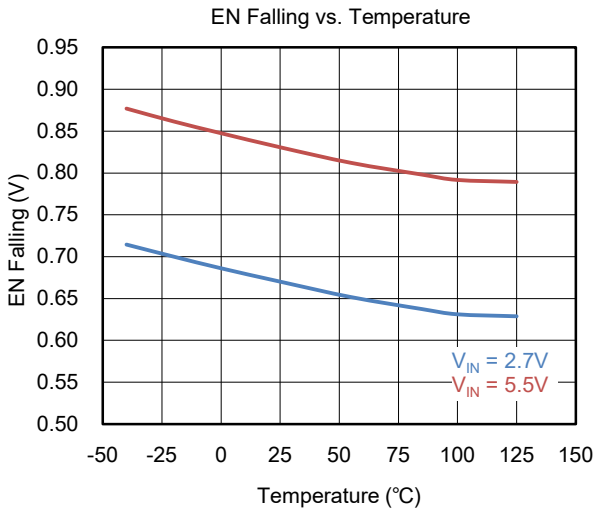
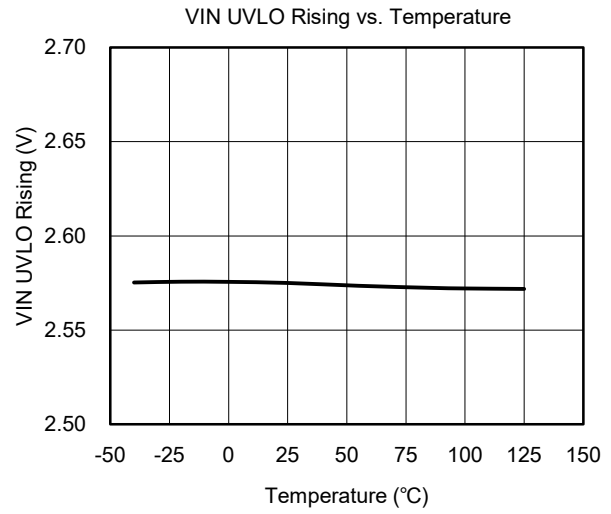
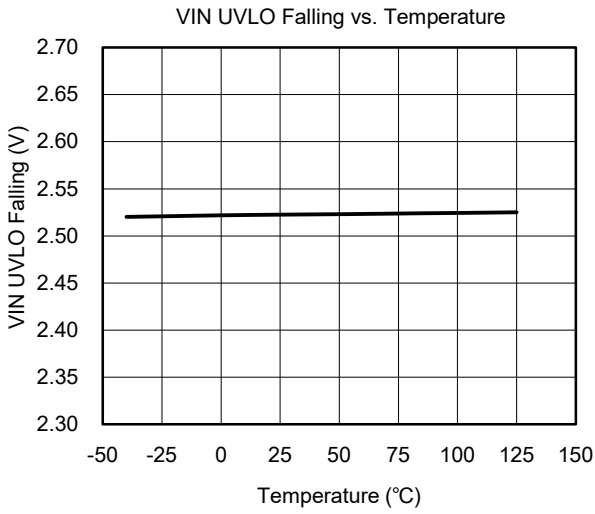
TYPICAL PERFORMANCE CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $L = 2\mu\text{H}$ and $C_{OUT} = 4.7\mu\text{F}$, unless otherwise noted.



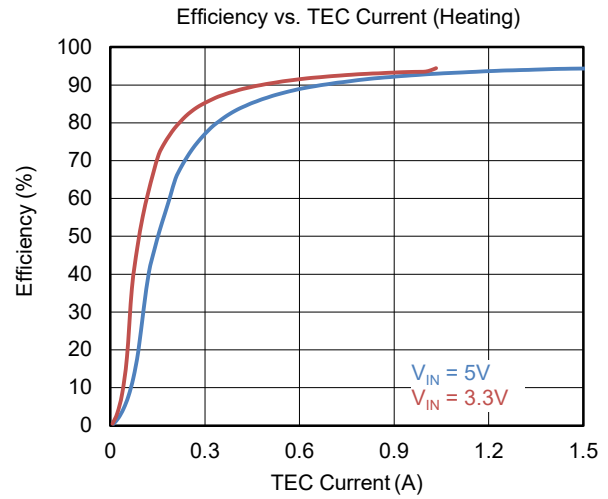
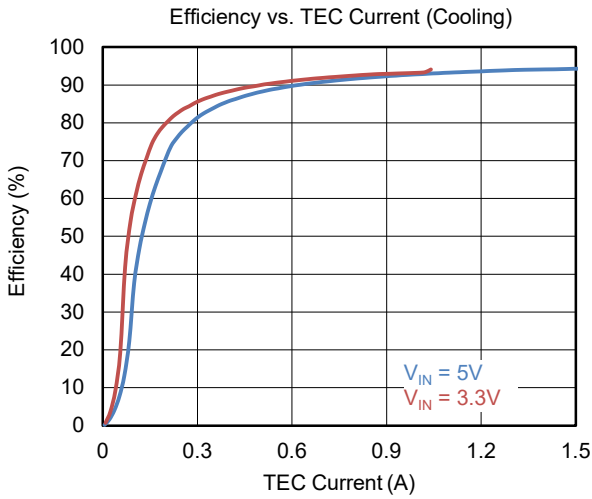
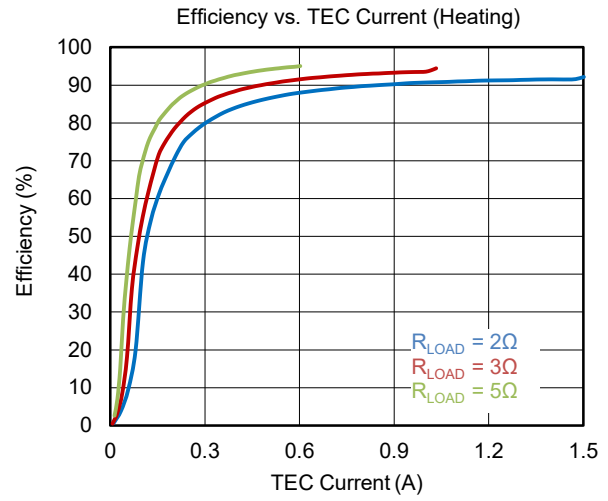
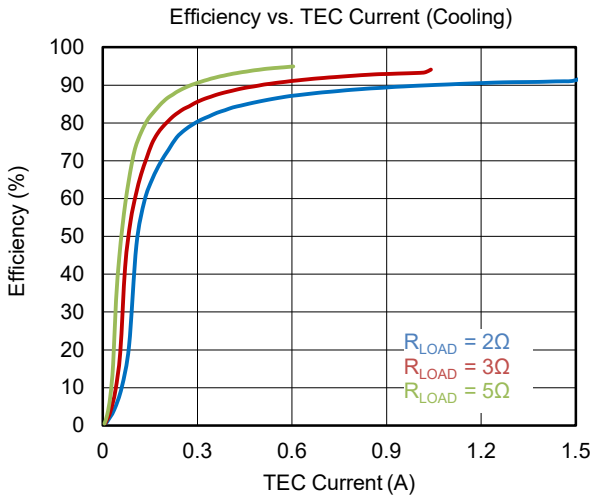
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $L = 2\mu\text{H}$ and $C_{OUT} = 4.7\mu\text{F}$, unless otherwise noted.



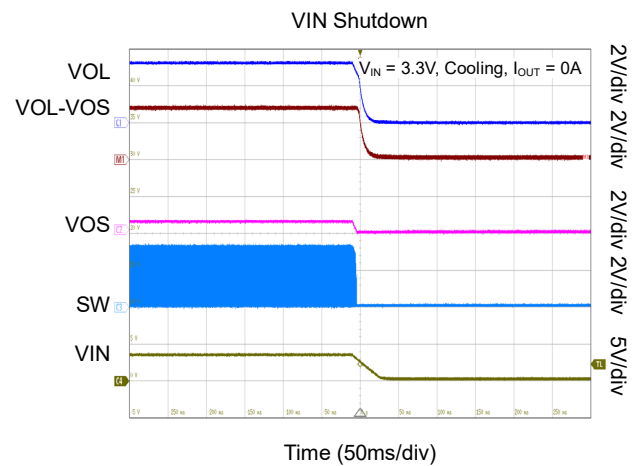
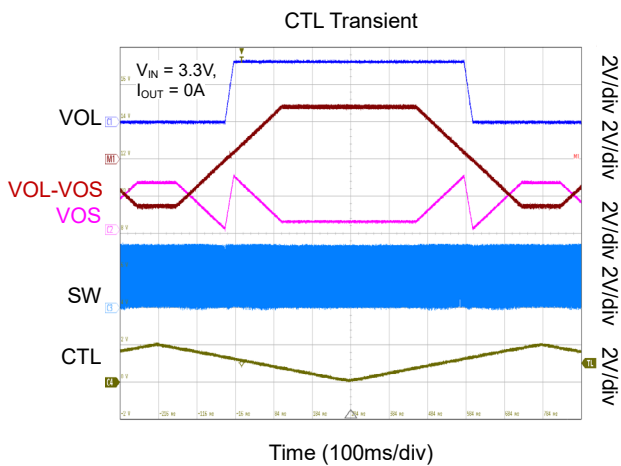
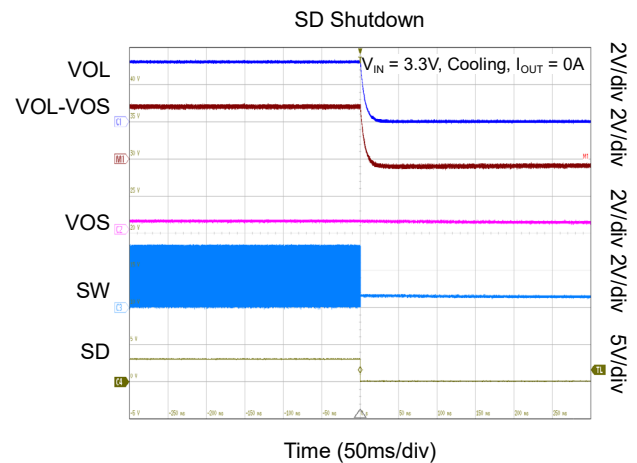
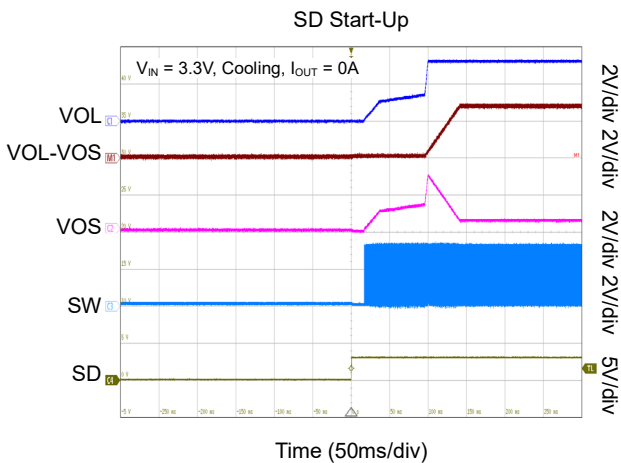
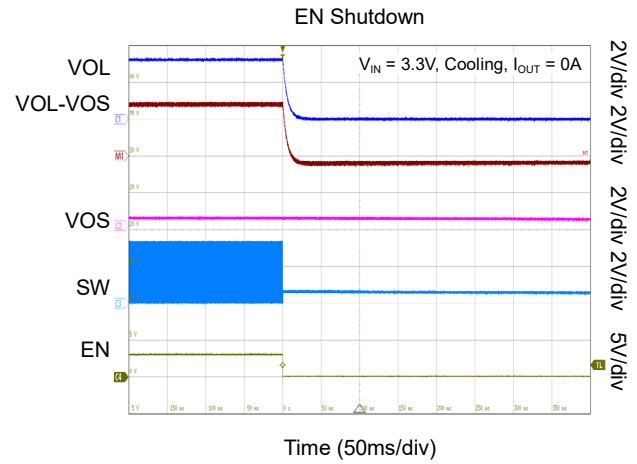
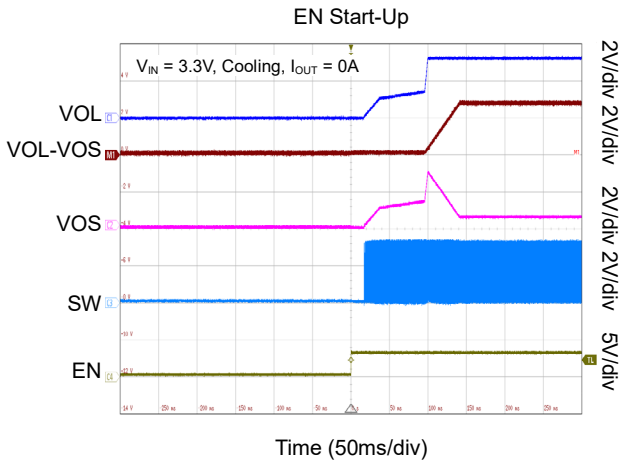
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $L = 2\mu\text{H}$ and $C_{OUT} = 4.7\mu\text{F}$, unless otherwise noted.



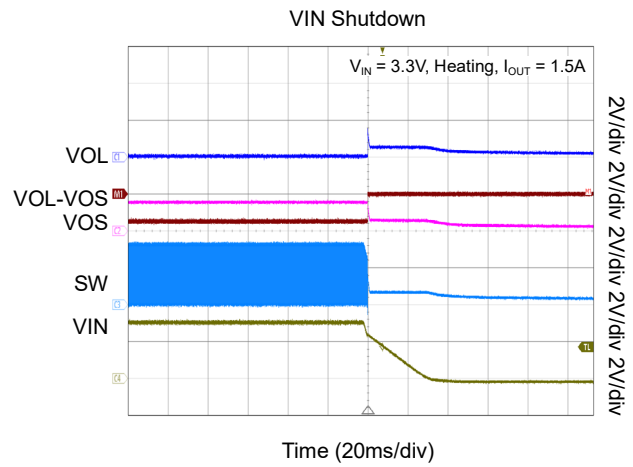
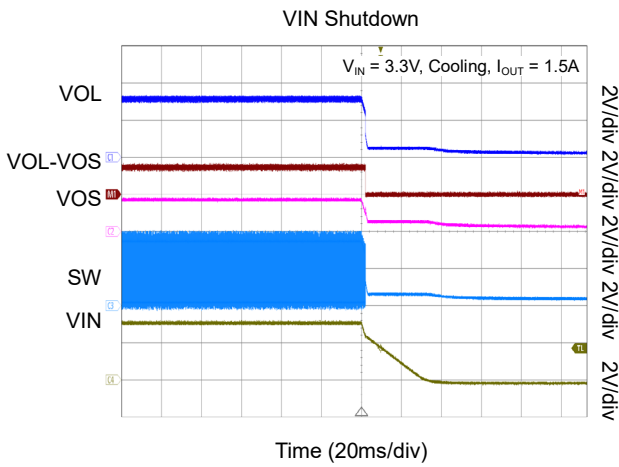
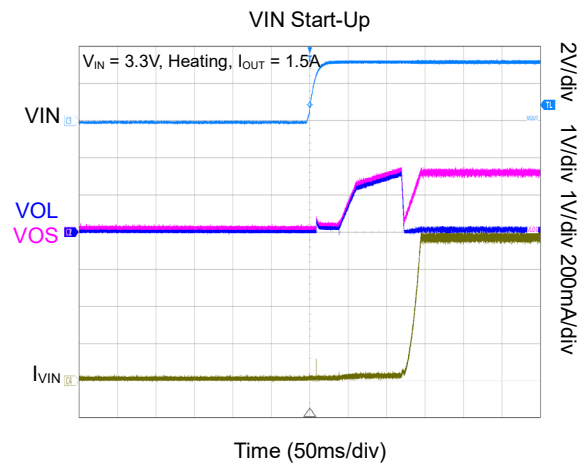
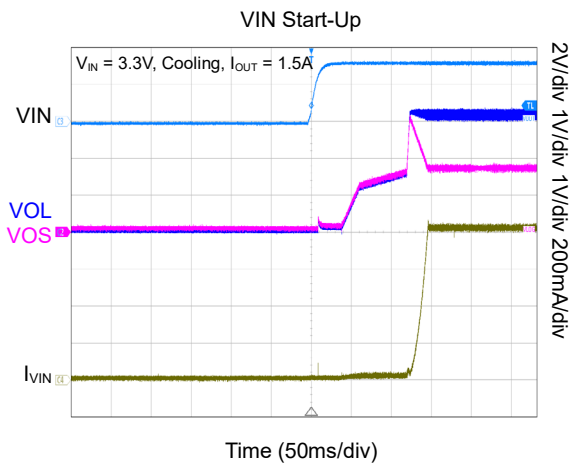
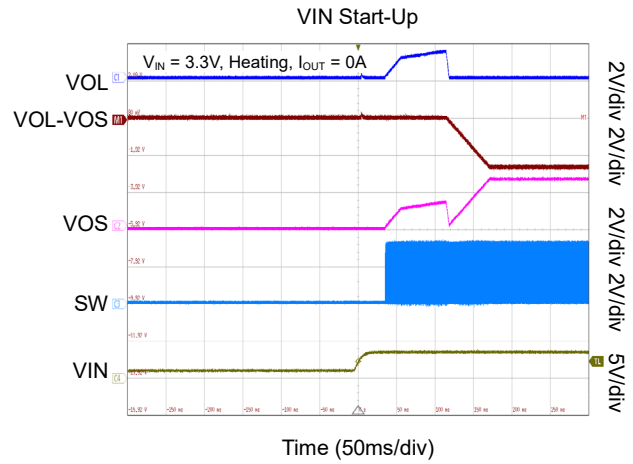
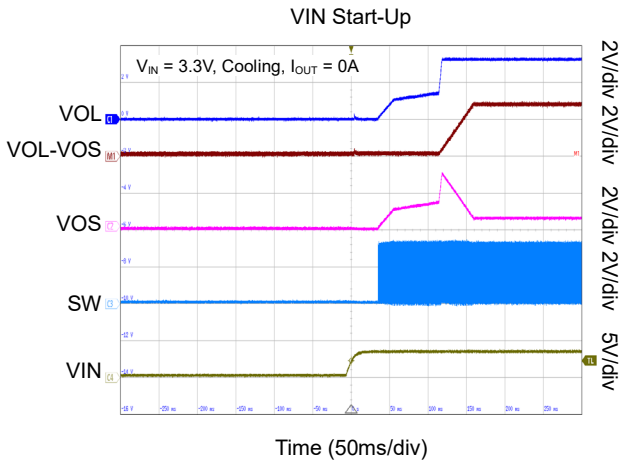
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $L = 2\mu\text{H}$ and $C_{OUT} = 4.7\mu\text{F}$, unless otherwise noted.



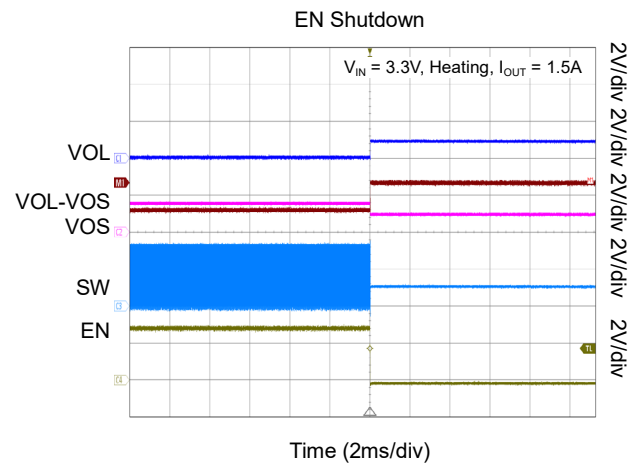
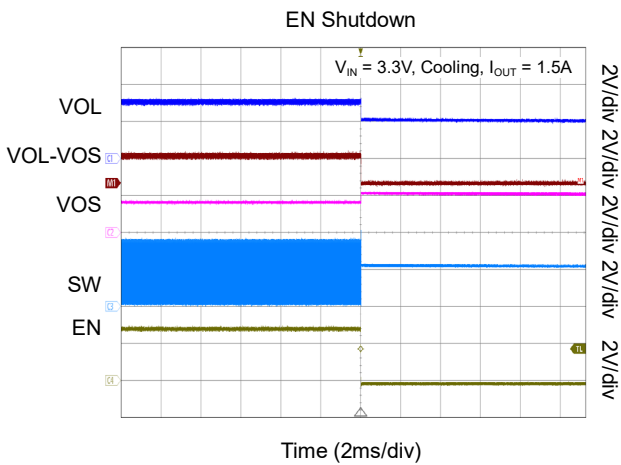
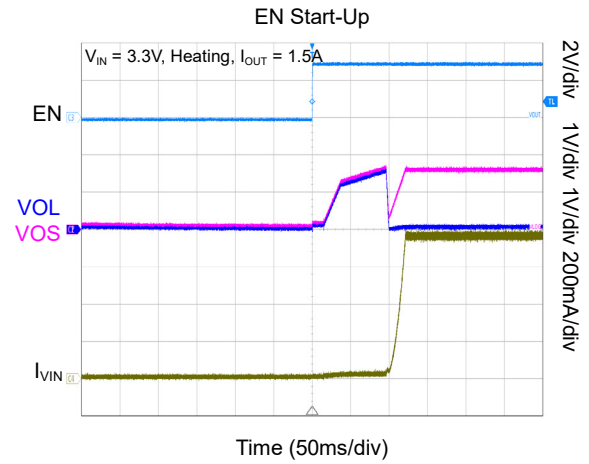
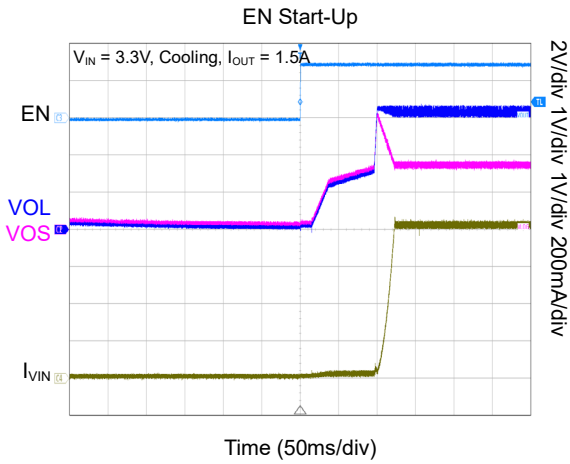
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $L = 2\mu\text{H}$ and $C_{OUT} = 4.7\mu\text{F}$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{IN} = 3.3\text{V}$, $L = 2\mu\text{H}$ and $C_{OUT} = 4.7\mu\text{F}$, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

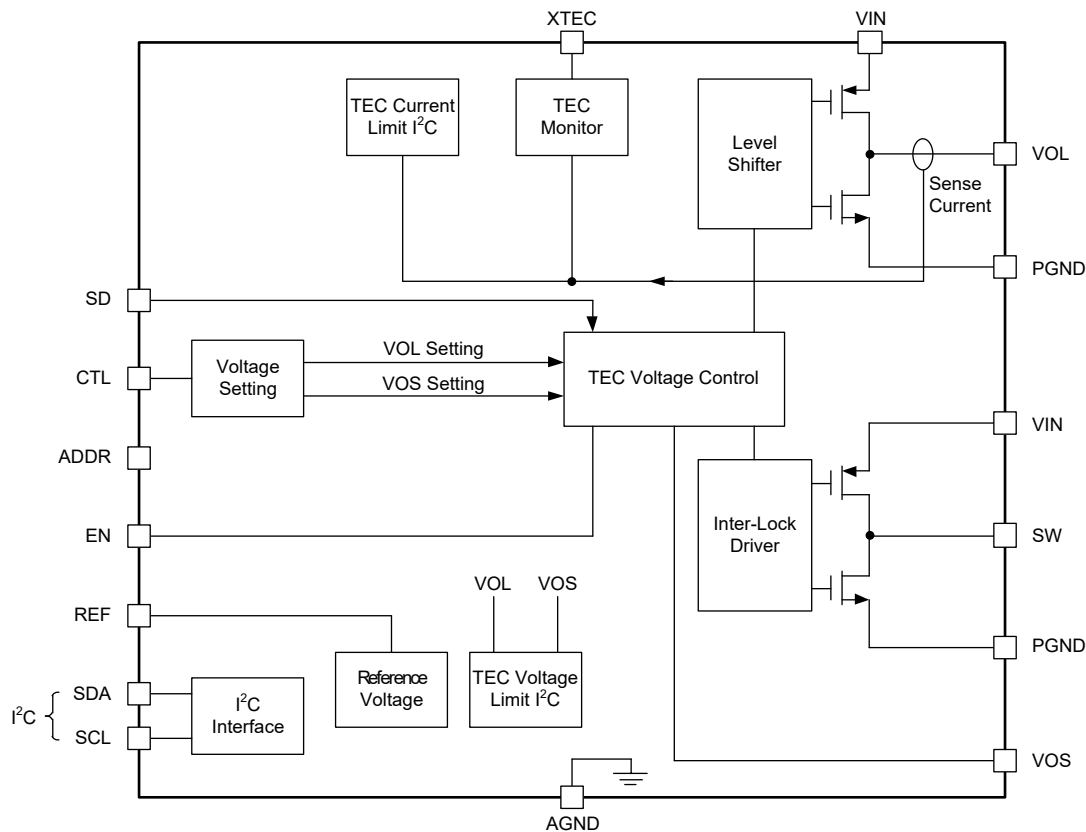


Figure 3. Block Diagram

REGISTER MAPS

Table 1. Register Map

| ADD | NAME | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|-----|-----------|-----|--------------------|----------|--------------------|---------------------|---------------------|--------------|---------|---------------------|--|
| 00 | SYS_SET | R/W | XTEC | RESERVED | | RESERVED | | SS_TIME[1:0] | REFRESH | I ² C_ON | |
| 01 | ILIM_HEAT | R/W | ENILIM_HEAT | RESERVED | ILIM_HEAT_SET[5:0] | | | | | | |
| 02 | ILIM_COOL | R/W | ENILIM_COOL | RESERVED | ILIM_COOL_SET[5:0] | | | | | | |
| 03 | VLIM_HEAT | R/W | ENVLIM_HEAT | VIN OVP | VLIM_HEAT_SET[5:0] | | | | | | |
| 04 | VLIM_COOL | R/W | ENVLIM_COOL | RESERVED | VLIM_COOL_SET[5:0] | | | | | | |
| 05 | ILIM | R/W | LDO_ILIM_HEAT[1:0] | | LDO_ILIM_COOL[1:0] | BUCK_ILIM_HEAT[1:0] | BUCK_ILIM_COOL[1:0] | | | | |
| 06 | ADDR | R | SLAVE_ADDRESS[6:0] | | | | | | | RESERVED | |
| 07 | RESERVED | R | RESERVED | | | | | | | | |
| 08 | RESERVED | R | RESERVED | | | | | | | | |
| 09 | STATUS | R | MODE[1:0] | | VLIM | ILIM | PWOR | RESERVED | OT | OTW | |
| 0A | ID | R | VENDOR_ID[3:0] | | | | VERSION_ID[3:0] | | | | |

Table 2. Register Default Values

| ADD | NAME | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----------|-----|----|----|----|----|----|----|----|----|
| 00 | SYS_SET | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01 | ILIM_HEAT | R/W | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 02 | ILIM_COOL | R/W | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 03 | VLIM_HEAT | R/W | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 04 | VLIM_COOL | R/W | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 05 | ILIM | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06 | RESERVED | R | NA | NA | NA | NA | NA | NA | NA | NA |
| 07 | RESERVED | R | NA | NA | NA | NA | NA | NA | NA | NA |
| 08 | RESERVED | R | NA | NA | NA | NA | NA | NA | NA | NA |
| 09 | STATUS | R | NA | NA | NA | NA | NA | NA | NA | NA |
| 0A | ID | R | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

ILIM TABLE

Table 3. I_{LIM} Selection Table (D[5:0] in REG01 and REG02), Default = 1482mA

| D[5:0] | I _{LIM} (mA) | D[5:0] | I _{LIM} (mA) | D[5:0] | I _{LIM} (mA) | D[5:0] | I _{LIM} (mA) |
|---------|-----------------------|---------|-----------------------|----------------|-----------------------|---------|-----------------------|
| 00 0000 | 0 | 01 0000 | 624 | 10 0000 | 1248 | 11 0000 | 1872 |
| 00 0001 | 39 | 01 0001 | 663 | 10 0001 | 1287 | 11 0001 | 1911 |
| 00 0010 | 78 | 01 0010 | 702 | 10 0010 | 1326 | 11 0010 | 1950 |
| 00 0011 | 117 | 01 0011 | 741 | 10 0011 | 1365 | 11 0011 | 1989 |
| 00 0100 | 156 | 01 0100 | 780 | 10 0100 | 1404 | 11 0100 | 2028 |
| 00 0101 | 195 | 01 0101 | 819 | 10 0101 | 1443 | 11 0101 | Reserved |
| 00 0110 | 234 | 01 0110 | 858 | 10 0110 | 1482 | 11 0110 | Reserved |
| 00 0111 | 273 | 01 0111 | 897 | 10 0111 | 1521 | 11 0111 | Reserved |
| 00 1000 | 312 | 01 1000 | 936 | 10 1000 | 1560 | 11 1000 | Reserved |
| 00 1001 | 351 | 01 1001 | 975 | 10 1001 | 1599 | 11 1001 | Reserved |
| 00 1010 | 390 | 01 1010 | 1014 | 10 1010 | 1638 | 11 1010 | Reserved |
| 00 1011 | 429 | 01 1011 | 1053 | 10 1011 | 1677 | 11 1011 | Reserved |
| 00 1100 | 468 | 01 1100 | 1092 | 10 1100 | 1716 | 11 1100 | Reserved |
| 00 1101 | 507 | 01 1101 | 1131 | 10 1101 | 1755 | 11 1101 | Reserved |
| 00 1110 | 546 | 01 1110 | 1170 | 10 1110 | 1794 | 11 1110 | Reserved |
| 00 1111 | 585 | 01 1111 | 1209 | 10 1111 | 1833 | 11 1111 | Reserved |

VLIM TABLE

Table 4. V_{LIM} Table (D[5:0] in REG03 and REG04), Default = 2732.8mV

| D[5:0] | V _{LIM} (mV) | D[5:0] | V _{LIM} (mV) | D[5:0] | V _{LIM} (mV) | D[5:0] | V _{LIM} (mV) |
|---------|-----------------------|----------------|-----------------------|---------|-----------------------|---------|-----------------------|
| 00 0000 | 0 | 01 0000 | 1561.6 | 10 0000 | 3123.2 | 11 0000 | 4684.8 |
| 00 0001 | 97.6 | 01 0001 | 1659.2 | 10 0001 | 3220.8 | 11 0001 | 4782.4 |
| 00 0010 | 195.2 | 01 0010 | 1756.8 | 10 0010 | 3318.4 | 11 0010 | 4880 |
| 00 0011 | 292.8 | 01 0011 | 1854.4 | 10 0011 | 3416 | 11 0011 | 4977.6 |
| 00 0100 | 390.4 | 01 0100 | 1952 | 10 0100 | 3513.6 | 11 0100 | 5075.2 |
| 00 0101 | 488 | 01 0101 | 2049.6 | 10 0101 | 3611.2 | 11 0101 | 5172.8 |
| 00 0110 | 585.6 | 01 0110 | 2147.2 | 10 0110 | 3708.8 | 11 0110 | 5270.4 |
| 00 0111 | 683.2 | 01 0111 | 2244.8 | 10 0111 | 3806.4 | 11 0111 | 5368 |
| 00 1000 | 780.8 | 01 1000 | 2342.4 | 10 1000 | 3904 | 11 1000 | 5465.6 |
| 00 1001 | 878.4 | 01 1001 | 2440 | 10 1001 | 4001.6 | 11 1001 | 5563.2 |
| 00 1010 | 976 | 01 1010 | 2537.6 | 10 1010 | 4099.2 | 11 1010 | Reserved |
| 00 1011 | 1073.6 | 01 1011 | 2635.2 | 10 1011 | 4196.8 | 11 1011 | Reserved |
| 00 1100 | 1171.2 | 01 1100 | 2732.8 | 10 1100 | 4294.4 | 11 1100 | Reserved |
| 00 1101 | 1268.8 | 01 1101 | 2830.4 | 10 1101 | 4392 | 11 1101 | Reserved |
| 00 1110 | 1366.4 | 01 1110 | 2928 | 10 1110 | 4489.6 | 11 1110 | Reserved |
| 00 1111 | 1464 | 01 1111 | 3025.6 | 10 1111 | 4587.2 | 11 1111 | Reserved |

REGISTER DESCRIPTIONS

All registers are 8-bit and individual bits are named from D[0] for LSB to D[7] for MSB.

R/W: Read/Write bit(s).

R: Read only bit(s).

PORV: Power-On-Reset Value.

n: Parameter code represented by the bits in unsigned binary number format.

I²C Slave Address: 0x21 if ADDR is pulled low to GND (< 50kΩ) or 0x60 if ADDR is floating or connected to a capacitor (< 150nF).

REG00 (Device Control)

Register address: 0x00; R/W

PORV = 10000001

Table 5. REG00 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|---------------------|---|------|------|
| D[7] | XTEC | Select Monitoring of VTEC or ITEC on the XTEC Output Pin. 0 = Select VTEC 1 = Select ITEC (default) | 1 | R/W |
| D[6:4] | Reserved | Reserved. | 000 | R/W |
| D[3:2] | SS_TIME[1:0] | Soft-Start Time. 00 = 120ms (default) 01 = 60ms 10 = 30ms 11 = 15ms | 00 | R/W |
| D[1] | REFRESH | Refresh Status Bits. (automatically resets to 0 after writing 1 on it) 0 = Disable (default) 1 = Enable (release all latched status bits) REFRESH should be set to 1 after either of the following states changes from low to high. (EN, SD, ENILIM_HEAT, ENILIM_COOL, ENVLIM_HEAT, ENVLIM_COOL) | 0 | R/W |
| D[0] | I ² C_ON | Power Stage Enable Control Bit. 0 = Disable power stage 1 = Enable power stage (default) | 1 | R/W |

REG01 (TEC Heating Mode Current Limiting Parameters)

Register address: 0x01; R/W

PORV = 10100110

Table 6. REG01 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|--------------------|---|--------|------|
| D[7] | ENILIM_HEAT | TEC Current Limit in Heating Mode. 0 = Disable 1 = Enable (default) | 1 | R/W |
| D[6] | RESERVED | Reserved. | 0 | R/W |
| D[5:0] | ILIM_HEAT_SET[5:0] | Sets the TEC Current Limit for the Heating Mode. See Table 3. | 100110 | R/W |

REG02 (TEC Cooling Mode Current Limiting Parameters)

Register address: 0x02; R/W

PORV = 10100110

Table 7. REG02 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|--------------------|---|--------|------|
| D[7] | ENILIM_COOL | TEC Current Limit in Cooling Mode. 0 = Disable 1 = Enable (default) | 1 | R/W |
| D[6] | RESERVED | Reserved. | 0 | R/W |
| D[5:0] | ILIM_COOL_SET[5:0] | Sets the TEC Current Limit for the Cooling Mode. See Table 3. | 100110 | R/W |

REGISTER DESCRIPTION (continued)**REG03 (TEC Heating Mode Voltage Limiting Parameters and VIN OVP Enable Control)**

Register address: 0x03; R/W

PORV = 11011100

Table 8. REG03 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|--------------------|---|--------|------|
| D[7] | ENVLIM_HEAT | TEC Voltage Limit Setting in Heating Mode. 0 = Disable 1 = Enable (default) | 1 | R/W |
| D[6] | VIN OVP | 0 = Disable VIN OVP function 1 = Enable VIN OVP function (default) | 1 | R/W |
| D[5:0] | VLIM_HEAT_SET[5:0] | Sets the TEC Voltage Limit for the Heating Mode. See Table 4. | 011100 | R/W |

REG04 (TEC Cooling Mode Voltage Limiting Parameters)

Register address: 0x04; R/W

PORV = 10011100

Table 9. REG04 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|--------------------|---|--------|------|
| D[7] | ENVLIM_COOL | TEC Voltage Limit Setting in Cooling Mode. 0 = Disable 1 = Enable (default) | 1 | R/W |
| D[6] | RESERVED | Reserved. | 0 | R/W |
| D[5:0] | VLIM_COOL_SET[5:0] | Sets the TEC Voltage Limit for the Cooling Mode. See Table 4. | 011100 | R/W |

REG05 (LDO Secondary Current Limits and Buck Current Limit Settings)

Register address: 0x05; R/W

PORV = 00000000

Table 10. REG05 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|---------------------|---|------|------|
| D[7:6] | LDO_ILIM_HEAT[1:0] | Sets the Secondary Current Limit of the LDO in Heating Mode. If this OCP occurs, the device will enter hiccup protection. 00 = 2A (default) 01 = 2.5A 10 = 3A 11 = 3.5A | 00 | R/W |
| D[5:4] | LDO_ILIM_COOL[1:0] | Sets the Secondary Current Limit of the LDO in Cooling Mode. If this OCP occurs, the device will enter hiccup protection. 00 = 2A (default) 01 = 2.5A 10 = 3A 11 = 3.5A | 00 | R/W |
| D[3:2] | BUCK_ILIM_HEAT[1:0] | Sets the Current Limit of the Buck in Heating Mode. If this OCP occurs, the device will enter hiccup protection. 00 = 2.5A (default) 01 = 3A 10 = 3.5A 11 = 4A | 00 | R/W |
| D[1:0] | BUCK_ILIM_COOL[1:0] | Sets the Current Limit of the Buck in Cooling Mode. If this OCP occurs, the device will enter hiccup protection. 00 = 2.5A (default) 01 = 3A 10 = 3.5A 11 = 4A | 00 | R/W |

REGISTER DESCRIPTION (continued)**REG06 (Read Slave Address)**

Register address: 0x06; Read only

PORV = NA

Table 11. REG06 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|--------------------|---|------|------|
| D[7:1] | SLAVE_ADDRESS[6:0] | Reports the 7-bit Slave Address Number (set by ADDR pin). | NA | R |
| D[0] | RESERVED | Reserved. | NA | R |

REG09 (Status Bits)

Register address: 0x09; Read only

PORV = NA

Table 12. REG09 Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|-----------|---|------|------|
| D[7:6] | MODE[1:0] | These Bits Report Heating or Cooling Operation Mode Status. 00 = Near cooling/heating boundary. 01 = Cooling mode. 10 = Heating mode. 11 = Reserved. | NA | R |
| D[5] | VLIM | TEC Voltage Status Bit. Latches if goes to 1 and is released by setting the REFRESH bit. 0 = TEC voltage is normal. 1 = TEC voltage has reached to a TEC voltage limit (set by I ² C). | NA | R |
| D[4] | ILIM | TEC Current Status Bit. Latches if goes to 1 and is released by setting the REFRESH bit. 0 = TEC current is normal. 1 = TEC current has reached to a TEC current limit (set by I ² C). | NA | R |
| D[3] | PWOR | Power Stage Status Bit. 0 = Power stage is disabled. 1 = Power stage is active. | NA | R |
| D[2] | RESERVED | Reserved. | NA | R |
| D[1] | OT | Over-Temperature Status Bit. Latches if goes to 1 and is released by setting the REFRESH bit. 0 = Die is operating below the over-temperature limit. 1 = Die over-temperature has occurred. | NA | R |
| D[0] | OTW | Over-Temperature Warning Bit. Latches if goes to 1 and is released by setting the REFRESH bit. 0 = Die temperature is below the warning threshold limit. 1 = Die temperature has exceeded the warning threshold (120°C). | NA | R |

REG0A (Vendor and Version Data)

Register address: 0x0A; Read only

PORV = 00010000

Table 13. REG0A Details

| BITS | BIT NAME | DESCRIPTION | PORV | TYPE |
|--------|-----------------|-------------|------|------|
| D[7:4] | VENDOR_ID[3:0] | Vendor ID. | 0001 | R |
| D[3:0] | VERSION_ID[3:0] | Version ID. | 0000 | R |

DETAILED DESCRIPTION

The SGM41296 is a compact monolithic I²C programmable driver with built-in power MOSFETs for powering a thermoelectric cooling device (TEC). It can provide 1.5A continuous current from a 2.7V to 5.5V input supply. The TEC voltage is controlled with a linear relationship to the analog input (CTL) that is typically received from a compensator in a temperature control loop to regulate the TEC temperature.

Some features such as TEC voltage or current limits can be changed on the fly by the host by the 1Mbps I²C interface. With the minimal external components and packed in a tiny TQFN package, the SGM41296 is an ideal solution for high density designs. Several protective features such as, soft-start, over-current, over-voltage and over-temperature are also provided.

Control of the TEC Voltage

A thermoelectric cooler is a heat pump that transfers the heat between its two surfaces depending on its voltage polarity. The TEC terminals are placed between the linear regulator (LDO) output (VOL) and the PWM regulator (synchronous Buck) output. The Buck output voltage is sensed by VOS pin. The Buck external inductor is placed between the switching node (SW) and the TEC terminal that is connected to VOS. So, the TEC bipolar voltage is $V_{TEC} = V_{VOL} - V_{VOS}$. Both LDO and Buck outputs can sink or source current up to 1.5A. V_{TEC} is controlled to have a linear relation with the V_{CTL} input but is limited to the lower of V_{IN} and V_{LIM} as shown in Figure 3.

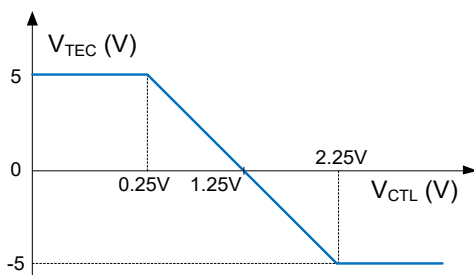


Figure 4. V_{TEC} Linear Relationship with V_{CTL}

In the linear region, the TEC voltage is expressed as:

$$V_{TEC} = -5 \times (V_{CTL} - 1.25V)$$

The terminal voltages themselves (V_{VOL} and V_{VOS}) are also limited to the V_{IN} and V_{LIM} and are given by:

$$V_{VOL} = V_{MID} - 40 \times (V_{CTL} - 1.25V)$$

$$V_{VOS} = V_{VOL} + 5 \times (V_{CTL} - 1.25V)$$

where $V_{MID} = 2.5V$ if $V_{IN} > 4V$; otherwise, $V_{MID} = 1.5V$.

TEC Current and Voltage Monitoring

The SGM41296 can monitor the TEC current or voltage. By setting the XTEC bit to 1 in REG00, the XTEC pin will output a voltage proportional to the TEC current. The accuracy is $\pm 5\%$ for currents larger than 0.5A. If V_{ITEC} is the XTEC pin voltage in current monitoring:

$$V_{ITEC} = 1.25V + 0.5 \times I_{OUT} (A); \text{ when cooling}$$

$$V_{ITEC} = 1.25V - 0.5 \times I_{OUT} (A); \text{ when heating}$$

The TEC current monitor provides information for the TEC current limit (set by I²C) comparator as well.

By setting the XTEC bit to 0, the XTEC pin will output a voltage proportional to the actual TEC voltage. If V_{ITEC} is the XTEC pin voltage in voltage monitoring:

$$V_{ITEC} = 1.25V + 0.2 \times (V_{VOL} - V_{VOS}); \text{ when cooling}$$

$$V_{ITEC} = 1.25V - 0.2 \times (V_{VOS} - V_{VOL}); \text{ when heating}$$

Internal Voltage Reference

The SGM41296 has an integrated 2.5V reference voltage with 1% accuracy. If $V_{IN} > 2.7V$, the V_{REF} voltage is fixed and will not be affected by the EN or SD input or the I²C registers.

Power Stage

A hybrid H-bridge power driver with a linear LDO leg and a switching Buck leg is integrated in this device to drive the TEC. The power stage turns on if:

- V_{IN} is above UVLO level.
- EN is high.
- SD is high.
- I²C_ON bit = 1.

Enable Pin (EN)

Pulling up the enable pin (EN) above 1.2V enables the device if the other conditions such as $V_{IN} > 2.6V$ (UVLO) are valid. After enabling the device, first any TEC bias voltage will be discharged to zero by the internal discharge paths and then the VOL and VOS outputs will start to ramp up. EN pin has an internal 0.36 μ A pull-down current source, so if it is left floating, it will be pulled low and the device will be disabled.

Shutdown Pin (SD)

The SD pin will disable and shut down the device if it is pulled low. It has an internal 1.3M Ω pull-down resistor. If it is pulled up, the device will turn on after a 30ms delay.

DETAILED DESCRIPTION (continued)

Soft-Start Procedure

To avoid input over-current during power-up or V_{TEC} overshoots after enabling the power stage, a three-step soft-start process is implemented in the device as shown in Figure 4. After discharging the VOL and VOS (step1), they first ramp up together towards the V_{MID} level (step 2) and then ramp separately (step 3) such that the TEC voltage ($V_{TEC} = V_{VOL} - V_{VOS}$) ramps up with a controlled slew rate. In the first step, both VOL and VOS outputs are discharged with internal 500Ω pull-down resistive paths for a short discharge time to make sure there is no voltage on the TEC. After confirming that the VOL and VOS are discharged and both are below 0.4V, the second step (1st start-up) begins, otherwise the discharge step will repeat with the same period. In the 1st start-up (second step), the LDO and Buck are turned on and the VOL and VOS rise together until they reach the V_{MID} level. At this point, the 2nd start-up (third step) begins and the VOL and VOS are separately controlled such that V_{TEC} ramps up towards its regulation target. The total start-up time (1st + 2nd) is set by I²C in REG00 D[3:2]. The 2nd start-up time is almost 8/19 of the total.

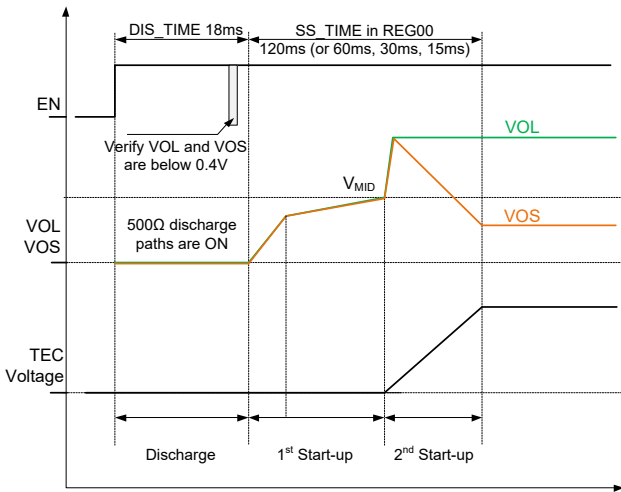


Figure 5. Three-Step Soft-Start of the Power Stage

TEC Voltage Limit Protection

To avoid TEC over-voltage risks, voltage limit protections are provided for both cooling and heating operations. These limits can be programmed by the I²C host. If the V_{TEC} reaches any of these limits, the Buck output (VOS) will not follow the V_{CTL} anymore and V_{TEC} will be regulated to its limit value as shown in Figure 5. The TEC heating and cooling voltage limits are set in

$VLIM_HEAT_SET[5:0]$ and $VLIM_COOL_SET[5:0]$ bits in REG03 and REG04, respectively. These voltage limits can be set between 97.6mV and 5.5V in 97.6mV steps. Due to the bipolar driving, a secondary over-voltage limit, which is 1V higher than the first voltage limit, is considered to protect the TEC from any fatal over-voltage caused by a short between one terminal and GND or VIN. If a secondary over-voltage is detected, the switching will stop immediately and the device enters into hiccup mode as shown in Figure 6.

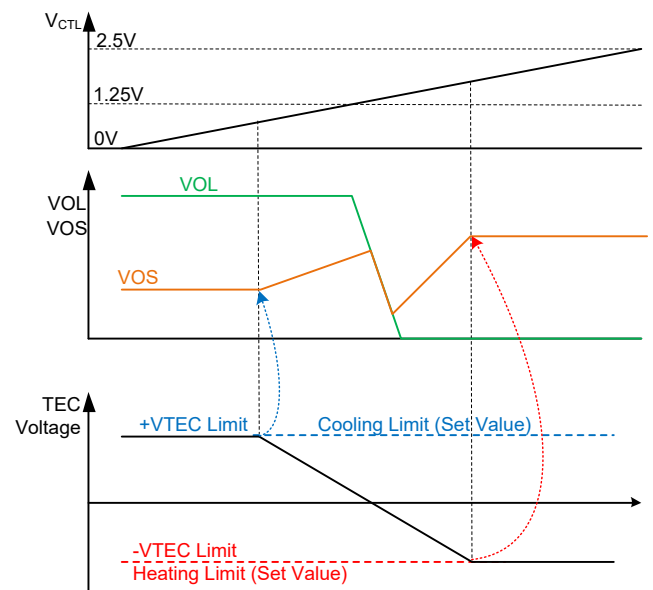


Figure 6. Primary TEC Voltage Limit Protection

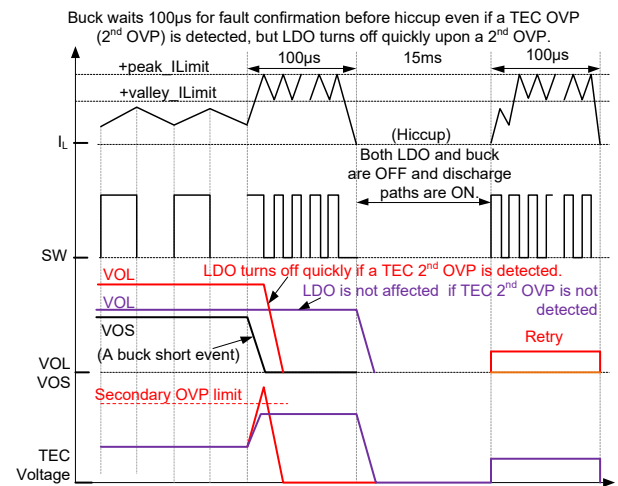


Figure 7. Secondary Voltage Limit Protection Hiccup

DETAILED DESCRIPTION (continued)

TEC Current limit

The SGM41296 includes I²C programmable current limit protections with no need for external components. If LDO (VOL) reaches to its 1st current limit, the VOL is kept at the same level and VOS is limited to the 1st current limit too. If the LDO reaches to its 2nd current limit (like a short), the power stage is turned off immediately and goes to the hiccup mode.

If the Buck (VOS) output reaches to its current limit, the power stage will enter hiccup mode after a 100µs confirmation delay.

The REG01 (ILIM_HEAT_SET[5:0] bits) and REG02 (ILIM_COOL_SET[5:0] bits) I²C registers can be set the TEC 1st current limit levels for heating and cooling modes respectively. These current limits can be set from 39mA to 2.028A in 39mA steps. Note that if the TEC current limit is set to 39mA, the TEC voltage must be 78mV or higher for current limit. When the TEC is in current limit status, the Buck output voltage (VOS) is determined by the limit current and is not controlled by V_{CTL}.

To protect the individual power output pins, secondary heating and cooling current limits for the LDO and independent heating and cooling current limits for the Buck are also considered that each can be set to one of the 4 available choices by I²C (REG05).

VOL has two current limit levels. If the VOL current ramps up and reaches to its 1st current limit, the VOL voltage will not be changed but VOS output voltage will be regulated such that the V_{TEC} voltage is not increased in order to keep the TEC current limited to the 1st limit as shown in Figure 7.

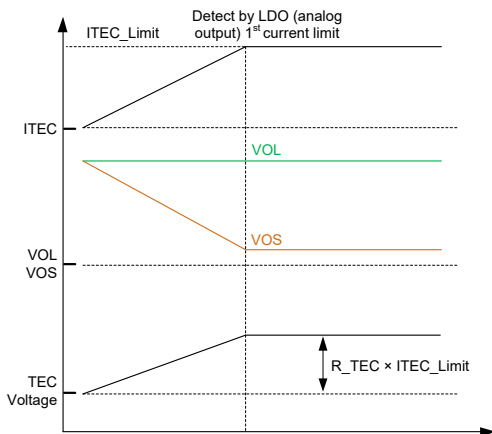


Figure 8. Primary Current Limit Protection (1st Limit)

If a large LDO over-current fault such as a short to VIN or GND occurs, the VOL current ramps up very quickly and exceeds the 2nd current limit. This event turns the power stage off immediately and starts hiccup mode as shown in Figure 8.

The Buck (VOS) output is protected by one current limit level and if it occurs, the device will recover automatically if the fault clears within a 100µs confirmation window. Otherwise the hiccup protection will start.

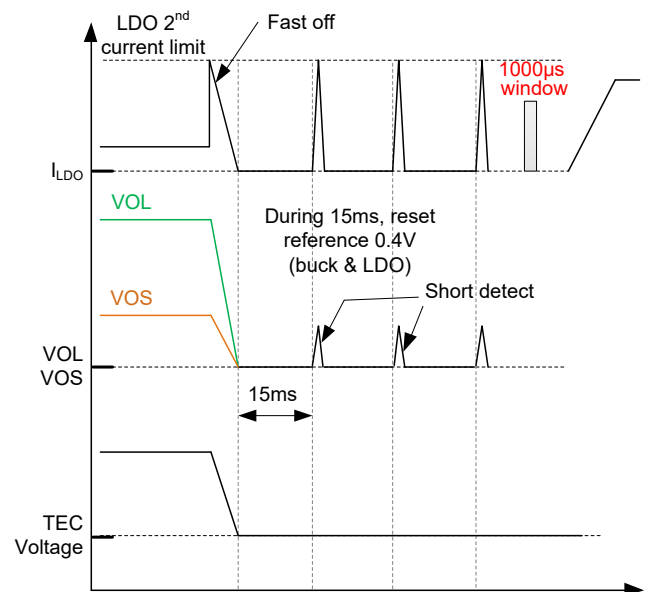


Figure 9. Secondary Current Limit Protection (2nd Limit)

Hiccup Protection

Hiccup feature is added to the SGM41296 for full protection against various risk conditions. Hiccup starts if any of the following critical faults occur:

- LDO output exceeds its 2nd current limit.
- Buck output exceeds its current limit.
- V_{TEC} voltage exceeds its 2nd voltage limit.

In the first 15ms of the hiccup mode, the power stage is disabled and VOL and VOS outputs are pulled down through the internal passive discharge paths. The discharge paths are always on. At the end of the 15ms window, V_{VOL} and V_{VOS} are measured and if either of them is above 0.4V, a new 15ms hiccup cycle will start. Existence of such voltage means that some residual energy or a fault is still present like a short to VIN. This feature prevents turn-on when one or both outputs are still in fault condition.

DETAILED DESCRIPTION (continued)

If both outputs are measured below 0.4V, a 1ms detection window will start in which the power stage is enabled to regulate both VOL and VOS to 0.4V. If there is no short from the outputs to GND and no over-current is detected, a new soft-start cycle will initiate after the 1ms period, otherwise a new 15ms hiccup cycle begins.

VIN Over-Voltage Protection

If the V_{IN} exceeds 5.75V, the VOL and VOS outputs are turned off and start to discharge. If V_{IN} drops below 5.5V, a new soft-start cycle begins.

Over-Temperature Protection

The device shuts down if the junction temperature exceeds the +165°C shutdown threshold and recovers automatically if T_J falls below the recovery threshold.

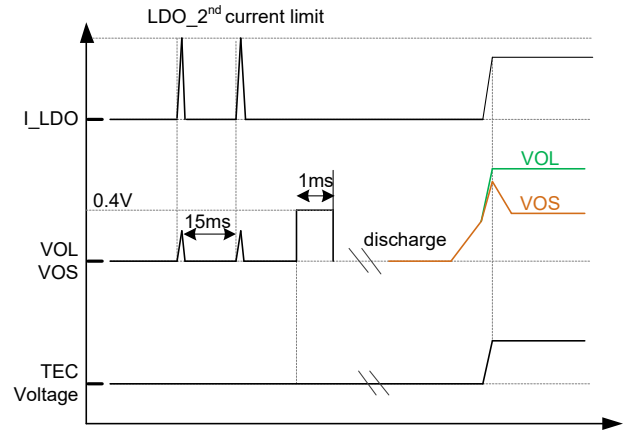


Figure 10. Hiccup Mode Protection

I²C INTERFACE

The SGM41296 is a highly flexible device thanks to the I²C interface and the ability to read or modify the parameters stored in its 9 8-bit registers. All registers are accessible if V_{IN} is above minimum, regardless of the EN and SD pins statuses.

I²C Slave Address

The SGM41296 is an I²C slave device. The I²C address is 0x60 if ADDR pin is floating or connected to a capacitor (< 150nF), and the I²C address is 0x21 if it is pulled down by a 50kΩ or smaller resistor to GND. After V_{IN} powers up, at least a 20ms delay is needed to detect ADDR state.

I²C Soft-Start Time Setting

Four choices of 15ms, 30ms, 60ms and 120ms (default) are available for the soft-start time. They can be selected by writing to the REG00 (SS_TIME[1:0] bits).

REFRESH Bit

The REFRESH bit in the REG00 D[1] is provided to acknowledge and clear the status bits that are latched after an event. Setting this bit to high will erase the latched status and makes them ready for a new detection. REFRESH automatically resets to prepare for the next refreshing write.

Power Stage Control by I²C

The I²C_ON bit in the REG00 can control the power stage similar to the EN and SD pins. Write 0 to I²C_ON bit for turn off or 1 to turn on. The power stage can turn on if I²C_ON bit and EN, SD pins are all high.

TEC Current and Voltage Limit Setting by I²C

The TEC heating and cooling current limits can be set by REG01 (ILIM_HEAT_SET[5:0] bits) and REG02 (ILIM_COOL_SET[5:0] bits) respectively. A current limit function is activated if the corresponding current limit enable bit in REG01 (ENILIM_HEAT bit) or REG02 (ENILIM_COOL bit) is set to 1.

Similarly, the TEC heating and cooling voltage limits can be set by REG03 (VLIM_HEAT_SET[5:0] bits) and REG04 (VLIM_COOL_SET[5:0] bits) respectively. A voltage limit function is activated if the corresponding voltage limit enable bit in REG03 (ENVLIM_HEAT bit) or REG04 (ENVLIM_COOL bit) is set to 1.

If the TEC current or voltage exceeds these limits, the Buck voltage (V_{OS}) will be adjusted to satisfy the limit and is not controlled by CTL pin anymore. This feature protects the TEC from the device by limiting the delivered current and voltage.

Secondary Current and Voltage Limits

The secondary heating and cooling current limits for the LDO and Buck are set by LDO_ILIM_HEAT[1:0], LDO_ILIM_COOL[1:0], BUCK_ILIM_HEAT[1:0] and BUCK_ILIM_COOL[1:0] bits in REG05. If an output short occurs, the internal MOSFET current rises fast and initiates the secondary current limit protection by entering hiccup mode (with 15ms cycles).

Status Bits

REG09 is a status register that indicates the TEC operation status.

The MODE[1:0] bits indicate the real-time status of heating (10) or cooling (01) mode. If MODE[1:0] = 00, the TEC is operating near the cooling/heating boundary.

The VLIM bit in the REG09 D[5] is set if a voltage limit event occurs. It is latched to 1 even if the VLIM status is cleared. The latch can be removed by the REFRESH bit in REG00. The REFRESH bit is default 0 and when it is set to 1, it will refresh the status bits and then returns to 0 automatically.

The ILIM bit in the REG09 D[4] is set if a current limit event occurs. This bit is latched if ILIM bit changes from 0 to 1. The latch can be removed by the REFRESH bit.

The PWOR bit in the REG09 D[3] is updated in real-time status. It is set to 1 when the power stage is operating normal. It will be latched to 0 in the following cases:

- During hiccup until the end of soft-start 1st stage.
- When EN or SD or I²C_ON is low.
- In over-temperature shutdown status.
- Before soft-start 1st stage ends in a normal start-up.

The OT bit in the REG09 D[1] is latched to 1 if a junction over-temperature occurs. The latch can be removed by the REFRESH bit.

The OTW bit in the REG09 D[0] is latched to 1 if the junction over-temperature warning threshold is exceeded. The latch can be removed by the REFRESH bit.

APPLICATION INFORMATION

Inductor

A 1.5 μ H to 3.3 μ H inductor works well in most applications with the $f_{SW} = 1$ MHz switching frequency. Use Equation 1 for calculating the inductance needed.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (1)$$

where ΔI_L is the inductor ripple current. It is typically chosen to be approximately 35% of the full load current. The maximum peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Choose an inductor with 20m Ω or lower DC resistance for better efficiency. Avoid unshielded inductors to minimize magnetic interference. A 2.2 μ H metal alloy or multilayer inductor will work well for most designs.

Input Capacitor

The Buck converter input current is discontinuous and a capacitor is needed to provide the AC current. Low ESR and stable ceramic capacitors with X5R or X7R dielectrics are recommended. For most designs, a 10 μ F ceramic capacitor works well. The capacitor ripple current rating should be high enough to provide the large input switching ripples. The RMS current can be estimated from Equation 3 in CCM mode:

$$I_{CIN,RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst case occurs at $V_{IN} = 2 \times V_{OUT}$:

$$I_{CIN,RMS} \approx \frac{I_{LOAD}}{2} \quad (4)$$

Choose a capacitor with an RMS current rating higher than half DC load current. If an electrolytic or tantalum capacitor is used, parallel a high quality 0.1 μ F ceramic capacitor close to the device. The total effective capacitance should be large enough such that the input ripple remains small (to keep the output regulated). The ripple can be estimated from Equation 5 in CCM mode:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Output Capacitor

Low ESR ceramic capacitors are recommended for the Buck output capacitor to stabilize the DC voltage and minimize the output voltage ripple. The output ripple can be estimated from Equation 6 in CCM mode:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (6)$$

where C_{OUT} is the output capacitance, L is the inductor value, and ESR is the equivalent series resistance of the output capacitor(s).

If ceramic capacitors are used, ESR can be ignored at the switching frequency, so:

$$\Delta V_{OUT} \approx \frac{V_{OUT}}{8 \times L \times C_{OUT} \times f_{SW}^2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

If a tantalum or electrolytic capacitor is used, the ESR dominates the capacitor impedance at the switching frequency and for simplification, the output ripple can be approximated by Equation 8:

$$\Delta V_{OUT} \approx \frac{V_{OUT}}{L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times ESR \quad (8)$$

Regulation system stability is affected by C_{OUT} characteristics.

For the linear LDO output use a 1 μ F capacitor.

PCB Layout

PCB layout has a significant impact on the performance of the switching power supplies. Follow the rules given below for designing a PCB for SGM41296.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Connect the device PGND to the PCB ground plane right at the GND pin.
- Keep the switching node (SW) trace away from the feedback network and short.
- Keep VOS sensing trace as short as possible and away from the inductor and specifically do not boarder or enclose the inductor by this trace.

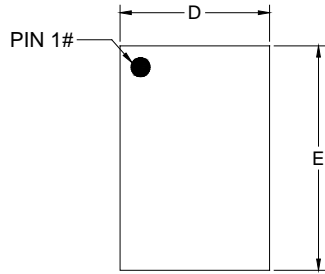
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

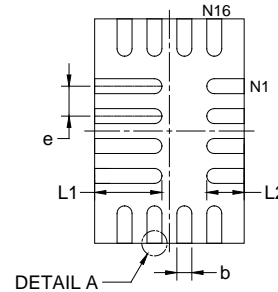
| JULY 2024 – REV.A.3 to REV.A.4 | Page |
|--|-------------|
| Added Package Thermal Resistance section..... | 2 |
| <hr/> | |
| JUNE 2023 – REV.A.2 to REV.A.3 | Page |
| Updated Electrical Characteristics section and Table 2..... | 5, 15 |
| Added I ² C Interface Timing Characteristics ⁽¹⁾ and I ² C Interface Timing Diagram sections..... | 6, 7 |
| <hr/> | |
| NOVEMBER 2022 – REV.A.1 to REV.A.2 | Page |
| Added Ordering Number (SGM41296XTRJ16G-K/TR)..... | 2 |
| Updated Tape and Reel Information section | 26, 27 |
| <hr/> | |
| APRIL 2022 – REV.A to REV.A.1 | Page |
| Updated Pin Description | 3 |
| Updated Electrical Characteristics | 5 |
| Updated Register Maps | 13 |
| Updated Register Descriptions | 15 |
| <hr/> | |
| Changes from Original (DECEMBER 2020) to REV.A | Page |
| Changed from product preview to production data..... | All |

PACKAGE OUTLINE DIMENSIONS

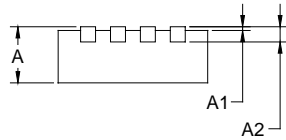
TQFN-2x3-16L



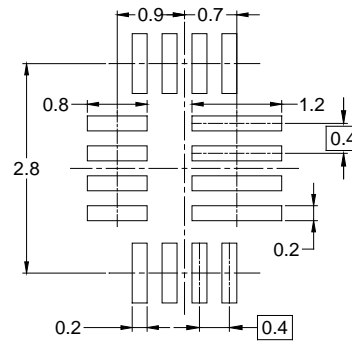
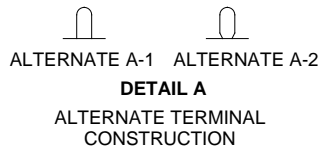
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|--------|---------------------------|-------|-------|
| | MIN | MOD | MAX |
| A | 0.800 | 0.850 | 0.900 |
| A1 | - | - | 0.050 |
| A2 | 0.203 REF | | |
| D | 1.950 | 2.000 | 2.050 |
| E | 2.950 | 3.000 | 3.050 |
| b | 0.150 | 0.200 | 0.250 |
| e | 0.400 BSC | | |
| L1 | 0.850 | 0.900 | 0.950 |
| L2 | 0.450 | 0.500 | 0.550 |

NOTE: This drawing is subject to change without notice.

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

| ORDERING NUMBER | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|----------------------|---------------|--------------------|---------|---------|---------|---------|---------|---------|--------|---------------|
| SGM41296XTRJ16G/TR | 7" | 9.0 | 2.30 | 3.30 | 1.05 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |
| SGM41296XTRJ16G-K/TR | 13" | 12.4 | 2.20 | 3.30 | 1.14 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|-------------|-------------|------------|-------------|--------------|
| 7" (Option) | 368 | 227 | 224 | 8 |
| 7" | 442 | 410 | 224 | 18 |
| 13" | 386 | 280 | 370 | 5 |

DD0002