SGM61031
3A High Efficiency Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61031 is an efficient high frequency synchronous Buck converter with an input voltage range of 2.7V to 5.5V and a wide output current range that is optimized for compact solutions. It operates in PWM mode at heavy loads and automatically enters power-save mode (PSM) at light loads to maintain its high efficiency.

To meet the requirements of system power rails, the output capacitors with values above 100μF can be used by the internal loop compensation.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved.

The SGM61031 is available in a Green TDFN-2×2-8AL package.

FEATURES

- **AHP-COT Architecture for Fast Transient Regulation**
- **2.7V to 5.5V Input Voltage Range**
- **3A Output Current**
- **100% Duty Cycle for Lowest Dropout**
- **Power-Save Mode for Light Load Efficiency**
- **Output Discharge Function**
- **Power Good Output**
- **Thermal Shutdown**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

Battery-Powered Applications
Portable Electronic Devices
Personal Computer, Notebook
Data Storage

TYPICAL APPLICATION

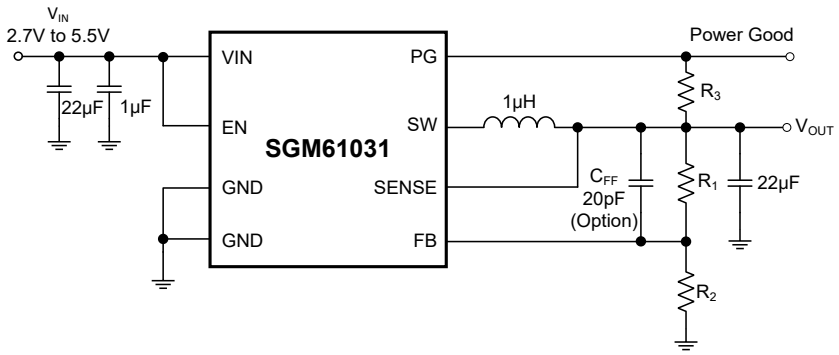


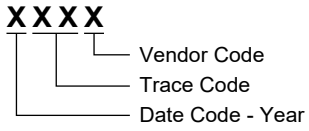
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61031	TDFN-2×2-8AL	-40℃ to +125℃	SGM61031XTDE8G/TR	S00W XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, PG, SENSE Voltages ..... -0.3V to 6V
SW, EN Voltages ..... -0.3V to V_{IN} + 0.3V
SW (AC, Less than 10ns) Voltage ..... -3V to 10V
FB Voltage ..... -0.3V to 3.6V
Power Good Sink Current 1mA
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... 91℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.7V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

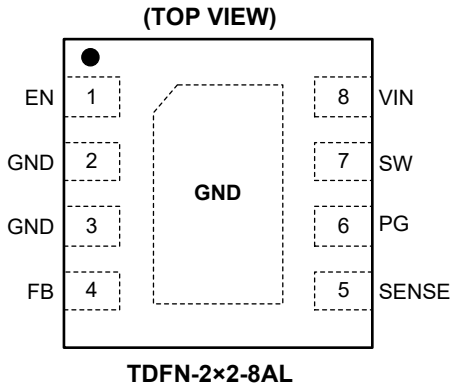
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
1	EN	I	Active High Enable Input. Logic high sets the device active. Logic low disables it and turns it into shutdown mode. Do not leave this pin floating.
2, 3	GND	G	Power and Signal Ground.
4	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
5	SENSE	I	Output Voltage Sense Pin. Must be connected to output voltage.
6	PG	O	Power Good Open-Drain Output. If the output voltage is less than the regulation limit, this pin is pulled low. Leave this pin floating when not in use.
7	SW	P	Switching Node.
8	VIN	P	Power Supply Voltage Input.
Exposed Pad	GND	—	Connect it to GND. The thermal pad must be soldered to improve heat dissipation.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

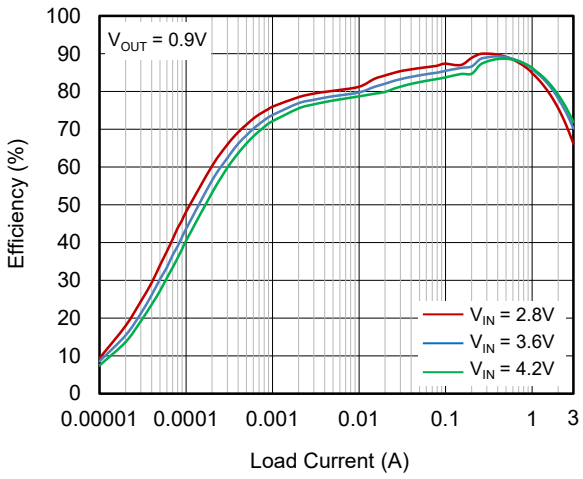
(V_{IN} = 3.6V, T_J = -40℃ to +125℃. Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Input Voltage Range	V_{IN}		2.7		5.5	V
Quiescent Current into VIN	I_Q	I_{OUT} = 0mA, device not switching		24	40	μA
Shutdown Current into VIN	I_{SD}	EN = Low		0.01	1	μA
Under-Voltage Lockout	V_{UVLO}	Input voltage falling	1.6	1.8	2	V
Under-Voltage Lockout Hysteresis		Rising above V_{UVLO}		130		mV
Thermal Shutdown	T_{JSD}	Temperature rising		160		℃
Thermal Shutdown Hysteresis		Temperature falling below T_{JSD}		30		℃
Logic Interface (EN)						
High Level Input Voltage	V_{IH}	V_{IN} = 2.7V to 5.5V	1			V
Low Level Input Voltage	V_{IL}	V_{IN} = 2.7V to 5.5V			0.4	V
Input Leakage Current	I_{LKG}			0.01	0.5	μA
Power Good						
Power Good Threshold	V_{PG}	V_{OUT} falling, (% of nominal V_{OUT})	-15	-10	-5	%
		Power Good Hysteresis (% of nominal V_{OUT})		-5		
PG Leakage Current	I_{PG_LKG}			0.02	0.8	μA
Output						
Feedback Regulation Voltage	V_{FB}	V_{IN} = 3.6V	0.439	0.450	0.461	V
Feedback input Bias Current	I_{FB}	V_{FB} = 0.45V		1	20	nA
Output Discharge Resistor	R_{DIS}	EN = Low, V_{OUT} = 1.8V		0.95	1.3	kΩ
High-side FET On-Resistance	R_{DSON_H}	I_{SW} = 500mA, V_{IN} = 3.6V		91	155	mΩ
Low-side FET On-Resistance	R_{DSON_L}	I_{SW} = 500mA, V_{IN} = 3.6V		46	90	mΩ
High-side FET Switch Current Limit	I_{LIM_H}	Rising inductor current, T_J = +25℃	4.3	5.6	7.2	A
Low-side FET Switch Current Limit	I_{LIM_L}	Rising inductor current, T_J = +25℃	2.8	3.4	5.0	A

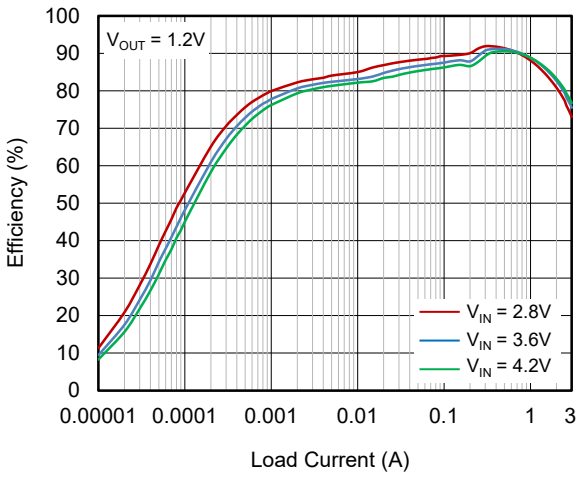
TYPICAL PERFORMANCE CHARACTERISTICS

DCR = 22mΩ, unless otherwise noted.

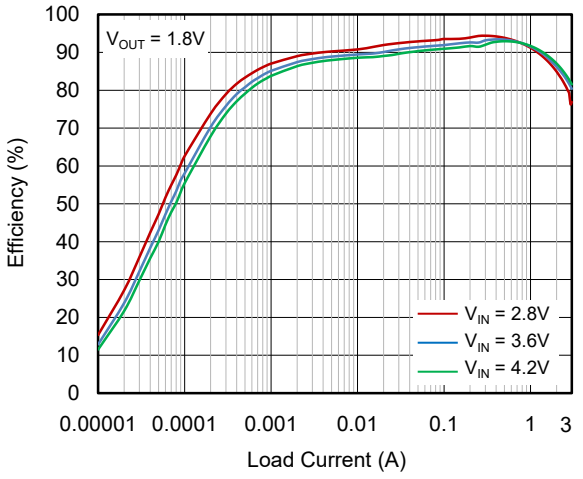
Efficiency vs. Load Current



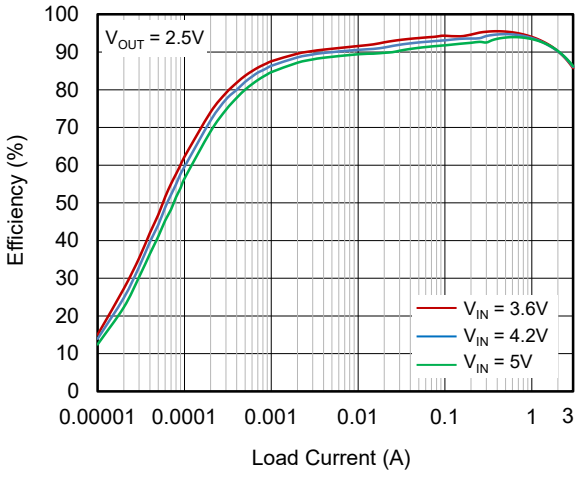
Efficiency vs. Load Current



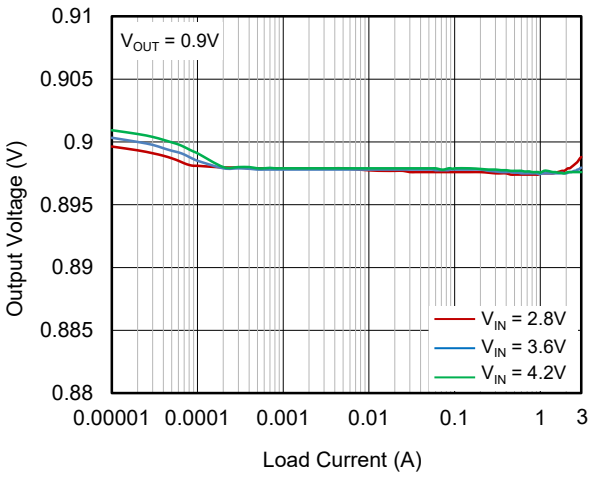
Efficiency vs. Load Current



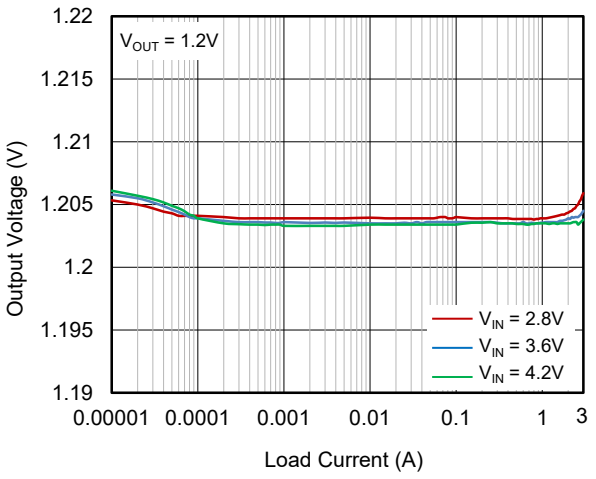
Efficiency vs. Load Current



Output Voltage vs. Load Current



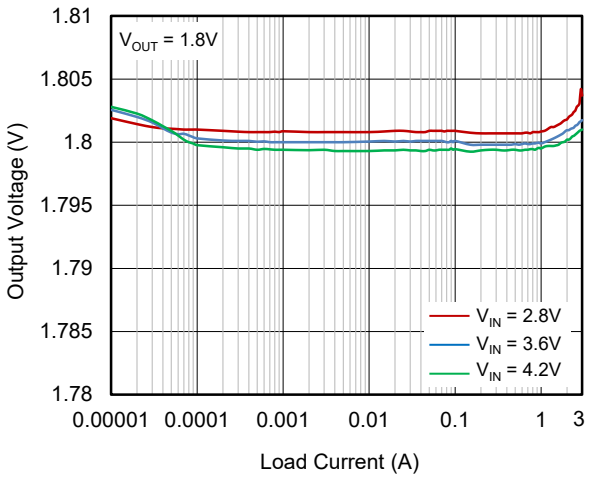
Output Voltage vs. Load Current



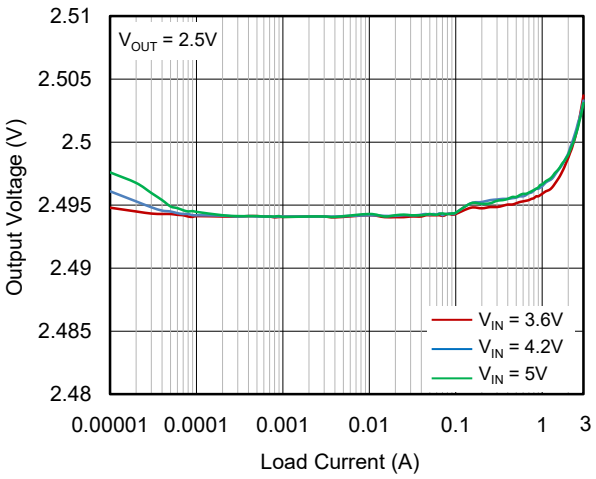
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

DCR = 22mΩ, unless otherwise noted.

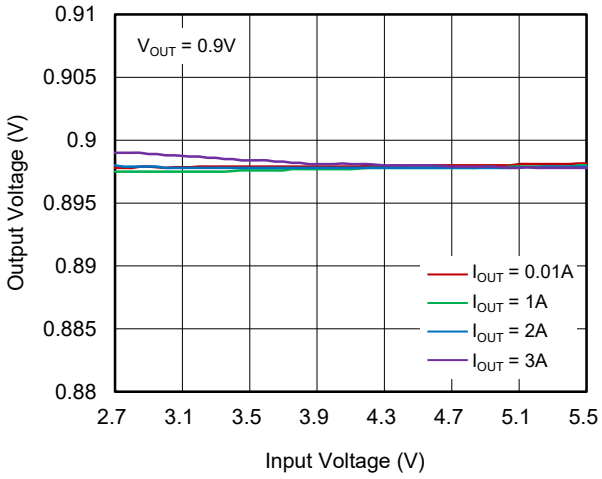
Output Voltage vs. Load Current



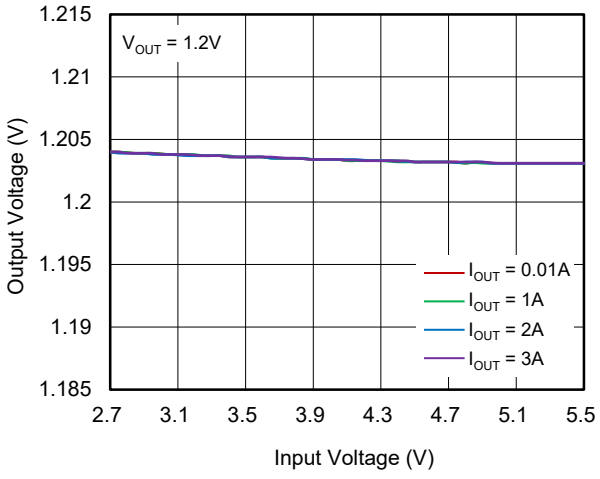
Output Voltage vs. Load Current



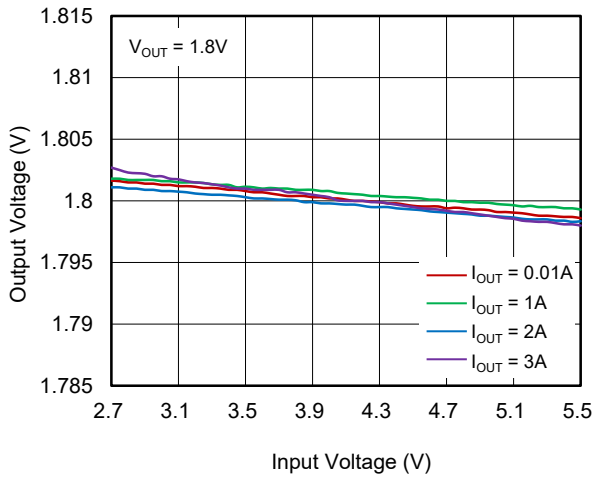
Output Voltage vs. Input Voltage



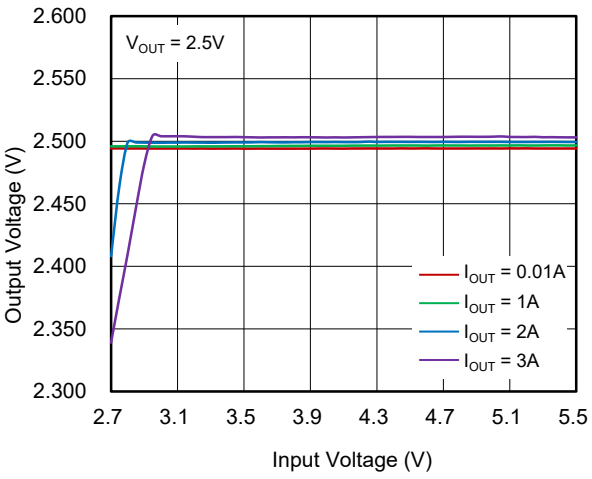
Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage

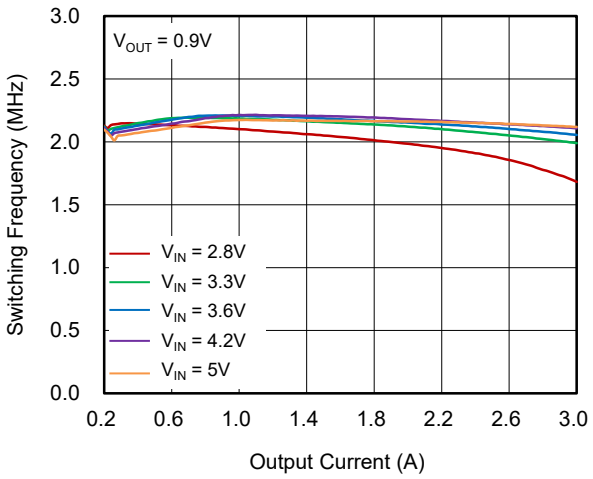


Output Voltage vs. Input Voltage

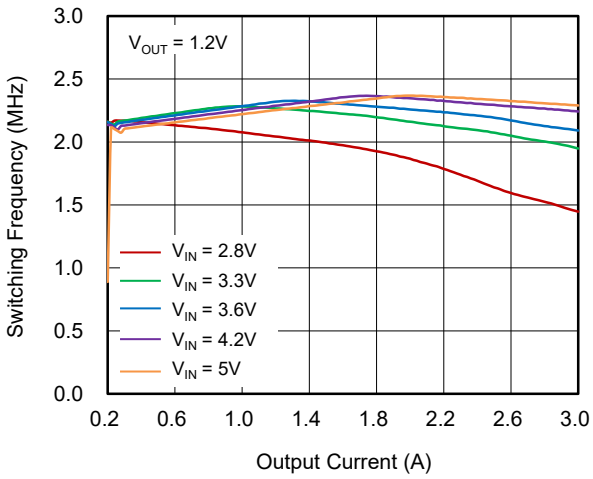


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

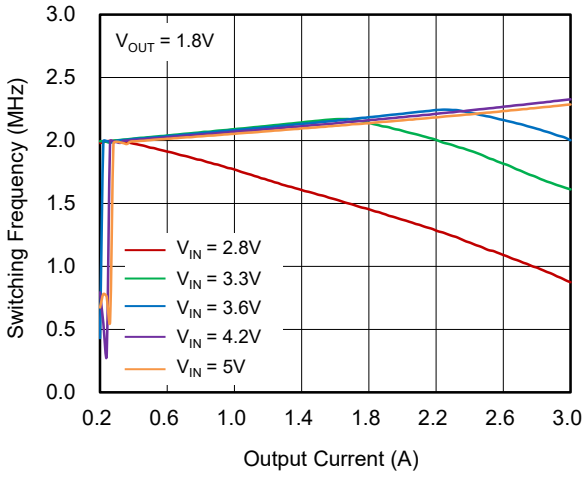
Switching Frequency vs. Output Current



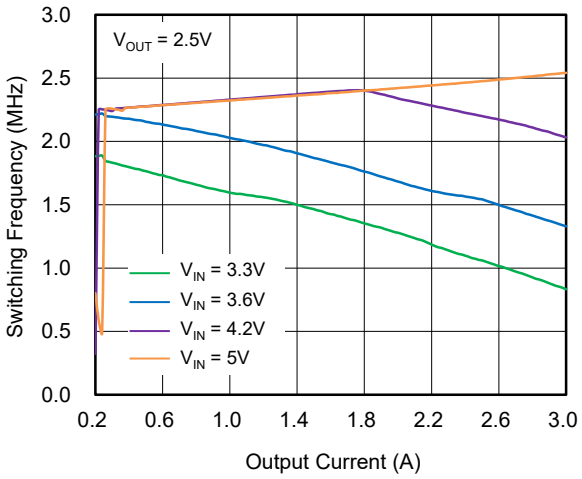
Switching Frequency vs. Output Current



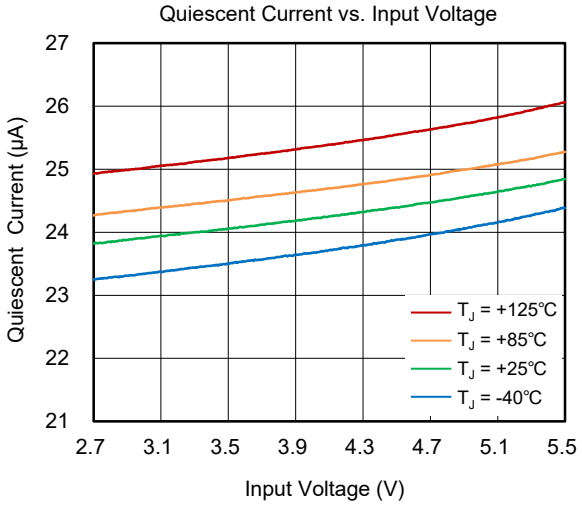
Switching Frequency vs. Output Current



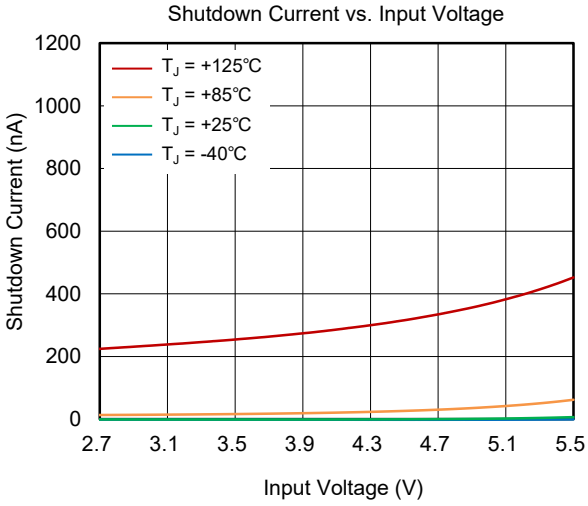
Switching Frequency vs. Output Current



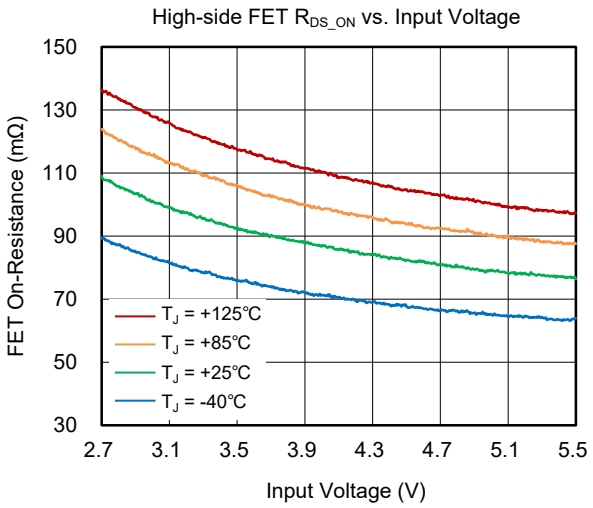
Quiescent Current vs. Input Voltage

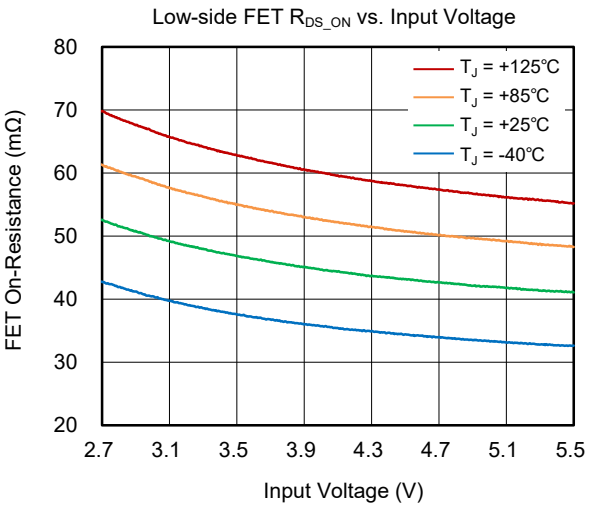


Shutdown Current vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

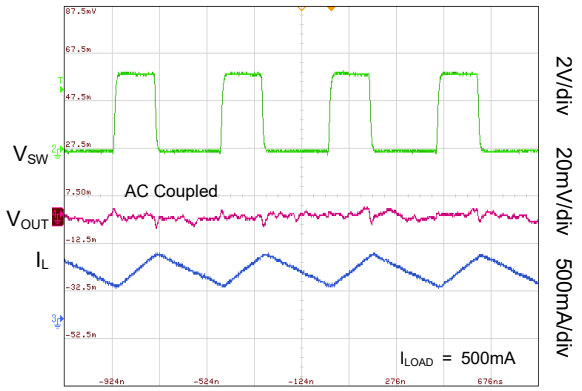




TYPICAL PERFORMANCE CHARACTERISTICS (continued)

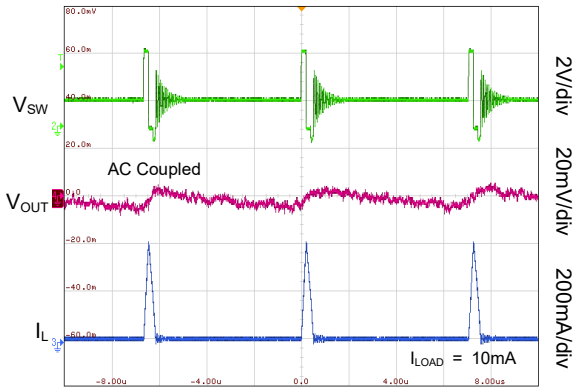
V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

Typical Application (PWM Mode)



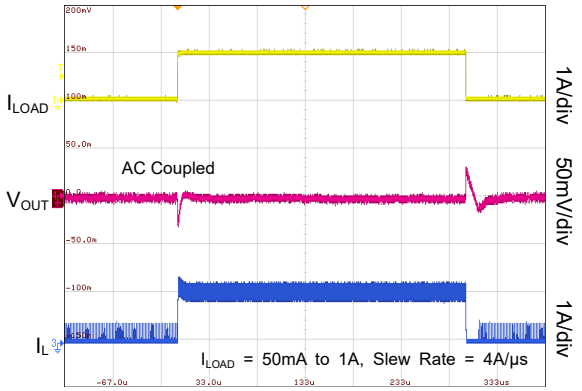
Time (200ns/div)

Typical Application (PSM Mode)



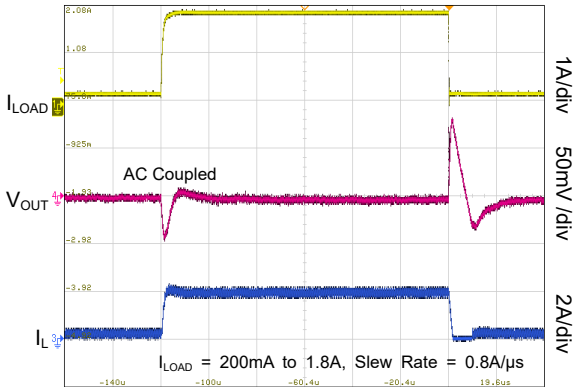
Time (2μs/div)

Load Transient



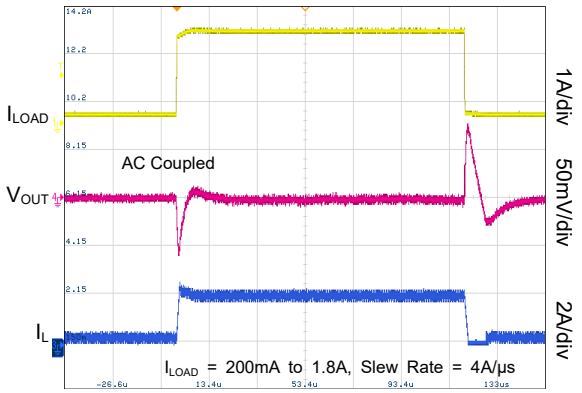
Time (50μs/div)

Load Transient



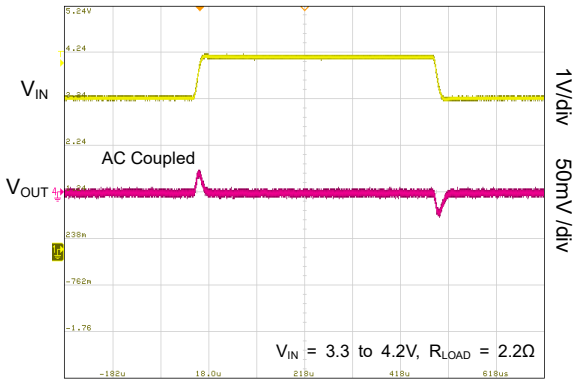
Time (20μs/div)

Load Transient



Time (20μs/div)

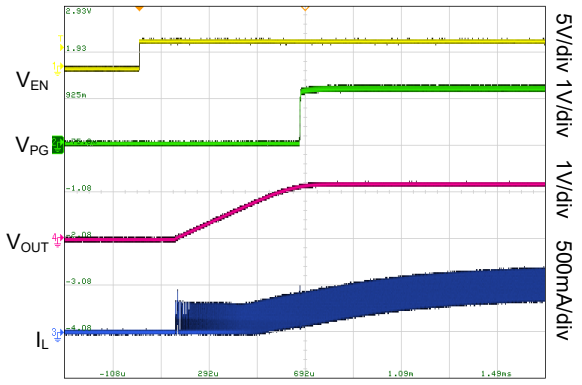
Line Transient



Time (100μs/div)

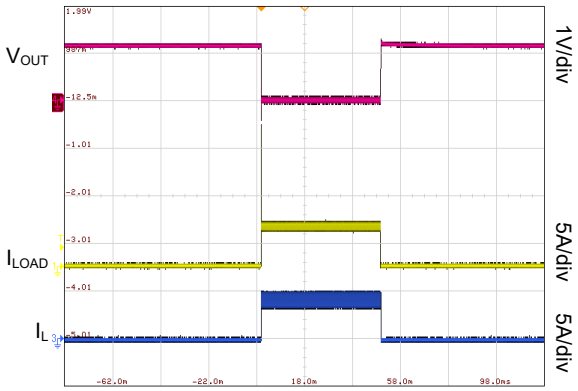
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Start-up (No Load)



Time (200μs/div)

Short-Circuit Recovery



Time (20ms/div)

FUNCTIONAL BLOCK DIAGRAM

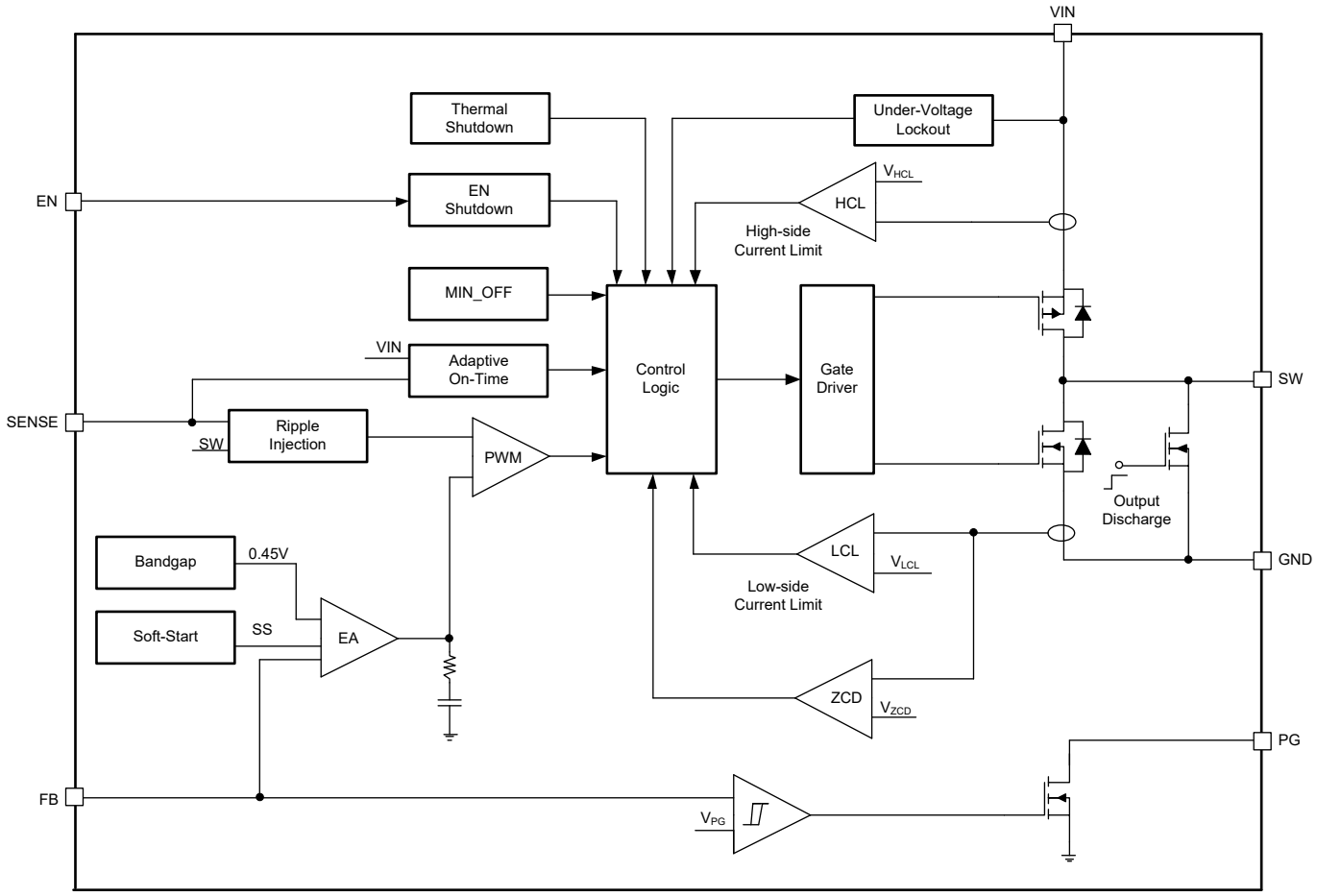


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61031 is a high-efficient Buck converter with AHP-COT architecture and advanced regulation topology.

At medium to heavy loads, the device works in pulse width modulation (PWM) mode. At light loads, it automatically switches to power-save mode (PSM). In PWM mode, the device works with a nominal switching frequency of 2MHz. When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 130mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Device Enable and Disable

A logic high input to EN pin activates the device, and a logic low disables the device. Do not leave it floating.

Power Good (PG)

The power good output of SGM61031 will be low in the condition that the output voltage is less than its nominal value. If the output exceeds 95% of the regulated voltage, the power good is in high-impedance state. If the output voltage is less than 90% of the regulated voltage, the power good is driven to low.

The PG pin is an open-drain output with a maximum of 0.5mA sink current. A pull-up resistor connecting to power good output is required. When the device is disabled, under-voltage lockout, or thermal shutdown, the PG pin is driven to High-Z (see Table 1). The PG signal connected to the EN pin of other converters can be used for multiple rails sequences. Leave the PG pin floating when not in use.

Table 1. Logic Table of PG Pin

Device Information		PG Logic Status	
		High-Z	Low
Enable (EN = High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} \leq V_{PG}$		√
Shutdown (EN = Low)		√	
UVLO	$0.7V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{JSD}$	√	
Power Supply Removal	$V_{IN} < 0.7V$	Undefined	

Low Dropout Operation (100% Duty Cycle)

The device provides low input-to-output voltage drop by going into 100% duty cycle mode. In this mode, the high-side MOSFET is constantly turned on and the low-side MOSFET is turned off. This function can increase the operation time to the utmost extent for battery powered applications. To maintain an appropriate output voltage, the minimum input voltage is calculated by:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage.
- I_{OUT_MAX} is the maximum output current.
- R_{DSON} is the high-side MOSFET on-resistance.
- R_L is the inductor ohmic resistance.

Output Discharge

Whenever the device is disabled by enable, thermal shutdown or under-voltage lockout, the output is discharged by the SW pin through a typical discharge resistor of R_{DIS}.

DETAILED DESCRIPTION (continued)

Soft-Start

When EN pin is set to logic high and after about 150μs delay, the device starts switching and V_{OUT} increases with 600μs (TYP) internal soft-start circuit.

Inductor Current Limit

If there is over-current or short-circuit, the device implements an inductor current limit. Both the peak current of high-side and valley current of low-side power MOSFETs are limited to protect the device. The high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current when the high-side switch current limit is triggered. The low-side MOSFET is turned off and the high-side switch is turned on again when the inductor current drops to the low-side switch current limit. It repeats until the inductor current falls below the high-side switch current limit. The actual current limit value may be larger than the static current limit due to internal propagation delays.

Power-Save Mode

Once the load current decreases, the SGM61031 will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous. Then a fixed on-time architecture is activated and the typical on-time is t_{ON} = 500ns × (V_{OUT}/V_{IN}).

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds the typical T_{JSD} (+160℃ TYP), the switching will stop. When the device temperature drops below the threshold minus hysteresis, the switching will resume automatically.

APPLICATION INFORMATION

The SGM61031 is a synchronous Buck converter with output voltage adjusted by feedback dividers. Taking SGM61031 typical application as a reference, the following sections discuss the design of external components and the way to achieve the application.

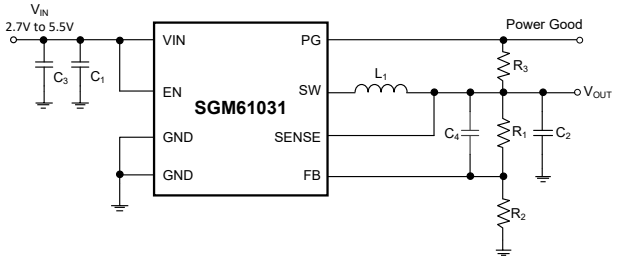


Figure 3. Typical Application Schematic

Design Requirements

For this design example, use Table 2 as the input parameters.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage Range	2.7V to 5.5V
Output Voltage	1.2V
Transient Response	±5% V_{OUT}
Input Voltage Ripple	400mV
Output Voltage Ripple	30mV
Output Current Rating	3A
Operating Frequency	2MHz

Design Details

Table 3 shows the components included in this example.

Table 3. Components List

Reference	Description	Manufacturer
C_1	1μF, Ceramic Capacitor, 10V, X5R, Size 0603	Std
C_2	22μF, Ceramic Capacitor, 16V, X5R, Size 0805	Std
C_3		
C_4	20pF, Ceramic Capacitor, 50V, C0G, Size 0603 (Option)	Std
L_1	1μH, DCR = 22mΩ, I_{SAT} = 9A, P/N:74437324010	WE
R_1	64.9kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_2	39kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_3	178kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std

Adjustable Output Voltage

An external resistor divider connected to FB pin is used for setting the output voltage. Through adjusting R_1 and R_2, the output voltage can be programmed to the desired value. Calculate R_1 and R_2 with Equation 2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.45V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

R_2 should be less than 40kΩ for higher accuracy. Make sure that the current flowing through R_2 is at least 100 times greater than the current of FB pin. A lower value of R_2 increases the robustness against noise injection, and higher values reduce the input current.

A feed-forward capacitor (C_4) is recommended to improve the performance of smooth transition into power-save mode and reduce undershoot during load transient. 10pF to 20pF is enough for typical applications.

Inductor Selection

Equation 3 is conventionally used to calculate the output inductance of a Buck converter. The inductor should be selected by its value and the saturation current. The saturation current of inductor should be higher than I_{L_MAX} in Equation 3, and sufficient margin should be reserved. Typically, the current above high-side current limit is enough, and a 10% to 30% ripple current is selected to calculate the inductance. Larger inductor can reduce the ripple current, but with an increasing response time.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where:

- I_{OUT_MAX} is the maximum output current.
- ΔI_L is the inductor current ripple.
- f_{SW} is the switching frequency.
- L is the inductor value.

APPLICATION INFORMATION (continued)

Capacitor Selection

For input capacitor design, a X5R/X7R dielectric ceramic capacitor should be selected for its low ESR and high frequency performance. 10μF is enough for most applications. The voltage rating of input capacitor must be considered for its significant bias effect. The input ripple voltage can be calculated from Equation 4.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (4)$$

The ripple current rating of input capacitor should be greater than I_{CIN_RMS} in Equation 5 and the maximum value occurs at 50% duty cycle. A 0.1μF capacitor is suggested to add for further input decoupling of device.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN}-V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For output capacitor design, output ripple, transient response and loop stability should be considered. Minimum capacitance of output ripple criteria can be calculated from Equation 6.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (6)$$

Both the input and output capacitors should be placed as close to VIN, SENSE and GND pins as possible to reduce noise caused by PCB parasitic parameters.

Higher nominal capacitance value or rating voltage must be chosen due to aging, temperature, and significant DC bias derating of the ceramic capacitors. In this example, 22μF/16V X5R ceramic capacitor is used as input and output capacitors.

Output Filter Design

To simplify customer's design process, the inductor and output capacitor combinations are recommended in Table 4.

Table 4. Inductor and Capacitor Combinations

L (μH) (1)	C_{OUT} (μF) (2)		
	10μF	22μF	2×22μF
0.47	(3)	(4)	√
1	√	√(5)(6)	√
2.2	√	√	(7)

NOTES:

1. Expected inductor tolerance and current de-rating. Effective inductance has +20% and -30% variation.

2. Expected capacitance tolerance and bias voltage de-rating. Effective capacitance has +20% and -50% variation.

3. Not recommended at low output voltage.

4. Not recommended to use feed-forward capacitor at low output voltage.

5. "√" means the recommended filter combinations.

6. Filter combination in typical application.

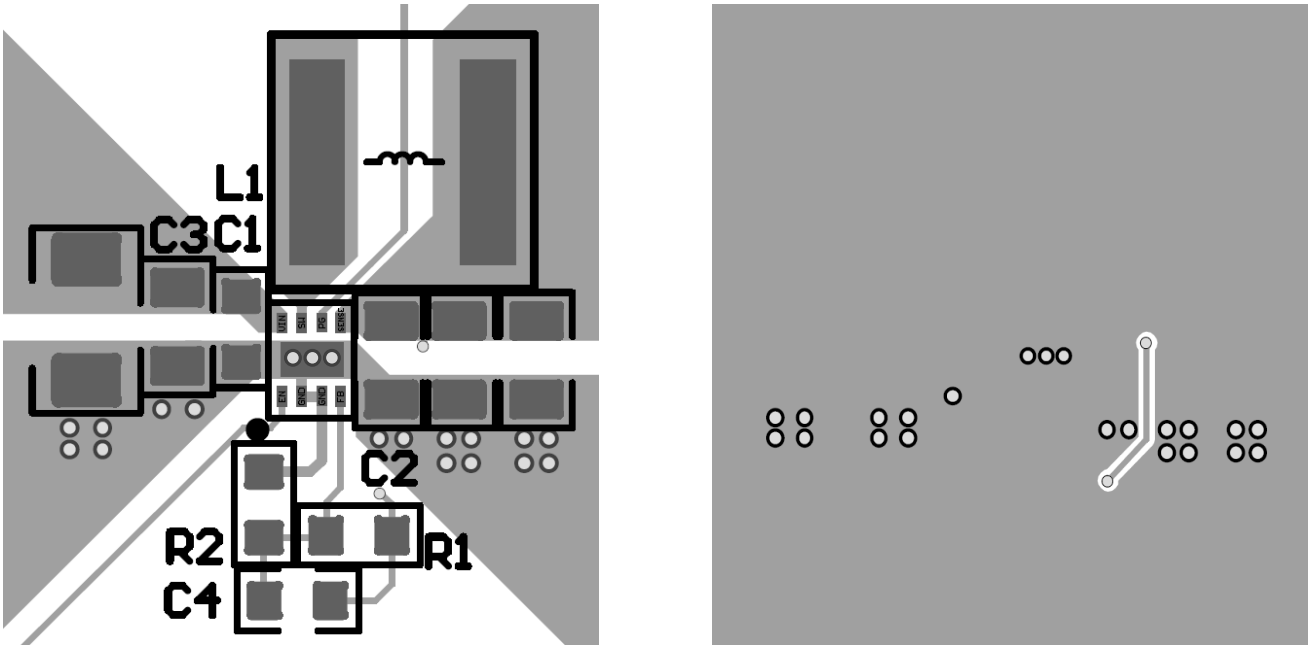
7. Recommended to use feed-forward capacitor.

LAYOUT Guidelines

Good PCB layout is the key factor for high performance operation of a device regarding the stability, regulation, efficiency and other performance measures.

A list of guidelines for designing the PCB layout of SGM61031 is provided below:

- Place the power components close together and connect them with short and wide routes. The low-side of the capacitors must be connected to GND properly to avoid potential shift.
- Signal traces are connected to the FB and SENSE pins. Connect the inductor with a short trace. Keep the traces away from SW nodes.
- Typical suggested layout is provided in Figure 4.



Top Layer Bottom Layer

Figure 4. PCB Layout

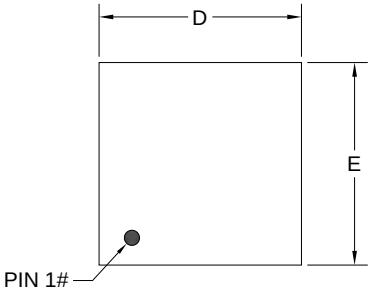
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

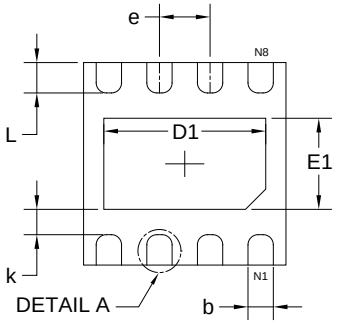
Changes from Original (OCTOBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

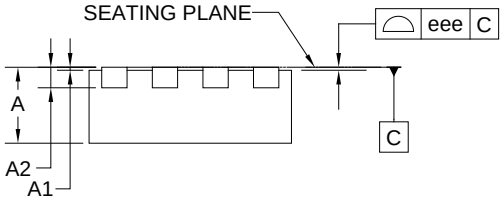
TDFN-2×2-8AL



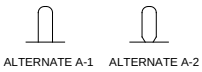
TOP VIEW



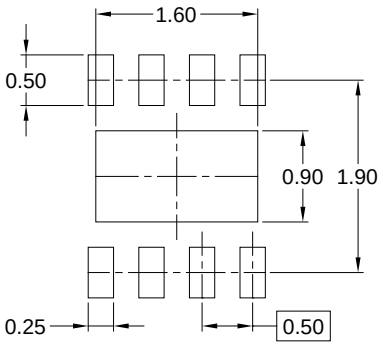
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



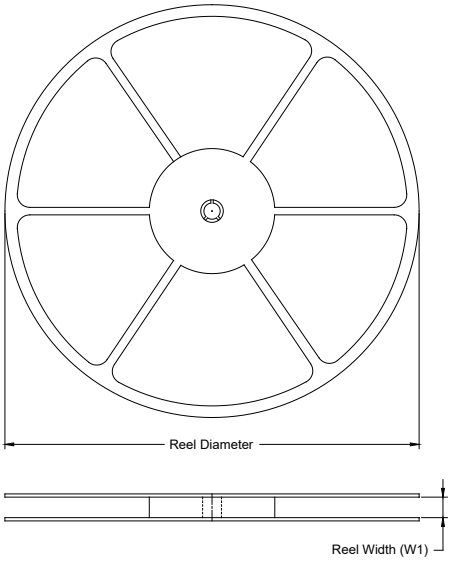
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	1.900	2.000	2.100
D1	1.450	1.600	1.700
E	1.900	2.000	2.100
E1	0.750	0.900	1.000
k	0.150	0.250	0.350
e	0.450	0.500	0.550
L	0.200	0.300	0.400
eee	0.080		

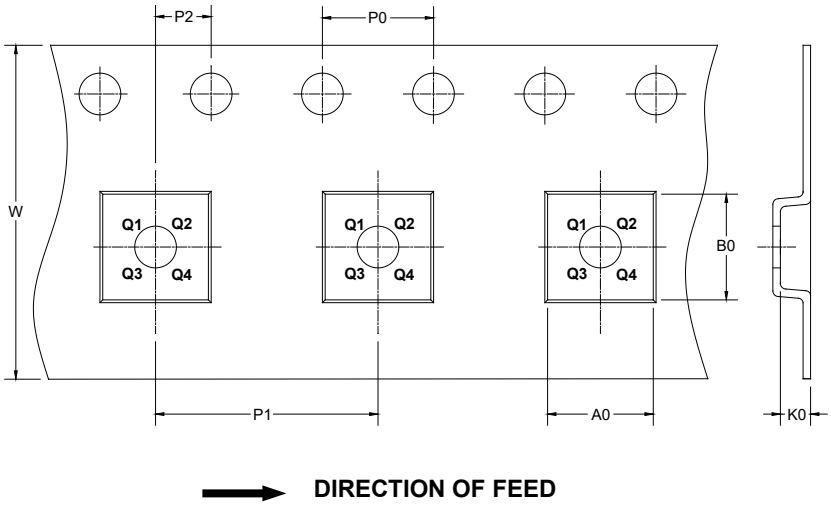
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

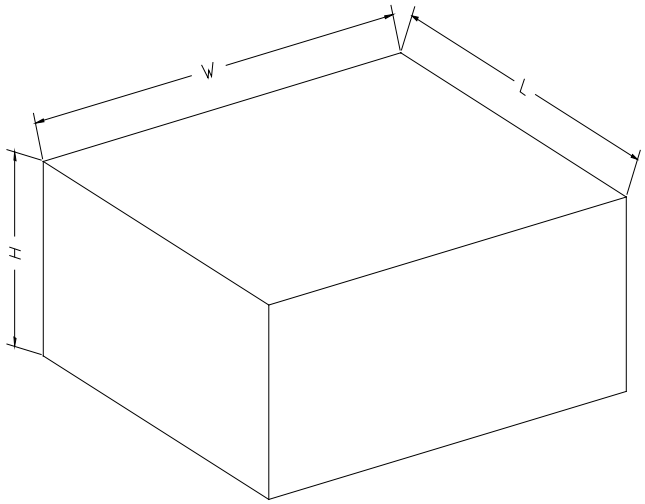
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002