SGM61412
1.2MHz, 1.2A, 42V Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61412 is a high frequency, synchronous Buck converter with integrated switches. It can deliver up to 1.2A to the output over a wide input voltage range of 4.5V to 42V. It is suitable for various industrial applications with high input voltage or for power conditioning from unregulated sources. Moreover, the low 55μA quiescent current and ultra-low shutdown current of only 1.2μA make it a suitable choice for battery-powered applications.

SGM61412 features high efficiency over a wide load range achieved by scaling down the switching frequency at light load condition to reduce switching and gate driving losses. Other features include internal compensation, internal monotonic soft-start even with pre-biased output and fast loop response due to the peak-current mode controller. Switching at 1.2MHz, the SGM61412 can prevent EMI noise problems, such as the ones found in AM radio, ADSL and PLC applications.

Protection features include current limit and short-circuit protection, thermal shutdown with auto recovery and output over-voltage protection. Frequency fold-back helps prevent inductor current runaway during startup.

The SGM61412 is available in a Green TSOT-23-6 package. It operates over a wide ambient temperature range of -40℃ to +125℃.

FEATURES

- **Wide 4.5V to 42V Input Voltage Range**
- **Current Output up to 1.2A**
- **1.2MHz Switching Frequency**
- **0.83V Internal Reference**
- **SGM61412A:PSM and PWM Mode**
- **SGM61412B: PFM and PWM Mode**
- **Low Quiescent Current: 55μA (TYP)**
- **Ultra-Low Shutdown Current: 1.2μA (TYP)**
- **0.83V to 20V Adjustable Output Voltage**
- **Internal Compensation and Soft-Start**
- **Precision Enable Function with UVLO Setting**
- **Monotonic Startup with Pre-biased Output**
- **Thermal Shutdown Protection**
- **Available in a Green TSOT-23-6 Package**
- **-40℃ to +125℃ Operating Temperature Range**

APPLICATIONS

High Voltage Power Conversions
Industrial Power Systems
Distributed Power Systems
Battery Powered Systems
Power Meters

TYPICAL APPLICATION

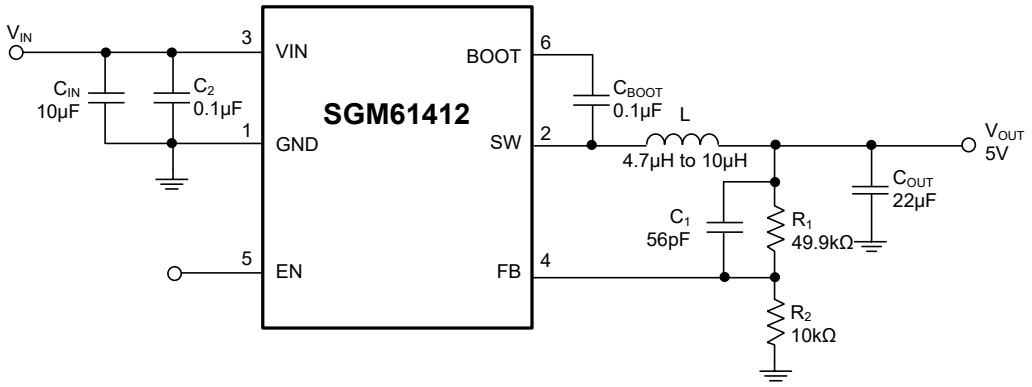


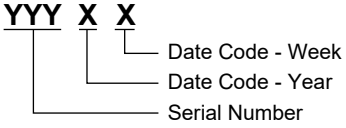
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61412A	TSOT-23-6	-40℃ to +125℃	SGM61412AXTN6G/TR	CN1XX	Tape and Reel, 3000
SGM61412B	TSOT-23-6	-40℃ to +125℃	SGM61412BXTN6G/TR	CN2XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN to GND ..... -0.3V to 45V
EN to GND ..... -0.3V to V_{IN} + 0.3V
FB to GND ..... -0.3V to 5.5V
SW to GND ..... -0.3V to V_{IN} + 0.3V
BOOT to SW ..... -0.3V to 5.5V
Package Thermal Resistance
TSOT-23-6, θ_{JA} ..... 132℃/W
TSOT-23-6, θ_{JB} ..... 31.7℃/W
TSOT-23-6, θ_{JC} ..... 61.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage Range ..... 4.5V to 42V
Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

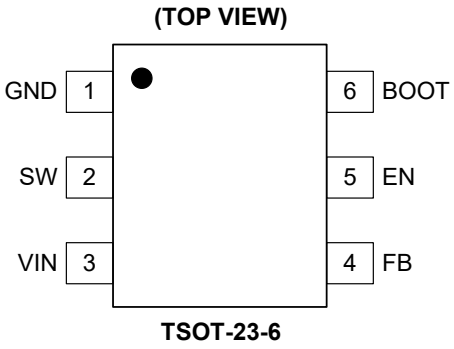
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GND	Ground Pin. It is the reference for input and the regulated output voltages. Special layout considerations are required.
2	SW	Switching Node Output. Switching node of the internal power converter and should be connect to the output inductor and bootstrap capacitor. This node should be kept small on the PCB to minimize capacitive coupling, noise coupling and radiation.
3	VIN	Power Supply Input Pin. This pin is connected to the input supply voltage and powers the internal control circuitry. VIN voltage is monitored by a UVLO lockout comparator. VIN is also connected to the drain of the converter high-side switch. Due to power switching, this pin has high di/dt transition edges and must be decoupled to the GND by input capacitors as close as possible to the GND pin to minimize the parasitic inductances.
4	FB	Feedback Input. Feedback pin for programming the output voltage. The SGM61412 regulates the FB pin to 0.83V. Connect the midpoint of the feedback resistor divider.
5	EN	Active High Enable Input. Internal pull-up current source. Pull below 0.9V to disable the device. Float to enable. Adjust the input under-voltage lockout with a resistor divider.
6	BOOT	Bootstrap Input. Bootstrap pin is used to provide a drive voltage, higher than the input voltage, to the high-side power switch. Place a 0.1μF Boost capacitor (C_{BOOT}) as close as possible to the IC between this pin and SW pin.

ELECTRICAL CHARACTERISTICS

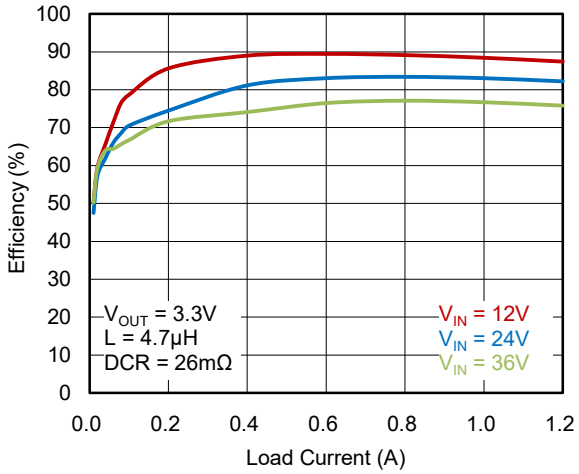
(V_{IN} = 24V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Input Voltage		V_{IN}		4.5		42	V
Under-Voltage Lockout Threshold		V_{UVLO}		4.00	4.25	4.50	V
Under-Voltage Lockout Threshold Hysteresis		V_{UVLO_HYS}			320		mV
VIN Quiescent Current	Shutdown	I_Q	$V_{EN/UV}$ = 0V		1.2	2.0	μA
	Sleep Mode		$V_{EN/UV}$ = 2V, non-switching, V_{IN} ≤ 36V SGM61412A		55	85	μA
			$V_{EN/UV}$ = 2V, non-switching, V_{IN} ≤ 36V SGM61412B		1.95	2.8	mA
Feedback Reference Voltage		V_{FB}		0.805	0.830	0.855	V
Feedback Pin Input Current		I_{FB}	V_{FB} = 1V		0.1	1	μA
Minimum High-side Switch On-Time		t_{ON_MIN}	I_{LOAD} = 1A		100		ns
Minimum High-side Switch Off-Time		t_{OFF_MIN}	I_{LOAD} = 1A		120		ns
Switching Frequency		f_{SW}		0.85	1.2	1.55	MHz
Switch Leakage Current		I_{SW_H}	V_{SW} = 42V		0.1	1	μA
		I_{SW_L}	V_{SW} = 0V		0.1	1	μA
High-side NMOS Current Limit		I_{LIM}	T_J = +25℃	1.6	2.0	2.4	A
High-side NMOS On-Resistance		R_{DSON}	I_{LOAD} = 0.1A		230	410	mΩ
Low-side NMOS On-Resistance			I_{LOAD} = 0.1A		130	230	mΩ
EN Input High Voltage		V_{IH}	V_{EN} rising	1.2	1.3	1.4	V
EN Input Low Voltage		V_{IL}	V_{EN} falling	0.8	0.9	1.0	V
EN Threshold, Hysteresis		V_{EN_HYS}			400		mV
Enable Leakage Current		I_{EN}	V_{EN} = 42V		0.1	1	μA
			V_{EN} = 0V	-1	-0.4		μA
Thermal Shutdown		T_{SHDN}			155		℃
Thermal Shutdown Hysteresis		T_{HYS}			30		℃

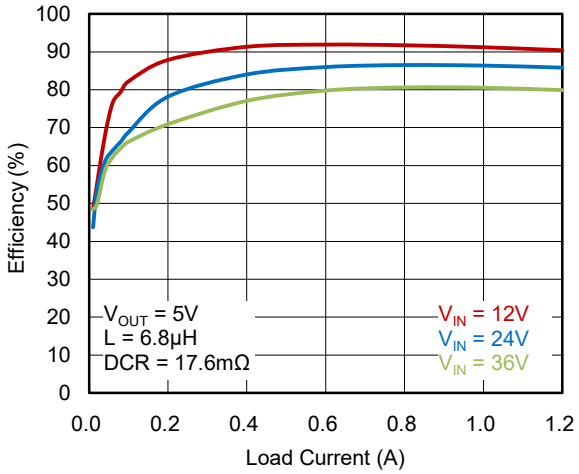
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, L = 6.8μH and C_{OUT} = 22μF, unless otherwise noted.

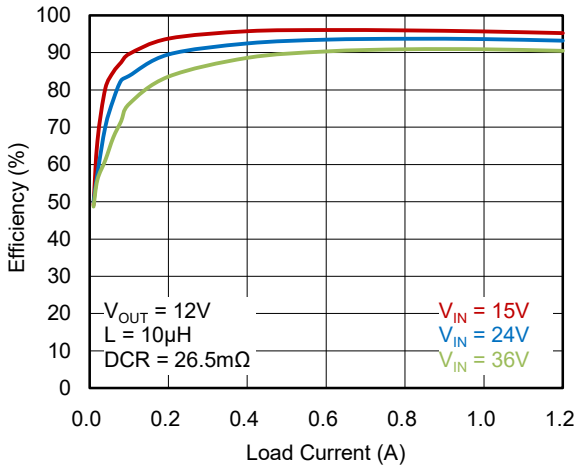
Efficiency vs. Load Current



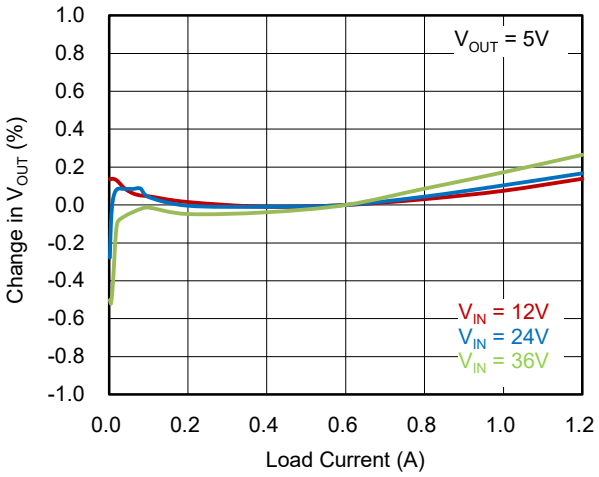
Efficiency vs. Load Current



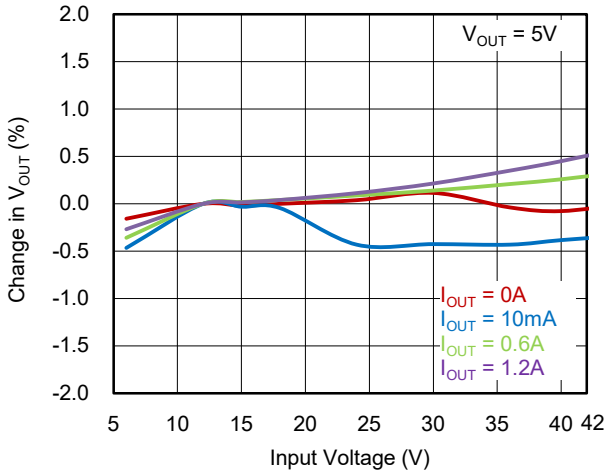
Efficiency vs. Load Current



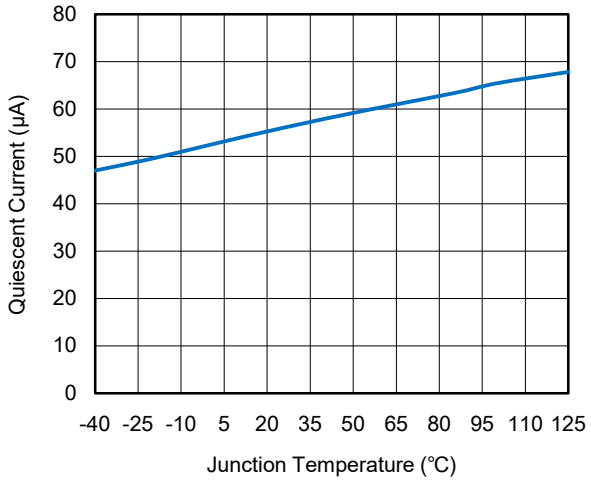
Load Regulation



Line Regulation



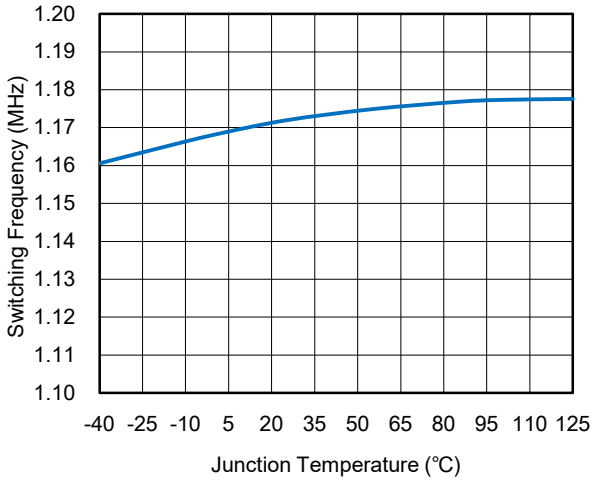
Quiescent Current vs. Temperature



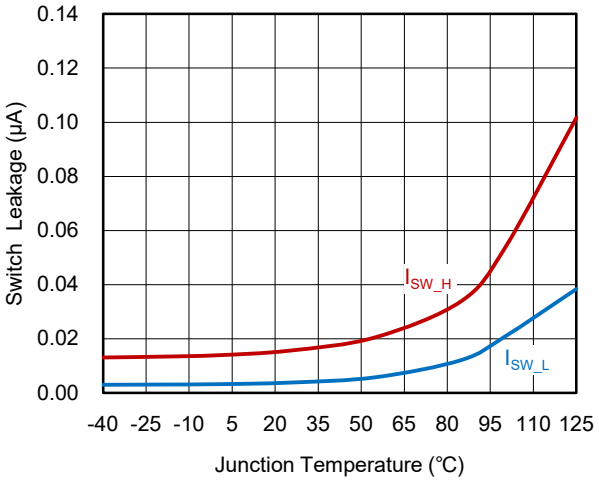
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, L = 6.8μH and C_{OUT} = 22μF, unless otherwise noted.

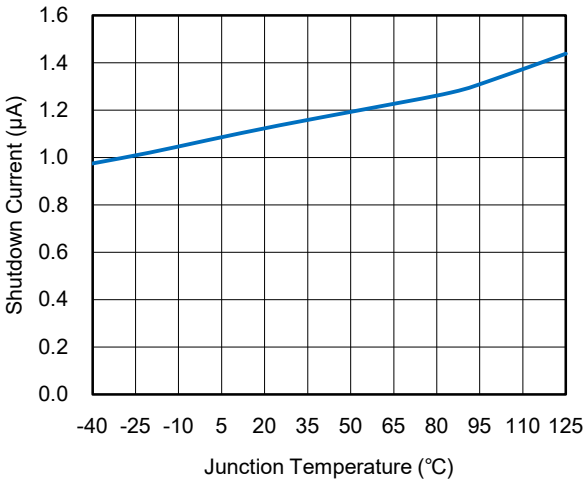
Switching Frequency vs. Temperature



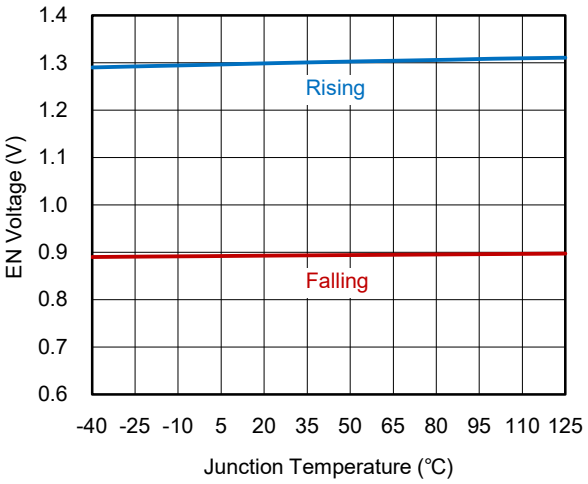
Switch Leakage vs. Temperature



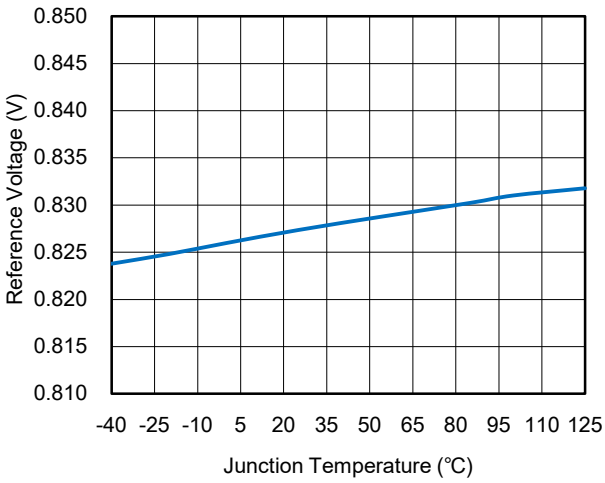
Shutdown Current vs. Temperature



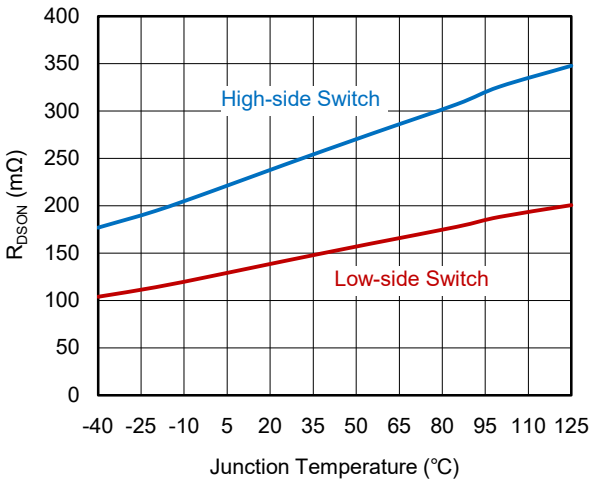
EN Voltage vs. Temperature



Reference Voltage vs. Temperature



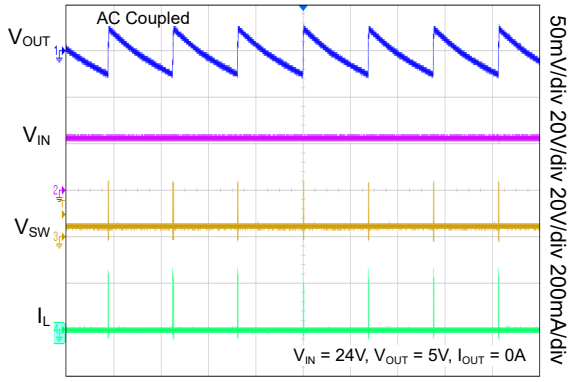
R_{DSON} vs. Temperature



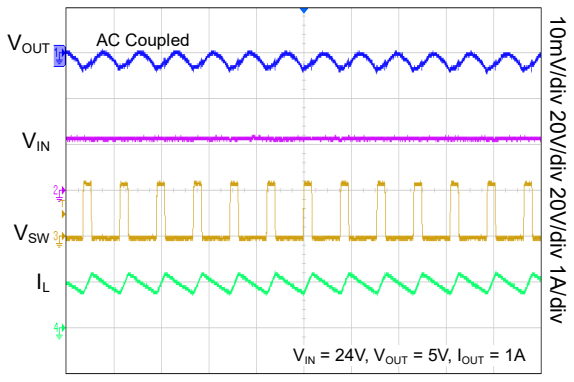
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, L = 6.8μH and C_{OUT} = 22μF, unless otherwise noted.

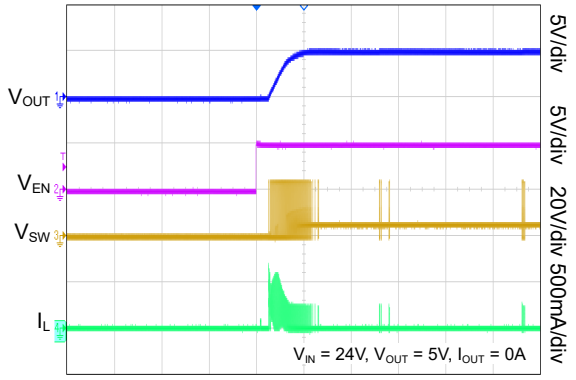
Output Voltage Ripple



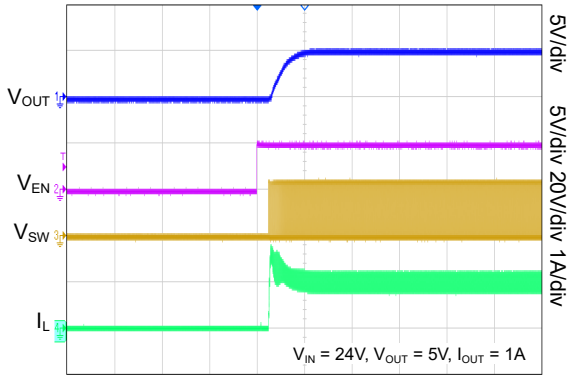
Output Voltage Ripple



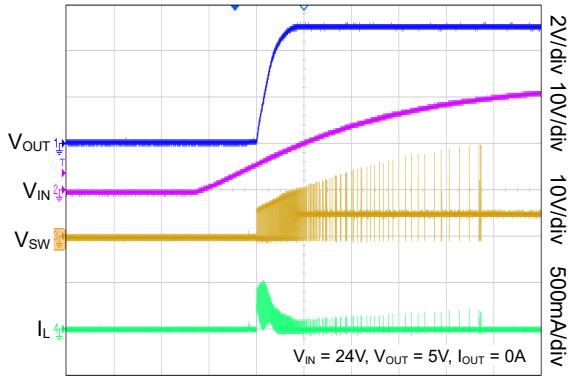
Enable Startup



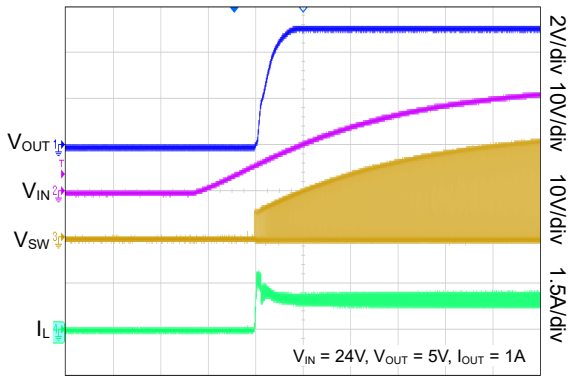
Enable Startup



VIN Startup



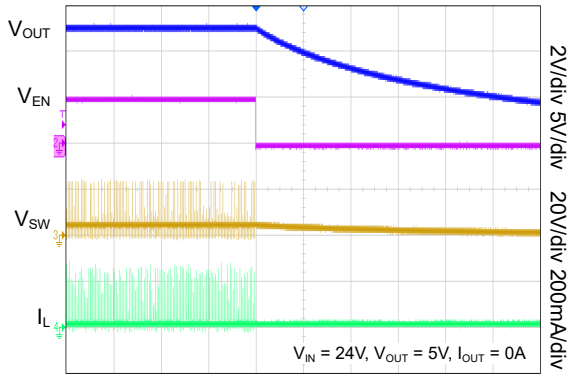
VIN Startup



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

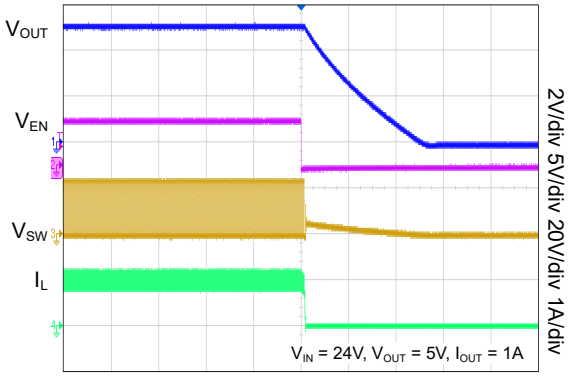
T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, L = 6.8μH and C_{OUT} = 22μF, unless otherwise noted.

Enable Shutdown



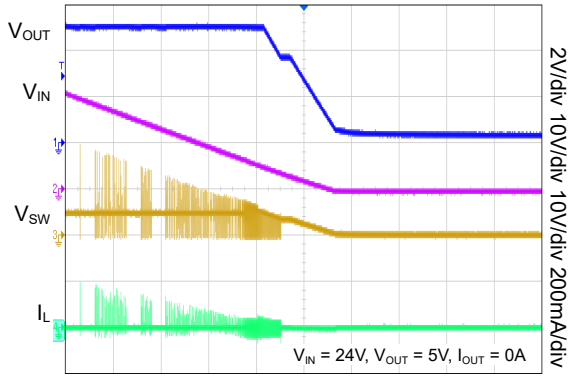
Time (200ms/div)

Enable Shutdown



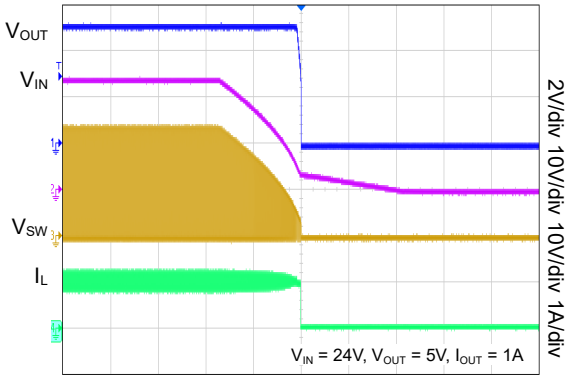
Time (50μs/div)

VIN Shutdown



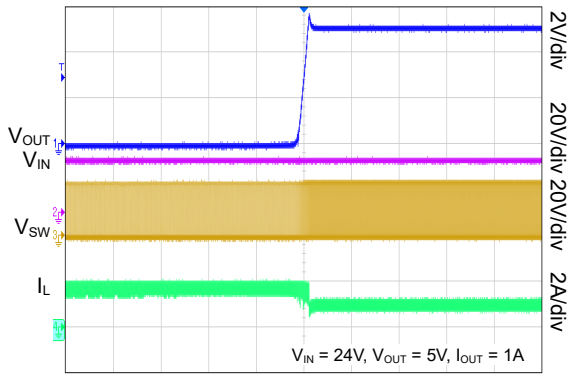
Time (20ms/div)

VIN Shutdown



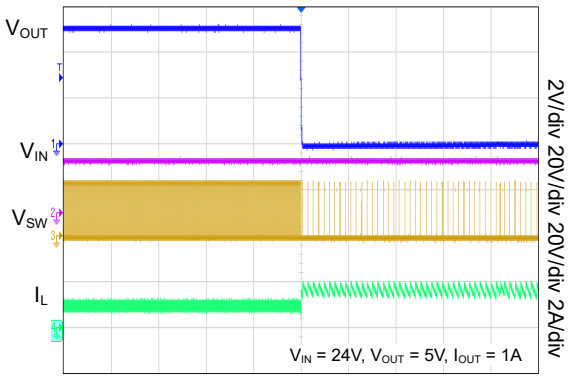
Time (10ms/div)

Short-Circuit Recovery



Time (1ms/div)

Short-Circuit Entry

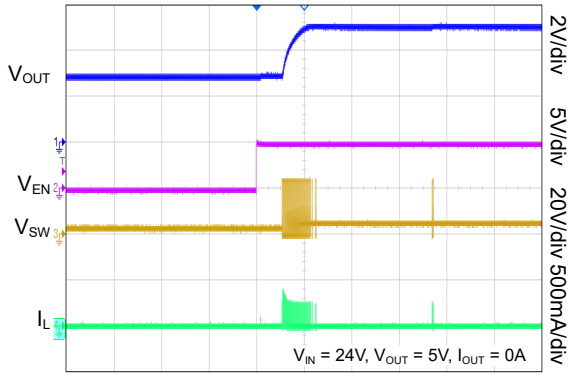


Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

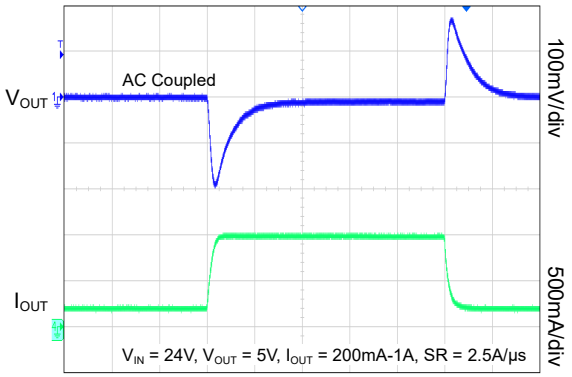
T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, L = 6.8μH and C_{OUT} = 22μF, unless otherwise noted.

Pre-biased Startup



Time (1ms/div)

Load Transient Response



Time (100μs/div)

FUNCTIONAL BLOCK DIAGRAM

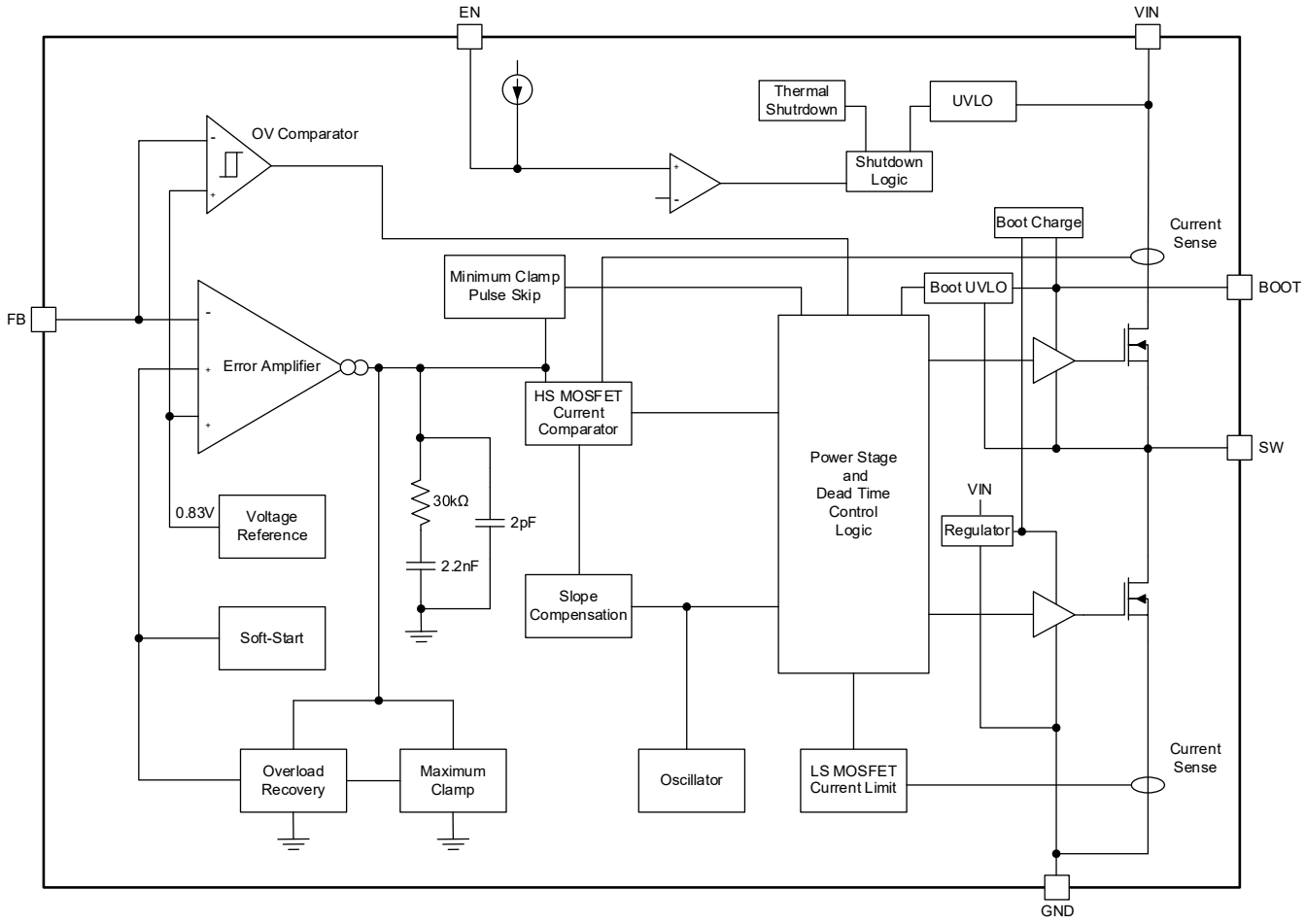


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61412 is an internally compensated wide input range current mode controlled synchronous Buck converter. It is designed for high reliability and is particularly suitable for power conditioning from unregulated sources or battery-powered applications that need low sleep and shutdown currents. It also features a power-save mode in which operating frequency is adaptively reduced under light load condition to reduce switching and gate losses and keep high efficiency. At no load and with switching stopped, the total operating current is approximately 55μA. If the device is disabled, the total consumption is typically 1.2μA.

Figure 2 shows the functional block diagram of the SGM61412. The two integrated MOSFET switches of the power stage are both over-current protected and can provide up to 1.2A of continuous current for the load. Current limit of the switches also prevents inductor current runaway. The converter switches are optimized for high efficiency at low duty cycle.

At the beginning of each switching cycle, the high-side switch is turned on. This is the time that feedback voltage (V_{FB}) is below the reference voltage (V_{REF}) and power must be delivered to the output. After the on-period, the high-side switch is turned off and the low-side switch is turned on until the end of switching cycle. For reliable operation and preventing shoot through, a short dead time is always inserted between gate pulses of the converter complimentary switches. During dead time, both switch gates are kept off.

The device is designed for safe monotonic start-up even if the output is pre-biased.

If the junction temperature exceeds a maximum threshold (T_{SHDN}, typically +155℃), thermal shutdown protection will happen and switching will stop. The device will automatically recover with soft-start when the junction temperature drops back well below the trip point. This hysteresis is typically 30℃.

The SGM61412 has current limit on both the high-side and low-side MOSFET switches. When current limit is activated frequency fold-back is also activated. This occurs in the case of output overload or short circuit. Note that SGM61412 will continue to provide its maximum output current and will not shut down. In such a case, the junction temperature may rise rapidly and trigger thermal shutdown.

During initial power-up of the device (soft-start), current limit and frequency fold-back are activated to prevent inductor current runaway while the output capacitor is charging to the desired V_{OUT}.

Peak-Current Mode (PWM Control)

Figure 2 shows the functional block diagram and Figure 3 shows the switching node operating waveforms of the SGM61412. Switching node voltage is generated by controlling the duty cycles of the complementary high-side and low-side switches. The high-side duty cycle is used as control parameter of the Buck converter to regulate output voltage and is defined as: $D = t_{ON}/t_{SW}$, where t_{ON} is the high-side switch on-time and t_{SW} is the switching period. When high-side switch is turned on, the SW pin voltage sharply rises towards V_{IN}, and the inductor current (I_L) starts ramping up with (V_{IN} - V_{OUT})/L slope. When high-side switch is turned off, the low-side switch is turned on after a very short dead time to avoid shoot-through, and I_L ramps down with -V_{OUT}/L slope. In ideal case, the output voltage is proportional to the input voltage and duty cycle ($D = V_{OUT}/V_{IN}$) if component parasitics are ignored.

The SGM61412 employs fixed-frequency, peak-current mode control in continuous conduction mode (CCM) (when inductor minimum current is above zero). In light load condition (when the inductor current reaches zero) the SGM61412 will enter discontinuous conduction mode (DCM) and the control mode will change to shift-frequency, peak-current mode to reduce the switching frequency and the associated switching and gate driving losses (power-save mode).

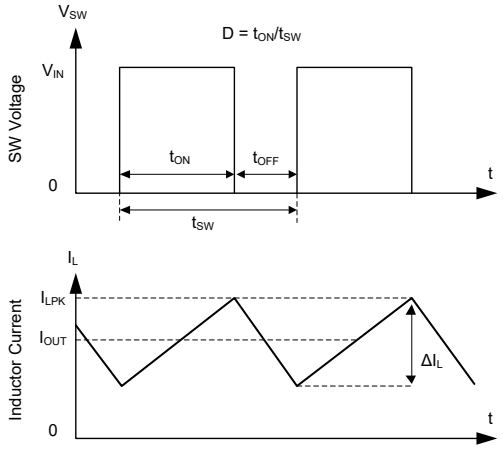


Figure 3. Converter Switching Waveforms in CCM

DETAILED DESCRIPTION (continued)

In CCM, SGM61412 operates at fixed-frequency using peak-current mode control scheme. The controller has an outer voltage feedback loop to get accurate DC voltage regulation. The output of the outer loop is fed to an inner peak-current control loop as reference command that adjusts the peak- current of the inductor. The inductor peak-current is sensed from the high-side switch and is compared to the peak-current reference to control the duty cycle. In other words, as soon as the inductor current reaches the reference peak-current determined by voltage loop, the high-side switch is turned off and the low-side switch is turned on after dead time.

The internally compensated voltage feedback loop allows for simpler design, fewer external components, and stable operation with almost any combination of output capacitors.

Power-Save Mode (SGM61412A Only)

The SGM61412A/B operate in PWM mode to provide lower ripple at heavy load. The SGM61412A operates in power-save mode (PSM) at light load to boost light load efficiency by reducing switching and gate drive losses. When the inductor peak-current is low and the internal V_{COMP} falls to the internal threshold, the device will enter PSM. After entering PSM for a delay time, some modules are shut down to minimum quiescent current. The high-side MOSFET will not switch until the output voltage falls for the internal V_{COMP} to rise above the internal threshold. Since the integrated current comparator catches the inductor peak-current only, the average load current entering PSM varies with the applications and external output filters.

Pulse Frequency Mode (SGM61412B Only)

As the load current decreases, the SGM61412B enters pulse frequency mode (PFM). When the inductor peak-current is low and the internal V_{COMP} falls to the internal threshold, the device will enter PFM. During PFM, when output feedback voltage V_{FB} falls below 0.83V typically, the device starts a PFM current pulse. The high-side MOSFET switch is turned on, and the inductor current ramps up. As the inductor peak-current rise for the current sense voltage V_{SENSE} reaches the internal threshold, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero. The converter effectively delivers a current to the output capacitor and the load. The resulting PFM frequency mainly depends on the load current. The lighter the load, the slower the output voltage drops, and the lower switching frequency. Lower switching frequency reduces the switching and gate drive losses, and improves the efficiency significantly. The PFM is left and PWM mode entered in case the output current rise for the internal V_{COMP} to rise above the internal threshold.

Floating Driver and Bootstrap Charging UVLO Protection

The high-side MOSFET driver is powered by a floating supply provided by an external bootstrap capacitor. The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between BOOT and SW nodes is below regulation, a PMOS pass transistor is turned on and connected VIN and BOOT pins internally, otherwise it will be turned off. The power supply for the floating driver has its own UVLO protection. The rising UVLO threshold is about 4.25V and with 320mV hysteresis; the falling threshold is about 3.93V. In case of UVLO, the reference voltage of the controller is reset to zero and after recovery a new soft-start process will start.

Minimum High-side On/Off-Time and Frequency Fold-Back

The shortest duration for the high-side switch on-time (t_{ON_MIN}) is 100ns (TYP). For the off-time (t_{OFF_MIN}) the minimum value is 120ns (TYP). The duty cycle (or equivalently the V_{OUT}/V_{IN} ratio) range in CCM operation is limited by t_{ON_MIN} and t_{OFF_MIN} depending on the switching frequency. Note that at 1.2MHz the total cycle time is t_{SW} = 833ns.

The minimum and maximum duty cycles without frequency fold-back are given by Equations 1 and 2:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (1)$$

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (2)$$

For any given output voltage, the highest input voltage without frequency fold-back can be calculated from:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (3)$$

The minimum V_{IN} is estimated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (4)$$

DETAILED DESCRIPTION (continued)

Input Voltage

The SGM61412 can operate efficiently for inputs as high as 42V. For CCM operation keeps duty cycle between 12% and 88%.

Output Voltage

The output voltage can be bucked to as low as the 0.83V reference voltage (V_{REF}). As explained before, when the output voltage is set to 0.83V and there is no voltage divider, a minimum small load will be needed. An 80kΩ resistor to ground will prevent the output voltage floating up.

Soft-Start

The integrated soft-start circuit in SGM61412 limits the input inrush current right after power-up or enabling the device. Soft-start is implemented by slowly ramping up the reference voltage that in turn slowly ramps up the output voltage to its target regulation value.

Enable

EN pin turns the SGM61412 operation in on or off condition. If an applied voltage is less than 0.9V, the device will shut down. If the voltage is more than 1.3V, the device will start the regulator. The simplest way to enable the device is to connect the EN pin to VIN pin via a resistor. This enables the SGM61412 to start up automatically when VIN is within the operating range. Many applications will profit from the employment of an enable divider R_{ENT} and R_{ENB} (see Figure 4) to build an accurate system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. This feature can be used for power supply sequencing which is required for proper power up of the system voltage rails. It can also be used as protection, such as preventing supply battery from depletion. Control of the enable input by logic signals may also be used for sequencing or protection.

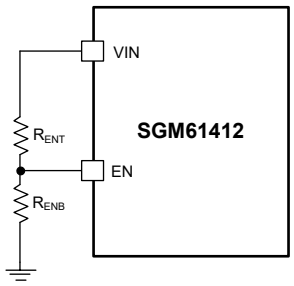


Figure 4. System UVLO by Enable Divider

Thermal Shutdown

Thermal protection is designed to protect the die against overheating damage. If the junction temperature exceeds +155℃, the switching stops and the device shuts down. Automatic recovery with an internal soft-start will begin when the junction temperature drops below the +125℃ falling threshold.

TYPICAL APPLICATION CIRCUITS

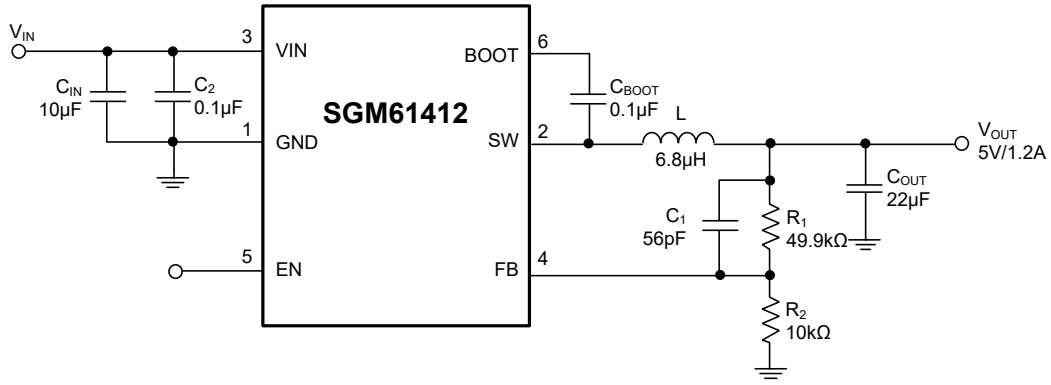


Figure 5. 5V Output Typical Application Circuit for Power Meters

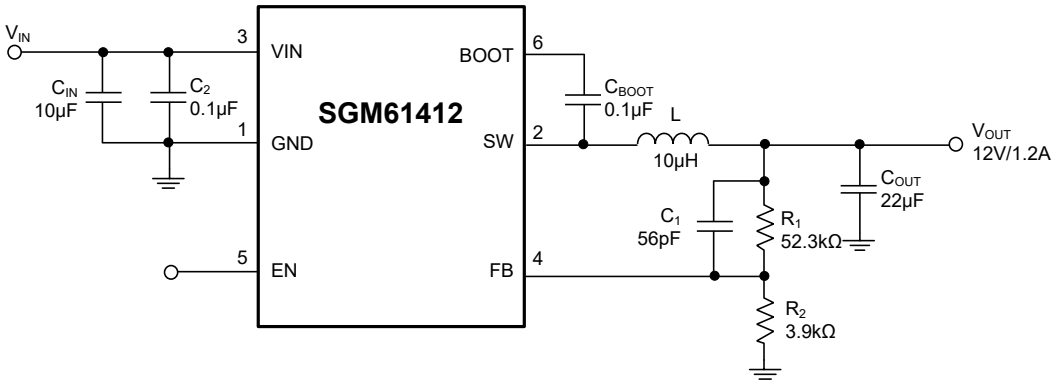


Figure 6. 12V Output Typical Application Circuit for Power Meters

APPLICATION INFORMATION

External Components

The following guides can be used to select external components.

f_{SW} (MHz)	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	L (μH)	C_{BOOT} (μF)	C_{IN} (μF)	C_{OUT} (μF)
1.2	3.3	30	10	4.7	0.1	10	22
	5	49.9	10	6.8	0.1	10	22
	12	52.3	3.9	10	0.1	10	22

Output Voltage Programming

Output voltage can be set with a resistor divider feedback network between output and FB pin as shown in Figure 5 and Figure 6. Usually, a design is started by selecting lower resistor R_1 and calculating R_2 with the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

where V_{REF} = 0.83V.

To keep operating quiescent current small and prevent voltage errors due to leakage currents, it is recommended to choose R_1 in the range of 10kΩ to 100kΩ.

The error amplifier is normally able to maintain regulation since the synchronous output stage has excellent sink and source capability. However it is not able to regulate output when the FB pin is disconnected or when the output is shorted to a higher supply like input supply. Also when V_{OUT} is set to its minimum (0.83V) usually there is no voltage divider and V_{OUT} is directly connected to FB through a resistor (R_1 in the divider) and there is no resistor to ground (no R_2). In such case and with no load, an internal current source of 5μA ~ 6μA from BOOT into the SW pin, which can slowly charge the output capacitor and pull V_{OUT} up to V_{IN}. Therefore a minimum load of at least 10μA must be always present on V_{OUT} (for example, an 80kΩ resistor: 0.83V/10.4μA = 80kΩ).

Inductor Selection

Higher operating frequency allows the designer to choose smaller inductor and capacitor values; however, the switching and gate losses are increased. On the other hand, at lower frequencies the current ripple (ΔI_L) is higher, which results in higher light load losses. Use Equation 6 to calculate the required inductance (L_{MIN}). K is the ratio of the inductor peak-to-peak ripple (ΔI_L) to the maximum operating DC current (I_{OUT}). The recommended selection range for K is between 0.2 and 0.4. Choosing a higher K value reduces the selected inductance, but a too high K factor may result in insufficient slope compensation. The inductance is selected based on the desired peak-to-peak ripple current (ΔI_L) for CCM. Equation 7 shows that ΔI_L is inversely proportional to f_{SW} × L and is increased at the maximum input voltage (V_{IN_MAX}). Therefore by accepting larger ΔI_L values, smaller inductances can be chosen but the cost is higher output voltage ripple and increased core losses. Inductor peak-current should never exceed the saturation even in transients to avoid over-current protection. Also inductor RMS rating should always be larger than operating RMS current even at maximum ambient temperature.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \quad (6)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

where $K_{IND} = \Delta I_L / I_{OUT}$ (DC Current, MAX).

Note that it is generally desired to choose a smaller inductance value for faster transient response, smaller size, and lower DCR. On the other hand, if the inductance is too small, current ripple will increase which can trigger over-current protection. The larger the ripple of inductance current is, the larger the ripple of output voltage of output capacitor is. For peak-current mode control, it is recommended to choose large current ripple, because controller comparator performs better with higher signal to noise ratio. So, for this design example, K_{IND} = 0.4 is chosen, and the minimum inductor value for 12V input voltage is calculated to be 5.1μH. The nearest standard value would be a 6.8μH ferrite inductor with a 2A RMS current rating and 2.5A saturation current that are well above the designed converter output current RMS and DC respectively.

APPLICATION INFORMATION (continued)

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor with 16V or higher voltage rating must be connected between the BOOT-SW pin to provide the gate drive supply voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. X7R or X5R dielectric types are recommended.

Input Capacitor Selection

The input capacitor also provides the high frequency switching transient currents. So, choosing a low-ESR and small size capacitor with high self-resonance frequency and sufficient RMS rating is necessary. Typically, 10μF high quality ceramic capacitor (X5R, X7R or better) with voltage rating twice the maximum input voltage is recommended for decoupling capacitor. If the source is away from the device (> 5cm), some bulk capacitances are also needed to damp the voltage spikes caused by the wiring or PCB trace parasitic inductances. The value for this capacitor is not critical but must be rated to handle the maximum input voltage including ripple.

In this example, one 10μF/50V/X7R capacitor and a 0.1μF ceramic capacitor placed right beside the device VIN and GND pins for very high-frequency filtering are used.

Output Capacitor Selection

This device is designed to be used with external LC filters. The minimum required capacitance to keep cost and size down and bandwidth high. The main parts for designing the output capacitance are output voltage ripple, loop stability and the voltage over/undershoot during load current transients. So, C_{OUT} should be chosen carefully. The output voltage ripple is determined of two factors. One is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (8)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \quad (9)$$

These AC components are not in phase and the total peak-to-peak ripple is less than $\Delta V_{OUT\_ESR} + \Delta V_{OUT\_C}$.

Transient performance specification usually limits output capacitance if the system requires tight voltage regulation in presence of large current steps and/or fast slew rate. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. The control loop of regulator usually requires 8 or more clock cycles to adjust the inductance current to the new load level. The output capacitance must be as large as possible to provide a current difference of 8 clock cycles to keep the output voltage within the specified range. Equation 10 shows the minimum output capacitance required to specify output overshoot/undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \quad (10)$$

where:

I_{OL} = Low level of the output current step during load transient.

I_{OH} = High level of the output current during load transient.

V_{OUT_SHOOT} = Target output voltage over/undershoot.

For this design example, the target output ripple is 30mV. Assuming $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C} = 30mV$, and choosing $K_{IND} = 0.4$, Equation 8 requires ESR to be less than 62.5mΩ and Equation 9 requires $C_{OUT} > 1.67\mu F$. The target over/undershoot range of 5V output is $\Delta V_{OUT\_SHOOT} = 5\% \times V_{OUT} = 250mV$. From Equation 10, $C_{OUT} > 16\mu F$. So, in summary, the most stringent criteria for the output capacitor is transient constrain of $C_{OUT} > 16\mu F$. For the derating margin, one 22μF, 10V, X7R ceramic capacitor with 10mΩ ESR is used.

APPLICATION INFORMATION (continued)

Layout Guide

Careful layout is always important to ensure good performance and stable operation to any kind of switching regulator. Place the capacitors close to the device, use the GND pin of the device as the center of star-connection to other grounds, and minimize the trace area of the SW node. With smaller transient current loops, lower parasitic ringing will be achieved.

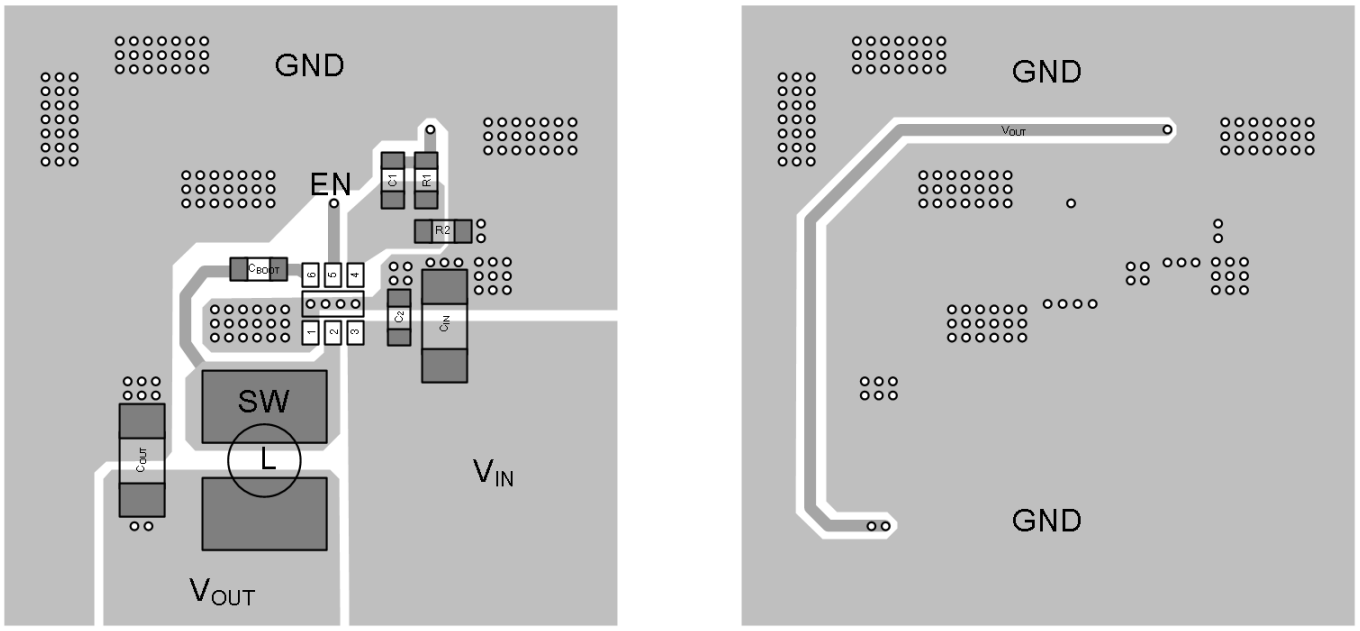


Figure 7. Suggested PCB

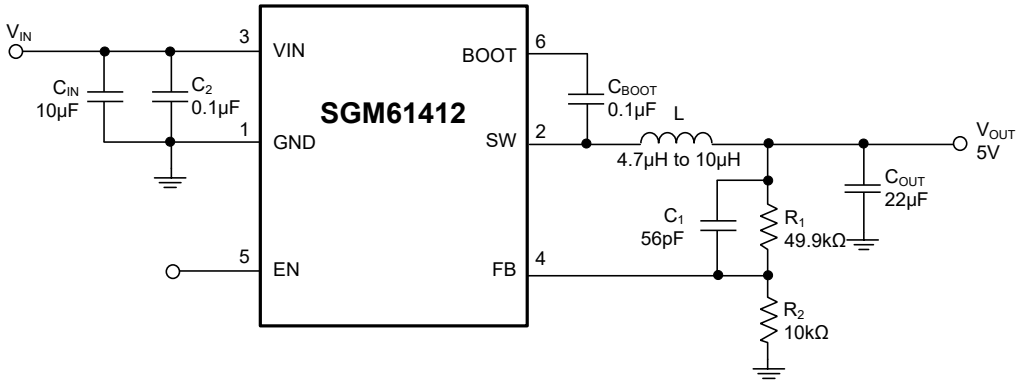


Figure 8. Typical Application Circuit

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2024 – REV.A.2 to REV.A.3	Page
Updated Package Thermal Resistance, Block Diagram and Package Outline Dimensions	2, 10, 19

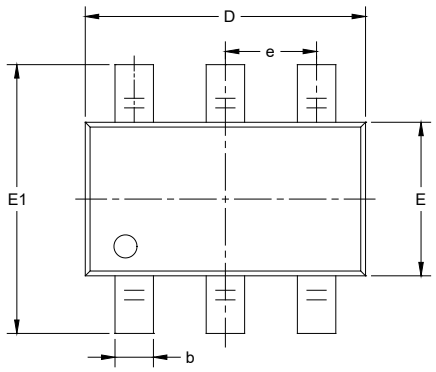
MAY 2022 – REV.A.1 to REV.A.2	Page
Updated Detailed Description and Application Information sections	11 to 17

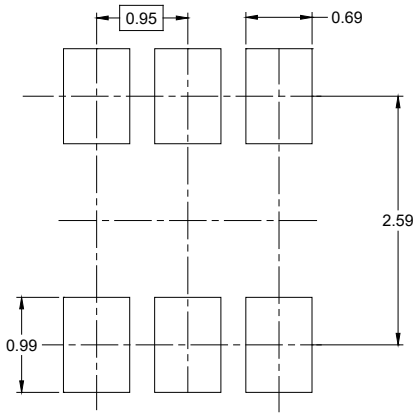
AUGUST 2021 – REV.A to REV.A.1	Page
Added the SGM61412B section	All

Changes from Original (APRIL 2021) to REV.A	Page
Changed from product preview to production data	All

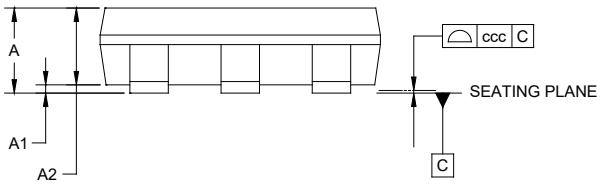
PACKAGE OUTLINE DIMENSIONS

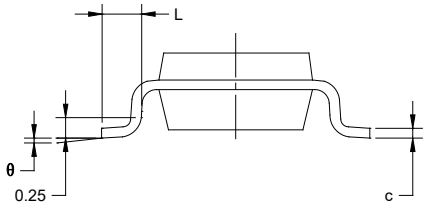
TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



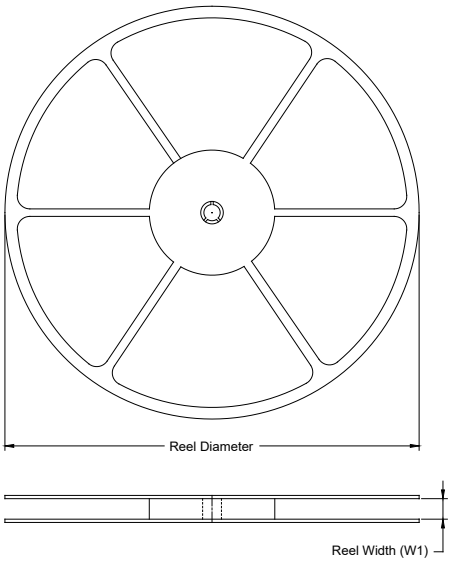


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700		1.000
b	0.300	-	0.500
c	0.080		0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

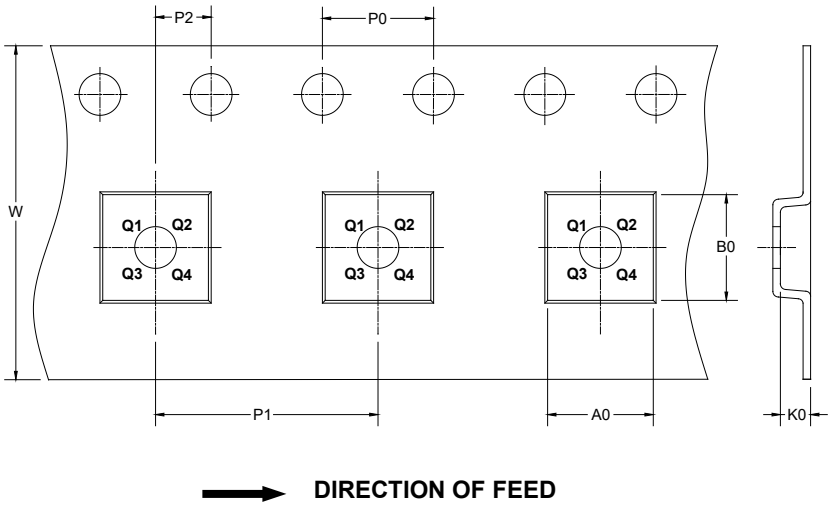
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



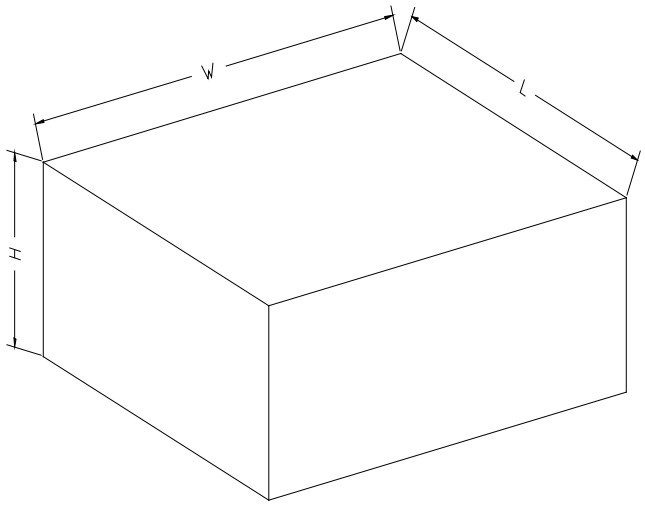
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-6	7″	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002