SGM63600
Up to 60V Input, Current Mode Synchronous Buck Controller

GENERAL DESCRIPTION

The SGM63600 is a 4.3V to 60V current mode controller for synchronous Buck converters. It is capable to efficiently drive two N-MOSFETs over the whole voltage range.

This device uses accurate cycle-by-cycle current limiting in PWM operation. Power-save mode (PSM) is used at light load to keep high efficiency. It can also enter non-synchronous PWM mode if the PSM is enabled.

Switching frequency can be set by an external resistor (R_{FREQ}), or an external clock (SYNC input) for low noise applications. The protection functions include UVLO, thermal shutdown, accurate output over-voltage protection (OVP) and over-current protection (OCP).

The SGM63600 is available in Green TQFN-3×4-20L and TSSOP-20 (Exposed Pad) packages. It can operate in the -40°C to +125°C junction temperature range.

TYPICAL APPLICATION

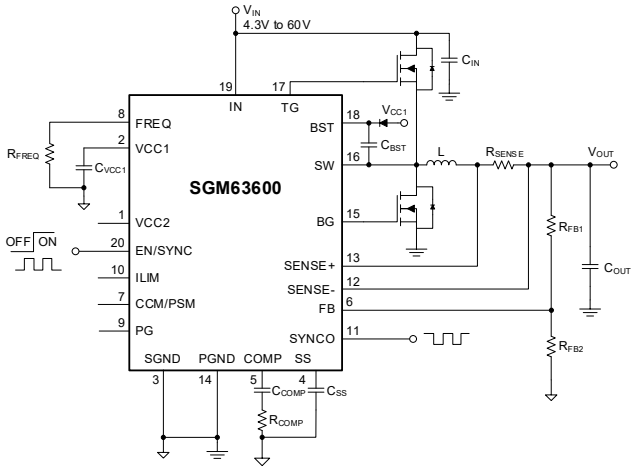


Figure 1. Typical Application Circuit

FEATURES

- **Integrated Dual N-MOSFET Drivers**
- **Wide 4.3V to 60V Input Voltage Range**
- **100kHz to 1MHz Adjustable Frequency Range**
- **Up to 99% Duty Cycle in Low Dropout Mode**
- **Adjustable Cycle-by-Cycle Current Limit**
- **Adjustable Soft-Start with Pre-biased Capability**
- **Thermal Shutdown**
- **Output OVP and OCP Protections**
- **Adjustable UVLO Protection through EN Input**
- **Hiccup Mode Current Limit**
- **Frequency Foldback Short Circuit Protection**
- **Synchronous Output (SYNCO) with 180º Phase Shift**
- **Power Good (PG) Indicator**
- **External Power Supply (VCC2) for Internal LDO**
- **PSM Capability for High Light-Load Efficiency**
- **Programmable PSM and CCM Operations**
- **Available in Green TQFN-3×4-20L and TSSOP-20 (Exposed Pad) Packages**

APPLICATIONS

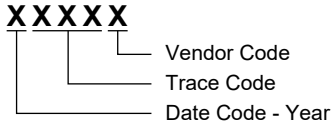
Industrial Power Supplies
General Purpose Wide V_{IN} Power Supplies
USB Dedicated Charging Port
PD Power Supply

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM63600	TQFN-3×4-20L	-40℃ to +125℃	SGM63600XTSF20G/TR	SGM 63600TSF XXXXX	Tape and Reel, 4000
	TSSOP-20 (Exposed Pad)	-40℃ to +125℃	SGM63600XPTS20G/TR	SGM08DXPTS20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM VOLTAGE RATINGS

Input Supply Voltage, V_{IN} ..... -0.3V to 65V
EN/SYNC ..... -0.3V to 50V
SW ..... -0.3V (-4V for < 20ns) to 65V
BST-SW Voltage ..... -0.3V to 6V
Supply Voltage, V_{CC1} ..... -0.3V to 6V
External Supply Voltage, V_{CC2} ..... -0.3V to 40V
SENSE+, SENSE - ..... -0.3V to 40V
Differential Sense (SENSE+ to SENSE-) ..... -0.7V to 0.7V
TG ..... V_{SW} - 0.3V to V_{BST} + 0.3V
BG ..... -0.3V to V_{CC1} + 0.3V
COMP ..... -0.3V to 5V
All Other Pins ..... -0.3V to 6V
Package Thermal Resistance
TQFN-3×4-20L, θ_{JA} ..... 44℃/W
TSSOP-20 (Exposed Pad), θ_{JA} ..... 28.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} (1) ..... 4.3V to 60V
Output Voltage, V_{OUT} ..... ≤ 32V
Supply Voltage for V_{CC2} ..... 5V to 32V
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTE:
1. The UVLO rising voltage is 5V, while its falling voltage is below 4.3V. Therefore, the input voltage must be higher than 5V for startup, and the SGM63600 can work down to 4.3V input voltage after startup.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

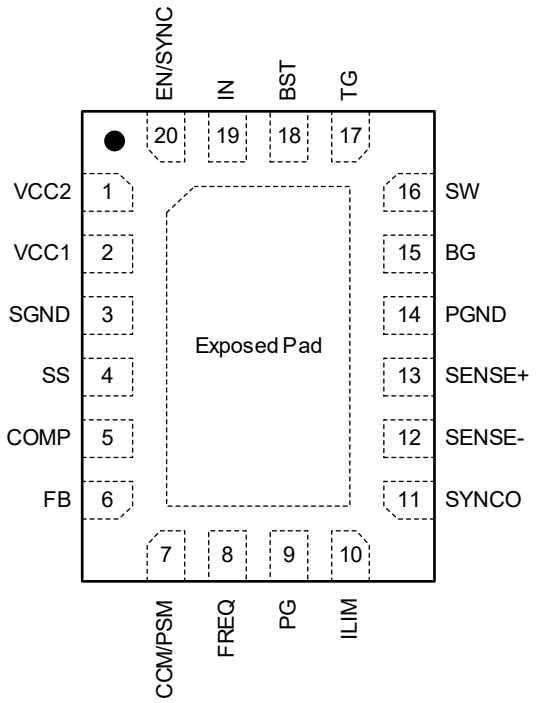
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

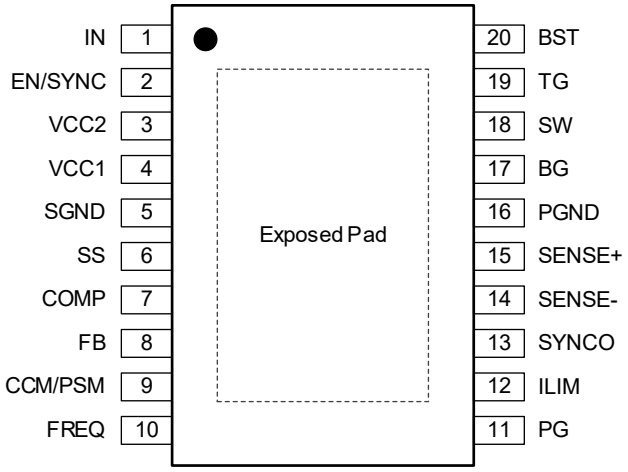
PIN CONFIGURATIONS

(TOP VIEW)



TQFN-3×4-20L

(TOP VIEW)



TSSOP-20 (Exposed Pad)

PIN DESCRIPTION

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	3	VCC2	Secondary Supply Input for the Internal VCC1 Regulator. Power input from V_{IN} is disabled when VCC2 is above VCC2 UVLO threshold. VCC2 supply must not exceed 32V.
2	4	VCC1	Internal Bias Supply Rail. Decouple this pin to SGND with a 1μF to 4.7μF ceramic capacitor.
3	5	SGND	Low Noise Signal Ground Return.
4	6	SS	Soft-Start Pin. Place an external capacitor (C_{SS}) between this pin and the SGND to set the soft-start time.
5	7	COMP	Compensation Pin. Use an RC network from COMP to SGND to compensate the internal loop. This network converts the current from the error amplifier to the control voltage.
6	8	FB	Feedback Input Pin. Connects to the midpoint of the output resistor divider. The FB voltage is compared to the 0.8V internal reference to set the output regulation voltage.
7	9	CCM/PSM	Set Pin for Selection of Continuous Conduction Mode (CCM) or Power-Save Mode (PSM). For CCM, float this pin or connect it to VCC1. For PSM, place a resistor (R_{PSM}) from this pin to SGND to choose PSM operation at light load. Light load voltage level for PSM voltage must be above 480mV.
8	10	FREQ	Switching Frequency Set Pin. An external resistor (R_{FREQ}) from FREQ to SGND sets the switching frequency.
9	11	PG	Open-Drain Power Good Output.
10	12	ILIM	Current Limit Setting Pin. The ILIM pin voltage determines the nominal sensed voltage threshold across the sense resistor for the peak inductor current (I_{PK}). With ILIM, the current limit threshold can be set to 3 fixed values: 27mV if ILIM is grounded, 52mV if ILIM is shorted to VCC1 and 78mV if ILIM is left float.
11	13	SYNCO	SYNC Clock Output. It is a 180° out-of-phase output clock relative to the clock source (internal oscillator or external SYNC) that is available only in CCM or DCM mode (not in sleep mode). This pin is used for dual channel applications. In all other modes such as sleep mode, low dropout and fault events the SYNCO outputs a DC voltage.
12	14	SENSE-	Current-Sense Negative Input (Connects to the current-sense resistor in series with the inductor).
13	15	SENSE+	Current-Sense Positive Input (Connects to the current-sense resistor in series with the inductor).
14	16	PGND	Power Ground. Power ground return for input supply, external low-side switch, load, internal low-side switch driver.
15	17	BG	Gate Driving Output for the Low-side Switch (the external synchronous N-MOSFET).
16	18	SW	Switching Node. Connects to the switching node of the converter and acts as return for the V_{BST} supply and provides a path for the high-side switch high bootstrapping currents.
17	19	TG	Gate Driving Output for the High-side Switch. Drives the high-side N-MOSFET. The TG driver is powered from the bootstrap (BST) capacitor (returned to SW) that is a floating supply.
18	20	BST	Bootstrap Pin. The bootstrap capacitor (C_{BST}) is placed between BST and SW pins. BST acts as the supply for the high-side switch floating driver. A diode from VCC1 to BST charges C_{BST} when the low-side switch is on.
19	1	IN	Power Supply Input Pin. Place a decoupling ceramic capacitor between this pin and PGND.
20	2	EN/SYNC	Enable and/or SYNC Input. A low DC signal on this pin will disable the device and a high DC voltage will enable it. EN can be used to increase (set) the input UVLO threshold with a resistor divider from V_{IN} input. If a CLOCK signal is sensed on this pin, it will act as SYNC input and the internal clock frequency will be locked and synced with that.
—	—	Exposed Pad	Thermal Exposed Pad. It is the main thermal relief path of the die connected to the ground plan on the PCB.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 24V, T_J = -40℃ to +125℃, V_{EN} = 2V, V_{ILIMIT} = 78mV, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
Input UVLO Threshold (Rising)	V_{UVLO_R}			4.6	5	V
Input UVLO Threshold (Falling)	V_{UVLO_F}			3.9	4.3	V
Input UVLO Hysteresis	V_{UVLO_HYS}			700		mV
Input Supply Current with VCC2 Bias	I_{Q_VCC2}	V_{CC2} = 12V, external bias		13	17	μA
Input Supply Current without VCC2 Bias	I_Q	V_{CC2} = 0V, V_{FB} = 1V, V_{PSM} = 5V, V_{SENSE+} = V_{SENSE-} = 0.3V		1100	1300	μA
Input PSM Current	I_{Q_PSM}	V_{PSM} = 0V, V_{FB} = 0.84V, V_{SENSE+} = V_{SENSE-} = 0.3V		280	346	μA
Input Shutdown Current	I_{SHDN}	V_{EN} = 0V		1.5	3	μA
VCC Regulator						
VCC1 Regulator Output Voltage from V_{IN}	V_{CC1_VIN}	V_{IN} > 6V		5		V
VCC1 Regulator Load Regulation from V_{IN}		Load = 0mA to 50mA, VCC2 floating or connects to GND		0.2	0.8	%
VCC1 Regulator Output Voltage from VCC2	V_{CC1_VCC2}	V_{CC2} > 6V		5		V
VCC1 Regulator Load Regulation from VCC2		Load = 0mA to 50mA, V_{CC2} = 12V		0.6	5.2	%
VCC2 UVLO Threshold (Rising)	V_{CC2_RISING}			4.7	4.95	V
VCC2 UVLO Threshold (Falling)	$V_{CC2\_FALLING}$			4.4		V
VCC2 Threshold Hysteresis	V_{CC2_HYS}			300		mV
VCC2 Supply Current	I_{VCC2}	V_{PSM} = 5V, V_{FB} = 1V, V_{CC2} = 12V		1110	1300	μA
		V_{PSM} = 0V, V_{FB} = 0.84V, V_{CC2} = 12V		275	336	
Feedback Input						
Reference Voltage	V_{REF}	4.3V ≤ V_{IN} ≤ 60V, T_J = +25℃, TQFN Package	0.794	0.800	0.818	V
		4.3V ≤ V_{IN} ≤ 60V, T_J = +25℃, TSSOP Package	0.794	0.800	0.820	
		4.3V ≤ V_{IN} ≤ 60V, T_J = -40℃ to +125℃, TQFN Package	0.792	0.800	0.820	
		4.3V ≤ V_{IN} ≤ 60V, T_J = -40℃ to +125℃, TSSOP Package	0.792	0.800	0.822	
Feedback Bias/Leakage Current	I_{FB}	V_{FB} = 0.84V		10		nA
Enable						
Enable Threshold (Rising)	V_{EN_RISING}		1.17	1.23	1.30	V
Enable Threshold (Falling)	$V_{EN\_FALLING}$		1.09	1.15	1.21	V
Enable Threshold Hysteresis	V_{EN_TH}			80		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		1.8		μA
Enable Turn-Off Delay Time	t_{OFF}			12		μs
Oscillator and Clock Synchronization						
Operating Frequency	f_{SW}	R_{FREQ} = 65kΩ	276	300	323	kHz
Foldback Operating Frequency	$f_{SW\_FOLDBACK}$	V_{FB} = 0.1V		50%		f_{SW}
Maximum Programmable Frequency	f_{SW_H}		1000			kHz
Minimum Programmable Frequency	f_{SW_L}				100	kHz
Clock Input Synchronization Range	f_{SYNC}		100		1000	kHz
SYNC Input Clock High Level	V_{SYNC_R}		2.1			V
SYNC Input Clock Low Level	V_{SYNC_F}				1.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 24V, T_J = -40℃ to +125℃, V_{EN} = 2V, V_{ILIMIT} = 78mV, typical values are at measured T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Sensing						
Common Mode Voltage Range	$V_{SENSE+/-}$		0		32	V
Current Limit Threshold Sense Voltage	V_{ILIMIT}	ILIM = GND, V_{SENSE+} = 3.3V	21	27	33	mV
		ILIM = VCC1, V_{SENSE+} = 3.3V	43	52	60	
		ILIM = FLOAT, V_{SENSE+} = 3.3V	69	78	86	
Reverse Current Limit Equivalent Sense Voltage	V_{REV_ILIMIT}	ILIM = GND, V_{SENSE+} = 3.3V		7		mV
		ILIM = VCC1, V_{SENSE+} = 3.3V		15		
		ILIM = FLOAT, V_{SENSE+} = 3.3V		23		
Valley Current Limit Sense Voltage	V_{VAL_ILIMIT}	ILIM = GND, V_{SENSE+} = 3.3V		25		mV
		ILIM = VCC1, V_{SENSE+} = 3.3V		50		
		ILIM = FLOAT, V_{SENSE+} = 3.3V		75		
Input Current of Current-Sense Inputs	I_{SENSE}	$V_{SENSE+/-(CM)}$ = 0V		-80		μA
		$V_{SENSE+/-(CM)}$ = 3.3V		160		
Soft-Start (SS)						
Soft-Start Source Current	I_{SS}	V_{SS} = 0.5V	3	4	5	μA
Error Amplifier						
Error Amp Transconductance	Gm	ΔV = 5mV		500		μA/V
Error Amp Open Loop DC Gain	A_O			70		dB
Error Amp Sink/Source Current	I_{EA}	V_{FB} = 0.7V/0.9V		±35		μA
Protections						
Output Over-Voltage Threshold	V_{OV}		109%	116%	123%	V_{REF}
Over-Voltage Hysteresis	V_{OV_HYS}			10%		V_{REF}
Thermal Shutdown				175		℃
Thermal Shutdown Hysteresis				25		℃
Gate Driver						
TG Pull-Up Resistance	R_{TG_PULLUP}	Source 20mA		2.3		Ω
TG Pull-Down Resistance	R_{TG_PULLDN}	Sink 20mA		0.8		Ω
BG Pull-Up Resistance	R_{BG_PULLUP}	Source 20mA		3.0		Ω
BG Pull-Down Resistance	R_{BG_PULLDN}	Sink 20mA		0.9		Ω
Dead Time	t_{DEAD}			40		ns
TG Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V		99		%
TG Minimum On Time (1)	$t_{ON\_MIN\_TG}$			92		ns
BG Minimum On Time (1)	$t_{ON\_MIN\_BG}$			175		ns
Power Good						
Power Good Low	V_{PG_Low}	I_{SINK} = 4mA		0.1	0.2	V
PG Rising Threshold	PG_{Vth_RSING}	V_{FB} rising	83%	90%	98%	V_{REF}
		V_{FB} falling	99%	106%	113%	
PG Falling Threshold	$PG_{Vth\_FALLING}$	V_{FB} falling	80%	87%	95%	V_{REF}
		V_{FB} rising	104%	111%	118%	
PG Threshold Hysteresis	PG_{Vth_HYS}			5%		V_{REF}
Power Good Leakage	I_{PG_LK}	V_{PG} = 5V		0.1	1	μA
Power Good Delay	t_{PG_DELAY}	PG rising and falling		25		μs
PSM/CCM						
PSM Output Current	I_{PSM}	R_{FREQ} = 65kΩ		9.3		μA
Required PSM Threshold Voltage for CCM	V_{CCM_TH}		2.6			V

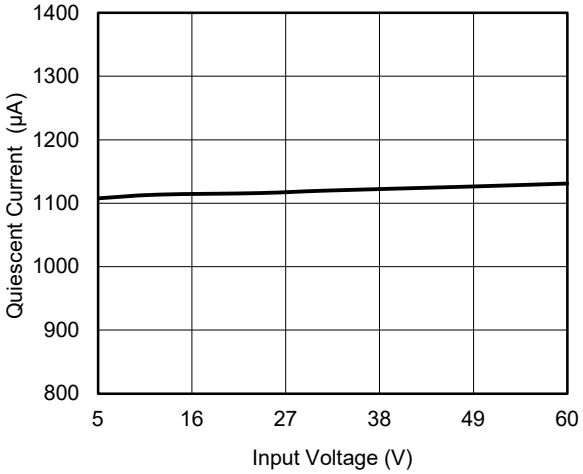
NOTE:

1. The value is guaranteed by design.

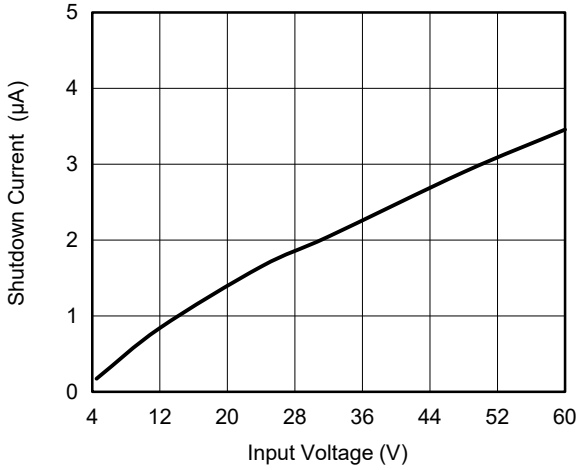
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

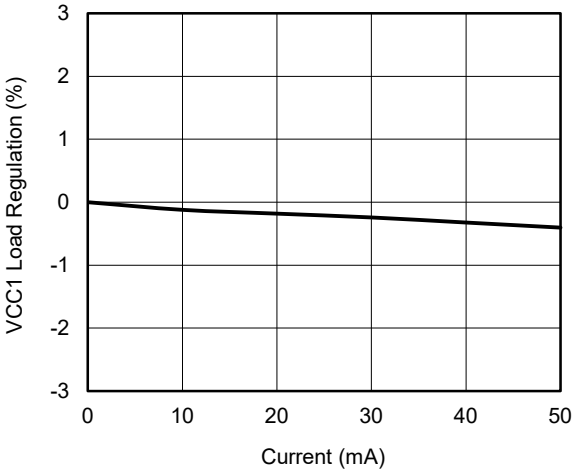
Quiescent Current vs. Input Voltage



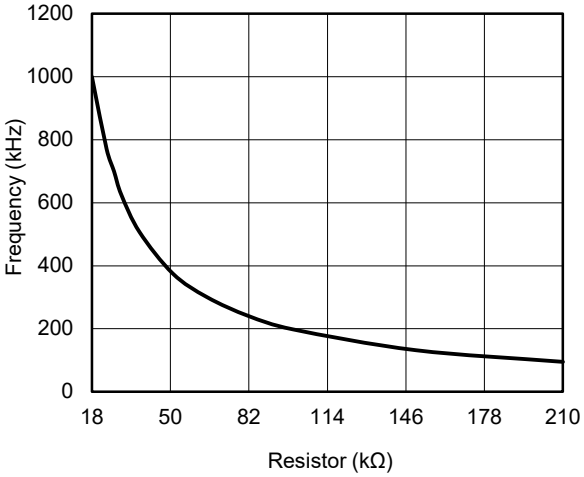
Shutdown Current vs. Input Voltage



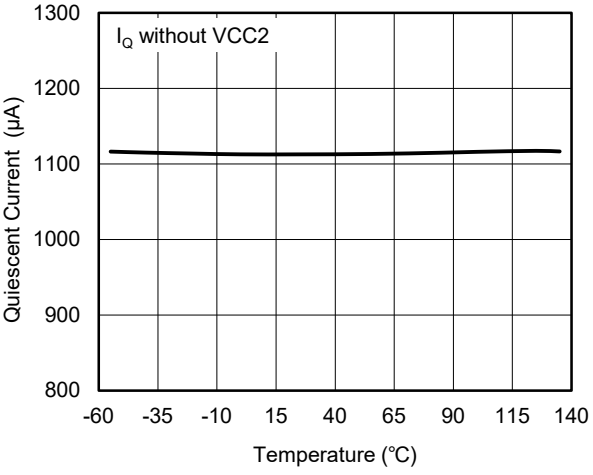
VCC1 Load Regulation



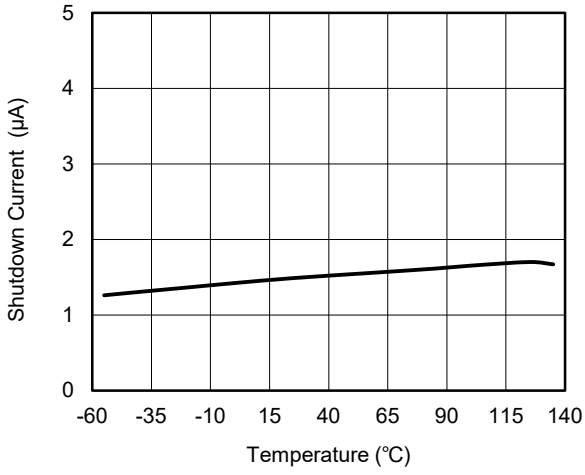
Frequency vs. Resistor



Quiescent Current vs. Temperature



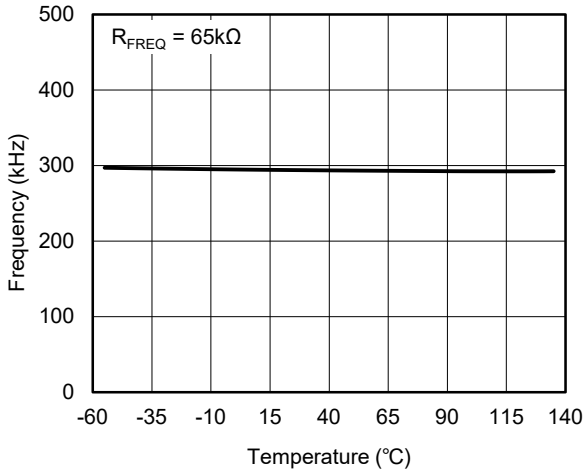
Shutdown Current vs. Temperature



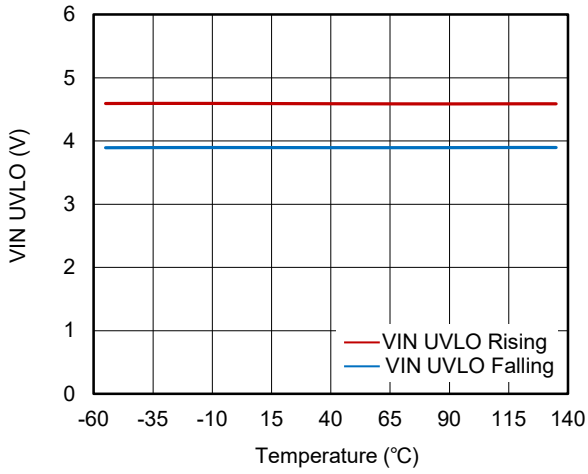
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

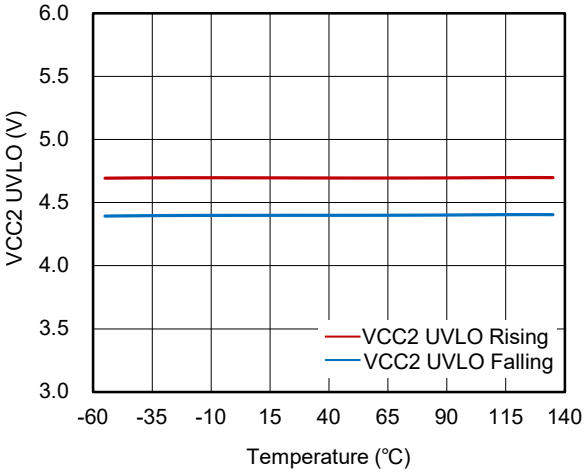
Frequency vs. Temperature



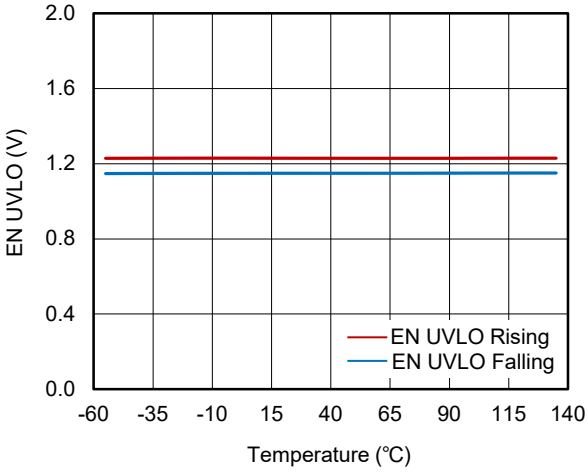
VIN UVLO vs. Temperature



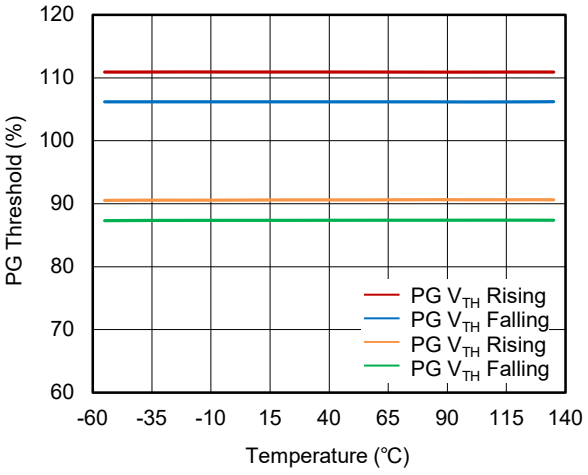
VCC2 UVLO vs. Temperature



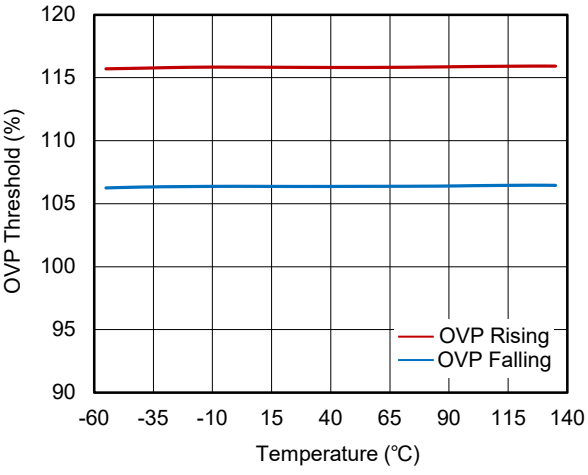
EN UVLO vs. Temperature



PG Threshold vs. Temperature



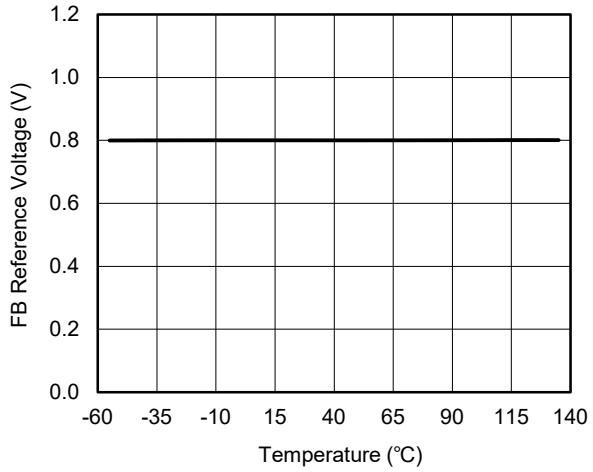
OVP Threshold vs. Temperature



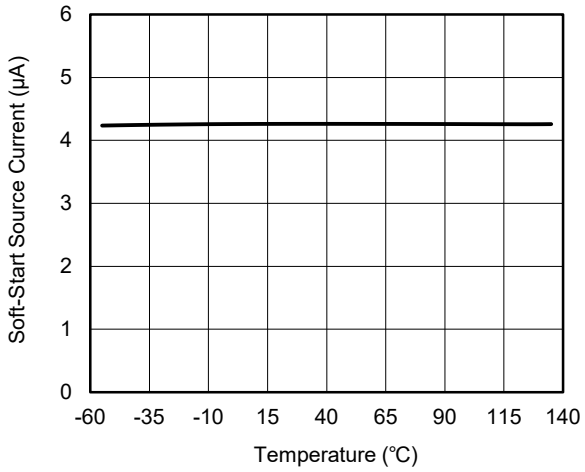
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

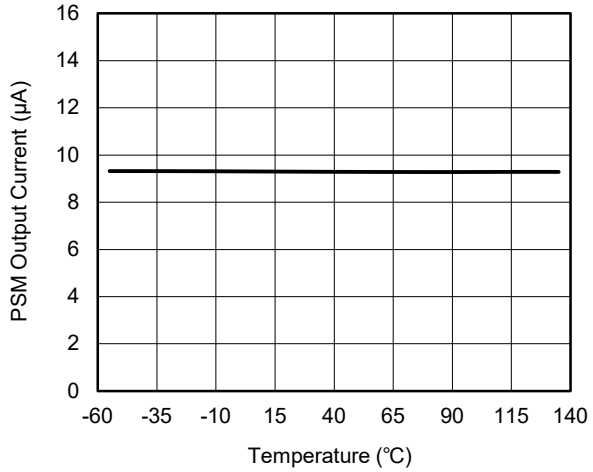
FB Reference Voltage vs. Temperature



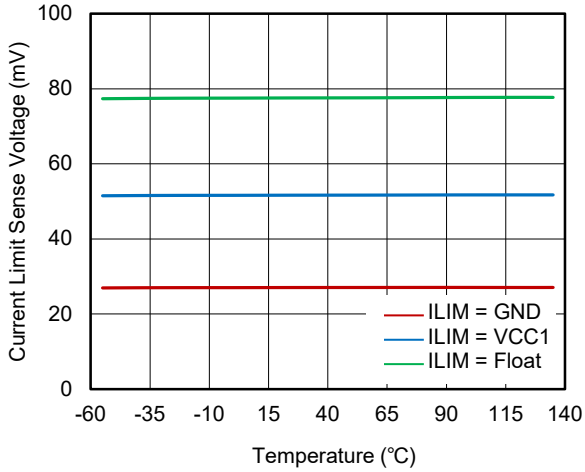
Soft-Start Source Current vs. Temperature



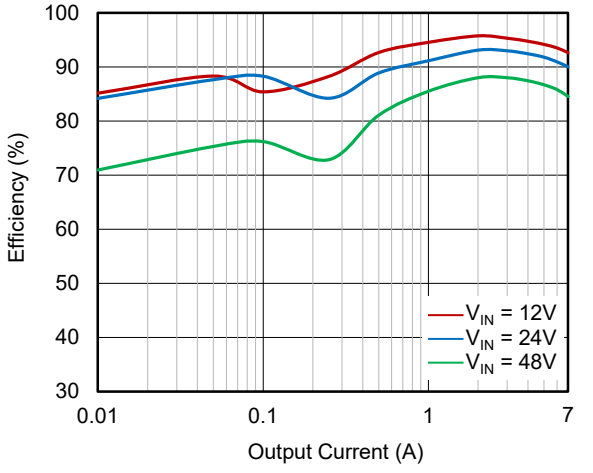
PSM Output Current vs. Temperature



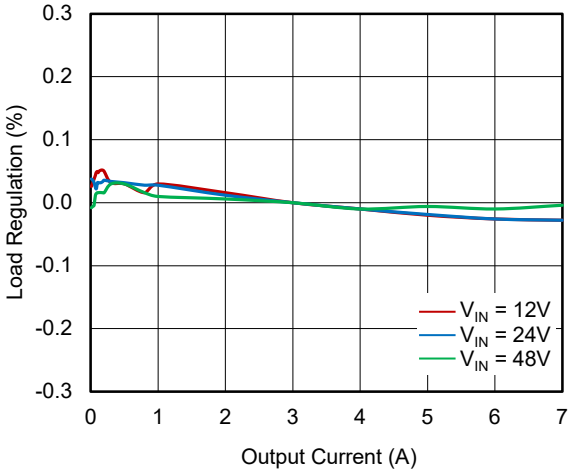
Current Limit Sense Voltage vs. Temperature



Efficiency vs. Output Current



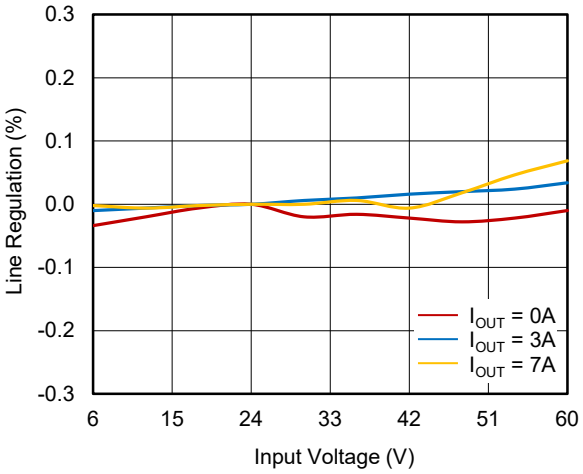
Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

Line Regulation



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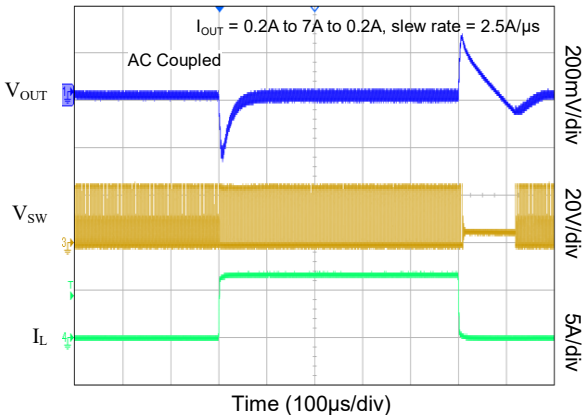
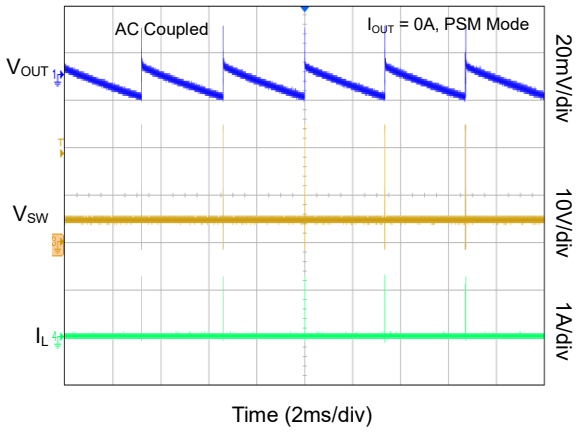


Steady State



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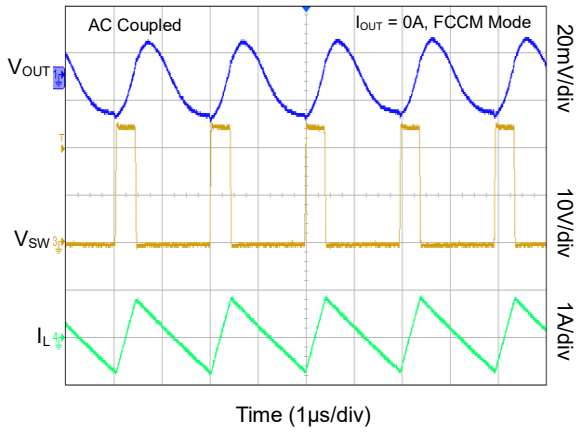

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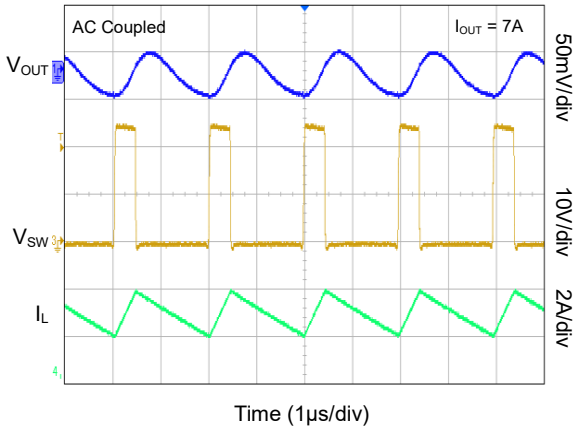
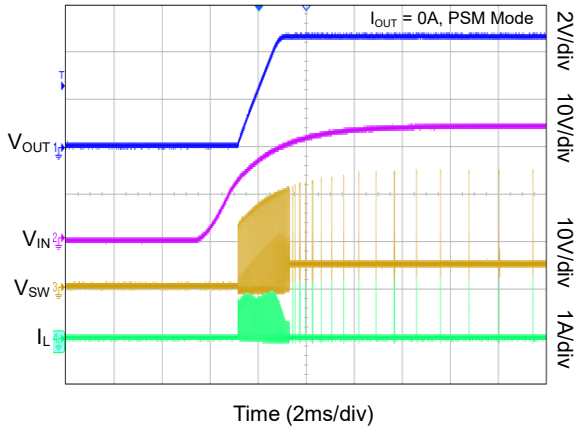


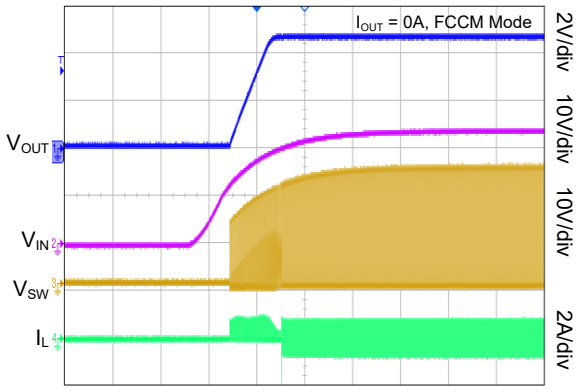
Startup through VIN



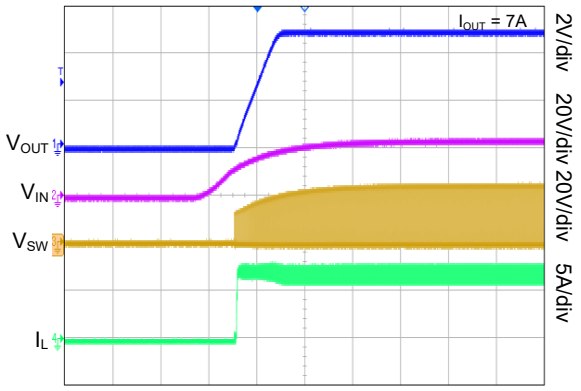
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

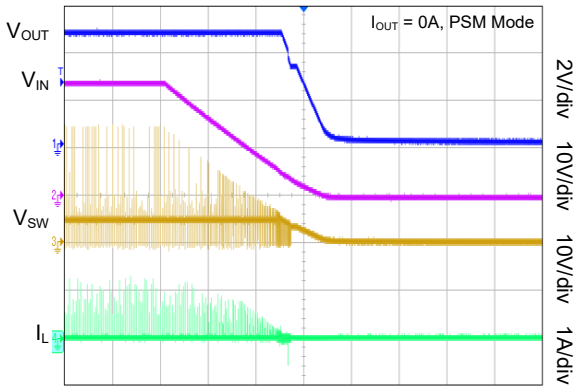
Startup through VIN



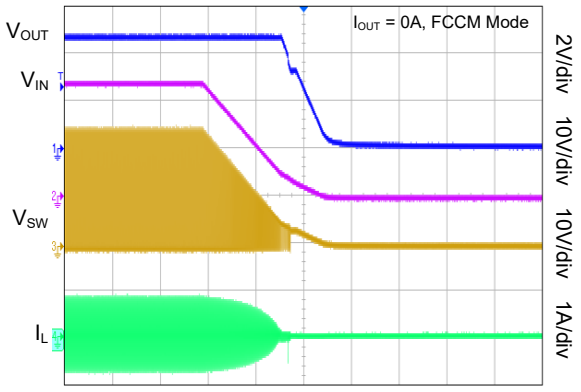
Startup through VIN



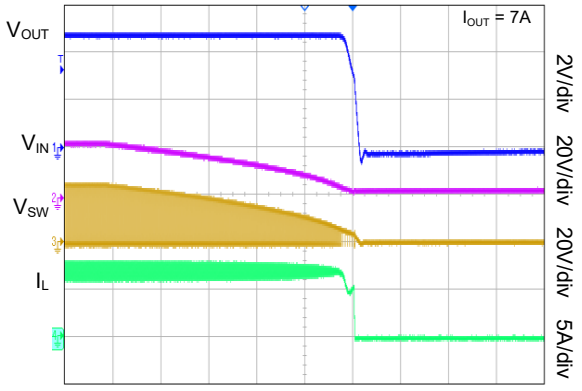
Shutdown through VIN



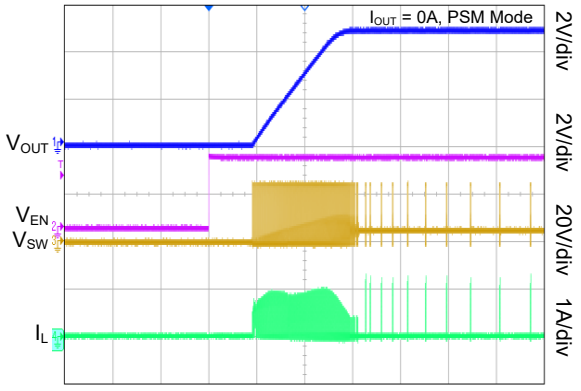
Shutdown through VIN



Shutdown through VIN



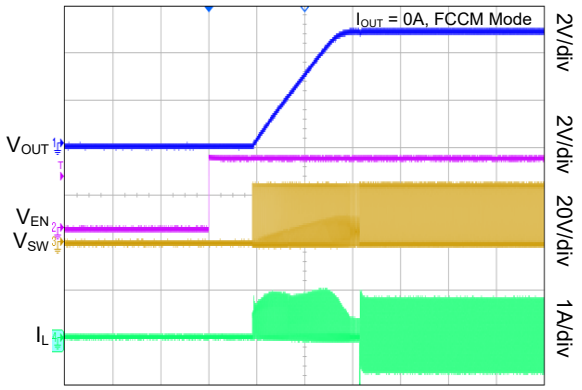
Startup through EN



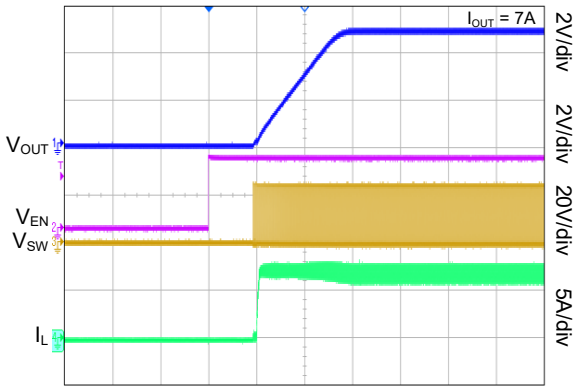
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

Startup through EN



Startup through EN



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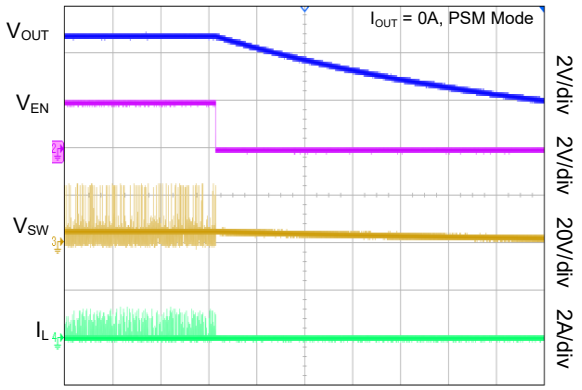
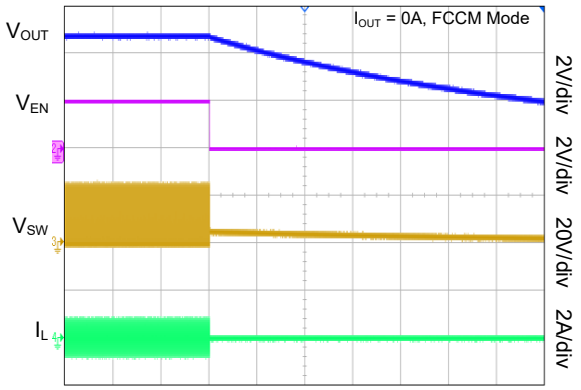
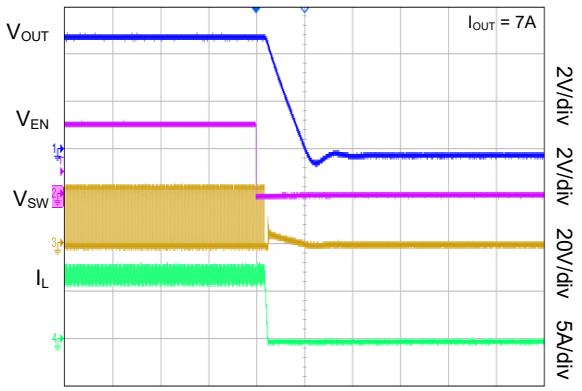


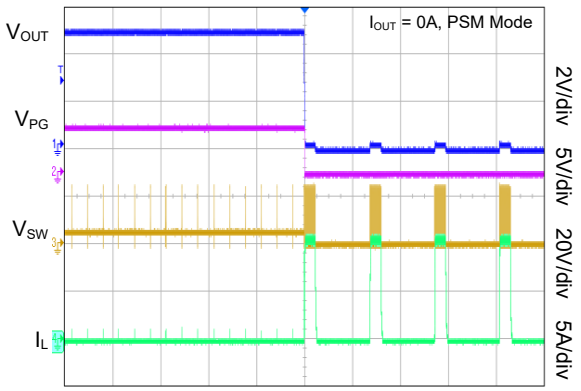
Shutdown through EN



Shutdown through EN



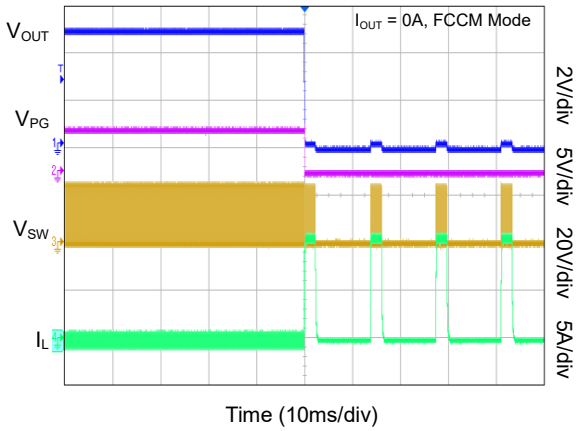
SCP Entry



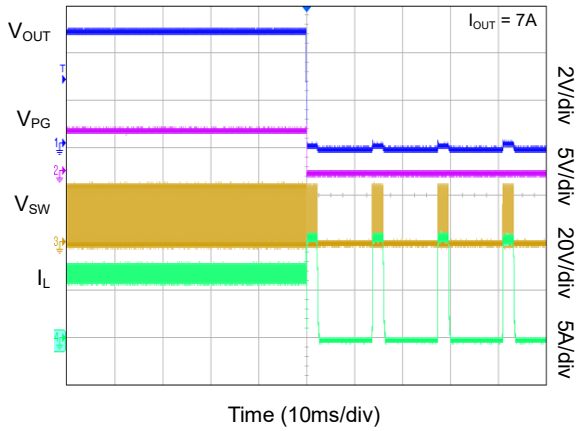
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

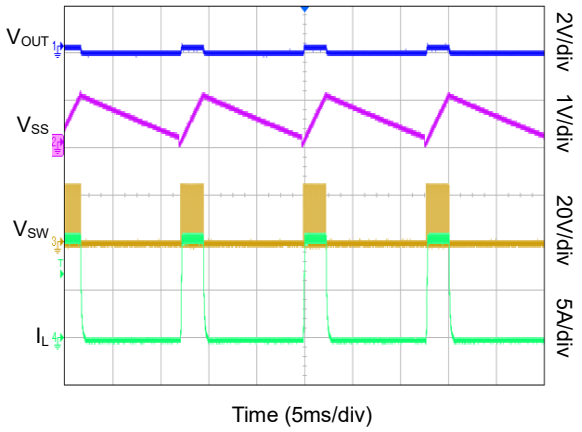
SCP Entry



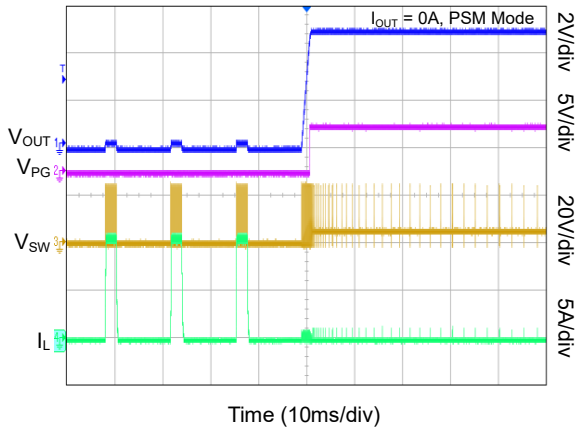
SCP Entry



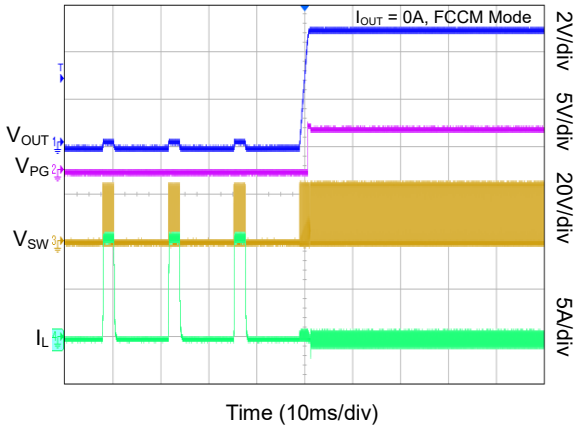
SCP Steady State



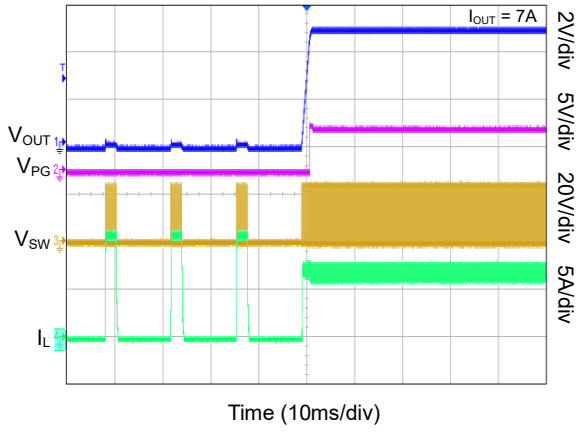
SCP Recovery



SCP Recovery



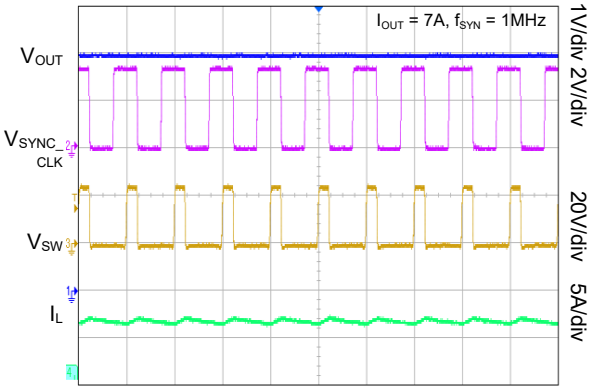
SCP Recovery



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

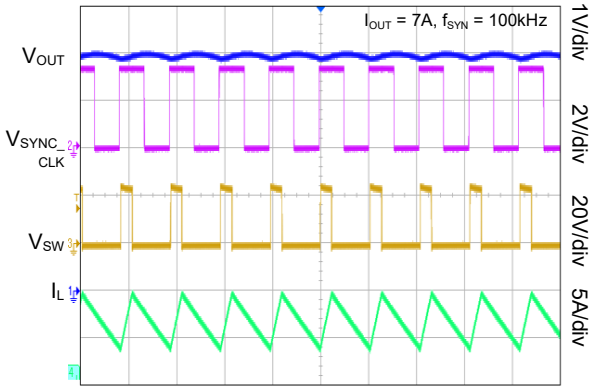
V_{IN} = 24V, V_{OUT} = 5V, L = 4.7μH, T_A = +25℃, unless otherwise noted.

SYNC Function



Time (1μs/div)

SYNC Function



Time (10μs/div)

FUNCTIONAL BLOCK DIAGRAM

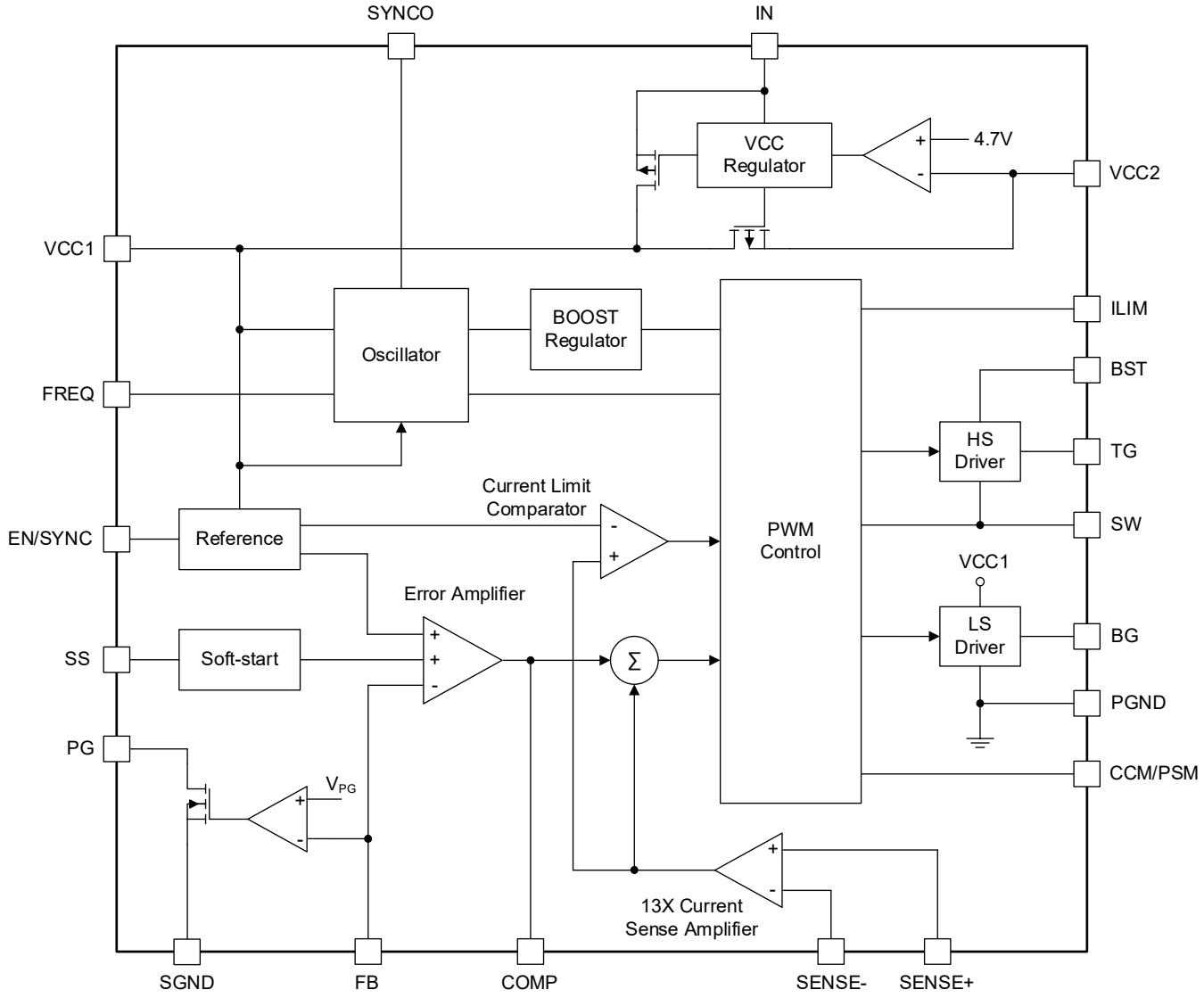


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM63600 is a wide input synchronous Buck current mode controller for MOSFET based DC/DC Buck converters. Using current mode control architecture and adjustable switching frequency, it can regulate the output voltage with high accuracy through two external N-MOSFETs.

The COMP pin voltage reflects the amplified error signal between the sensed output voltage at the FB pin and the internal 0.8V reference. This voltage is compared with the sensed inductor current plus a slope compensation ramp to generate the gate pulse signals for switch control.

The controller operates in PWM mode unless the load is light and PSM mode is selected. The high-side switch gate pulse is turned on at the beginning of each cycle and stays on for the ON-time (duty cycle is determined by the controller). Then the top gate turns off and after a short dead time the bottom gate is turned on until the end of the cycle.

Under-Voltage Lockout (UVLO)

The Under-voltage lockout protection is necessary to avoid device malfunction due to insufficient V_{IN} supply voltage. The rising and falling UVLO thresholds of the SGM63600 are about 4.6V and 3.9V respectively.

Adjustable UVLO (EN Input)

The EN/SYNC pin acts as an active high enable input. This pin uses an accurate 1.23V threshold that can be used to set a higher level for the V_{IN} UVLO. Pulling this pin high enables the device and pulling it low (for at least 12μs) disables it.

To set the UVLO, the EN/SYNC pin needs to be tied to V_{IN} with a resistor divider (R_{EN1} and R_{EN2} in **Figure 3**). The EN falling threshold is 1.15V, therefore the new V_{IN} UVLO falling threshold will be 1.15V × (1+ R_{EN1}/R_{EN2}).

Make sure EN/SYNC pin voltage is always below 50V in input high-voltage applications.

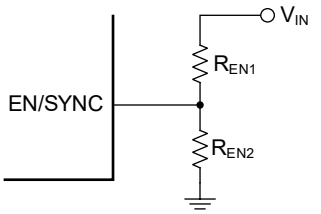


Figure 3. EN Resistor Divider

Synchronization (SYNC Input)

The internal oscillator can synchronize to an external logic clock applied to the EN/SYNC pin in the 100kHz to 1000kHz range. The rising edge of the internal clock syncs with rising edge of the external clock.

It is recommended that the on and off pulse widths of external clock are both more than 100ns.

Startup and Shutdown

The SGM63600 will start up if V_{IN} is above UVLO and the enable pin is active high. First the voltage reference circuitry is powered to get stable voltages and current references and then the internal regulator is turned on to supply the remaining circuitry.

The device shuts down if one of the following three events occurs:

1. Enable goes low;
2. V_{IN} falls below UVLO;
3. Die temperature exceeds shutdown threshold.

During shutdown, the shutdown signal path is blocked to prevent any other fault triggering and then the COMP pin and the internal supply rail are pulled down. The floating high-side driver is not included in the shutdown process.

Pre-Bias Start-Up

The SGM63600 can startup in pre-biased conditions. If a voltage is detected on the output during startup (that is, V_{FB} is higher than the SS ramp), the TG and BG driver outputs will not turn on until the soft start ramp (SS) exceeds the pre-biased voltage on the output (FB).

Soft-Start (SS)

Soft start feature is necessary to have a smooth startup without over-current, output voltage transient or hiccup. Without soft-start, such protections may occur due to charging of the output capacitors or input voltage drop (below UVLO) due to high startup current and should be avoided. Soft-start is implemented by a ramp voltage which rises slowly from 0V towards 0.8V and replaces the V_{REF} during startup for the output voltage regulation. When this ramp reaches or exceeds V_{REF}, The V_{REF} itself will regain control as reference for regulation.

DETAILED DESCRIPTION (continued)

Except for output OVP, for all other faults the device resets with a new soft start after recovery.

The ramp slope is set by an external capacitor (C_{SS}) placed between SS and SGND pins. It will be charged by an internal I_{SS} = 4μA current source to generate the ramp voltage. The soft-start time (t_{SS}) can be calculated from Equation 1:

There is no internal soft-start capacitance inside the device.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (1)$$

Transconductance Error Amplifier (EA)

The difference between V_{FB} and the internal reference (V_{REF} = 0.8V) is amplified to an output current signal at COMP pin with a G_{EA} (A/V) gain. This current is injected in the compensation network to generate the V_{COMP} control signal that determines the inductor (switch) current by controlling duty cycle. The control loop response is determined by the RC network between the COMP and SGND pins and can be optimized for best stability and transient response.

PSM Mode

An optional power-save mode (PSM) is provided in SGM63600 to improve light or no load efficiency. This option can be enabled by pulling CCM/PSM pin low with a proper resistor (R_{PSM}) such that the pin voltage (V_{PSM}) is above 480mV. Equation 2 can be used to determine the R_{PSM}:

$$V_{PSM}\ (mV) = I_{PSM}\ (\mu A) \times R_{PSM}\ (k\Omega) \quad (2)$$

The I_{PSM} is the PSM pin output current given by Equation 3:

$$I_{PSM} = \frac{600mV}{R_{FREQ}\ (k\Omega)} \quad (3)$$

The R_{FREQ} is the frequency setting resistor connected between the FREQ and SGND pins and its value is calculated from the equation given in the Switching Frequency Selection section.

If the CCM/PSM pin is floating or connected to VCC1 the PSM will be disabled.

If PSM is enabled, and load is large enough to have continuous conduction, the converter continues operation like PWM, but if load is reduced and inductor current reaches zero, the device first enters non-synchronous operation without frequency reduction in which the bottom switch turns off when inductor current reaches to zero in each cycle. If the load is further decreased to very light or no load, the V_{COMP} falls below the PSM threshold (≈ V_{PSM} + V_{OFFSET}), and the SGM63600 enters PSM mode with frequency reduction (V_{OFFSET} ≈ 190mV). In this mode, a new cycle starts whenever V_{COMP} exceeds the PSM threshold. The time reference for the next cycle is the V_{COMP} crossover time. If the load gets heavier, the DC component of the V_{COMP} will increase and when it exceeds the PSM threshold, the device will operate with fixed frequency again (in DCM or CCM depending on load).

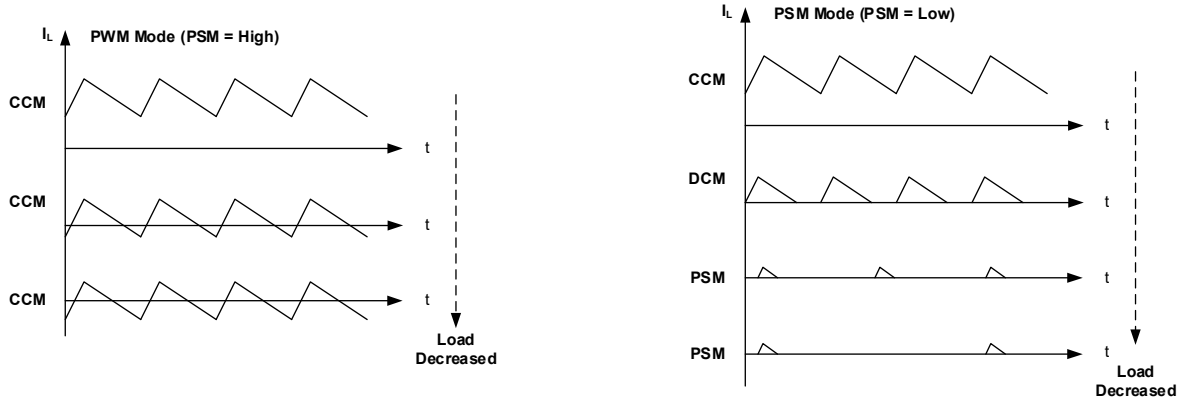


Figure 4. Converter Operation with Forced PWM (PSM disabled) and PSM Enabled (constant or reduced frequency)

DETAILED DESCRIPTION (continued)

Floating Driver and Bootstrap Charging

The floating top gate driver is powered by an external bootstrap capacitor (C_{BST}), which is normally refreshed when the high-side MOSFET turns off. This floating driver has its own UVLO protection. This UVLO's falling threshold is 3.05V with a hysteresis of 600mV.

Internal Regulator (VCC1) and Secondary Supply (VCC2)

Almost all internal circuits and the gate drivers are powered from the internal low dropout VCC1 regulator that receives power from V_{IN} or VCC2. VCC1 must be decoupled to SGND with a 1μF to 4.7μF ceramic capacitor.

When the VCC2 pin is float or has low voltage (< 4.4V), VCC1 will be powered from V_{IN} by a 5V regulator. If V_{CC2} is high enough (> 4.7V), the 5V regulator from V_{IN} will be disabled and another 5V regulator turns on to supply VCC1 from VCC2. When 4.4V < V_{CC2} < 5V, this regulator operates in dropout mode and V_{CC1} is almost equal to V_{CC2}. If V_{CC2} > 5V (not exceed 32V), then VCC1 will be regulated at 5V. Supplying from VCC2 provides better efficiency when a source is available. If the converter output can be used to supply VCC2, it is in the 4.7V to 32V range.

Current Limit

Current limit can be set to 3 fixed values selected by an ILIM pin. If ILIM pin is grounded, the sensed voltage threshold (V_{ILIMIT}) for current limit is 27mV. It will be 52mV when ILIM pin is connected to VCC1 and 78mV when ILIM pin is floating.

If the inductor peak current tends to exceed this limit, the output voltage will start to drop to reduce the load current. If V_{FB} falls below 62.5% of V_{REF}, the device enters hiccup mode in which the device will turn off switching and restart cyclically until the over current fault is cleared. If V_{FB} falls below 0.5V the frequency foldback will reduce the switching frequency as well. This reduction is particularly helpful when an extended short circuit to ground occurs and significantly reduces the average short current and device overheating.

Low Dropout Mode

A low dropout operating mode is included to minimize converter dropout when input voltage is close to the output voltage. In this mode the duty cycle is kept at maximum (the high-side switch on-time is maximized) as much as bootstrap UVLO voltage allows. The off-time must be sufficient to recharge the bootstrap capacitor such that the bootstrap voltage (V_{BST} - V_{SW}) remains above its UVLO threshold (3.05V). If it falls below its UVLO the high-side switch (HS) is turned off and the low-side switch (LS) is turned on to recharge the C_{BST} capacitor. After the recharge, the HS is turned on again to regulate the output. As long as the V_{BST} voltage is above its UVLO, the HS switch can remain on for more than one cycle and only is turned off shortly for refreshing the C_{BST} capacitor. This will increase the regulator effective duty cycle. The maximum on-time of high-side switch is 30μs typically.

This mode is a very useful feature of the SGM63600 in some application such as automotive cold cranking.

Power Good Indicator (PG)

The open-drain power good output goes high whenever the output is within ±10% of regulation (TYP). PG is pulled low if the output voltage goes out of the ±10% range. The pull-up voltage must be 5V or lower. Usually, a large resistor (e.g., 100kΩ) is used for pull-up. The PG indicator reaction delay time is 25μs.

To ensure that the PG is low logic with no input for SGM63600, it is recommended to pull up the PG pin to the VCC1 of SGM63600.

Output Over-Voltage Protection (OVP)

The output voltage is monitored through FB pin voltage and if it exceeds for about 16% above the V_{REF}, an OVP will be triggered. When OVP occurs, device enters discharge mode in which HS is turned off and LS is turned on until the reverse current limit is triggered. At this point the LS will be also turned off and inductor current rises to zero. The LS will be turned on again in the next cycle. The discharge mode will continue until the over-voltage condition is cleared.

Thermal Shutdown

To protect the device from overheating damage the junction temperature is constantly monitored and if it reaches the +175°C limit the device will shut down. It will automatically recover normal operation with a soft start when the die cools down for about 25°C and the temperature falls below +150°C (TYP).

APPLICATION INFORMATION

Output Voltage Setting

The output voltage is set using an external resistor divider as shown in **Figure 5**.

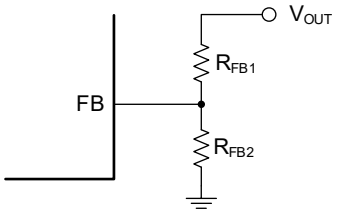


Figure 5. Output Voltage (V_{OUT}) Setting

Use Equation 4 to calculate the divider resistors for a desired output voltage (V_{OUT}). Select low tolerance resistors for the divider (1% or better) for more accurate and thermally stable output. Choose a reasonable value for R_{FB2} considering divider loss (R_{FB1} + R_{FB2} not too small) and FB leakage/bias current offsets at highest operating temperature and noise sensitivity ($R_{FB1}||R_{FB2}$ not too large). Table 1 lists some proper resistor values for more common output voltages.

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (4)$$

Table 1. Divider Resistors for Some Common Output Voltages

V_{OUT} (V)	R_{FB2} (kΩ), 1%	R_{FB1} (kΩ), 1%
3.3	12	37.4
5	12	63.4
12	12	169

Current Sensing and Limit Setting

A current sensing resistor (R_{SENSE}) should be placed in series with the inductor on the load side. R_{SENSE} value is selected based on the desired current limit threshold. Use Equation 5 to find the proper R_{SENSE} value based on the desired peak inductor current (I_{PK}) and the current limit sense voltage selected by ILIM pin as described below. R_{SENSE} is typically selected in the 5mΩ to 50mΩ range.

$$R_{SENSE} = \frac{V_{ILIM}}{I_{PK}} \quad (5)$$

The ILIM pin can be connected to ground, VCC1 or kept floating to set three fixed V_{ILIMIT} values of 27mV, 52mV and 78mV.

Switching Frequency Selection

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate charge losses and lower frequency requires larger inductance and capacitances and results in larger overall physical size and higher cost. Therefore, a tradeoff is needed between losses and component size. If the application is noise-sensitive to a frequency range, the frequency should be selected out of that range.

The switching frequency of the SGM63600 can be set between 100kHz to 1000kHz using a resistor placed between FREQ and SGND pins. Equation 6 can be used to calculate the R_{FREQ} to set the desired operating frequency to f_{SW}.

$$R_{FREQ}\ (k\Omega) = \frac{20000}{f_{SW}\ (kHz)} - 1 \quad (6)$$

As an example, for f_{SW} = 500kHz a 39kΩ resistor can be chosen for R_{FREQ}. The resistor values for some common frequencies are given in Table 2. The SGM63600 does not work if the FREQ pin is floating, and the switching frequency is out of the normal frequency range if the FREQ pin is shorted to GND.

Table 2. R_{FREQ} Values for Some Switching Frequencies

Frequency (kHz)	Resistor (kΩ)
300	65
500	39
1000	19

APPLICATION INFORMATION (continued)

Powering VCC1 Regulator

The internal VCC1 regulator can be powered from both VIN and VCC2 as shown in Figure 6. Powering from VCC2 with a proper voltage improves the regulator efficiency. VCC2 voltage should be between 4.7V to 32V.

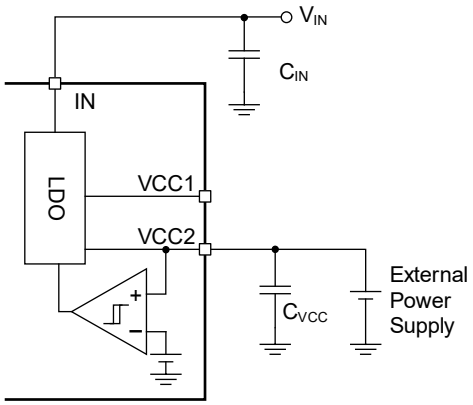


Figure 6. Connecting VCC2 External Supply for More Efficient Powering of the Device (VCC1 Regulator)

If V_{OUT} is between 4.7V and 32V, the VCC2 can be connected to V_{OUT} through 5.1Ω resistor as shown in Figure 7.

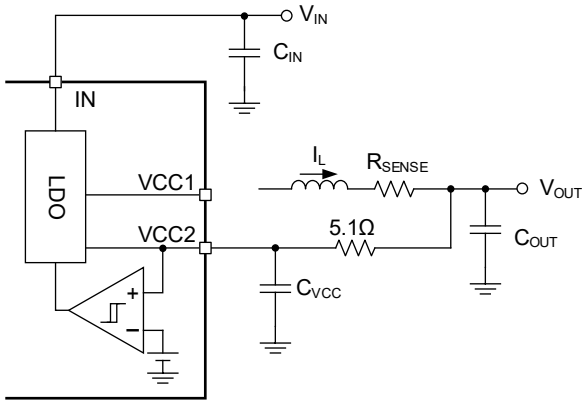


Figure 7. Powering VCC2 from V_{OUT}

Inductor

The inductance is typically selected such that the current peak-to-peak ripple (ΔI_L) is between 20% to 40% of the load current. The DC current rating of the selected inductor should be at least 25% above the maximum load current. The inductor saturation current must be high enough such that it does not saturate in any normal or transient operating condition. Use Equation 7 to calculate the inductance. ΔI_L can be selected equal to 30% of maximum load current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S} \quad (7)$$

The maximum inductor peak current for a given load current (I_{LOAD}) is calculated by Equation 8:

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (8)$$

Input Capacitor (C_{IN})

The input capacitor is necessary to circulate the high frequency ripples and switching currents of the converter and keep them away from the input line and the source. The input voltage ripple must be small enough to avoid device malfunctions. The selected capacitors must have enough RMS current rating to absorb all AC currents on the input. Equation 9 can be used to calculate the input capacitor current ripple:

$$I_{RMS} = I_{LOAD} \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case occurs at 50% duty cycle where $V_{IN} = 2 \times V_{OUT}$, resulting in $I_{RMS} = I_{LOAD}/2$.

Output Capacitor (C_{OUT})

The output capacitor is designed based on the required output voltage ripple, stability, and transient response peaks and settling times. C_{OUT} impedance must be lower than the load at the switching frequency. The output voltage ripple is estimated from Equation 10:

$$\Delta V_{OUT} \approx \frac{V_{OUT}}{L \times f_S} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_S}\right) \quad (10)$$

R_{ESR} is the equivalent series resistance (ESR) of the capacitor. For tantalum or electrolytic capacitors, the ESR is high and dominates the capacitor impedance at the switching frequency, so, the ripple can be approximated by Equation 11 for high ESR capacitors:

$$\Delta V_{OUT} \approx \frac{V_{OUT}}{L \times f_S} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

APPLICATION INFORMATION (continued)

Compensation Network

The SGM63600 is a current-mode controller that simplifies compensation and provides faster transient response compared to the voltage mode control. The COMP pin is the error amplifier output and controls stability and loop response. A series RC network sets a pole-zero combination and determines control loop characteristics. The DC gain of the voltage feedback loop is shown in Equation 12:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_O \times \frac{V_{FB}}{V_{OUT}} \quad (12)$$

where A_O = 3000V/V (70dB) is the error-amplifier voltage gain, G_{CS} is the current-sense transconductance (1/(13 × R_{SENSE}) in A/V), and R_{LOAD} is the load resistance.

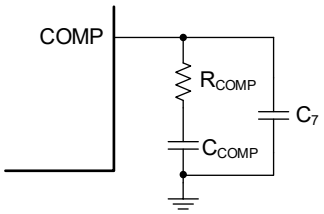


Figure 8. SGM63600 External Compensation

This system has two poles. One is determined by the compensation network (C_{COMP} in Figure 8 and the EA output conductance) and the other one is determined by the converter and load (C_{OUT} and R_{LOAD}), as given in Equation 13:

$$f_{P1} = \frac{G_m}{2\pi \times C_{COMP} \times A_O} \quad (13)$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (14)$$

where G_m is the error-amplifier transconductance (G_m = 500μA/V), R_{LOAD} is the load resistor and C_{OUT} is the output capacitor.

One important zero is caused by the compensator (C_{COMP} and R_{COMP}) and is located at:

$$f_{Z1} = \frac{1}{2\pi \times C_{COMP} \times R_{COMP}} \quad (15)$$

A large ESR creates another zero at:

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (16)$$

If the ESR is large, the effect of this zero can be compensated by adding C_7 to the compensation network that places a third pole at:

$$f_{P3} = \frac{1}{2\pi \times C_7 \times R_{COMP}} \quad (17)$$

The main goal of the compensation network is to adjust the shape of the converter transfer function to get a desired loop gain. The crossover frequency at which the loop gain is 1 (0dB) is an important factor that determines the bandwidth (how fast is the converter transient response). Setting the crossover at a too high frequency, results in instability.

For design, the crossover frequency is initially set to around 10% of the switching frequency (0.1 × f_S) and then the following steps are taken to design the compensation network with the sufficient phase margin:

1. Select R_{COMP} based on the desired crossover frequency (f_C) value:

$$R_{COMP} = \frac{2\pi \times C_{OUT} \times f_C}{G_m \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (18)$$

2. Select C_{COMP} to get sufficient phase margin. In the applications using typical inductor values, placing the compensation zero (f_{Z1}) at f_{Z1} < 0.25 × f_C would be sufficient and C_{COMP} can be calculated using Equation 19:

$$C_{COMP} > \frac{4}{2\pi \times R_{COMP} \times f_C} \quad (19)$$

3. Use C_7 if the ESR zero is located below f_S/2. This condition is valid if Equation 20 is true:

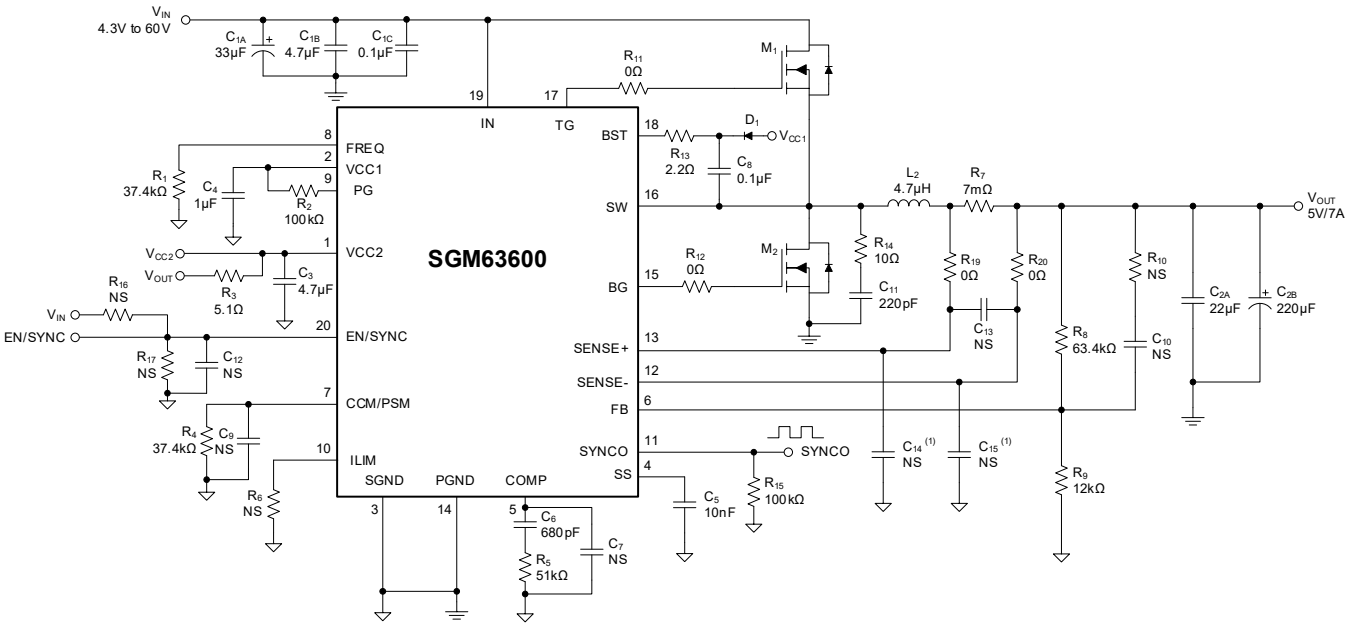
$$\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} < \frac{f_{SW}}{2} \quad (20)$$

In this case, choose C_7 from Equation 21 to set a pole (f_{P3}) over the ESR zero:

$$C_7 = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}} \quad (21)$$

APPLICATION INFORMATION (continued)

Typical Application Circuit



NOTE: 1. The recommended values for C_{14} and C_{15} are 10nF in TSSOP package.

Figure 9. Application Circuit for 5V Output

LAYOUT DESIGN

PCB layout is an important part of the converter design. A weak layout can results in poor performance, resistive losses, EMI issues and instability problems. The following guidelines are helpful for designing a good layout for the SGM63600:

1. Place the input capacitor as close as possible to the switches (drain of the high-side switch and the source of the low-side switch) to keep the input AC current loop as small as possible.

2. The SW node trace area should be as short as possible and wide enough to carry the switch currents. Keep them away from sensitive traces such as feedback resistors and traces.

3. Use small size high frequency decoupling capacitors near input and ground pins.

4. Sensitive signals and feedback loop should be away from noisy traces and components such as SW node, gate driver and switching side of the inductor body. Place divider resistor as close as possible to the FB and SGND pins.

5. Route the SENSE+, SENSE- as paired traces with smallest distance and loop area. Use a filter capacitor across sense signals close to the IC pins. Place two capacitors separately. One is between the SENSE+ pin and SGND, and the other is between the SENSE- pin and SGND. These two filter capacitors also should be close to the IC pins.

6. Use a short and wide shunt resistor for current sensing.

7. Place decoupling capacitors on VCC1 and VCC2 as close as possible to those pins.

8. Route the gate drive traces as straight as possible. The traces that carry forward and return currents must be close together (side-by-side on a single layer or over each other on adjacent layers) to minimize the gate drive path parasitic inductance.

9. SGND and PGND are connected to a single point on the exposed pad of the IC.

10. The ground connection between the input capacitor and the IC must be kept as short as possible. It is recommended to use vias to connect large copper planes on other layers for a more efficient ground connection between the ground of the input capacitor and the ground of the IC.

11. Use large copper areas on all layers and stich them with thermal vias for better heat transfer and dissipation especially for heavy load applications.

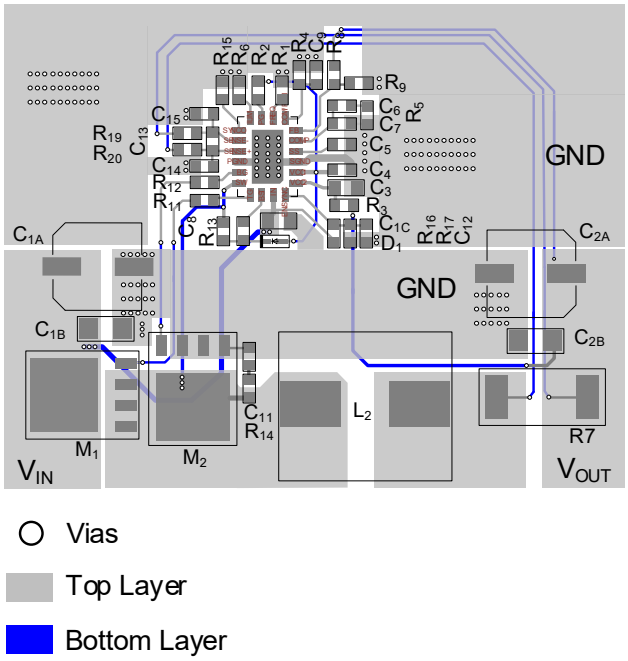


Figure 10. Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

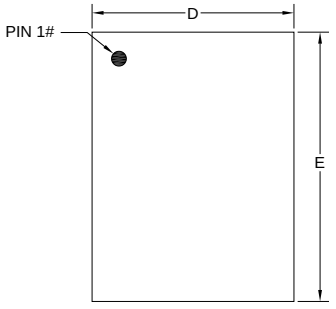
NOVEMBER 2023 – REV.A.1 to REV.A.2	Page
Added TSSOP package	3, 5, 22, 25

AUGUST 2023 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	9
Updated Application Information section	22
Updated Layout Design section	23

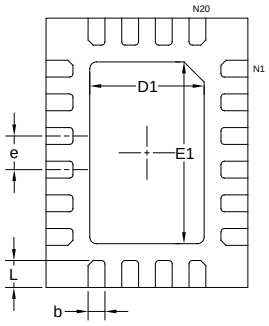
Changes from Original (MAY 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

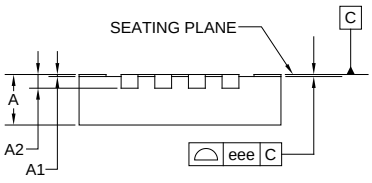
TQFN-3×4-20L



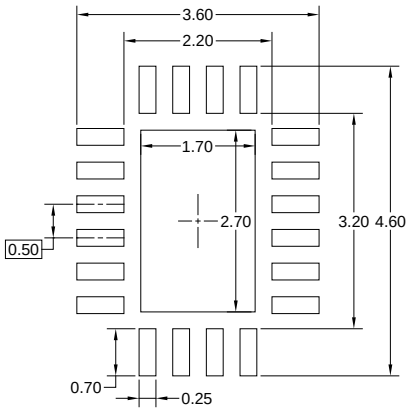
TOP VIEW



BOTTOM VIEW



SIDE VIEW



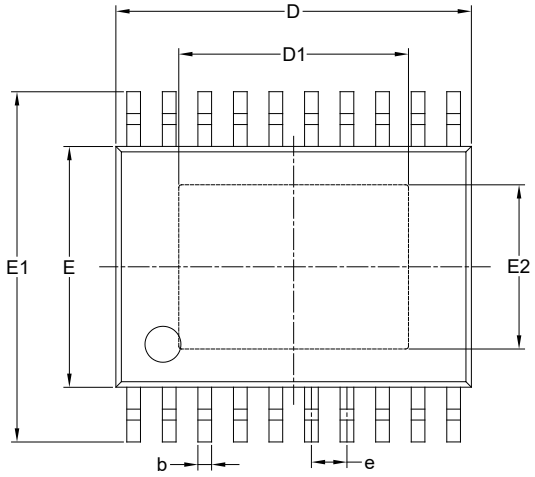
RECOMMENDED LAND PATTERN (Unit: mm)

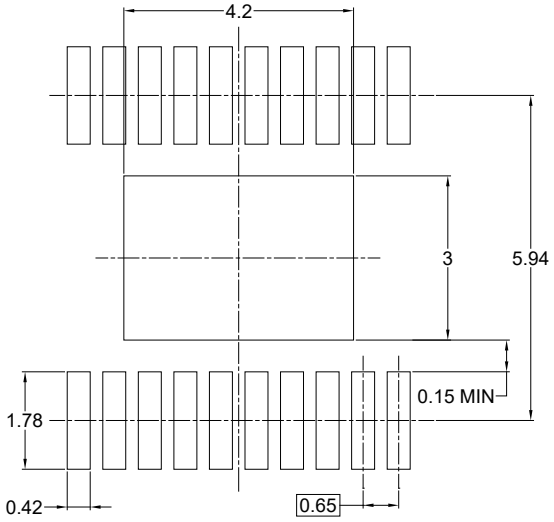
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	2.900	3.000	3.100
E	3.900	4.000	4.100
D1	1.600	1.700	1.800
E1	2.600	2.700	2.800
L	0.300	0.400	0.500
e	0.500 BSC		
eee	0.080		

NOTE: This drawing is subject to change without notice.

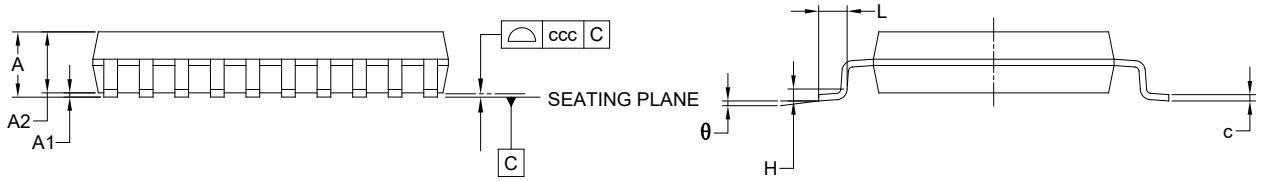
PACKAGE OUTLINE DIMENSIONS

TSSOP-20 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

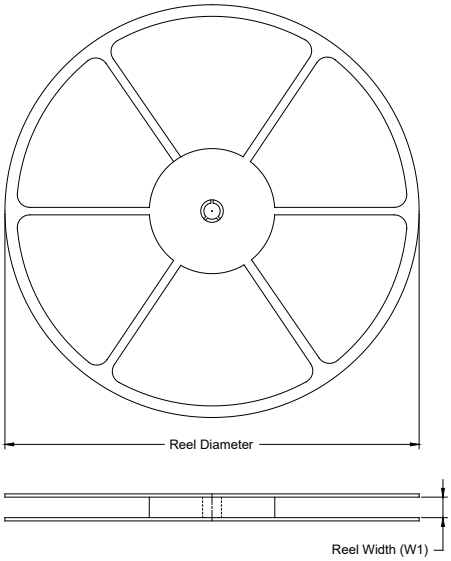


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.000	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
D1	4.000	-	4.400
E	4.300		4.500
E1	6.200	-	6.600
E2	2.800	-	3.200
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

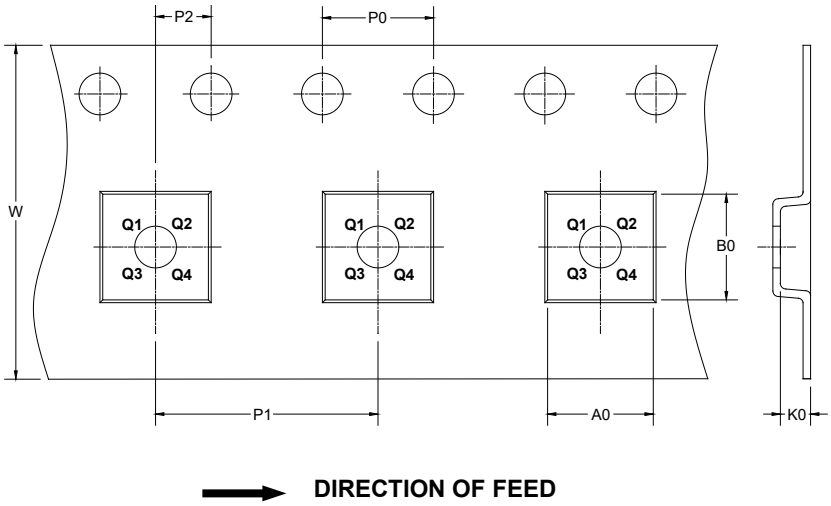
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



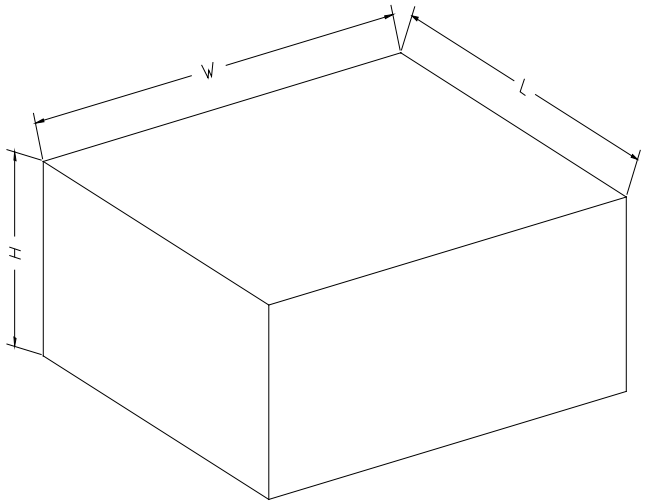
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-20L	13″	12.4	3.40	4.40	1.10	4.0	8.0	2.0	12.0	Q1
TSSOP-20 (Exposed Pad)	13"	16.4	6.80	6.90	1.50	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002