SGM6611
12.6V, 7A Fully-Integrated Synchronous Boost Converter

GENERAL DESCRIPTION

The SGM6611 family includes the SGM6611A and the SGM6611B. The SGM6611 is a fully-integrated synchronous Boost converter. The 2.7V to 12V operating input voltage is suitable for single-cell or two-cell Li-Ion/Polymer batteries. This device is capable of providing 7A continuous switch current and an output voltage range of 4.5V to 12.6V. It also has an adjustable switching frequency ranging from 200kHz to 2.2MHz.

The SGM6611 family has two operation modes, the pulse width modulation (PWM) mode and pulse frequency modulation (PFM). The SGM6611 family adopts the PWM mode at moderate to heavy load. The PFM mode is applied at light load by SGM6611A to improve the efficiency. However, the SGM6611B still adopts the PWM mode to prevent the device from low switching frequency faults. The protection features include output over-voltage protection at 13.2V, cycle-by-cycle over-current protection and thermal shutdown. The device also involves the functions of 4ms built-in soft-start and adjustable switch peak current limit.

The SGM6611A and SGM6611B are both available in a Green TQFN-2×2.5-11L package.

FEATURES

- **2.7V to 12V Input Voltage Range**
- **4.5V to 12.6V Output Voltage Range**
- **Up to 90% Efficiency**
  (V_{IN} = 3.3V, V_{OUT} = 9V, I_{OUT} = 2A)
- **Adjustable Peak Current Limit up to 9.5A for High Pulse Current**
- **Adjustable Switching Frequency: 200kHz to 2.2MHz**
- **4ms Built-in Soft-Start Time**
- **PFM Mode at Light Load (SGM6611A)**
- **Forced PWM Mode at Light Load (SGM6611B)**
- **13.2V Internal Output Over-Voltage Protection**
- **Over-Current Protection**
- **Thermal Shutdown**
- **Available in a Green TQFN-2×2.5-11L Package**

APPLICATIONS

Portable POS Machine
Bluetooth Speaker
E-Cigarette
Fast-Charging Power Bank

YPICAL APPLICATION

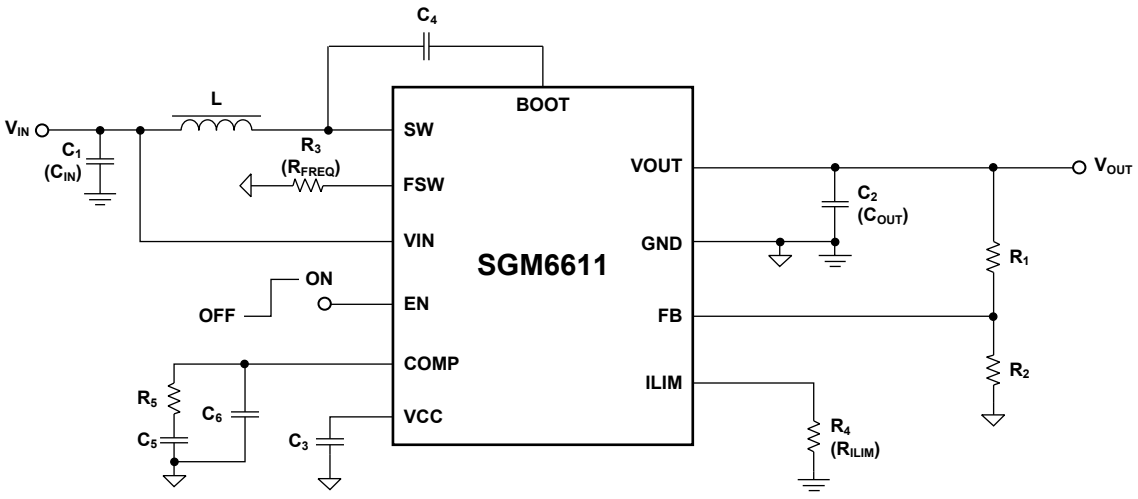


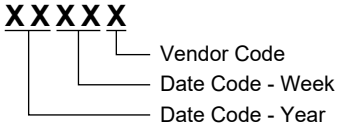
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6611A	TQFN-2×2.5-11L	-40℃ to +85℃	SGM6611AYTQV11G/TR	6611A XXXXX	Tape and Reel, 3000
SGM6611B	TQFN-2×2.5-11L	-40℃ to +85℃	SGM6611BYTQV11G/TR	6611B XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

BOOT Voltage ..... -0.3V to V_{SW} + 6V
VIN, SW, FSW, VOUT Voltages ..... -0.3V to 14.5V
EN, VCC, COMP, ILIM, FB Voltages ..... -0.3V to 6V
SW Node (Transient: 10ns) ..... -2V to 16.5V
Package Thermal Resistance
TQFN-2×2.5-11L, θ_{JA} ..... 60℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 1500V
MM 300V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.7V to 12V
Output Voltage Range ..... 4.5V to 12.6V
Inductance, Effective Value, L ..... 0.47μH to 10μH
Input Capacitance, Effective Value, C_{IN} ..... 10μF (MIN)
Output Capacitance, Effective Value, C_{OUT} ... 10μF to 1000μF
Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Ambient Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

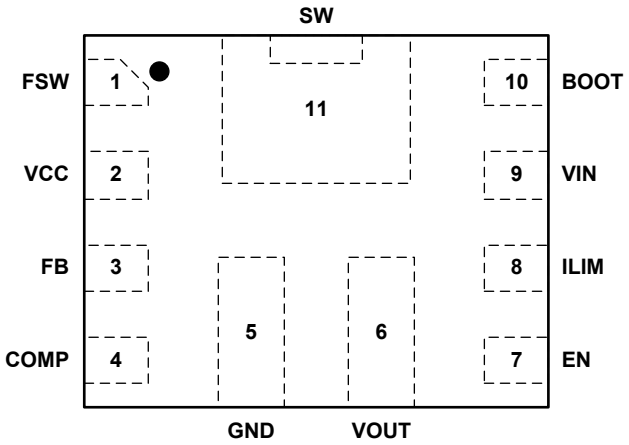
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM6611A/SGM6611B (TOP VIEW)



TQFN-2×2.5-11L

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	FSW	I	The switching frequency is programmed by a resistor between this pin and the GND pin.
2	VCC	O	Output. The VCC pin connects a ceramic capacitor (> 1.0μF) to ground.
3	FB	I	Output Voltage Feedback.
4	COMP	O	Error Amplifier Output. Connect a loop compensation network between this pin and the GND pin.
5	GND	-	Ground.
6	VOUT	O	Boost Converter Output.
7	EN	I	Enable Logic Input. Logic high makes the circuit enabled, logic low makes it disabled and the device enters shutdown mode.
8	ILIM	O	Adjustable Switch Peak Current Limit. Connect an external resistor between ILIM pin and the GND pin.
9	VIN	I	IC Power Supply Input.
10	BOOT	O	Power Supply for High-side MOSFET Gate Driver. Connect a capacitor between the BOOT pin and the SW pin.
11	SW	I	Switching Node Pin. Drain connection of low-side power MOSFET and source connection of the high-side power MOSFET.

NOTE: I = input, O = output.

ELECTRICAL CHARACTERISTICS

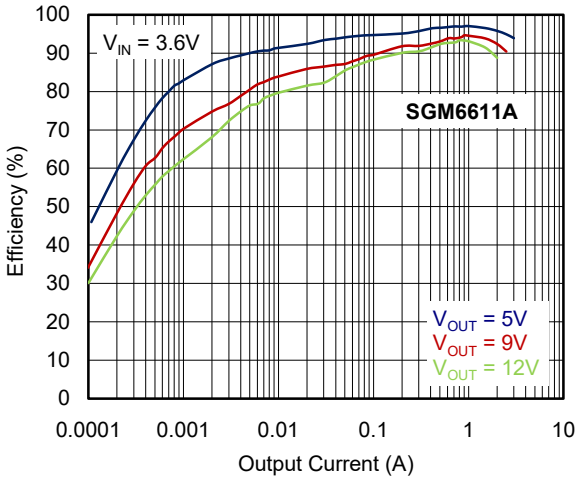
(V_{IN} = 2.7V to 5.5V, V_{OUT} = 9V. Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Power Supply								
Input Voltage Range		V_{IN}		Full	2.7		12	V
VIN Under-Voltage Lockout Threshold		V_{IN_UVLO}	V_{IN} rising	+25℃		2.5	2.62	V
			V_{IN} falling			2.4		
VIN Under-Voltage Lockout Hysteresis		V_{IN_HYS}		+25℃		100		mV
VCC Regulation		V_{CC}	I_{CC} = 2mA, V_{IN} = 8V	+25℃		5		V
VCC Under-Voltage Lockout Threshold		V_{CC_UVLO}	V_{CC} falling	+25℃		2.1		V
Operating Quiescent Current	VIN Pin	I_Q	IC enabled, no load, V_{FB} = 1.3V, V_{OUT} = 12V	+25℃		0.23	0.4	μA
	VOUT Pin					90	130	
Shutdown Current into the VIN Pin		I_{SHDN}	IC disabled	+25℃		0.6	1.1	μA
Output								
Output Voltage Range		V_{OUT}		Full	4.5		12.6	V
Reference Voltage at the FB Pin		V_{REF}	PWM mode	Full	1.181	1.205	1.229	V
			PFM mode	+25℃		1.207		
Leakage Current into the FB Pin		I_{FB_LKG}	V_{FB} = 1.2V	+25℃		10	100	nA
Output Over-Voltage Protection Threshold		V_{OVP}	V_{OUT} rising	Full	12.95	13.2	13.55	V
Output Over-Voltage Protection Hysteresis		V_{OVP_HYS}	V_{OUT} falling below V_{OVP}	+25℃		0.15		V
Soft Startup Time		t_{SS}	C_{OUT} (effective) = 47μF, I_{OUT} = 0A	+25℃		4		ms
Error Amplifier								
COMP Pin Sink Current		I_{SINK}	V_{FB} = V_{REF} + 100mV, V_{COMP} = 1.2V	+25℃		120		μA
COMP Pin Source Current		I_{SOURCE}	V_{FB} = V_{REF} - 100mV, V_{COMP} = 1.2V	+25℃		15		μA
High Clamp Voltage at the COMP Pin		V_{CCLPH}	V_{FB} = 1.1V, R_{ILIM} = 127kΩ	+25℃		2.0		V
Low Clamp Voltage at the COMP Pin		V_{CCLPL}	V_{FB} = 1.3V, R_{ILIM} = 127kΩ	+25℃		0.4		V
Error Amplifier Transconductance		G_{EA}	V_{COMP} = 1.2V	+25℃		135		μS
Power Switch								
High-side MOSFET On-Resistance		$R_{DS(ON)}$	V_{CC} = 5V	+25℃		27	34	mΩ
Low-side MOSFET On-Resistance			V_{CC} = 5V	+25℃		15	20	mΩ
Switching Frequency								
Switching Frequency		f_{SW}	R_{FREQ} = 301kΩ	+25℃	440	470	500	kHz
			R_{FREQ} = 46.4kΩ	+25℃		2200		kHz
Minimum On-Time		t_{ON_MIN}	V_{CC} = 5V	+25℃		120		ns
Current Limit								
Switch Peak Current Limit (SGM6611A)		I_{LIM}	R_{ILIM} = 127kΩ	+25℃	8.5	9.5	10.8	A
Reference Voltage at the ILIM Pin		V_{ILIM}		+25℃		1.205		V
EN Logic Input								
EN Logic High Threshold		V_{ENH}		Full	1.2			V
EN Logic Low Threshold		V_{ENL}		Full			0.4	V
EN Pull-Down Resistor		R_{EN}		+25℃		800		kΩ
Thermal Shutdown								
Thermal Shutdown Threshold		T_{SD}	T_A rising			160		℃
Thermal Shutdown Hysteresis		T_{SD_HYS}	T_A falling below T_{SD}			20		℃

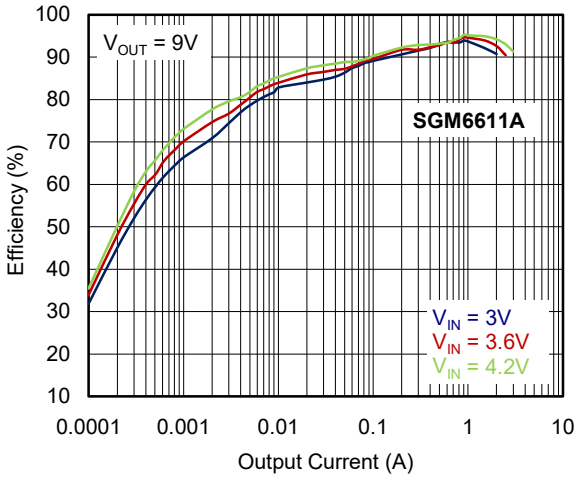
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 9V, unless otherwise noted.

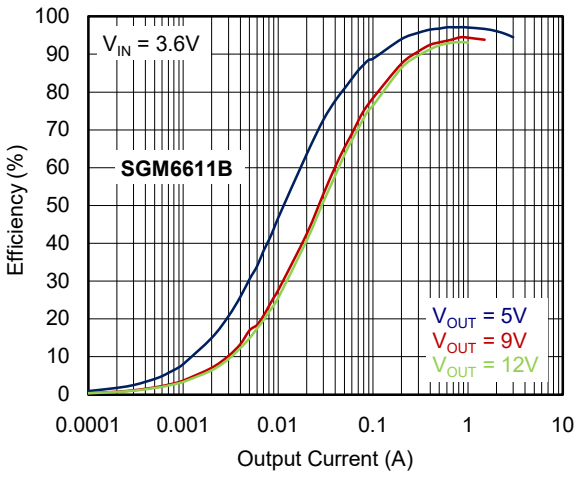
Efficiency vs. Output Current



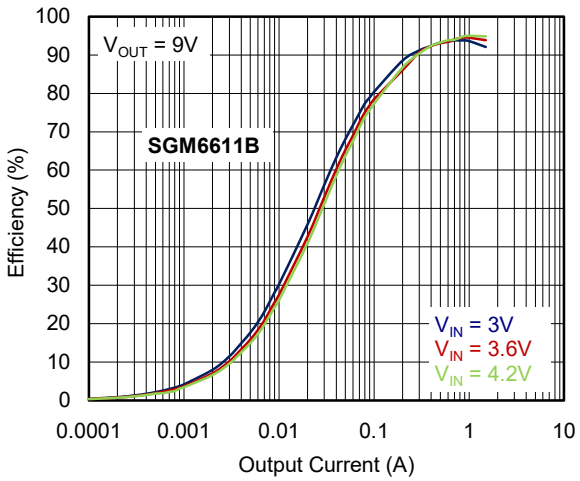
Efficiency vs. Output Current



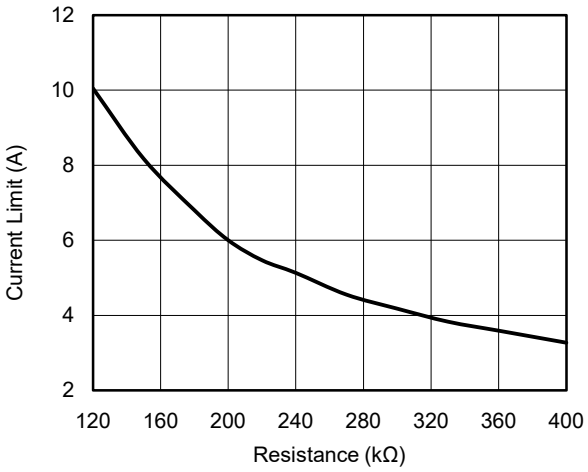
Efficiency vs. Output Current



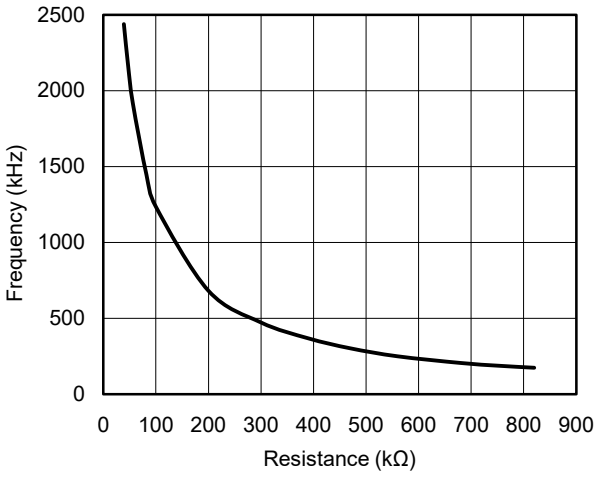
Efficiency vs. Output Current



Current Limit vs. Setting Resistance



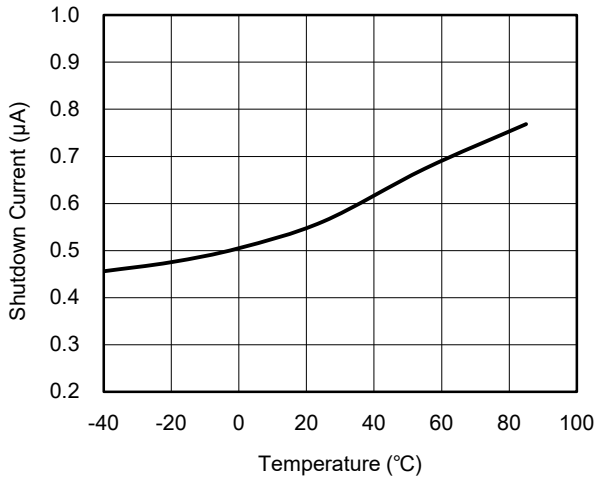
Switching Frequency vs. Setting Resistance



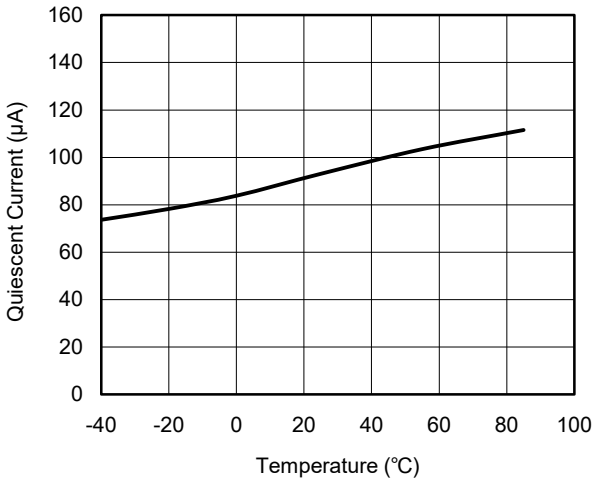
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 9V, unless otherwise noted.

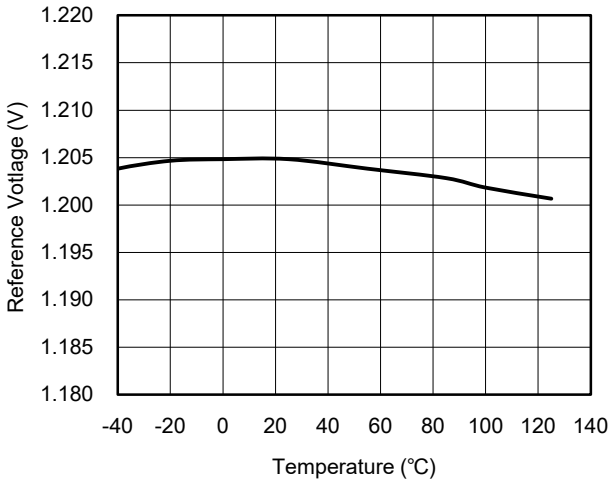
Shutdown Current vs. Temperature



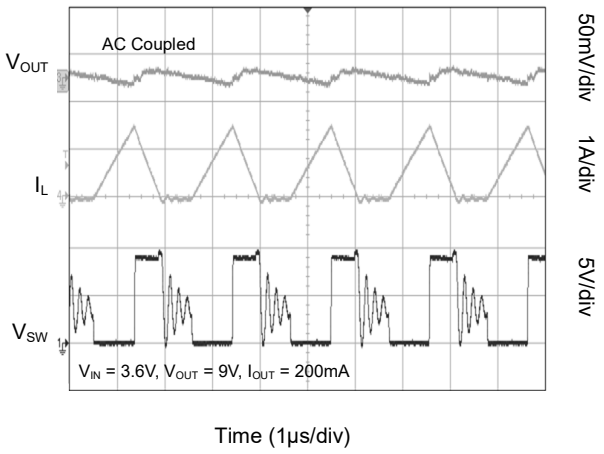
Quiescent Current vs. Temperature



Reference Voltage vs. Temperature



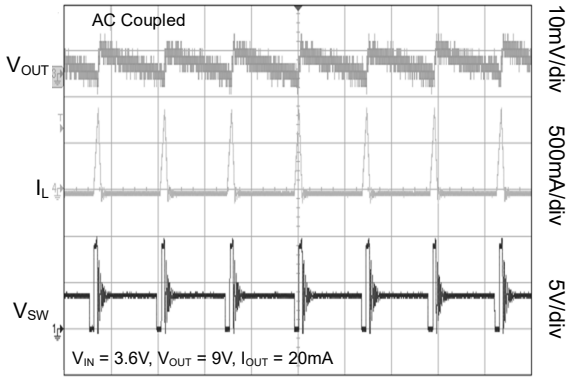
Switching Waveforms in PFM Mode



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

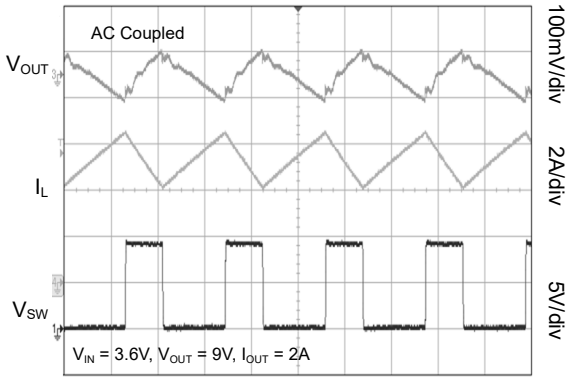
At T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 9V, unless otherwise noted.

Switching Waveforms in DCM



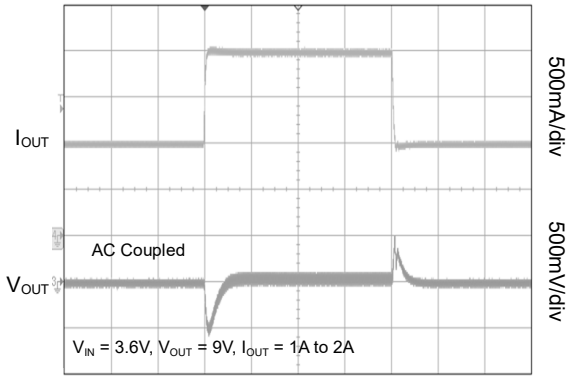
Time (1μs/div)

Switching Waveforms in CCM



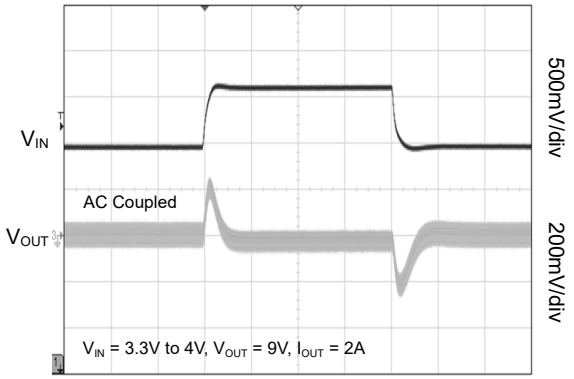
Time (1μs/div)

Load Transient Response



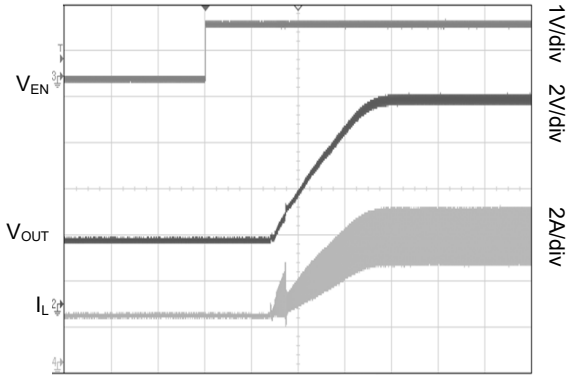
Time (500μs/div)

Line Transient Response



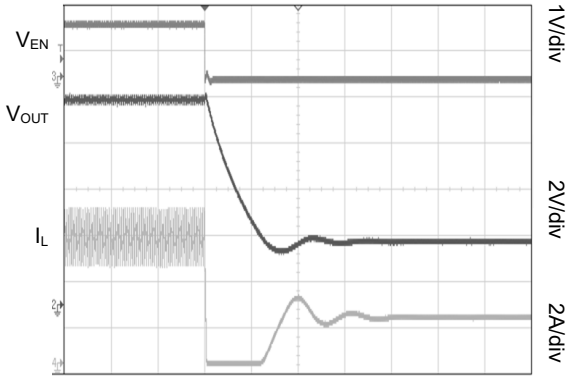
Time (500μs/div)

Startup Waveforms



Time (1ms/div)

Shutdown Waveforms



Time (50μs/div)

FUNCTIONAL BLOCK DIAGRAM

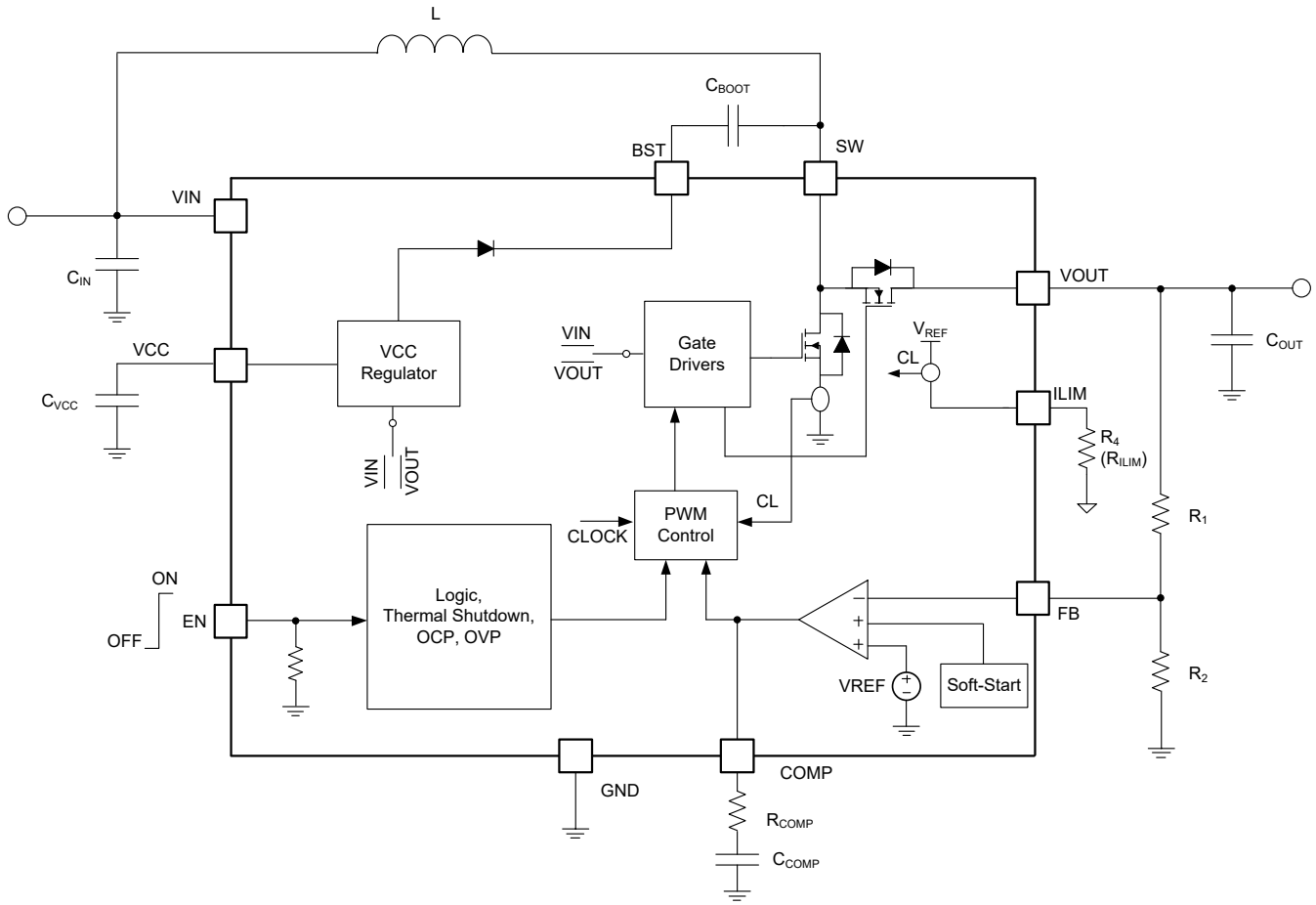


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM6611 family is a synchronous Boost converter with two integrated power FETs and is capable of delivering up to 9.5A (TYP) switch current. The device has adjustable switching frequency ranging from 200kHz to 2.2MHz. The SGM6611 automatically operates in pulse frequency modulation (PFM) mode at light load to improve the efficiency. In moderate to heavy load conditions, SGM6611 works at a constant frequency pulse width modulation (PWM) mode. In light load condition, the SGM6611A works in pulse frequency modulation (PFM) mode and the SGM6611B works in forced PWM (FPWM) mode. The device provides excellent line and load transient responses, in addition, the compensation network is configured externally which brings flexibility to applications with different inductor and output capacitor selections. The device also implements various protection features such as cycle-by-cycle current limit for abnormal load conditions, output over-voltage protection and thermal shutdown.

Enable and Disable

The input voltage applied to SGM6611 needs to be higher than the maximum UVLO threshold of 2.5V and the EN pin voltage is higher than 1.2V to enable the device. Pulling the EN pin below 0.4V disables the device, where all internal blocks are turned off, and no voltage is present on VCC pin. While disabled, the device stops switching and enters shutdown mode, which only consumes less than 1.1μA current. VIN and VOUT are connected through the body diode of the high-side rectifier FET in the shutdown mode.

Adjustable Switching Frequency

SGM6611 also has an adjustable switching frequency ranging from 200kHz to 2.2MHz. A resistor between the FSW pin and the GND pin is used to set the switch frequency. And do not leave the FSW pin open. Equation 1 is used to calculate the resistor.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \right)}{C_{FREQ}} \quad (1)$$

where R_{FREQ} is the resistor connected between the FSW pin and the GND pin, C_{FREQ} = 30pF, t_{DELAY} = 86ns, and f_{SW} is the desired switching frequency.

Adjustable Peak Current Limit

The peak current mode control provides inherent over-current protection as the device monitors the changes of inductor current. As the peak current reaches 9.5A (TYP), the device stops switching and turning off the low-side FET to stop inductor current to rise. The peak current limit threshold is programmable via a resistor connected on ILIM pin to ground. Use Equation below to calculate the desired current limit threshold.

$$I_{LIM} = \frac{1.2 \times 10^6}{R_{ILIM}} \quad (2)$$

where R_{ILIM} is the resistor connected between the ILIM pin and ground, and I_{LIM} is the switch peak current limit.

When I_{LIM} is 9.5A (TYP), the resistor value for SGM6611A is 127kΩ.

Soft-Start

The SGM6611 implements internal soft-start function of 4ms (TYP). When enabled, the device slowly ramps the reference voltage to prevent large inrush current during startup.

Under-Voltage Lockout (UVLO)

An under-voltage lockout (UVLO) circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The SGM6611 has both VIN UVLO function and VCC UVLO function. It disables the device from switching when the falling voltage at the VIN pin trips the UVLO threshold V_{IN_UVLO}, which is typically 2.4V. The input UVLO function implements a 100mV hysteresis to prevent the false turn-on due to line voltage variations, where the device cannot be turned on until the input voltage increases to 2.5V or higher. When the falling voltage at the VCC pin trips the UVLO threshold V_{CC_UVLO}, typically 2.1V, the device is also disabled.

Over-Voltage Protection (OVP)

The device implements over-voltage protection to prevent the device from damage and protect the device connected to the output of SGM6611. When the voltage present on the VOUT pin exceeds 13.2V (TYP), the device stops switching immediately to prevent the output voltage from rising. As the output voltage drops below 150mV (TYP) of hysteresis voltage that is lower than the OVP threshold, the device resumes operation.

DETAILED DESCRIPTION (continued)

Thermal Shutdown

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once a junction temperature of +160℃ (TYP) is exceeded, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20℃.

Device Functional Modes

Operation

The SGM6611 adopts the fixed frequency pulse width modulation (PWM) mode in moderate to heavy load condition. At the start of each clock cycle, the low-side power FET is turned on to ramp up the inductor current until the inductor current reaches the level determined by the output of the internal error amplifier. When the current is reached, LS FET is turned off, and a dead time is issued which is used to prevent shoot-through. During the dead time, the inductor current flows through the body diode of the high-side FET. As the dead time ends, the high-side FET is turned on to ramp down the inductor current to replenish the output capacitor and deliver current to the load.

The SGM6611A operates in PFM mode for applications with high efficiency requirement at light load. And the SGM6611B operates in forced PWM mode to avoid switching noise for applications with fixed switching frequency requirement.

Forced PWM Mode

For forced PWM mode, the switching frequency of SGM6611B is fixed at light load. The internal error amplifier output drops along with the load current. When the output current further decreases, the current of the inductor can be reduced to zero during turn-off. The high-side N-MOSFET remains open even when the current is zero, with only inductor current direction changed. The efficiency is low in forced PWM mode. However, no problems are caused by the low efficiency in forced PWM mode, such as the audible noise.

PFM Mode

In order to improve the light load efficiency, the SGM6611A implements PFM operation at light load. At light load, the internal error amplifier's output decreases to lower the inductor current. As the current reaches zero during the low-side off-time, the high-side FET turns off till the next switching cycle starts. As the load current decreases further, the output of the error amplifier reaches a voltage that is corresponds to I_{LIM}/10. The output of the error amplifier is clamped at this value and no longer decreases. The SGM6611A automatically adjusts the off-time in PFM mode to meet the load demand, and lower load current results in longer off-time. The output voltage is regulated to 0.2% higher than the nominal programmed output voltage at PFM mode. The SGM6611A is capable of achieving above 70% efficiency when the load current is less than 1mA. Output voltage ripple is also lower in PFM mode since the peak inductor current is lower.

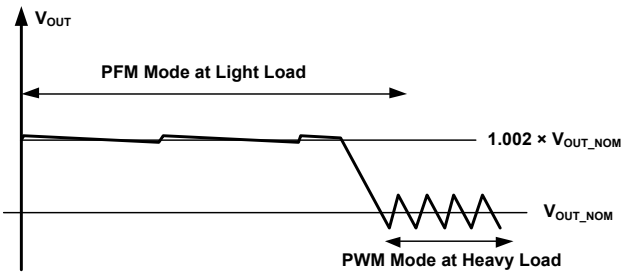


Figure 3. Output Voltage in PWM Mode and PFM Mode

APPLICATION INFORMATION

The SGM6611 family is capable of supporting up to 12.6V output voltage, while providing 9.5A (TYP) continuous switch current. At heavy load, the device works in PWM mode. At light load, the SGM6611A works in the PFM mode and the SGM6611B works in the forced PWM mode. The peak current control scheme provides excellent line and load transient responses. The external loop compensation enables design flexibility with various inductor and output capacitor combinations. It also supports adjustable switching frequency ranging from 200kHz to 2.2MHz.

Table 1. Design Parameters

Design Parameters	Example Values
Input Voltage Range	3.0V to 4.35V
Output Voltage	9V
Output Voltage Ripple	100mV peak-to-peak
Output Current Rating	2A
Operating Frequency	500kHz
Operation Mode at Light Load	PFM (SGM6611A)

Setting Switching Frequency

A resistor connected between the FSW pin and the GND pin is used to set the switching frequency. Equation 3 can be used to calculate the resistor value.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \right)}{C_{FREQ}} \quad (3)$$

where R_{FREQ} is the resistor connected between the FSW pin and the GND pin, C_{FREQ} = 30pF, t_{DELAY} = 86ns, and f_{SW} is the desired switching frequency.

Setting Peak Current Limit

The peak current limit is programmed via an external resistor on ILIM pin. The resistor value can be calculated by Equation 4:

$$I_{LIM} = \frac{1.2 \times 10^6}{R_{ILIM}} \quad (4)$$

where R_{ILIM} is the resistance connected between the ILIM pin and ground, and I_{LIM} is the switch peak current limit.

A standard 127kΩ provides the 9.5A typical current limit. Considering variation due to tolerance and temperature, the worst-case required peak current should be lower than the minimal current limit rating to ensure that the SGM6611 can regulate the output voltage. For Boost converter, the worst case occurs at the lowest VIN and the highest load current.

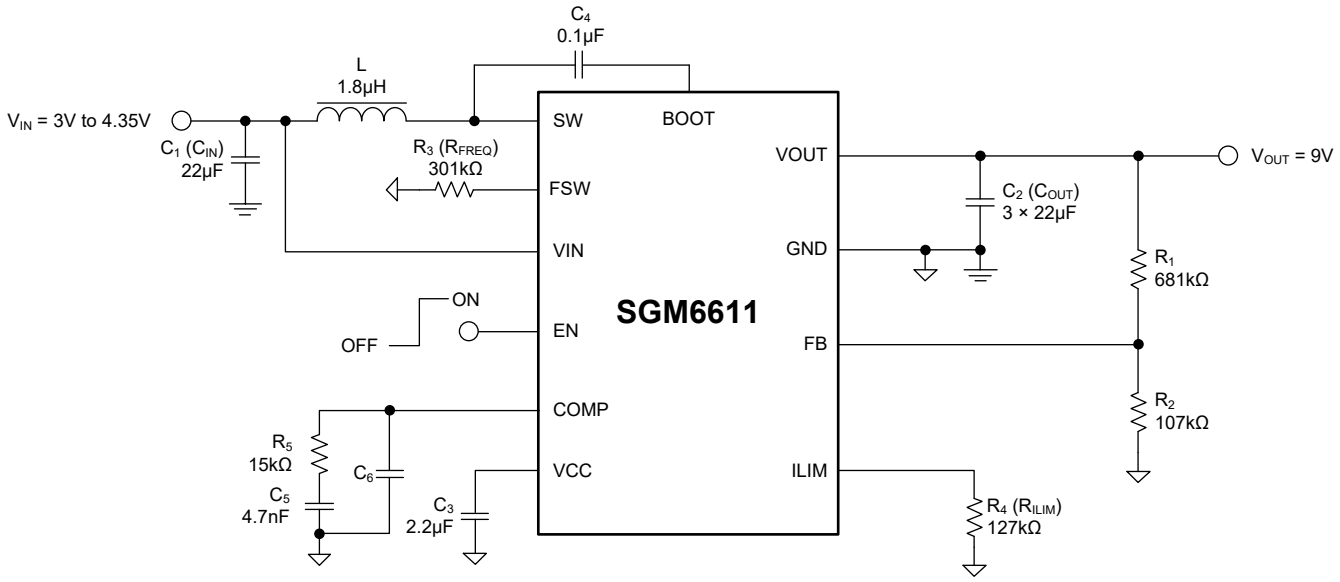


Figure 4. SGM6611 Single-Cell Li-Ion Battery to 9V/2A Output Converter

APPLICATION INFORMATION (continued)

Setting Output Voltage

The output voltage of SGM6611 is programmed by a resistive divider connected to FB pin. Use Equation below to program the output voltage. R1 is the top feedback resistor and R2 is the bottom feedback resistor. The recommended value for R2 should be less than 120kΩ.

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (5)$$

Inductor Selection

Inductor is an essential element for DC/DC switch mode power supplies regardless of topology. Inductor serves as the energy storage element for power conversion. Inductance and inductor's saturation current are the two most important criterions for inductor selection. For general rule of thumb, the selected inductance should provide a peak-to-peak ripple current that is around 30% of the average inductor current at full load and nominal input voltage. The average inductor current for a Boost converter is the input current. The SGM6611 is optimized to work with inductor values between 0.47μH and 10μH. Lower inductance part generally has smaller size while providing sufficient saturation current rating, and larger inductance provides lower peak-to-peak ripple current, which helps to maximize the output current delivery.

Equations 6 to 8 show the calculated key parameters for selecting the inductor. The selected inductor should meet the worst case that occurs at minimum input voltage and maximal load current. Margin should be added to cover inductance de-rating and conversion efficiency.

For Boost converter, the average inductor current is the average input current, Equation 6 is used to calculate the average inductor current:

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, I_{OUT} is the output current, and η is the power conversion efficiency.

Use Equation 7 below to calculate the inductor current peak-to-peak ripple.

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \quad (7)$$

where I_{PP} is the inductor peak-to-peak ripple, L is the inductor value, V_{OUT} is the output voltage, and V_{IN} is the input voltage, f_{SW} is the switching frequency.

The peak inductor current is the sum of average current plus half of the peak-to-peak inductor current shown in Equation 8:

$$I_{LPEAK} = I_{DC} + \frac{I_{PP}}{2} \quad (8)$$

The selected inductor should have the saturation current rating higher than the calculated peak current, and the calculated peak current should be lower than the peak current limit of SGM6611.

Inductor's DCR, material type, DC/DC's power FET resistance and switching speed affect the overall efficiency of the converter, therefore, careful inductor selection is critical to ensure good performance.

APPLICATION INFORMATION (continued)

Table 2 lists the recommended inductors for SGM6611.

Table 2. Recommended Inductors

Part Number	L (μH)	DCR MAX (mΩ)	Saturation Current/ Heat Rating Current (A)	Size MAX (L mm × W mm × H mm^3)	Manufacturer
CDMC8D28NP-1R8MC	1.8	12.6	9.4/9.3	9.5 × 8.7 × 3.0	Sumida
744325180	1.8	3.5	18/14	10.5 × 10.2 × 4.7	Wurth-Elektronik
744311150	1.5	7.2	14.0/11.0	7.3 × 7.2 × 4.0	Wurth-Elektronik
744311220	2.2	12.5	13.0/9.0	7.3 × 7.2 × 4.0	Wurth-Elektronik
PIMB103T-2R2MS	2.2	9.0	16/13	11.2 × 10.3 × 3.0	Cyntec
PIMB065T-2R2MS	2.2	12.5	12/10.5	7.4 × 6.8 × 5.0	Cyntec

Input Capacitor Selection

Boost converter's input capacitor has continuous current throughout the entire switching cycle. A 10μF ceramic capacitor is recommended to place between the VIN pin and GND pin of SGM6611 as close as possible. For the applications where the SGM6611 is located far away from the input source, a 47μF or higher capacitance capacitor is recommended to damp the wiring harness's inductance.

The VCC pin is the output of the internal regulator, a 1μF ceramic capacitor is recommended to place on the VCC pin.

Output Capacitor Selection

The output capacitors of Boost converter dictate the output voltage ripple and load transient response. Equation 9 is used to estimate the necessary capacitance to achieve the desired output voltage ripple, where ΔV is the maximum allowed ripple. Three 22μF ceramic output capacitors are recommended for SGM6611. Due to the DC de-rating effect of the ceramic capacitor, margin should be considered, where higher capacitance improves the transient response.

$$V_{RIPPLE\_DIS} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (9)$$

ESR of the output capacitor affects the output ripple. Use Equation 10 to calculate the output ripple caused by ESR.

$$V_{RIPPLE\_ESR} = I_{LPEAK} \times R_{ESR} \quad (10)$$

APPLICATION INFORMATION (continued)

Loop Stability

The compensation network of SGM6611 is completed externally to improve design flexibility. The SGM6611 implements a transconductance error amplifier, where the COMP pin is the output of the internal error amplifier. A Type-II compensation network consisting of R5, C5 and C6 connected on COMP pin is used to configure the loop response of SGM6611.

The power stage small signal loop response of peak current control can be modeled by Equation 11.

$$G_{PS}(S)=\frac{R_O\times(1-D)}{2\times R_{SENSE}}\times\frac{(1+\frac{S}{2\times\pi\times f_{ESRZ}})(1-\frac{S}{2\times\pi\times f_{RHPZ}})}{1+\frac{S}{2\times\pi\times f_P}} \quad (11)$$

where R_O is the output load resistance, D is the switching duty cycle, R_{SENSE} is the equivalent internal current sense resistor, which is 0.08Ω, f_P is the pole's frequency, f_{ESRZ} is the zero's frequency, and f_{RHPZ} is the right-half-plane-zero's frequency.

The D, f_P, f_{ESRZ} and f_{RHPZ} can be calculated by following equations.

$$D=1-\frac{V_{IN}\times\eta}{V_{OUT}} \quad (12)$$

where η is the power conversion efficiency.

$$f_P=\frac{2}{2\pi\times R_O\times C_{OUT}} \quad (13)$$

where C_{OUT} is effective capacitance of the output capacitor.

$$f_{ESRZ}=\frac{1}{2\pi\times R_{ESR}\times C_{OUT}} \quad (14)$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ}=\frac{R_O\times(1-D)^2}{2\pi\times L} \quad (15)$$

Equation 16 shows the small signal transfer function of the compensation network.

$$G_C(S)=\frac{G_{EA}\times R_{EA}\times V_{REF}}{V_{OUT}}\times\frac{(1+\frac{S}{2\times\pi\times f_{COMZ}})}{(1+\frac{S}{2\times\pi\times f_{COMP1}})(1+\frac{S}{2\times\pi\times f_{COMP2}})} \quad (16)$$

where G_{EA} is the amplifier's transconductance, R_{EA} is the amplifier's output resistance, V_{REF} is the reference voltage at the FB pin, V_{OUT} is the output voltage, f_{COMP1}, f_{COMP2} are the pole's frequency of the compensation network, and f_{COMZ} is the zero's frequency of the compensation network.

Once the error amplifier and power stage's poles and zeros are determined, the compensation network's component value can be designed. The designed loop crossover frequency f_C should be within 1/5 of the RHPZ frequency (f_{RHPZ}) or 1/10 of the switching frequency. Higher crossover frequency could improve the transient response. However, the crossover frequency should be designed to avoid instability.

With a selected f_C, use Equation 17 to calculate the required R5.

$$R_5=\frac{2\pi\times V_{OUT}\times R_{SENSE}\times f_C\times C_{OUT}}{(1-D)\times V_{REF}\times G_{EA}} \quad (17)$$

Equation 18 is used to calculate the value of C_5.

$$C_5=\frac{R_O\times C_{OUT}}{2R_5} \quad (18)$$

Equation 19 is used to calculate the value of C_6.

$$C_6=\frac{R_{ESR}\times C_{OUT}}{R_5} \quad (19)$$

For application with only ceramic capacitor, or if the value of C_6 is less than 10pF after calculation, C_6 is not needed.

To measure good loop compensation design, greater than 45° of phase margin and greater than 10dB gain margin could provide good loop stability and avoid output voltage ringing during load and line transient.

APPLICATION INFORMATION (continued)

Layout Guidelines

In addition to component selection, layout is a critical step to ensure the performance of any switch mode power supplies. Poor layout could result in system instability, EMI failure, and device damage. Thus, place the inductor, input and output capacitors as close to the IC as possible, and use wide and short traces for current carrying traces to minimize PCB inductance.

For Boost converter, the output capacitor's current loop from VOUT pin back to the GND pin of the device should be as small as possible. Use small traces and small copper area of all traces connected to the SW node to minimize SW node vias and to prevent radiation of high-frequency noise. It is also recommended to place a ground plane below the DC/DC to minimize inter plane coupling.

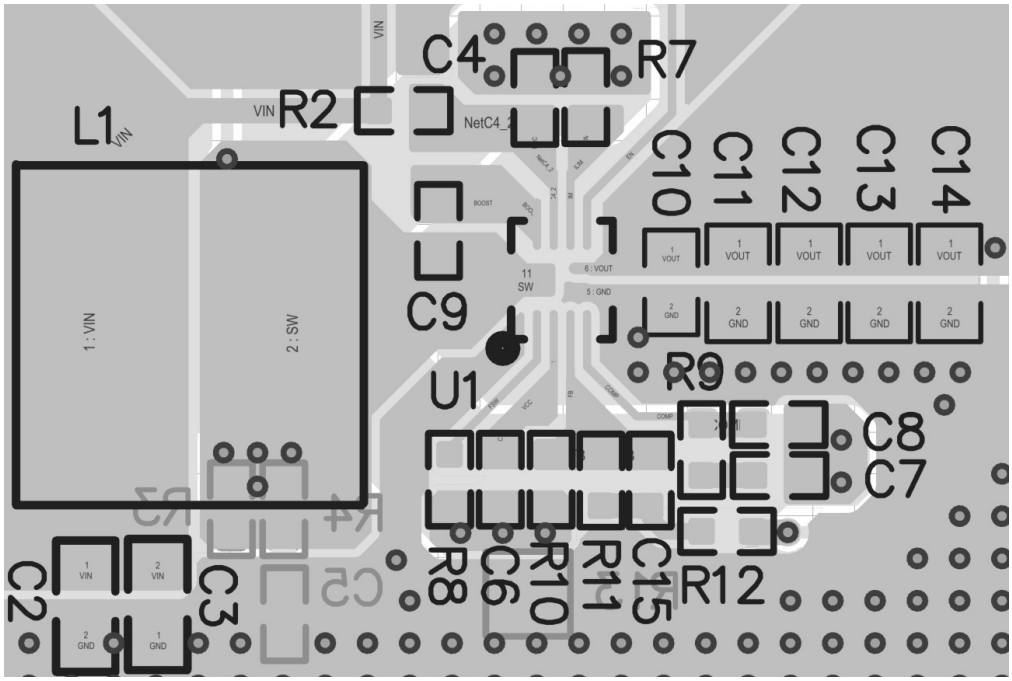


Figure 5. Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2022 – REV.A.4 to REV.B **Page**

Updated Equations 1 and 3, C_{FREQ}, t_{DELAY} 9, 11

JULY 2022 – REV.A.3 to REV.A.4 **Page**

Added SW Node in Absolute Maximum Ratings 2
Updated Detailed Description and Application Information sections 9, 10, 11, 12, 13

OCTOBER 2021 – REV.A.2 to REV.A.3 **Page**

Updated the Enable and Disable section 9
Added the Figure 5. Layout Example 15

APRIL 2021 – REV.A.1 to REV.A.2 **Page**

Updated Loop Stability section 14

MARCH 2021 – REV.A to REV.A.1 **Page**

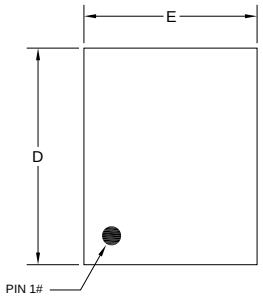
Updated Package Outline Dimensions section 17

Changes from Original (JULY 2018) to REV.A

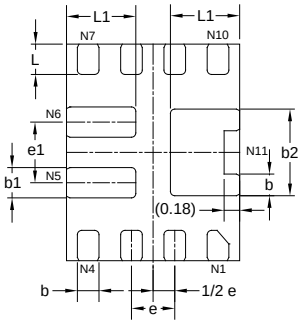
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

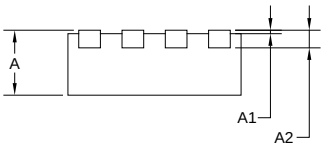
TQFN-2×2.5-11L



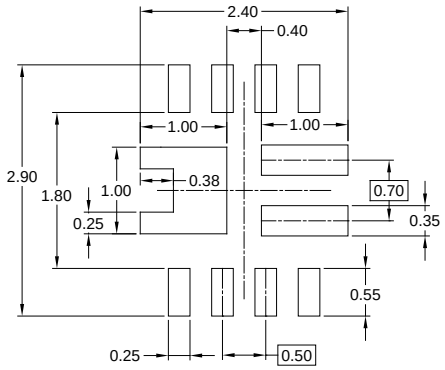
TOP VIEW



BOTTOM VIEW



SIDE VIEW



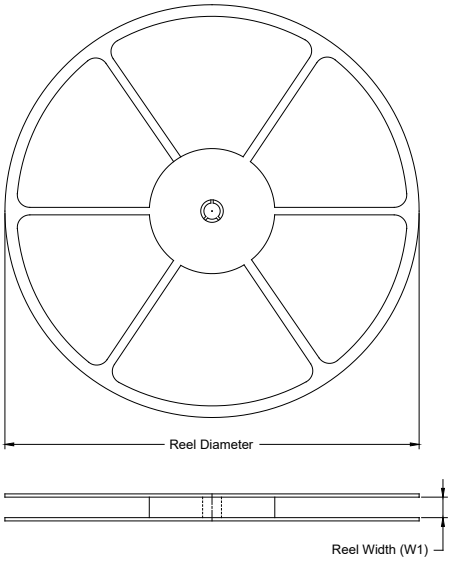
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A2	0.203 REF		
D	2.400	2.500	2.600
E	1.900	2.000	2.100
e	0.500 BSC		
e1	0.700 BSC		
b	0.200	0.250	0.300
b1	0.300	0.350	0.400
b2	0.950	1.000	1.050
L	0.300	0.350	0.400
L1	0.750	0.800	0.850

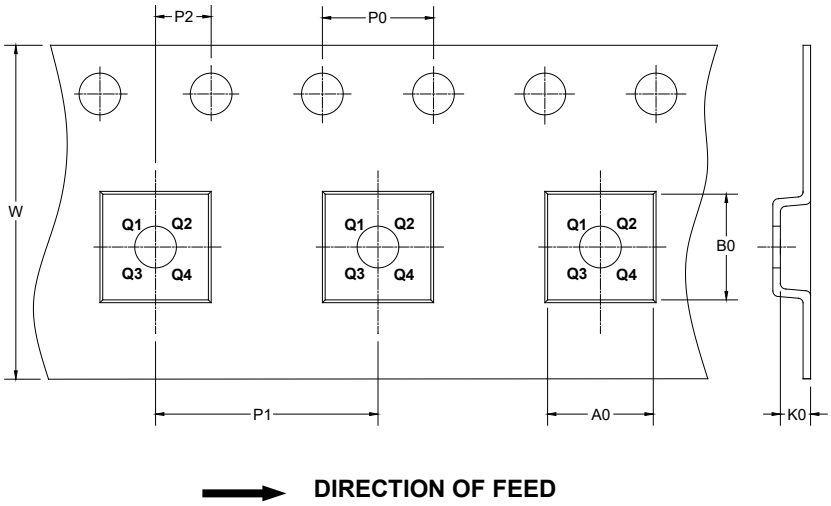
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



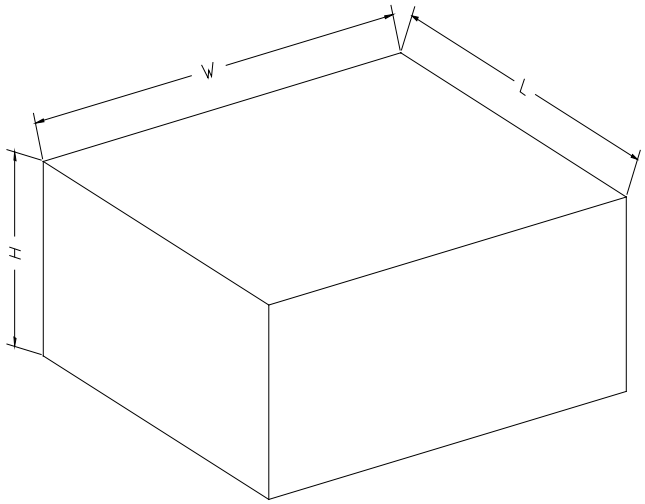
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2.5-11L	7″	9.5	2.20	2.70	0.95	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002