SGM7220
USB Type-C Configuration Channel Logic and Port Control

GENERAL DESCRIPTION

The SGM7220 enables USB Type-C ports with the Configuration Channel (CC) logic needed for Type-C interface. The SGM7220 uses the CC pins to determine port attachment and detachment, cable orientation, role detection and port control for Type-C current mode. The SGM7220 can be configured as a downstream facing port (DFP), an upstream facing port (UFP) or a dual role port (DRP) making it ideal for most applications.

The SGM7220 alternates configuration as a DFP or an UFP according to the Type-C specifications. The CC logic block monitors the CC1 and CC2 pins for pull-up or pull-down resistances to determine when a USB port has been attached, the orientation of the cable and the role detected. The CC logic detects the Type-C current mode as default, medium or high depending on the role detected. V_{BUS} detection is implemented to determine a successful attachment in UFP and DRP modes.

The SGM7220 operates over a wide supply range and has low power consumption. The device is available in a Green UTQFN-1.6×1.6-12L package and operates in industrial and commercial temperature range of -40℃ to +125℃.

FEATURES

- **Supply Voltage Range: 2.7V to 5V**
- **Supports USB Type-C Specification 1.1**
- **Enable Control: Active Low ($\overline{EN}$ Pin)**
- **Backward Compatible with USB Type-C Specification 1.0**
- **Supports up to 3A of Current Advertisement and Detection**
- **Mode Configuration**
  - **Host Only - DFP (Source)**
  - **Device Only - UFP (Sink)**
  - **Dual Role Port - DRP**
  - **Try.SNK**
- **Channel Configuration (CC)**
  - **Attachment of USB Port Detection**
  - **Cable Orientation Detection**
  - **Role Detection**
  - **Type-C Current Mode (Default, Medium or High)**
- **V_{BUS} Detection**
- **I^2C or GPIO Control**
- **Supports 400kHz I^2C Bus**
- **Role Configuration Control through I^2C**
- **Low Current Consumption**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green UTQFN-1.6×1.6-12L Package**

APPLICATIONS

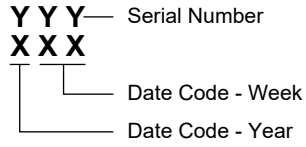
Host, Device, Dual Role Port Applications
Mobile Phones
Tablets and Notebooks
USB Peripherals

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM7220	UTQFN-1.6×1.6-12L	-40℃ to +125℃	SGM7220XUQT12G/TR	GXE XXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.3V to 6V
Control Pins (CC1, CC2, PORT, ADDR, ID, $\overline{EN}$, INT_N/OUT3).....-0.3V to V_{DD} + 0.3V
Control Pins (SDA/OUT1, SCL/OUT2) ....-0.3V to V_{DD} + 0.3V
Control Pin (VBUS_DET)..... -0.3V to 5V
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
MM.....400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD} .....2.7V to 5V
System V_{BUS} Voltage, V_{BUS} .....4.2V to 28V (5V TYP)
VBUS_DET Threshold Voltage on the Pin, V_{BUS_DET} .....5V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

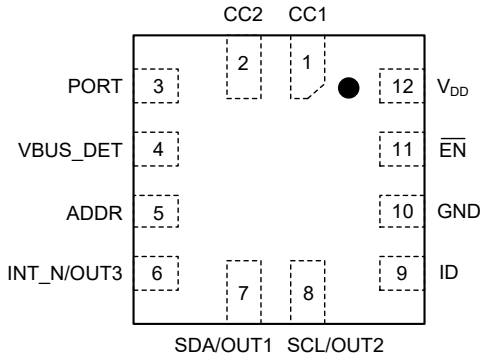
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



UTQFN-1.6×1.6-12L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	CC1	I/O	Type-C Configuration Channel Signal 1.
2	CC2	I/O	Type-C Configuration Channel Signal 2.
3	PORT	I	Tri-Level Input Pin to Indicate Port Mode. The state of this pin is sampled when $\overline{EN}$ is asserted low and V_{DD} is active. This pin is also sampled following an I^2C_SOFT_RESET. H - DFP (Pulled up to V_{DD} if DFP mode is desired). L - UFP (Pulled down or tie to GND if UFP mode is desired). NC - DRP (Left unconnected if DRP mode is desired).
4	VBUS_DET	I	5V to 28V V_{BUS} Input Voltage. V_{BUS} detection determines UFP attachment. An 866kΩ external resistor is required between system V_{BUS} and VBUS_DET pin.
5	ADDR	I	Tri-Level Input Pin to Indicate I^2C Address or GPIO Mode. H - I^2C is enabled and I^2C 7-bit address is 0x67. L - I^2C is enabled and I^2C 7-bit address is 0x47. NC - GPIO mode (I^2C is disabled). ADDR pin should be pulled up to V_{DD} if high configuration is desired.
6	INT_N/OUT3	O	INT_N and OUT3 Dual-Function Pin. When used as the INT_N, the pin is an open-drain output in I^2C control mode and is an active low interrupt signal for indicating changes in I^2C registers. When used as OUT3, the pin is in audio accessory detection in GPIO mode. H - No detection. L - Audio accessory connection detected.
7	SDA/OUT1	I/O	SDA and OUT1 Dual-Function Pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open-drain output for communicating Type-C current mode detection when the SGM7220 is in UFP mode. H - Default current mode detected. L - Medium or high current mode detected.
8	SCL/OUT2	I/O	SCL and OUT2 Dual-Function Pin. When I^2C is enabled (ADDR pin is high or low), this pin is the I^2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open-drain output for communicating Type-C current mode detection when the SGM7220 is in UFP mode. H - Default or medium current mode detected. L - High current mode detected.
9	ID	O	Open-Drain Output. Asserted low when the CC pins detect device attachment when port is a source (DFP), or dual role (DRP) acting as source (DFP).
10	GND	G	Ground.
11	$\overline{EN}$	I	Enable Signal. SGM7220 is active low ($\overline{EN}$ pin). Pulled up to V_{DD} internally to disable the SGM7220 device.
12	V_{DD}	P	Positive Supply Voltage.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5V, T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Consumption							
Current Consumption	Unattached Mode	$I_{UNATTACHED\_UFP}$	V_{DD} = 4.5V, $\overline{EN}$ = L, ADDR = NC, PORT = L when port is unconnected and waiting for connection		70	85	μA
	Active Mode	I_{ACTIVE_UFP}	V_{DD} = 4.5V, $\overline{EN}$ = L, ADDR = NC, PORT = L		70	90	
Leakage Current		$I_{SHUTDOWN}$	V_{DD} = 4.5V, $\overline{EN}$ = H, when V_{DD} is supplied but the SGM7220 is not enabled		0.04	0.5	μA
CC1 and CC2 Pins							
Pull-Down Resistor		R_{CC_DB}	In dead battery mode	4.80	5.1	5.60	kΩ
		R_{CC_D}	In UFP or DRP mode	4.85	5.1	5.45	
Voltage Threshold for Detecting a DFP Attachment		$V_{TH\_UFP\_CC\_USB}$	When configured as an UFP and DFP is advertising default current source capability	0.15		0.25	V
		$V_{TH\_UFP\_CC\_MED}$	When configured as an UFP and DFP is advertising medium (1.5A) current source capability	0.61		0.73	
		$V_{TH\_UFP\_CC\_HIGH}$	When configured as an UFP and DFP is advertising high (3A) current source capability	1.16		1.31	
Voltage Threshold for Detecting an UFP Attachment		$V_{TH\_DFP\_CC\_USB}$	When configured as a DFP and advertising default current source capability	1.49		1.67	V
		$V_{TH\_DFP\_CC\_MED}$	When configured as a DFP and advertising medium (1.5A) current source capability	1.49		1.67	
		$V_{TH\_DFP\_CC\_HIGH}$	When configured as a DFP and advertising high (3A) current source capability	2.45		2.74	
Pull-Up Current Source	Default Mode	$I_{CC\_DEFAULT\_P}$	When operating in DFP or DRP mode	64	80	96	μA
	Medium (1.5A) Mode	$I_{CC\_MED\_P}$		166	180	194	
	High (3A) Mode (1)	$I_{CC\_HIGH\_P}$		304	330	356	
Control Pins: PORT, ADDR, INT_N/OUT3, $\overline{EN}$, ID							
Low-Level Control Signal Input Voltage (PORT, ADDR, $\overline{EN}$)		V_{IL}				0.4	V
Mid-Level Control Signal Input Voltage (PORT, ADDR)		V_{IM}		0.31 × V_{DD}		0.55 × V_{DD}	V
High-Level Control Signal Input Voltage (PORT, ADDR, $\overline{EN}$)		V_{IH}		V_{DD} - 0.3			V
High-Level Input Current		I_{IH}		-10		10	μA
Low-Level Input Current		I_{IL}		-10		10	μA

NOTE:

1. V_{DD} must be 3.5V or greater to advertise 3A current.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control Pins: PORT, ADDR, INT_N/OUT3, $\overline{EN}$, ID						
Internal Pull-Up Resistance for $\overline{EN}$	R_{EN_L}			1.3		MΩ
Internal Pull-Up Resistance (PORT, ADDR)	R_{PU}			1.4		MΩ
Internal Pull-Down Resistance (PORT, ADDR)	R_{PD}			1		MΩ
Low-Level Signal Output Voltage (Open-Drain) (INT_N/OUT3, ID)	V_{OL}	I_{OL} = -1.6mA			0.2	V
External Pull-Up Resistor on Open-Drain IOs (INT_N/OUT3, ID)	R_{p_ODext}			200		kΩ
Tri-Level Input External Pull-Up Resistor (PORT, ADDR)	R_{p_TLext}			4.7		kΩ
I^2C - SDA/OUT1, SCL/OUT2 can operate from 1.8V or 3.3V (±10%) (2)						
Supply Range for I^2C (SDA/OUT1, SCL/OUT2)	V_{DD_I2C}		1.65	1.8	3.6	V
High-Level Signal Voltage	V_{IH}		1.05			V
Low-Level Signal Voltage	V_{IL}				0.4	V
Low-Level Signal Output Voltage (Open-Drain)	V_{OL}	I_{OL} = -1.6mA			0.25	V
VBUS_DET Pin (Connected to System V_{BUS} Signal)						
V_{BUS} Threshold Range	V_{BUS_THR}		2.1	3.1	4	V
External Resistor Between V_{BUS} and VBUS_DET Pin	R_{VBUS}		857	866	875	kΩ
Internal Pull-Down Resistance for VBUS_DET	R_{VBUS_PD}			102		kΩ

NOTE:
2. When using 3.3V for I^2C, customer must ensure V_{DD} is above 3V at all times.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
I^2C (SDA, SCL)					
Data Set-up Time	$t_{SU:DAT}$	100			ns
Data Hold Time	$t_{HD:DAT}$	10			ns
Set-up Time, SCL to Start Condition	$t_{SU:STA}$		600		ns
Hold Time, (Repeated) Start Condition to SCL	$t_{HD:STA}$		600		ns
Set-up Time for Stop Condition	$t_{SU:STO}$		600		ns
Bus Free Time between a Stop and Start Condition	t_{BUF}		600		ns
SCL Clock Frequency; I^2C Mode for Local I^2C Control	f_{SCL}			400	kHz
Rise Time of both SDA and SCL Signals	t_r		100		ns
Fall Time of both SDA and SCL Signals	t_f		60		ns
Total Capacitive Load for Each Bus Line when Operating at ≤ 100kHz	C_{BUS_100kHz}			400	pF
Total Capacitive Load for Each Bus Line when Operating at ≤ 400kHz	C_{BUS_400kHz}			100	pF

SWITCHING CHARACTERISTICS

(T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-on Default of CC1 and CC2 Voltage Debounce Time	$t_{CCCB\_DEFAULT}$	DEBOUCE register = 2'b00		168		ms
Debounce of VBUS_DET Pin after Valid V_{BUS_THR}	t_{VBUS_DB}	See Figure 1		2		ms
Power-on Default of Percentage of Time DRP Advertises DFP during a t_{DRP}	$t_{DRP\_DUTY\_CYCLE}$	DRP_DUTY_CYCLE register = 2'b00		30		%
The Period During which SGM7220 in DFP Mode Completes a DFP to UFP and Back Advertisement	t_{DRP}		50	75	100	ms
Time from $\overline{EN}$ Low and V_{DD} Active to I^2C Access Available	t_{I2C_EN}				15	ms
Soft Reset Duration	t_{SOFT_RESET}		6	10	15	ms

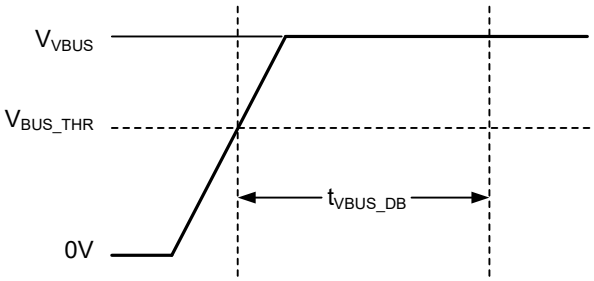


Figure 1. VBUS Detect and Debounce

SIMPLIFIED SCHEMATIC

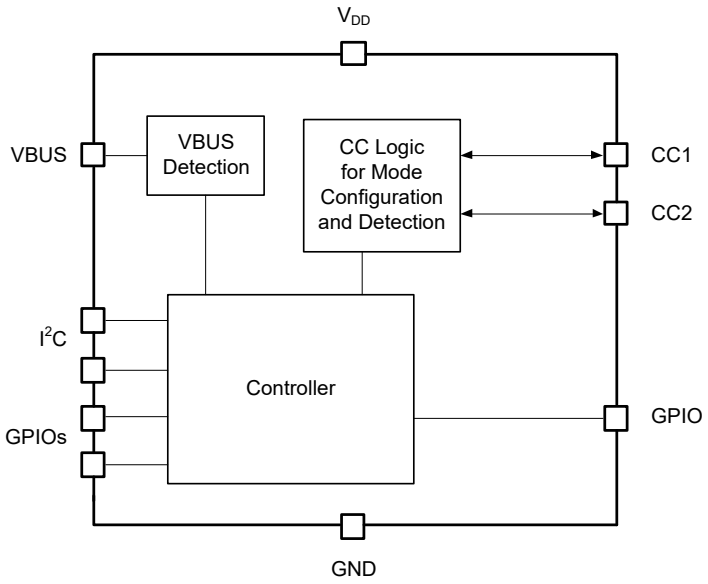


Figure 2. Simplified Schematic

FUNCTIONAL BLOCK DIAGRAM

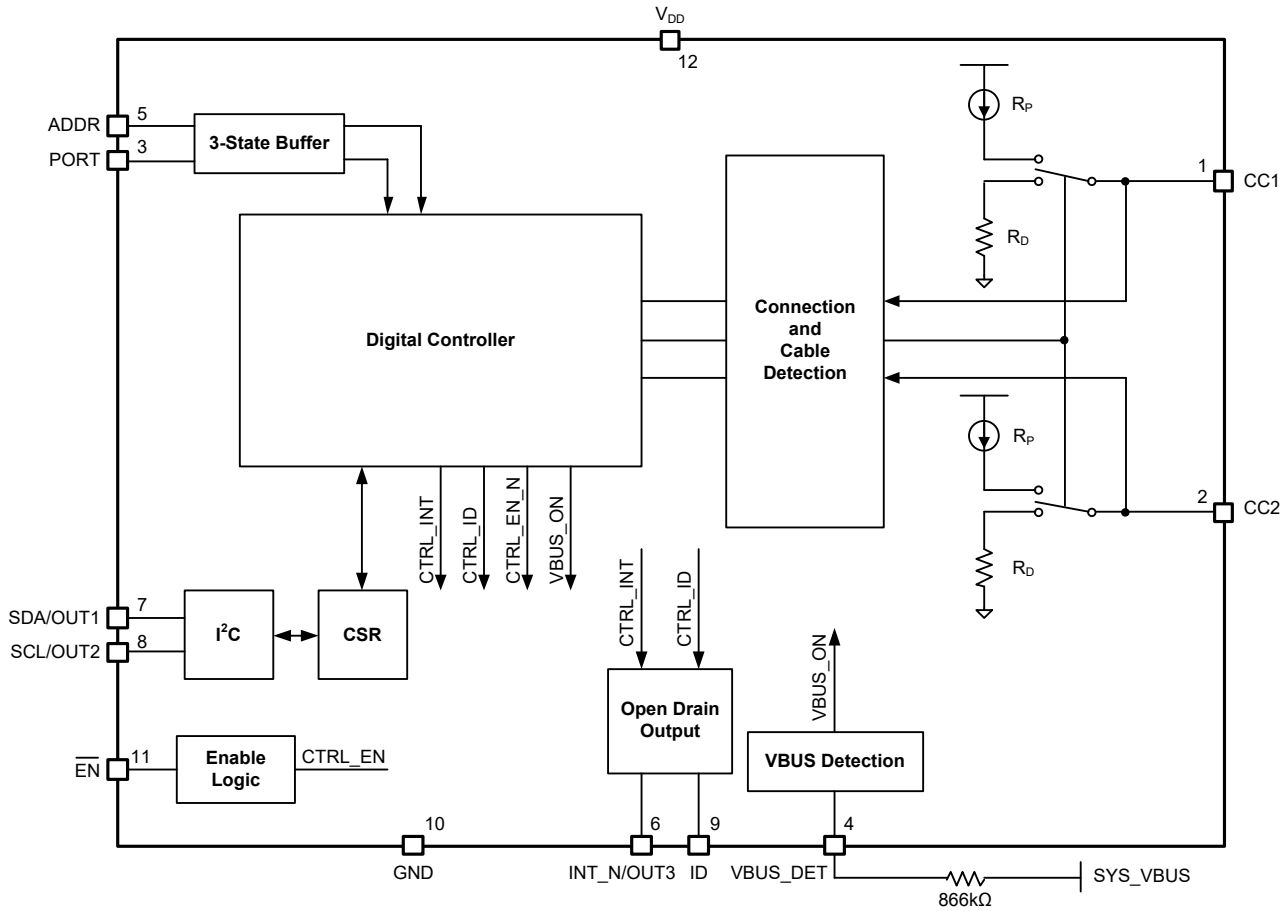


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The USB Type-C ecosystem operates around a small form factor connector and cable that is flippable and reversible. Because of the feature of the connector, a scheme is needed to determine the connector orientation. Additional schemes are needed to determine when a USB port is attached and what the acting role of the USB port (DFP, UFP or DRP) is, as well as to communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C specifications. The SGM7220 provides Configuration Channel (CC) logic for determining USB port attachment and detachment, role detection, cable orientation and Type-C current mode. The SGM7220 also contains several features such as mode configuration and low standby current which make this device ideal for source or sinks in USB2.0 applications.

Cables, Adapters, and Direct Connect Devices

Type-C specification 1.1 defines several cables, plugs and receptacles to be used to attach ports. The SGM7220 supports all cables, receptacles, and plugs. The SGM7220 does not support e-marking.

USB Type-C Receptacles and Plugs

Below is a list of Type-C plugs and receptacles supported by the SGM7220:

- USB Type-C receptacle for USB2.0 platforms and devices.
- USB full-featured Type-C plug.
- USB2.0 Type-C plug.

USB Type-C Cables

Below is a list of Type-C cables supported by the SGM7220:

- USB full-featured Type-C cable.
- USB2.0 Type-C cable with USB2.0 plug.
- Captive cable with either a USB full-featured plug or USB2.0 plug.

Legacy Cable Adapters

The SGM7220 supports legacy cable adapters as defined by the Type-C specification. The cable adapter must correspond to the mode configuration of the SGM7220 (see Figure 4).

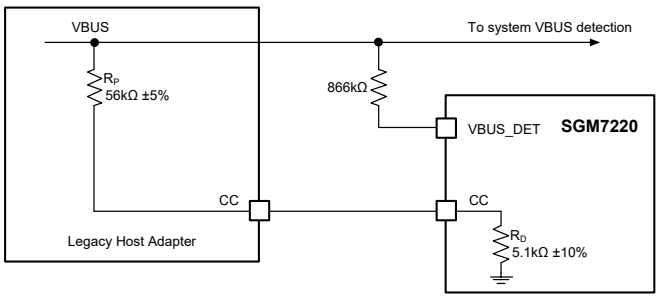


Figure 4. Legacy Adapter Implementation Circuit

Audio Adapters

Additionally, the SGM7220 supports audio adapters for audio accessory mode, including:

- Passive audio adapter.
- Charge through audio adapter.

Direct Connect Devices

The SGM7220 supports the attaching and detaching of a direct-connect device.

FEATURE DESCRIPTION

Port Role Configuration

The SGM7220 can be configured as a downstream facing port (DFP), an upstream facing port (UFP), or a dual-role port (DRP) using the tri-level PORT pin. The PORT pin should be pulled high to V_{DD} with a pull-up resistance, low to GND or left floated on the PCB to achieve the desired mode. This flexibility allows the SGM7220 to be used in a variety of applications. The SGM7220 samples the PORT pin after reset and maintains the desired mode until the SGM7220 is reset again. Table 1 lists the supported features in each mode.

Table 1. Supported Features for the SGM7220 by Mode

Supported Features	PORT = H (DFP Only)	PORT = L (UFP Only)	PORT = NC (DRP)
Port Attach and Detach	Yes	Yes	Yes
Cable Orientation (through I^2C)	Yes	Yes	Yes
Current Advertisement	Yes	-	Yes (DFP)
Current Detection	-	Yes	Yes (UFP)
Accessory Modes (Audio and Debug)	Yes	Yes	Yes
Try.SNK	-	-	Yes
Active Cable Detection	Yes	-	Yes (DFP)
I^2C/GPIO	Yes	Yes	Yes
Legacy Cables	Yes	Yes	Yes
V_{BUS} Detection	-	Yes	Yes (UFP)

Downstream Facing Port (DFP) - Source

The SGM7220 can be configured as a DFP only by pulling the PORT pin high through a resistance to V_{DD} or by changing the MODE_SELECT register. In DFP mode, the SGM7220 constantly presents pull-up resistors (R_P) on both CC Pins. In DFP mode, the SGM7220 initially advertises default USB Type-C current. The Type-C current can be adjusted through I^2C if the system needs to increase the amount advertised. The SGM7220 adjusts the pull-up resistors (R_P) to match the desired Type-C current advertisement. In GPIO mode, the SGM7220 only advertises default Type-C current.

When configured as a DFP, the SGM7220 can operate with older USB Type-C 1.0 devices except for a USB Type-C 1.0 DRP device. The SGM7220 cannot operate with a USB Type-C 1.0 DRP device. This limitation is a result of backwards compatibility problem between a USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

Upstream Facing Port (UFP) - Sink

The SGM7220 can be configured as an UFP only by pulling the PORT pin low to GND. In UFP mode, the SGM7220 constantly presents pull-down resistors (R_D) on both CC pins. The SGM7220 monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The SGM7220 debounces the CC pins and waits for V_{BUS} detection before successfully attaching. As an UFP, the SGM7220 detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs (if in GPIO mode) or through the I^2C CURRENT_MODE_ DETECT register one time in the Attached.SNK state.

After initial connection, the advertised current by the connected DFP could change due to changes in its system power resource. For example, a DFP could advertise high current on initial connection but then decide to reduce to default current because user removed external power adapter from their notebook. Because the SGM7220 will only advertise on OUT1 and OUT2 the initial advertised current, it is recommend to monitor the advertised current through the I^2C interface from the CURRENT_MODE_DETECT register. System software must periodically perform an I^2C_SOFT_RESET register in order to update the CURRENT_MODE_DETECT register based on the state of the CC pins.

Dual Role Port (DRP)

The SGM7220 can be configured to operate as a DRP mode when the PORT pin is left floating on the PCB. In DRP mode, the SGM7220 toggles between operating as a DFP and an UFP. When functioning as a DFP in DRP mode, the SGM7220 complies with all operations as defined for a DFP according to the Type-C specification. When presenting as an UFP in DRP mode, the SGM7220 operates as defined for an UFP according to the Type-C specification.

FEATURE DESCRIPTION (continued)

Type-C Current Mode

When a valid cable detection and attachment have been completed, the DFP has the option to advertise the level of Type-C current that an UFP can sink. The default current advertisement for the SGM7220 is 500mA (MAX) for USB2.0 or 900mA (MAX) for USB3.1. If a higher level of current is available, the I^2C registers can be written to provide medium current at 1.5A or high current at 3A. When the CURRENT_MODE_ ADVERTISE register has been written to advertise higher default current, the DFP adjusts the pull-up resistors (R_P) for the specified current level. If the DFP advertises 3A, it ensures that the V_{DD} of the SGM7220 is 3.5V or greater. Table 2 lists the Type-C current advertisements in GPIO and I^2C modes.

Table 2. Type-C Current Advertisement for GPIO and I^2C Modes

Type-C Current		GPIO Mode (ADDR = NC)		I^2C Mode (ADDR = H or L)	
		UFP (PORT Pin L)	DFP (PORT Pin H)	UFP	DFP
Default	500mA (MAX) for USB2.0 900mA (MAX) for USB3.1	Current Mode Detected and Output through OUT1/OUT2	Only Advertisement	Current Mode Detected and Read through I^2C Register	I^2C Register Default is 500mA or 900mA (MAX)
Medium - 1.5A (MAX)			N/A		Advertisement Selected through Writing I^2C Register
High - 3A (MAX)					

Accessory Support

The SGM7220 supports audio and debug accessories in UFP, DFP and DRP mode. Audio and debug accessory is provided through reading of I^2C registers. Audio accessory is also supported through GPIO mode with INT_N/OUT3 pin (audio accessory is detected when INT_N/OUT3 pin is low).

Audio Accessory

Audio accessory mode is supported through two types of adapters. Firstly, the passive audio adapter can be used to convert the Type-C connector into an audio port. In order to effectively detect the passive audio adapter, the SGM7220 must detect a resistance < R_A on both of the CC pins.

Secondly, a charge through audio adapter may be used. The primary difference between a passive and charge through adapter is that the charge through adapter supplies 500mA of current over V_{BUS}. The charge through adapter contains a receptacle and a plug. The plug acts as a DFP and supply V_{BUS} when the plug detects a connection.

When operating in GPIO mode, the OUT3 pin is used in place of the INT_N pin to determine if an audio accessory is detected and attached. The OUT3 pin is pulled low when an audio accessory is detected.

Debug Accessory

Debug is an additional state supported by USB Type-C. The specification does not define a specific user scenario for this state, but it is important because the end user could use debug accessory mode to enter a test state for production specific to the application. Charge through debug accessory is not supported by SGM7220 when in DRP or UFP mode.

I^2C and GPIO Control

The SGM7220 can be configured for I^2C communication or GPIO outputs using the ADDR pin. The ADDR pin is a tri-level control pin. When the ADDR pin is left floating, the SGM7220 is in GPIO output mode. When the ADDR pin is pulled high or pulled low, the SGM7220 is in I^2C mode.

All outputs for the SGM7220 are open-drain configuration.

The OUT1 and OUT2 pins are used to output the Type-C current mode when in GPIO mode. Additionally, the OUT3 pin is used to communicate with the audio accessory mode in GPIO mode. Table 3 lists the output pin settings. See for more information.

Table 3. Simplified Operation for OUT1 and OUT2

OUT1	OUT2	Advertisement
H	H	Default Current in Unattached State.
H	L	Default Current in Attached State.
L	H	Medium Current (1.5A) in Attached State.
L	L	High Current (3A) in Attached State.

FEATURE DESCRIPTION (continued)

When operating in I^2C mode, the SGM7220 uses the SCL and SDA lines for clock and data. The INT_N pin is used to communicate a change in I^2C registers, or an interrupt to the system. The INT_N pin is pulled low when the SGM7220 updates the registers with new information. The INT_N pin is an open-drain. The INTERRUPT_STATUS register should be set when the INT_N pin is pulled low. To clear the INTERRUPT_STATUS register, the end user writes to I^2C.

When the SGM7220 is configured in GPIO mode, the OUT3 pin determines if an audio accessory is connected. When an audio accessory is detected, the OUT3 pin is pulled low.

NOTE: When using the 3.3V supply for I^2C, the end user must ensure that the V_{DD} is 3V or above. Otherwise the I^2C may back power the device.

V_{BUS} Detection

The SGM7220 supports V_{BUS} detection according to the Type-C specification. V_{BUS} detection is used to determine the attachment or detachment of an UFP and to determine the entering or exiting of accessory modes. V_{BUS} detection is also used to successfully resolve the role in DRP mode.

The system V_{BUS} voltage must be routed through an 866kΩ resistor to the VBUS_DET pin on the SGM7220 if the PORT pin is configured as a DRP or an UFP. If the SGM7220 is configured as a DFP and only ever used in DFP mode, the VBUS_DET pin can be left unconnected.

FUNCTIONAL MODE DESCRIPTION

The SGM7220 has 4 functional modes. Table 4 lists these modes:

Table 4. USB Type-C States According to SGM7220 Functional Modes

Modes	General Behavior	PORT Pin	States (1)
Unattached	USB port unattached. ID, PORT are operational. I^2C on. CC pins configure according to PORT pin.	UFP	Unattached.SNK
			AttachWait.SNK
		DRP	Toggle Unattached.SNK → Unattached.SRC
			AttachedWait.SRC or AttachedWait.SNK
		DFP	Unattached.SRC
			AttachWait.SRC
Active	USB port attached. All GPIOs are operational. I^2C on.	UFP	Attached.SNK
		DRP	Attached.SNK
			Attached.SRC
			Audio accessory
			Debug accessory
		DFP	Attached.SRC
			Audio accessory
			Debug accessory
Dead Battery	No operation. V_{DD} not available.	UFP/DRP/DFP	Default device state to UFP/SNK with R_D.
Shutdown	V_{DD} available. SGM7220 $\overline{EN}$ pin high.	UFP/DRP/DFP	Default device state to UFP/SNK with R_D.

NOTE: 1. Required; not in sequential order.

FUNCTIONAL MODE DESCRIPTION (continued)

Unattached Mode

Unattached mode is the primary mode of operation for the SGM7220, because a USB port can be unattached for a lengthy period of time. In unattached mode, V_{DD} is available, and all IOs and I^2C are operational. After the SGM7220 is powered up, the part enters unattached mode until a successful attachment has been determined. Initially, right after power up, the SGM7220 comes up as an Unattached.SNK. The SGM7220 checks the PORT pin and operates according to the mode configuration. The SGM7220 toggles between the UFP and the DFP if configured as a DRP. In unattached mode, I^2C can be used to change the mode configuration or port role if the board configuration of the PORT pin is not the desired mode. Writing to the I^2C MODE_SELECT register can override the PORT pin only in unattached mode. The PORT pin is only sampled at reset or power up. I^2C must be used after reset to change the device mode configuration.

Active Mode

Active mode is defined as the port being attached. In active mode, all GPIOs are operational, and I^2C is read/write (R/W). When in active mode, the SGM7220 communicates to the AP that the USB port is attached. This happens through the ID pin if SGM7220 is configured as a DFP or DRP connected as source. If SGM7220 is configured as a UFP or a DRP connected as a sink, the OUT1/OUT2 and INT_N/OUT3 pins are used. The SGM7220 exits active mode under the following conditions:

- Cable unplug.
- V_{BUS} removal if attached as a UFP.
- Dead battery; system battery or supply is removed.
- $\overline{EN}$ pin floated or pulled high.

During active mode, I^2C cannot be used to change the mode configuration. This can only be done if SGM7220 is in unattached state.

Dead Battery Mode

During dead battery mode, V_{DD} is not available. CC pins always connect to pull-down resistors (R_D) by default in dead battery mode. Dead battery mode means:

- SGM7220 in UFP with 5.1kΩ±20% R_D; cable connected and providing charge.
- SGM7220 in UFP with 5.1kΩ±20% R_D; nothing connected (application could be off or have a discharged battery).

NOTE: When V_{DD} is off, the SGM7220 non-failsafe pins (VBUS_DET, ADDR, PORT, ID, OUT[3:1] pins) could back-drive the SGM7220 if not handled properly. When necessary to pull these pins up, it is recommended to pull up PORT, ADDR, INT_N/OUT3 and ID to the device's V_{DD} supply. The VBUS_DET must be pulled up to V_{BUS} through an 866kΩ resistor.

Shutdown Mode

Shutdown mode for SGM7220 is defined as follows:

- Supply voltage is available and $\overline{EN}$ pin is pulled high.
- $\overline{EN}$ pin has an internal pull-up resistor.
- The SGM7220 is off, but still maintains the R_D on the CC pins.

PROGRAMMING

For further programmability, the SGM7220 can be controlled using I^2C. The SGM7220 local I^2C interface is available for reading/writing after t_{I2C_EN} when the device is powered up. The SCL and SDA terminals are used for I^2C clock and I^2C data respectively. If I^2C is the preferred method of control, the ADDR pin must be set accordingly.

Table 5. SGM7220 I^2C Addresses

SGM7220 I^2C Target Address								
ADDR Pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
H	1	1	0	0	1	1	1	0/1
L	1	0	0	0	1	1	1	0/1

The following procedure should be followed to write to SGM7220 I^2C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SGM7220 7-bit address and a zero-value R/W bit to indicate a write cycle.
2. The SGM7220 acknowledges the address cycle.
3. The master presents the sub-address (I^2C register within the SGM7220) to be written, consisting of one byte of data, MSB-first.
4. The SGM7220 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^2C register.
6. The SGM7220 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the device.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the SGM7220 I^2C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SGM7220 7-bit address and a zero-value R/W bit to indicate a read cycle.
2. The SGM7220 acknowledges the address cycle.
3. The SGM7220 transmits the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the SGM7220 I^2C register occurred prior to the read, then the SGM7220 starts at the sub-address specified in the write.
4. The SGM7220 waits for a not-acknowledge (NACK) from the master after one byte of data transfer.
5. The master terminates the read operation by generating a stop condition (P).

REGISTER MAPS

Table 6. CSR Registers

Access Tag	Name	Meaning
R	Read	The field may be read by software.
W	Write	The field may be written by software.
S	Set	The field may be set by a write of one. Writing of zeros to the field have no effect.
C	Clear	The field may be cleared by a write of one. Writing of zeros to the field have no effect.
U	Update	Hardware may autonomously update this field.
NA	No Access	Not accessible or not applicable.

Table 7. CSR Registers Bit Address and Description

Address	Bit(s)	Bit Name	Description	Access
0x00 ~ 0x07	7:0	DEVICE_ID	These fields return a string of ASCII characters returning SGM7220. Addresses 0x07 ~ 0x00 = {0x00, 0x54, 0x55, 0x53, 0x42, 0x33, 0x32 and 0x30}	R
0x08	7:6	CURRENT_MODE_ADVERTISE	These bits are programmed by the application to raise the current advertisement from default. 00 - Default (500mA/900mA) initial value at startup 01 - Medium (1.5A) 10 - High (3A) 11 - Reserved	RW
	5:4	CURRENT_MODE_DETECT	These bits are set when an UFP determines the Type-C current mode. 00 - Default (value at start up) 01 - Medium 10 - Charge through accessory - 500mA 11 – High	RU
	3:1	ACCESSORY_CONNECTED	These bits are read by the application to determine if an accessory was attached. 000 - No accessory attached (default) 001 - Reserved 010 - Reserved 011 - Reserved 100 - Audio accessory 101 - Audio charged thru accessory 110 - Debug accessory 111 - Reserved	RU
	0	ACTIVE_CABLE_DETECTION	This flag indicates that an active cable has been plugged into the Type-C connector. When this field is set, an active cable is detected.	RU
0x09	7:6	ATTACHED_STATE	This is an additional method to communicate attachment other than the ID pin. These bits can be read by the application to determine what was attached. 00 - Not attached (default) 01 - Attached.SRC (DFP) 10 - Attached.SNK (UFP) 11 - Attached to an accessory	RU
	5	CABLE_DIR	Cable orientation. The application can read these bits for cable orientation information. 0 - CC1 1 - CC2 (default)	RU
	4	INTERRUPT_STATUS	The INT pin is pulled low whenever a CSR changes. When a CSR change has occurred this bit should be held at 1 until the application clears it. 0 - Clear 1 - Interrupt (When INT_N is pulled low, this bit will be 1. This bit is 1 whenever any CSR are changed.)	RCU
	3		Reserved.	R
	2:1	DRP_DUTY_CYCLE	Percentage of time that a DRP advertises DFP during t_{DRP}. 00 - 30% (default) 01 - 40% 10 - 50% 11 - 60%	RW

REGISTER MAPS (continued)

Table 7. CSR Registers Bit Address and Description (continued)

Address	Bit(s)	Bit Name	Description	Access
0x09	0	DISABLE_UFP_ACCESSORY	Settings this field will disable UFP accessory support. 0 - UFP accessory support enabled (default) 1 - UFP accessory support disabled	RW
0x0A	7:6	DEBOUNCE	The nominal amount of time the SGM7220 debounce the voltages on the CC pins. 00 - 168ms (default) 01 - 118ms 10 - 134ms 11 - 152ms	RW
	5:4	MODE_SELECT	This register can be written to set the SGM7220 mode operation. The ADDR pin must be set to I^2C mode. If the default is maintained, the SGM7220 operates according to the PORT pin levels and modes. The MODE_SELECT can only be changed when in the unattached state. 00 - Maintain mode according to PORT pin selection (default) 01 - UFP mode (unattached.SNK) 10 - DFP mode (unattached.SRC) 11 - DRP mode (start from unattached.SNK)	RW
	3	I^2C_SOFT_RESET	This resets the digital logic. The bit is self-clearing. A write of 1 starts the reset. The following registers maybe affected after setting this bit: CURRENT_MODE_DETECT ACTIVE_CABLE_DETECTION ACCESSORY_CONNECTED ATTACHED_STATE CABLE_DIR	RSU
	2:1	SOURCE_PREF	This field controls the SGM7220 behaviors when configured as a DRP. 00 - Standard DRP (default) 01 - DRP will perform Try.SNK 10 - Reserved 11 - Reserved	RW
	0	DISABLE_TERM	This field will disable the termination on the CC pins and transition the CC state machine of the SGM7220 to the disable state. 0 - Termination enabled according to PORT (default) 1 - Termination disabled and state machine held in disabled state	RW
0x45	7:3		Reserved.	R
	2	DISABLE_RD_RP	When this field is set, R_D and R_P are disabled. 0 - Normal operation (default) 1 - Disable R_D and R_P	RW
	1:0		Reserved. Do not change default value.	RW

APPLICATION INFORMATION

The SGM7220 is a Type-C configuration channel logic and port controller. The SGM7220 can detect when a Type-C device is attached, what type of device is attached, the orientation of the cable, and power capabilities (both detection and broadcast). The SGM7220 can be used in a source application (DFP) or in a sink application (UFP).

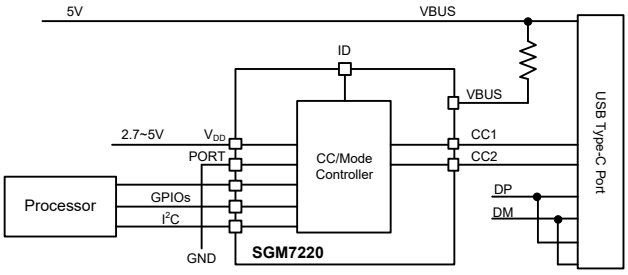


Figure 5. SGM7220 in UFP Mode Supporting Default Implementation

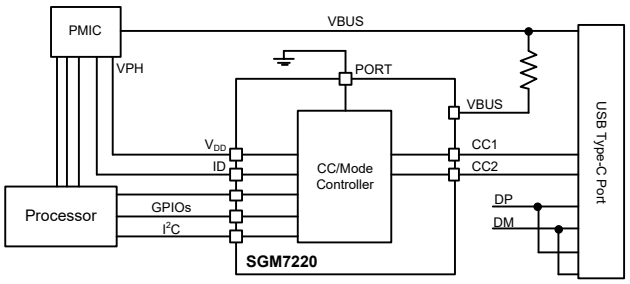


Figure 6. SGM7220 in UFP Mode Supporting Advanced Power Delivery

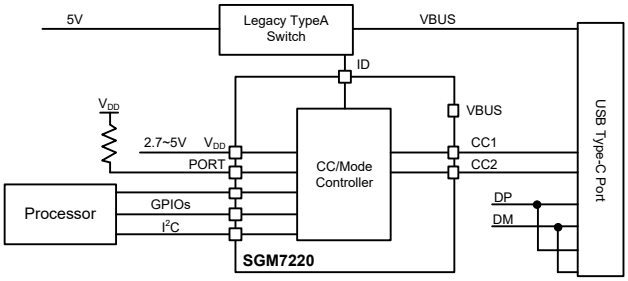


Figure 7. SGM7220 in DFP Mode Supporting Default Implementation

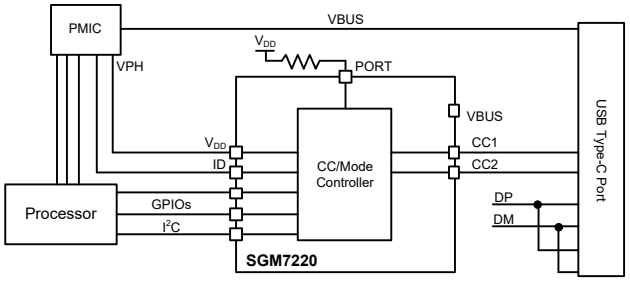


Figure 8. SGM7220 in DFP Mode Supporting Advanced Power Delivery

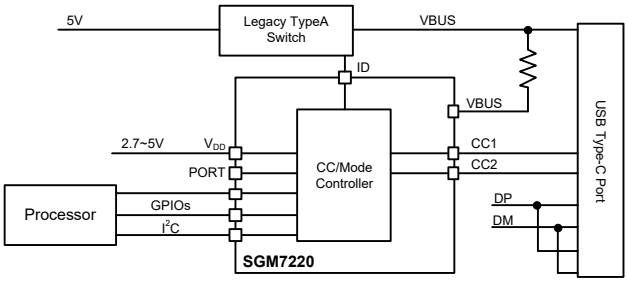


Figure 9. SGM7220 in DRP Mode Supporting Default Implementation

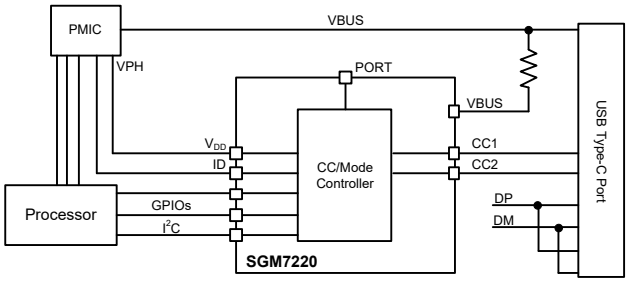


Figure 10. SGM7220 in DRP Mode Supporting Advanced Power Delivery

APPLICATION INFORMATION (continued)

DRP in I²C Mode

Figure 11 shows the SGM7220 configured as a DRP in I²C mode.

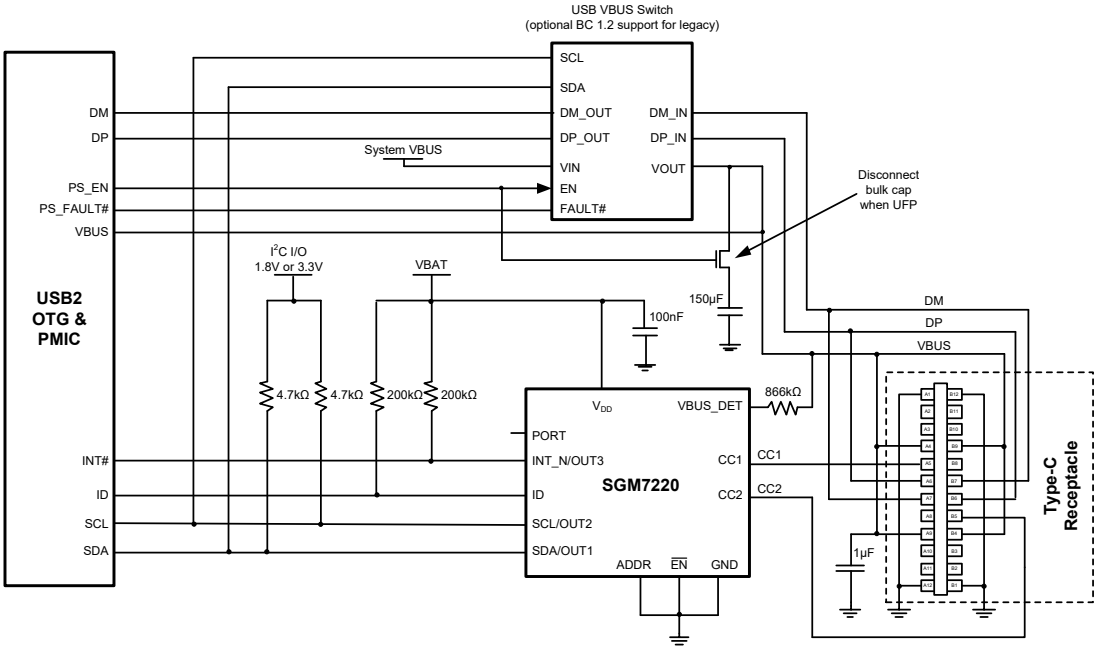


Figure 11. DRP in I²C Mode Schematic

Design Requirements

For this design example, use the parameters listed in Table 8.

Table 8. Design Requirements for DRP in I²C Mode

Design Parameter	Value
V_{DD} (2.75V to 5V)	VBAT (less than 5V)
Mode (I²C or GPIO)	I²C: ADDR pin must be pulled down or pulled up.
I²C Address (0x47 or 0x67)	0x47: ADDR pin must be pulled low or tied to GND.
Type-C Port Type (UFP, DFP or DRP)	DRP: PORT pin is NC.
Shutdown Support ($\overline{EN}$ Control)	No

Detailed Design Procedure

The SGM7220 supports a V_{DD} in the range of 2.75V to 5V. In this particular use case, VBAT which must be in the required V_{DD} range is connected to the V_{DD} pin. A 100nF capacitor is placed near V_{DD} pin.

The SGM7220 is placed into I²C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in an I²C address of 0x47. The SDA and SCL must be pulled up to either 1.8V or 3.3V. When pulled up to 3.3V, the V_{DD} supply must be at least 3V to keep from back-driving the I²C interface.

The SGM7220 can enter shutdown mode by pulling the $\overline{EN}$ pin high, which puts the SGM7220 into a low power state. In this case, external control of the $\overline{EN}$ pin is not implemented and therefore the $\overline{EN}$ pin is tied to V_{DD} pin.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the SGM7220 I²C registers occurs. This pin is an open-drain output and requires an external pull-up resistor. The pin should be pulled up to V_{DD} with a 200kΩ resistor.

The ID pin is used to indicate when a connection has occurred if the SGM7220 is a DFP while configured for DRP. An OTG USB controller can use this pin to determine when to operate as a USB host or USB device. When this pin is driven low, the OTG USB controller functions as a host and then enables V_{BUS}. The Type-C standard requires that a DFP does not enable V_{BUS} until it is in the Attached.SRC state. If the ID pin is not low but V_{BUS} is detected, then OTG USB controller functions as a device. The ID pin is an open-drain output and requires an external pull-up resistor. It should be pulled up to V_{DD} with a 200kΩ resistor.

APPLICATION INFORMATION (continued)

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is not connected, the SGM7220 is in DRP mode. The Type-C port mode can also be controlled by the MODE_SELECT register through the I^2C interface when the SGM7220 is in the unattached state.

The VBUS_DET pin must be connected through an 866kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the SGM7220 from large V_{BUS} voltage that is possible in present systems. This resistor along with internal pull-down keeps the voltage observed by the SGM7220 in the recommended range.

The USB2.0 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the SGM7220 in a DRP mode, it alternates between UFP and DFP. If the SGM7220 connects as an UFP, the large bulk capacitance must be removed. The FET in Figure 11 performs this task.

Table 9. USB2 Bulk Capacitance Requirements

Port Configuration	Min	Max	Units
Downstream Facing Port (DFP)	120		μF
Upstream Facing Port (UFP)	1	10	μF

Application Curve

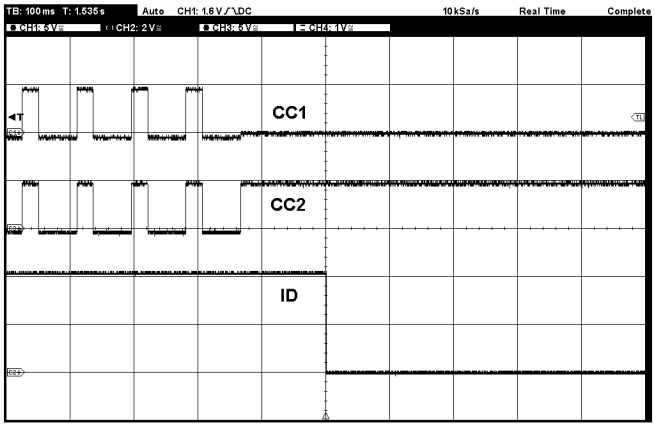


Figure 12. Application Curve for DRP in I^2C Mode

APPLICATION INFORMATION (continued)

DFP in I²C Mode

Figure 13 shows the SGM7220 configured as a DFP in I²C mode.

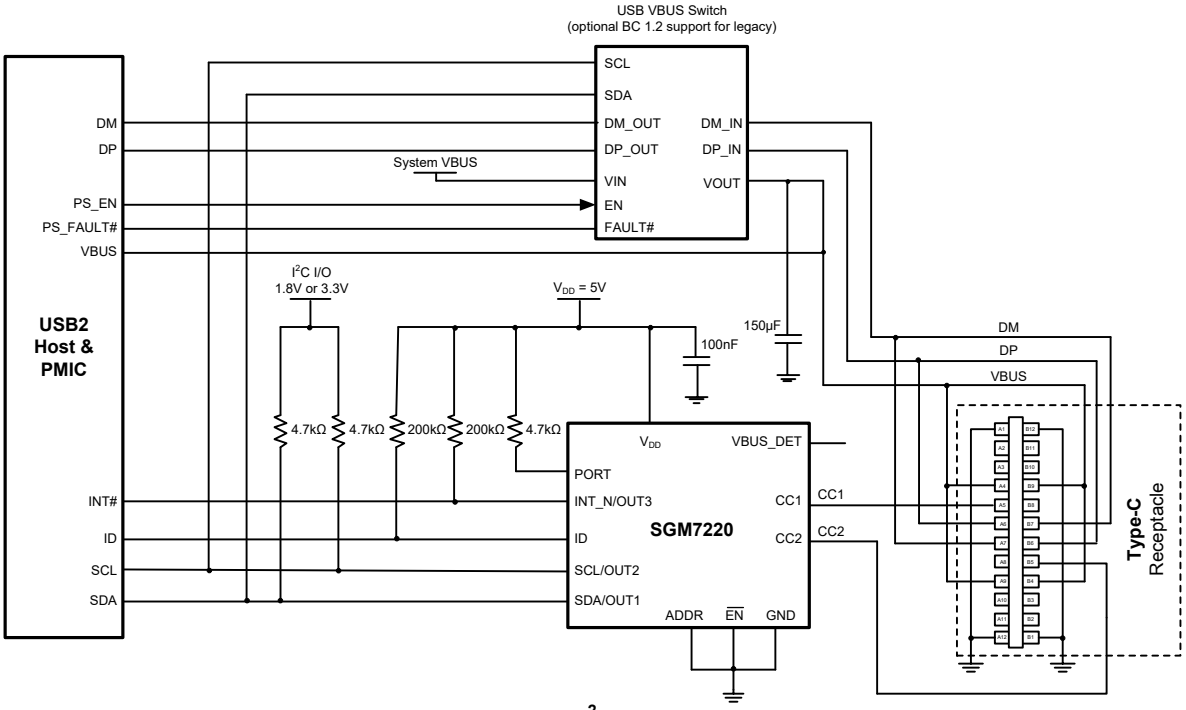


Figure 13. DFP in I²C Mode Schematic

Design Requirements

For this design example, use the parameters listed in Table 10.

Table 10. Design Requirements for DFP in I²C Mode

Design Parameter	Value
V_{DD} (2.75V to 5V)	5V
Mode (I²C or GPIO)	I²C: ADDR pin must be pulled down or pulled up.
I²C Address (0x47 or 0x67)	0x47: ADDR pin must be pulled low or tied to GND.
Type-C Port Type (UFP, DFP or DRP)	DFP: PORT pin is pulled up.
Shutdown Support ($\overline{EN}$ Control)	No

Detailed Design Procedure

The SGM7220 supports a V_{DD} in the range of 2.75V to 5V. In this particular case, V_{DD} is set to 5V. A 100nF capacitor is placed near V_{DD} pin.

The SGM7220 is placed into I²C mode by either pulling the ADDR pin high or low. In this particular case, the ADDR pin is tied to GND which results in an I²C address of 0x47. The SDA and SCL must be pulled up to either 1.8V or 3.3V. When pulled up to 3.3V, the V_{DD} supply must be at least 3V to keep from back-driving the I²C interface.

The SGM7220 can enter shutdown mode by pulling the $\overline{EN}$ pin high, which puts the SGM7220 into a low power state. In this case, external control of the $\overline{EN}$ pin is not implemented and therefore the $\overline{EN}$ pin is tied to V_{DD} pin.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the SGM7220 I²C registers occurs. This pin is an open-drain output and requires an external pull-up resistor. The pin should be pulled up to V_{DD} with a 200kΩ resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is pulled high, the SGM7220 is in DFP mode. The Type-C port mode can also be controlled by the MODE_SELECT register through the I²C interface when the SGM7220 is in the unattached state.

APPLICATION INFORMATION (continued)

The VBUS_DET pin must be connected through an 866kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the SGM7220 from large V_{BUS} voltage that is possible in present systems. This resistor along with internal pull-down keeps the voltage observed by the SGM7220 in the recommended range.

The USB2.0 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the SGM7220 in a DFP mode, a bulk capacitance of 120μF at least is required. In this particular case, a 150μF capacitor was chosen.

Application Curve

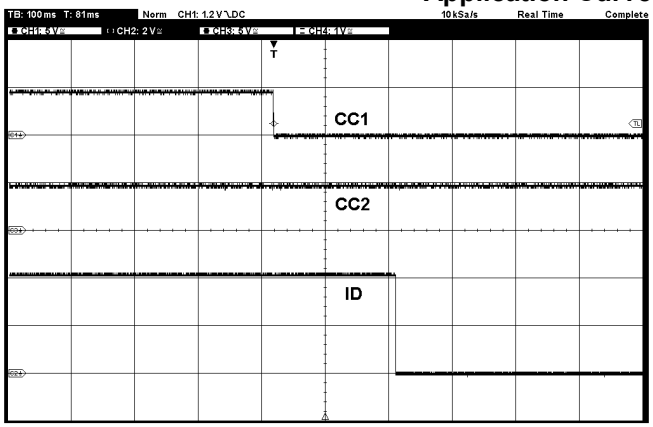


Figure 14. Application Curve for DFP in I^2C Mode

APPLICATION INFORMATION (continued)

UFP in I²C Mode

Figure 15 shows the SGM7220 device configured as an UFP in I²C mode.

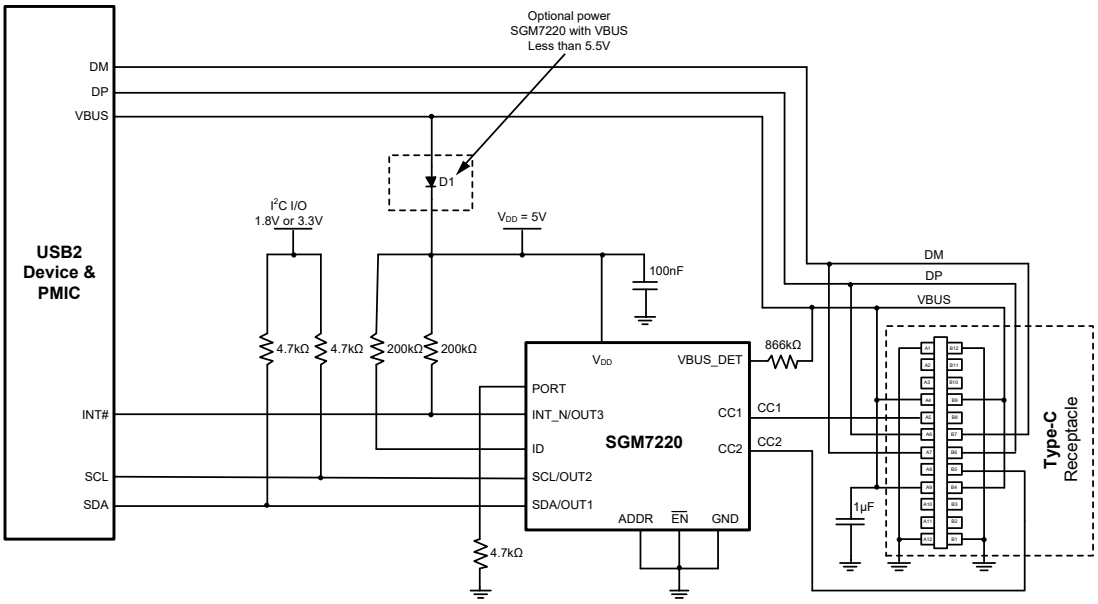


Figure 15. UFP in I²C Mode Schematic

Design Requirements

For this design example, use the parameters listed in Table 11.

Table 11. Design Requirements for UFP in I²C Mode

Design Parameter	Value
V_{DD} (2.75V to 5V)	5V
Mode (I²C or GPIO)	I²C: ADDR pin must be pulled down or pulled up.
I²C Address (0x47 or 0x67)	0x47: ADDR pin must be pulled low or tied to GND.
Type-C Port Type (UFP, DFP or DRP)	DFP: PORT pin is pulled down.
Shutdown Support ($\overline{EN}$ Control)	No

Detailed Design Procedure

The SGM7220 supports a V_{DD} in the range of 2.75V to 5V. In this particular case, V_{DD} is set to 5V. A 100nF capacitor is placed near V_{DD} pin. If V_{BUS} is guaranteed to be less than 5.5V, powering the SGM7220 through a diode can be implemented.

The SGM7220 is placed into I²C mode by either pulling the ADDR pin high or low. In this case, the ADDR pin is tied to GND which results in a I²C address of 0x47. The SDA and SCL must be pulled up to either 1.8V or 3.3V. When pulled up to 3.3V, the V_{DD} supply must be at least 3V to keep from back-driving the I²C interface.

The SGM7220 can enter shutdown mode by pulling the $\overline{EN}$ pin high, which puts the SGM7220 into a low power state. In this case, external control of the $\overline{EN}$ pin is not implemented and therefore the $\overline{EN}$ pin is tied to V_{DD} pin.

The INT_N/OUT3 pin is used to notify the PMIC when a change in the SGM7220 I²C registers occurs. This pin is an open-drain output and requires an external pull-up resistor. The pin should be pulled up to V_{DD} with a 200kΩ resistor.

The Type-C port mode is determined by the state of the PORT pin. When the PORT pin is pulled low, the SGM7220 is in UFP mode. The Type-C port mode can also be controlled by the MODE_SELECT register through the I²C interface when the SGM7220 is in the unattached state.

The VBUS_DET pin must be connected through an 866kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the SGM7220 from large V_{BUS} voltage that is possible in present systems. This resistor along with internal pull-down keeps the voltage observed by the SGM7220 in the recommended range.

APPLICATION INFORMATION (continued)

The USB2.0 specification requires the bulk capacitance on V_{BUS} based on UFP or DFP. When operating the SGM7220 in an UFP mode, a bulk capacitance between 1μF to 10μF is required. In this particular case, a 1μF capacitor was chosen.

Application Curves

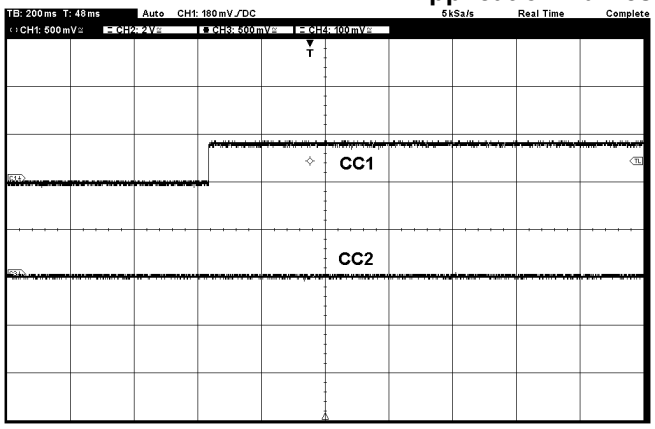


Figure 16. Application Curve for UFP in I^2C Mode

Initialization Set-Up

The general power-up sequence for the SGM7220 ($\overline{EN}$ tied to ground) is as follows:

1. System is powered off (device has no V_{DD}). The SGM7220 is configured internally in UFP mode with pull-down resistors (R_D) on CC pins (dead battery).
2. V_{DD} ramps - POR circuit.
3. I^2C supply ramps up.
4. The SGM7220 enters unattached mode and determines the voltage level from the PORT pin. This determines the mode in which the SGM7220 operates (DFP, UFP or DRP).
5. The SGM7220 monitors the CC pins to determine as a DFP and V_{BUS} for attachment as an UFP.
6. The SGM7220 enters active mode when attachment has been successfully detected.

Power Supply Recommendations

The SGM7220 has a wide power supply range from 2.7V to 5V. The SGM7220 can be run off of a system power such as a battery.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

AUGUST 2021 – REV.A.2 to REV.A.3 ..... **Page**

Updated Package Outline Dimensions section 23

APRIL 2020 – REV.A.1 to REV.A.2 ..... **Page**

Updated Features section 1
Updated Electrical Characteristics section 5
Updated Timing Requirements section 6

AUGUST 2019 – REV.A to REV.A.1 ..... **Page**

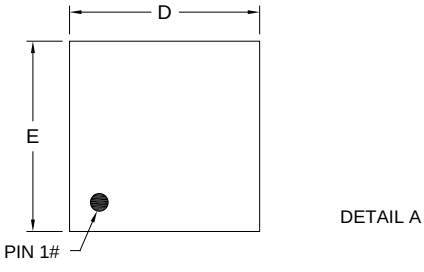
Updated Electrical Characteristics section 4, 5
Updated Timing Requirements section 6
Updated Switching Characteristics section 6

Changes from Original (DECEMBER 2018) to REV.A ..... **Page**

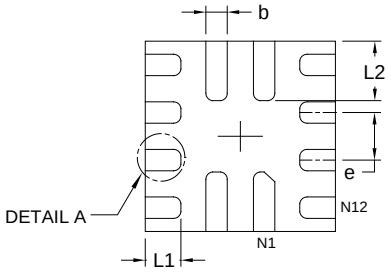
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

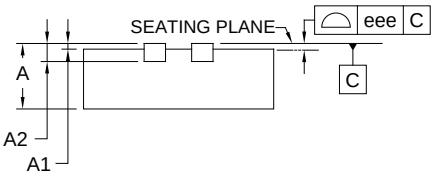
UTQFN-1.6×1.6-12L



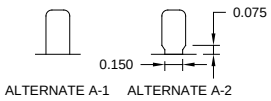
TOP VIEW



BOTTOM VIEW

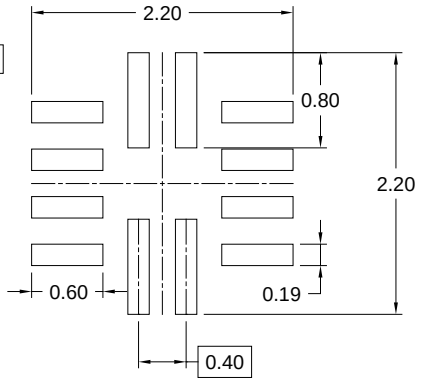


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



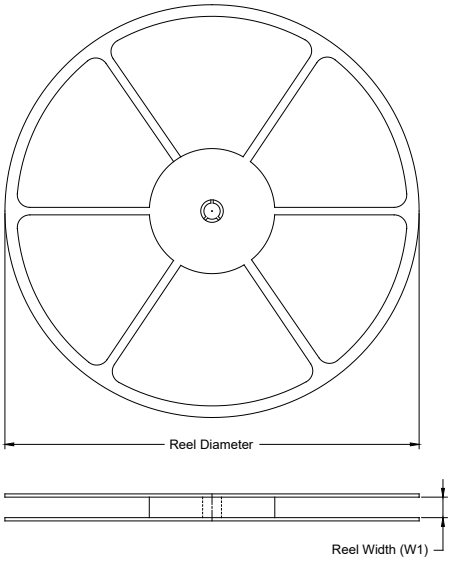
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.450	-	0.600
A1	-	-	0.050
A2	0.152 REF		
e	0.400 BSC		
D	1.550	1.600	1.650
E	1.550	1.600	1.650
b	0.130	0.190	0.250
L1	0.250	0.300	0.350
L2	0.450	0.500	0.550
eee	-	0.080	-

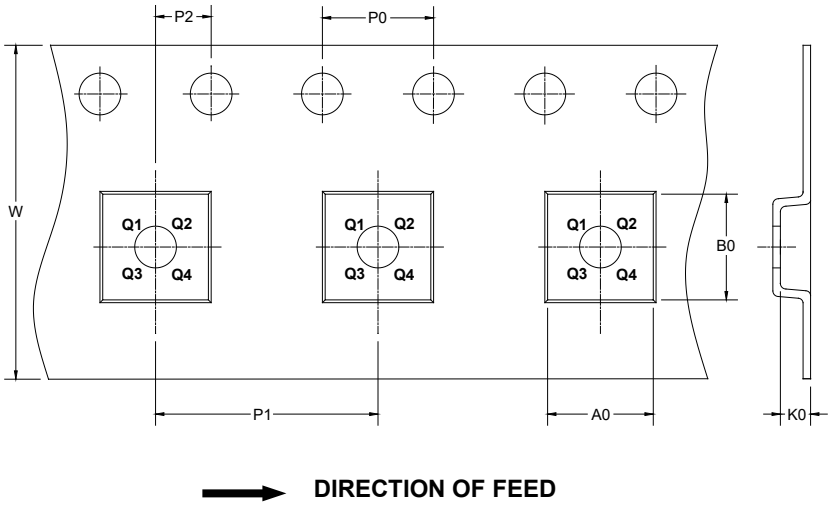
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



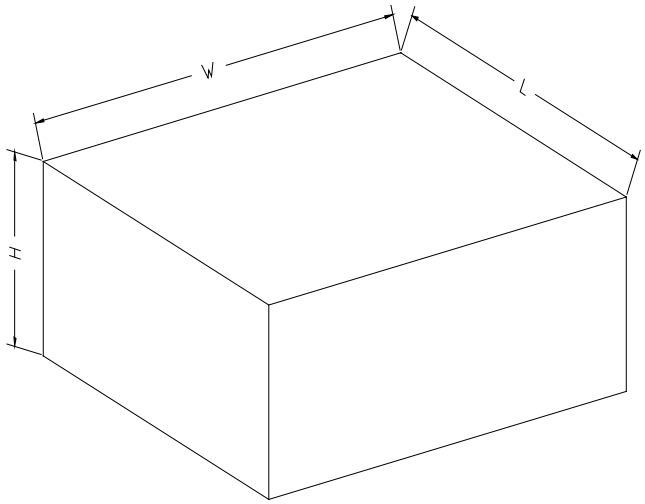
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTQFN-1.6×1.6-12L	7″	9.0	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002