SGM860
Quad Supply Voltage Supervisors with Adjustable Delay and Watchdog Timer

GENERAL DESCRIPTION

The SGM860 is a family of supply voltage supervisors (SVSs). It has four channels and each one can monitor a power rail with a high threshold accuracy of 0.35% typically. It also features very low quiescent current of 6μA (TYP).

Among the supply voltage supervisor (SVS-x, x = 1, 2, 3, 4) circuits, four power rails are higher than 0.4V and one power rail is less than 0.4V (even with negative voltage). Once the SENSEy (y = 1, 2, 3, 4L, 4H) input voltage goes down below the configurable threshold, a nRESETx signal can be asserted by each SVS-x. The threshold of each SVS-x can be configured by the external resistors.

A delay can be configured for each SVS-x before nRESETx is released. The delay time for each SVS-x can be set independently between 1.45ms and 10s via the CTx pin connection. Only SVS-1 has a manual reset signal (nMR) that the nRESETx is activated by a logic low of nMR. SVS-4 has two comparators to monitor the threshold window and the extra comparator can be used as a fifth SVS to monitor the negative voltage based on the voltage reference VREF.

The SGM860 is available in a Green TQFN-4×4-20BL package. It operates over a junction temperature range of -40℃ to +125℃.

FEATURES

- **Four Separate Voltage Supervisors**
- **Channel 1:**
  - **Adjustable Threshold Down to 0.4V**
  - **Manual Reset (nMR) Input**
- **Channels 2, 3:**
  - **Adjustable Threshold Down to 0.4V**
- **Channel 4:**
  - **Adjustable Positive or Negative Threshold**
  - **Window Comparator**
- **Adjustable Delay Time: 1.45ms to 10s**
- **Threshold Accuracy: 0.35% (TYP)**
- **Low Quiescent Current: 6μA (TYP)**
- **Dedicated Output for Watchdog Timer**
- **Well-Controlled Output during Power-Up**
- **Output Options:**
  - **SGM860A: Open-Drain nRESETx and nWDO**
  - **SGM860B: Push-Pull nRESETx and nWDO**
- **Available in a Green TQFN-4×4-20BL Package**

APPLICATIONS

Applications with DSP and Microcontroller
Applications with FPGA and ASIC
Telecom and Wireless Infrastructure
Industrial Equipment
Analog Sequencing

TYPICAL APPLICATION

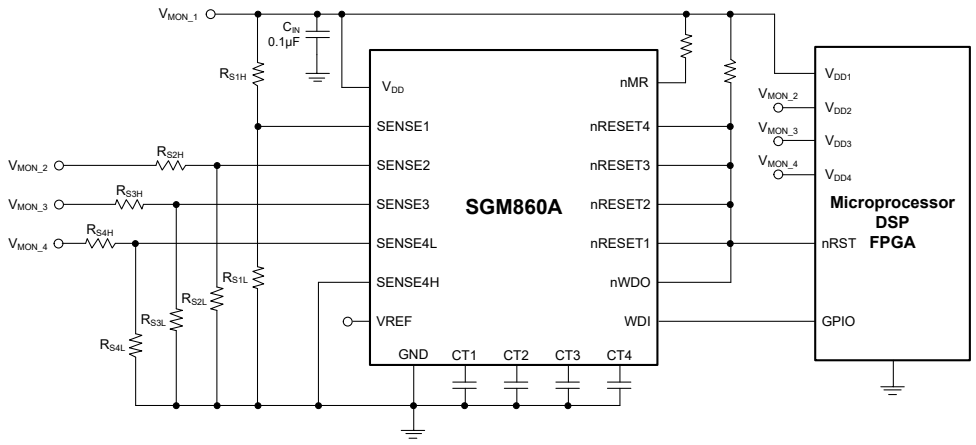


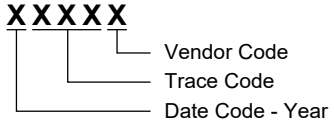
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM860A	TQFN-4×4-20BL	-40℃ to +125℃	SGM860AXTUJ20G/TR	SGM860A XTUJ20 XXXXX	Tape and Reel, 3000
SGM860B	TQFN-4×4-20BL	-40℃ to +125℃	SGM860BXTUJ20G/TR	SGM860B XTUJ20 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{DD} ..... -0.3V to 7V
CTx Pin Voltage ..... -0.3V to V_{DD} + 0.3V
nRESETx, nMR, SENSEy, WDI, nWDO Pin Voltage .....
..... -0.3V to 7V
nRESETx, nWDO Pin Current 45mA
VREF Pin Current 15mA
Package Thermal Resistance
TQFN-4×4-20BL, θ_{JA} ..... 54.6℃/W
TQFN-4×4-20BL, θ_{JB} ..... 30.6℃/W
TQFN-4×4-20BL, $\theta_{JC(TOP)}$ ..... 44.2℃/W
TQFN-4×4-20BL, $\theta_{JC(BOT)}$ ..... 18.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{DD} ..... 1.8V to 6.5V
All Sense Input Voltage, V_{SENSEy} ..... 0V to V_{DD}
WDI High Input Voltage, V_{IH} ..... 0.7 × V_{DD} to V_{DD}
WDI Low Input Voltage, V_{IL} ..... 0V to 0.3 × V_{DD}
nMR Pin Voltage ..... 0V to V_{DD}
CTx Pin Capacitor ..... 0.22nF to 1μF
Pull-up Resistor, R_P ..... 6.5kΩ to 10MΩ (0.1MΩ, TYP)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

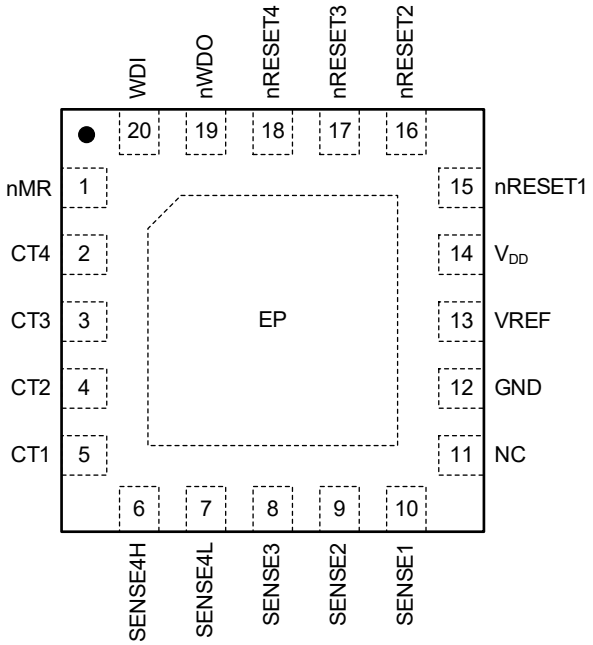
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-20BL

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	nMR	I	Manual Reset Input Pin for SVS-1. Pulling this pin low will assert nRESET1.
2	CT4	—	Reset Delay Configuration Pins for SVS-1 to SVS-4 Respectively. If it requires a fixed delay time, place a resistor of 40kΩ to 200kΩ between CTx and V_{DD}, or just leave it floating. If it requires a configurable delay time, place a capacitor larger than 220pF between CTx and GND.
3	CT3	—	
4	CT2	—	
5	CT1	—	
6	SENSE4H	I	Rising Edge Detection to SVS-4. nRESET4 is active-low when SENSE4H voltage is higher than the positive threshold V_{ITP}. Negative voltage can be monitored with the VREF pin. Connect it to GND if not used.
7	SENSE4L	I	Falling Edge Detection to SVS-4. nRESET4 is active-low when SENSE4L voltage is lower than the negative threshold V_{ITN}.
8	SENSE3	I	Voltage Sensing to SVS-3. nRESET3 is active-low when SENSE3 voltage is lower than the negative threshold V_{ITN}.
9	SENSE2	I	Voltage Sensing to SVS-2. nRESET2 is active-low when SENSE2 voltage is lower than the negative threshold V_{ITN}.
10	SENSE1	I	Voltage Sensing to SVS-1. nRESET1 is active-low when SENSE1 voltage is lower than the negative threshold V_{ITN}.

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
11	NC	—	No Internal Connection. It is recommended to connect this pin to GND.
12	GND	G	Ground.
13	VREF	O	Reference Voltage Output Pin. SENSE4H can monitor a negative voltage if a resistor is connected between VREF and the negative power rail. This pin is designed to output current to the resistor(s). The resistor(s) does(do) not allow a voltage higher than 1.2V. This pin cannot be connected to a capacitor only.
14	V_{DD}	I	Supply Voltage Pin. It is recommended to connect a 0.1μF ceramic capacitor near this pin.
15	nRESET1	O	nRESET1 to nRESET4 are the active-low reset outputs of for SVS-1 to SVS-4 respectively. For SGM860A, nRESETx is an open-drain output pin. A pull-up resistor connected to V_{DD} or other source is required. nRESETx goes low when asserted and goes high when released after the delay time set by CTx ends. For SGM860B, nRESETx is a push-pull output pin. This pin goes low when nRESETx is asserted and goes high when nRESETx is released after the delay time set by CTx ends.
16	nRESET2	O	
17	nRESET3	O	
18	nRESET4	O	
19	nWDO	O	Watchdog Timer Output Pin. For SGM860A, nWDO is an open-drain output pin. When the watchdog timer runs out, this pin goes low. If not, it remains high. For SGM860B, nWDO is a push-pull output pin. When the watchdog timer runs out, this pin goes low. If not, it remains high.
20	WDI	I	Watchdog Timer Trigger Input Pin. A rising or falling edge within 630ms (TYP) period at this pin avoids the timeout failure of nWDO. The timer starts again once nRESET1 is released.
Exposed Pad	EP	G	Exposed Pad. Connect it to GND or other thermal pattern on the PCB.

NOTE: O = output; I = input; G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.8V to 6.5V, T_J = -40℃ to +125℃, $R_{nRESETx}$ = 100kΩ to V_{DD} (SGM860A only), $C_{nRESETx}$ = 50pF to GND, R_{nWDO} = 100kΩ to V_{DD} (SGM860A only), C_{nWDO} = 50pF to GND, V_{nMR} = 100kΩ to V_{DD}, WDI = GND, and CTx open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}			1.8		6.5	V
Supply Current (Current into V_{DD} Pin)	I_{DD}	nRESETx not asserted, WDI toggling (1), no output load, and VREF open	V_{DD} = 3.3V		6	14	μA
			V_{DD} = 6.5V		8	17	
Power-up Reset Voltage (2) (3)		V_{OL_MAX} = 0.2V, $I_{nRESETx}$ = 15μA				0.9	V
Negative-Going Input Threshold Voltage	V_{ITN}	SENSE1, SENSE2, SENSE3, SENSE4L		394	400	406	mV
Positive-Going Input Threshold Voltage	V_{ITP}	SENSE4H		394	400	406	mV
Hysteresis (Positive-Going) on V_{ITN}	V_{HYSN}	SENSE1, SENSE2, SENSE3, SENSE4L			3.5	10	mV
Hysteresis (Negative-Going) on V_{ITP}	V_{HYSP}	SENSE4H			3.5	10	mV
Input Current at SENSEy Pin	I_{SENSEy}	V_{SENSEy} = 0.42V		-30	±1	30	nA
CTx Pin Charging Current	I_{CTx}	C_{CTx} > 220pF, V_{CT1} = 0.5V (4)		220	285	350	nA
CTx Pin Threshold	V_{TH_CTx}	C_{CTx} > 220pF		1.195	1.240	1.290	V
nMR and WDI Logic Low Input	V_{IL}					0.3 × V_{DD}	V
nMR and WDI Logic High Input	V_{IH}			0.7 × V_{DD}			V
Low-Level nRESETx Output Voltage	V_{OL}	I_{OL} = 1mA				0.3	V
		SENSEy = 0V, 1.3V < V_{DD} < 1.8V, I_{OL} = 0.4mA (2)				0.3	
Low-Level nWDO Output Voltage	V_{OL}	I_{OL} = 1mA				0.3	V
High-Level nRESETx and nWDO Output Voltage (SGM860B only)	V_{OH}	I_{OL} = -1mA		V_{DD} - 0.4			V
Input UVLO Threshold (Rising)	V_{UVLO_H}				1.65		V
Input UVLO Threshold (Falling)	V_{UVLO_L}				1.63		V
nRESETx and nWDO Leakage Current (SGM860A only)	I_{LKG}	$V_{nRESETx}$ = 6.5V, nRESETx, nWDO = high		-300		300	nA
Reference Voltage Output	V_{REF}	1μA < I_{VREF} < 0.2mA (source only, no sink)		1.176	1.200	1.224	V
Input Pin Capacitance	C_{IN}	CTx = 0V to V_{DD}, other pins = 0V to 6.5V			5		pF

NOTES:

1. If the WDI is toggled for a duration shorter than the watchdog timer timeout period (t_{WDT}), it has a negitive influence on I_{DD}.

2. These parameters are outside the recommended V_{DD} range and only determine the performance of the nRESETx output during V_{DD} ramp up.

3. The lowest supply voltage (V_{DD}) required to activate nRESETx is defined as t_{RISE_VDD}, and it must be greater than or equal to 15μs/V.

4. CTx are constant current charging sources that operate within the range of 0V to V_{TH_CTx}, while the device is evaluated at V_{CTx} = 0.5V.

TIMING REQUIREMENTS

(V_{DD} = 1.8V to 6.5V, T_J = -40℃ to +125℃, $R_{nRESETx}$ = 100kΩ to V_{DD} (SGM860A only), $C_{nRESETx}$ = 50pF to GND, R_{nWDO} = 100kΩ to V_{DD} (SGM860A only), C_{nWDO} = 50pF to GND, V_{nMR} = 100kΩ to V_{DD}, WDI = GND, and CTx open, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Pulse Width to SENSEy and nMR Pins	t_W	SENSEy: 1.05 × V_{ITN} → 0.95 × V_{ITN} or 0.95 × V_{ITP} → 1.05 × V_{ITP}		3		μs
		nMR: 0.7 × V_{DD} → 0.3 × V_{DD} → 0.7 × V_{DD}		100		ns
nRESETx Delay Time	t_D	CTx Open	15	21	27	ms
		CTx = V_{DD}	225	315	410	
Watchdog Timer Timeout Period (1)	t_{WDT}		450	630	820	ms

NOTE:
1. Start from nRESET1 release or last WDI transition.

TIMING DIAGRAMS

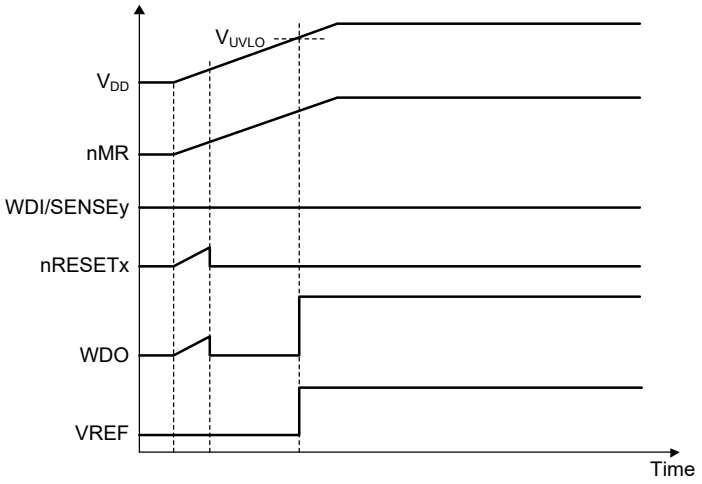


Figure 2. Initial Power-On State

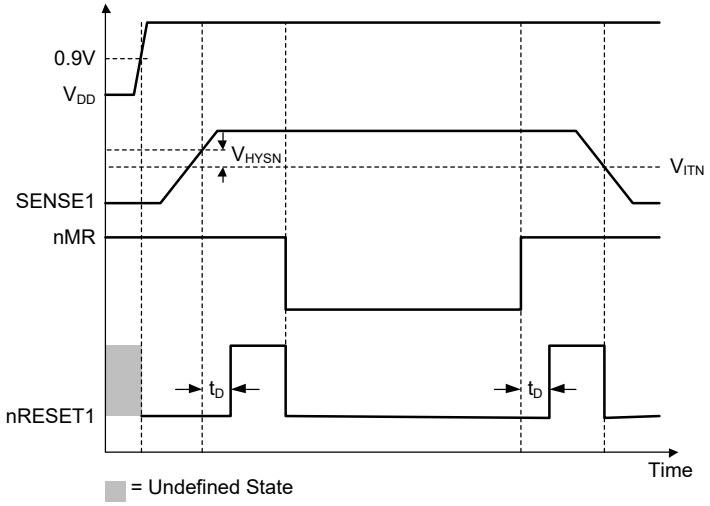


Figure 3. SVS-1 Timing Diagram

TIMING DIAGRAMS (continued)

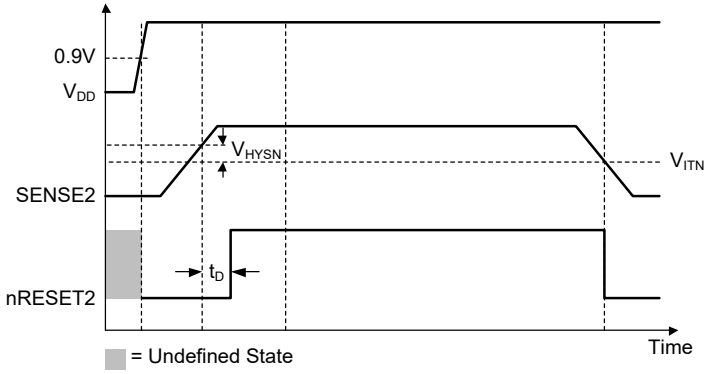


Figure 4. SVS-2 Timing Diagram

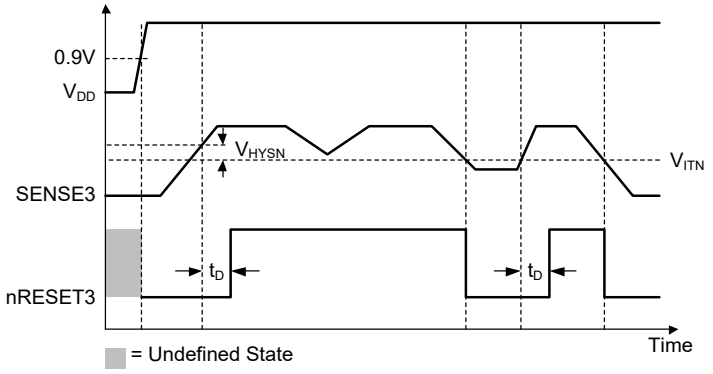


Figure 5. SVS-3 Timing Diagram

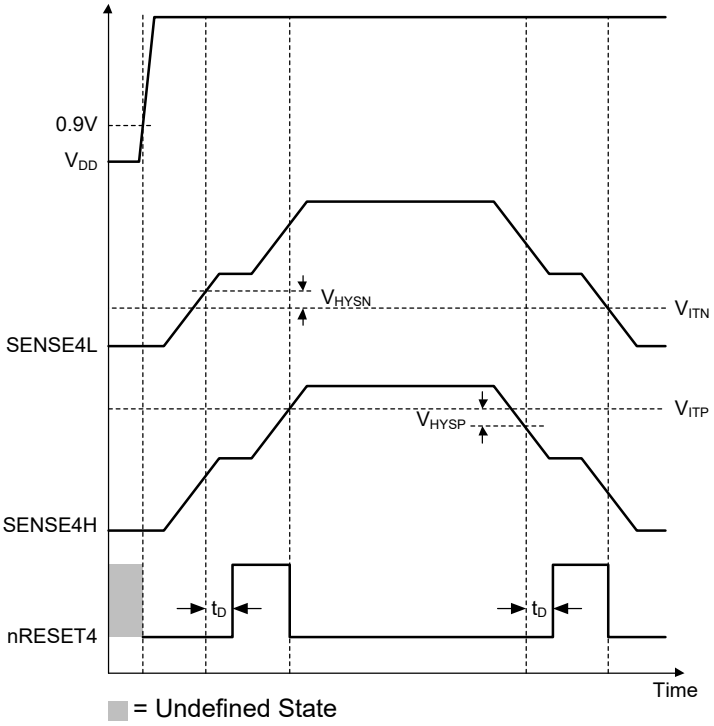


Figure 6. SVS-4 Timing Diagram

TIMING DIAGRAMS (continued)

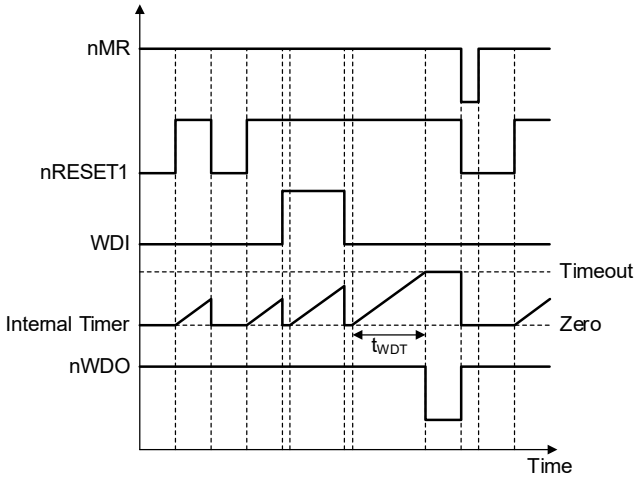


Figure 7. WDT Timing Diagram

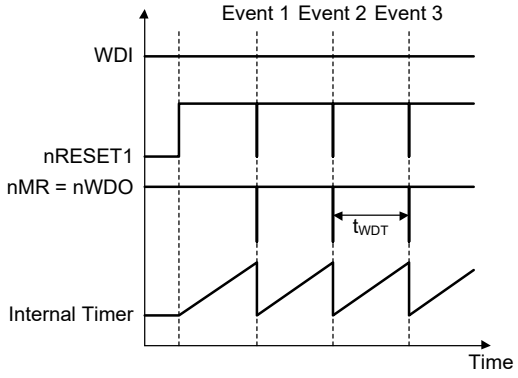


Figure 8. Legacy WDT Configuration Timing Diagram

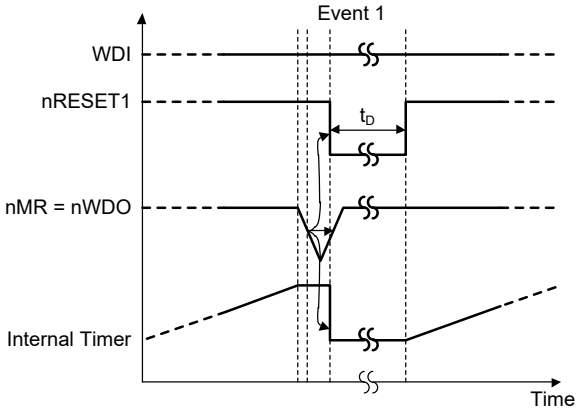
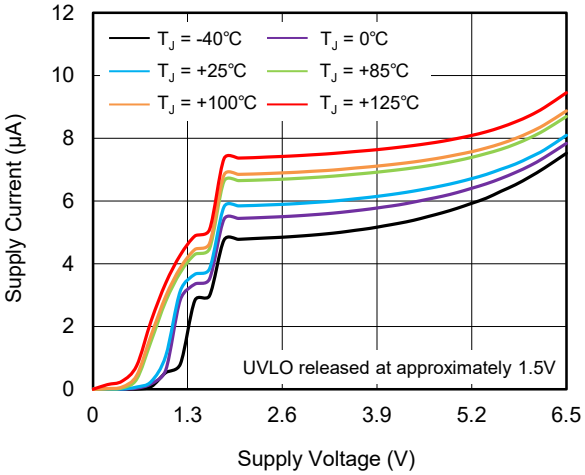


Figure 9. Enlarged View of Event 1 from Figure 8

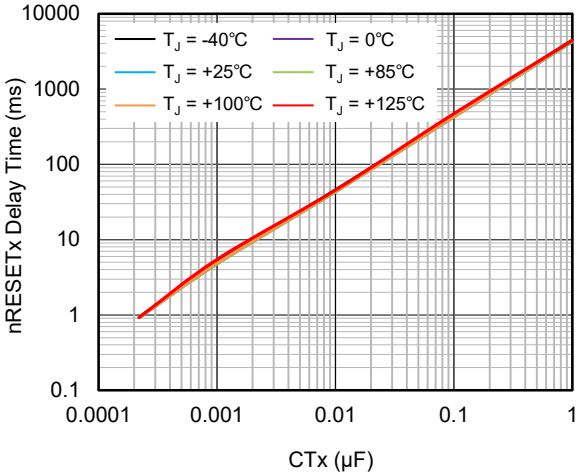
TYPICAL PERFORMANCE CHARACTERISTICS

SGM860A and SGM860B have the same characteristics, T_J = +25℃ and V_{DD} = 3.3V, unless otherwise noted.

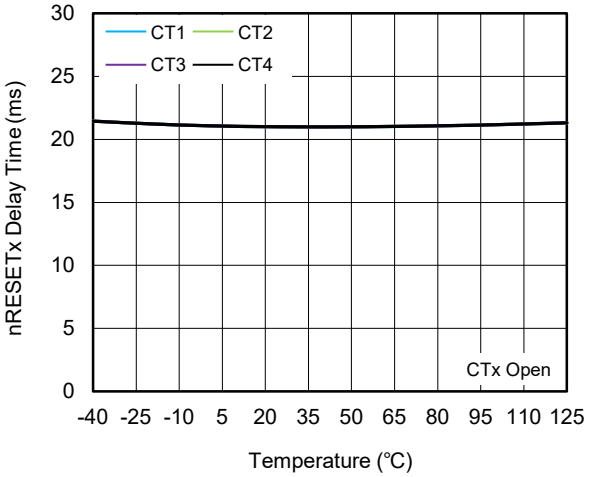
Supply Current vs. Supply Voltage



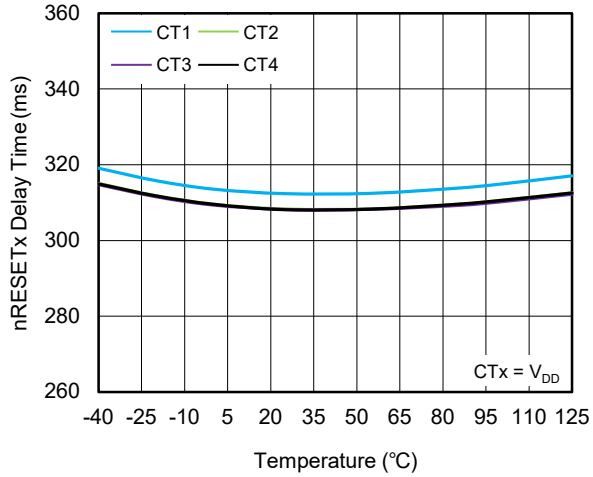
nRESETx Delay Time vs. CTx



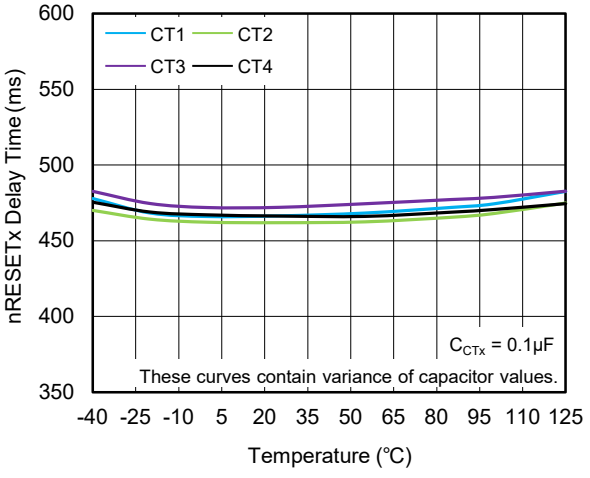
nRESETx Delay Time vs. Temperature



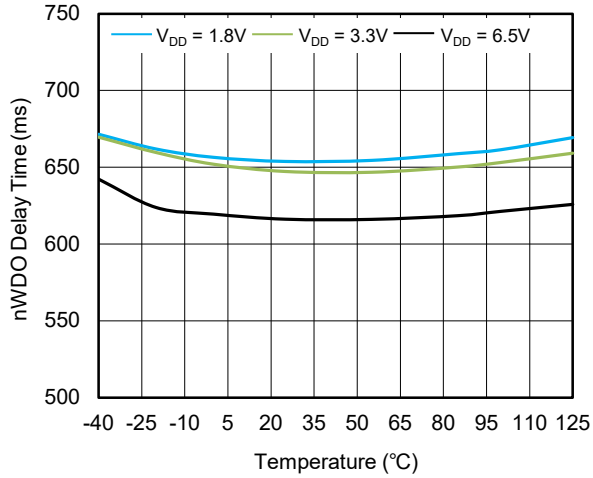
nRESETx Delay Time vs. Temperature



nRESETx Delay Time vs. Temperature (CTx = 0.1μF)



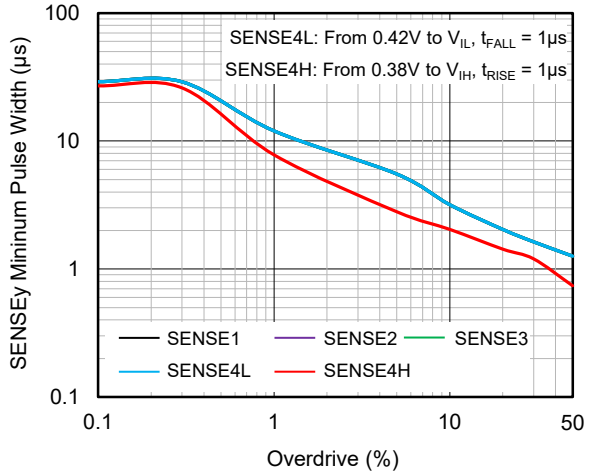
nWDO Delay Time vs. Temperature



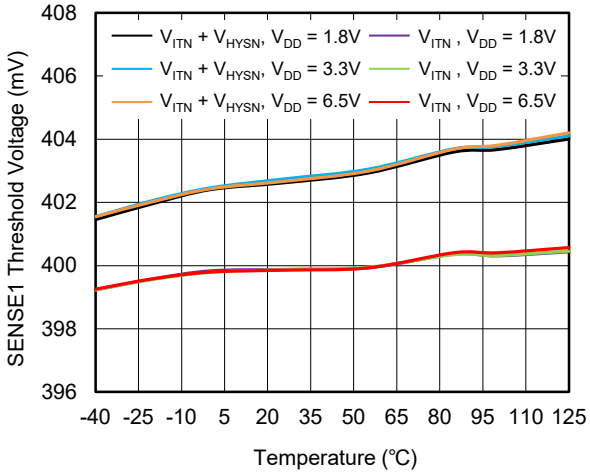
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SGM860A and SGM860B have the same characteristics, T_J = +25℃ and V_{DD} = 3.3V, unless otherwise noted.

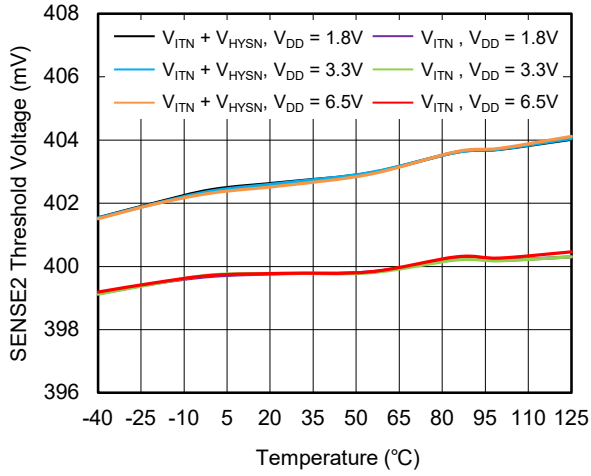
SENSEy Minimum Pulse Width vs. Threshold Overdrive Voltage



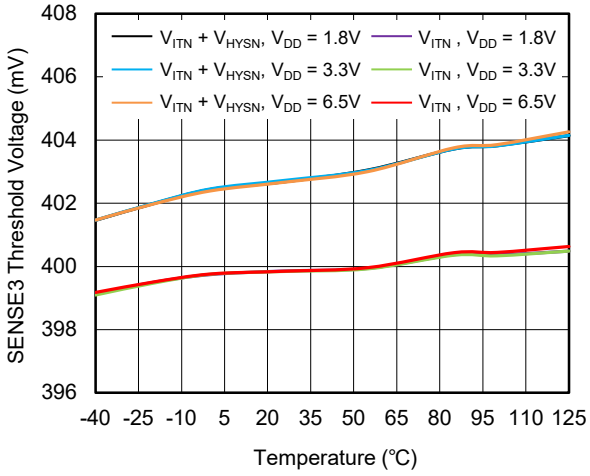
SENSE1 Threshold Voltage vs. Temperature



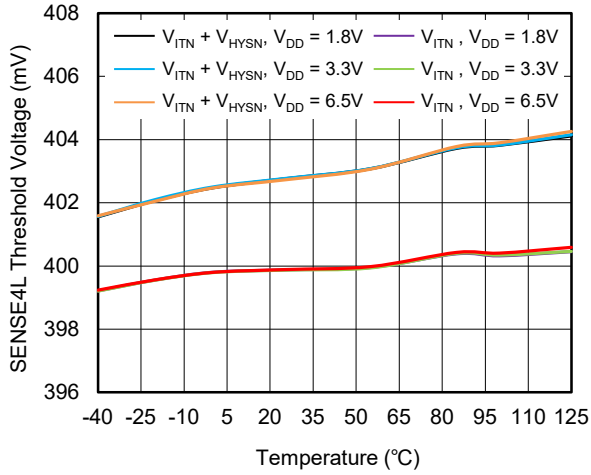
SENSE2 Threshold Voltage vs. Temperature



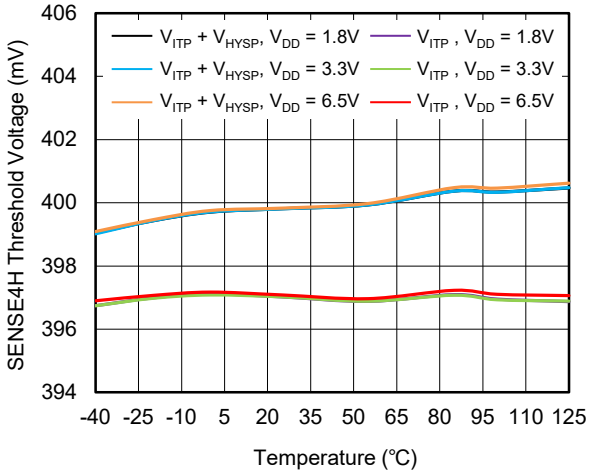
SENSE3 Threshold Voltage vs. Temperature



SENSE4L Threshold Voltage vs. Temperature



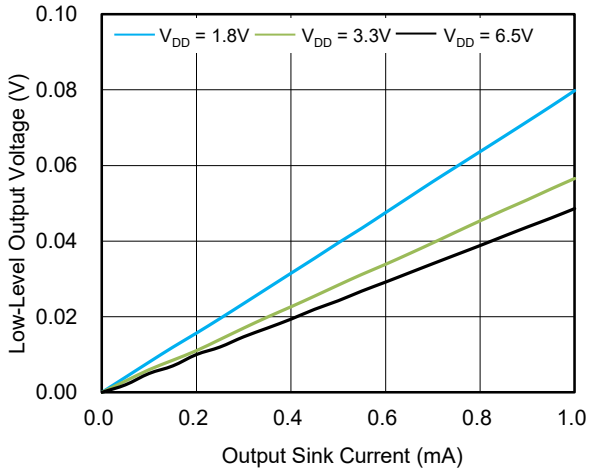
SENSE4H Threshold Voltage vs. Temperature



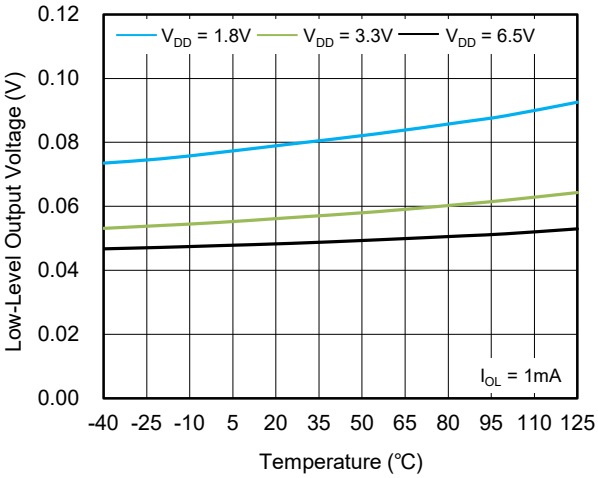
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SGM860A and SGM860B have the same characteristics, T_J = +25℃ and V_{DD} = 3.3V, unless otherwise noted.

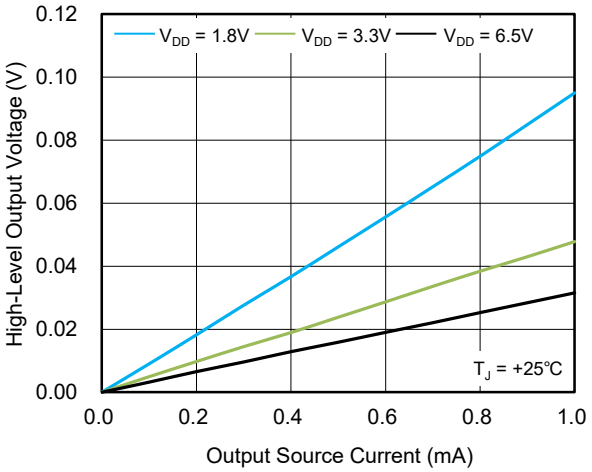
Low-Level Output Voltage vs. Output Sink Current



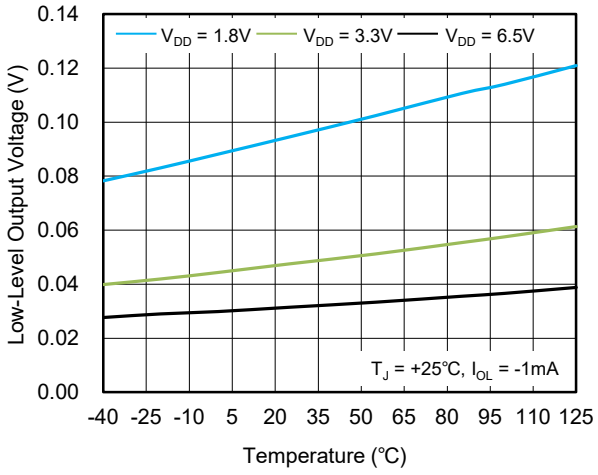
Low-Level Output Voltage vs. Temperature



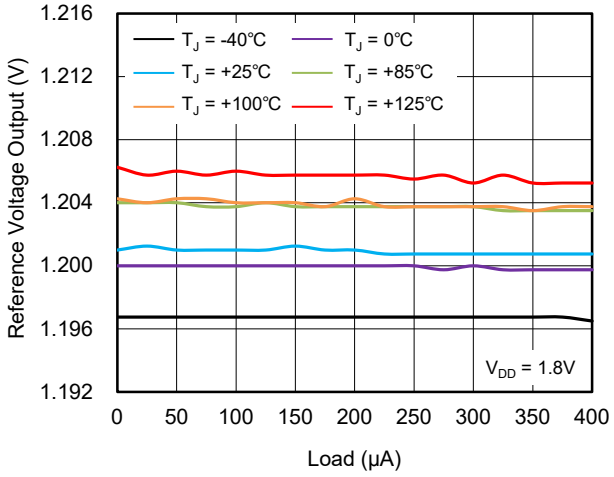
High-Level Output Voltage vs. Output Source Current



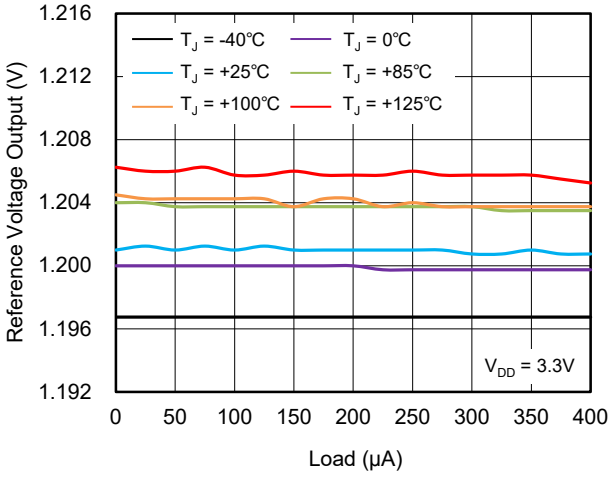
High-Level Output Voltage vs. Temperature



Reference Voltage Output Load Regulation



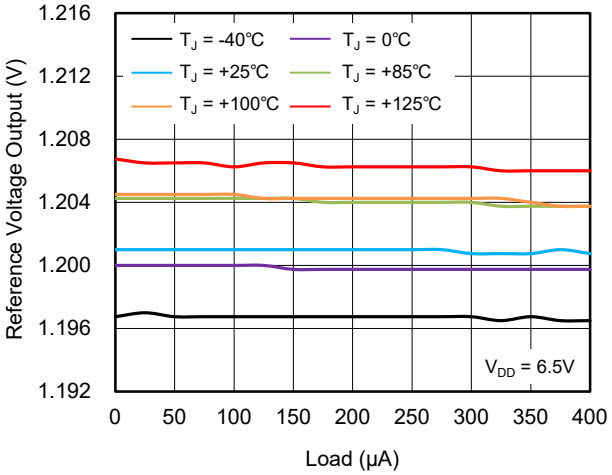
Reference Voltage Output Load Regulation



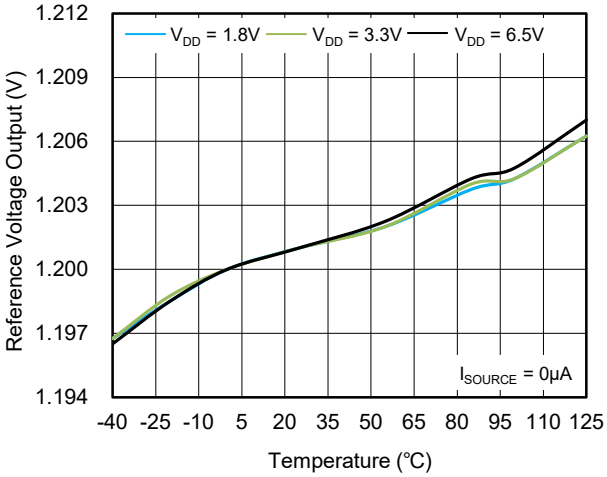
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SGM860A and SGM860B have the same characteristics, T_J = +25℃ and V_{DD} = 3.3V, unless otherwise noted.

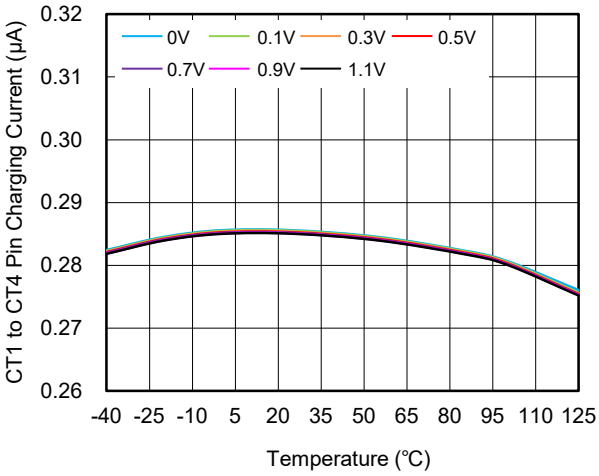
Reference Voltage Output Load Regulation



Reference Voltage Output vs. Temperature



CT1 to CT4 Pin Charging Current vs. Temperature Over CTx Pin Voltage



PARAMETER MEASUREMENT INFORMATION

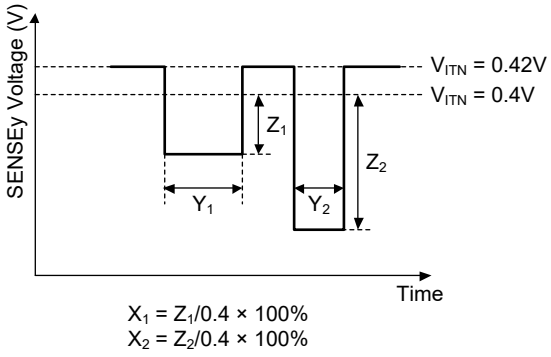


Figure 10. Overdrive Measurement Method

- X_1 and X_2 are overdrive (%) values calculated from actual SENSEy voltage amplitudes measured as Z_1 and Z_2.
- Y_N is the minimum pulse width that gives nRESETx or transition.
- Greater Z_N produces shorter Y_N.
- For SENSE4H, invert this graph with 180° on the voltage axis.

FUNCTIONAL BLOCK DIAGRAM

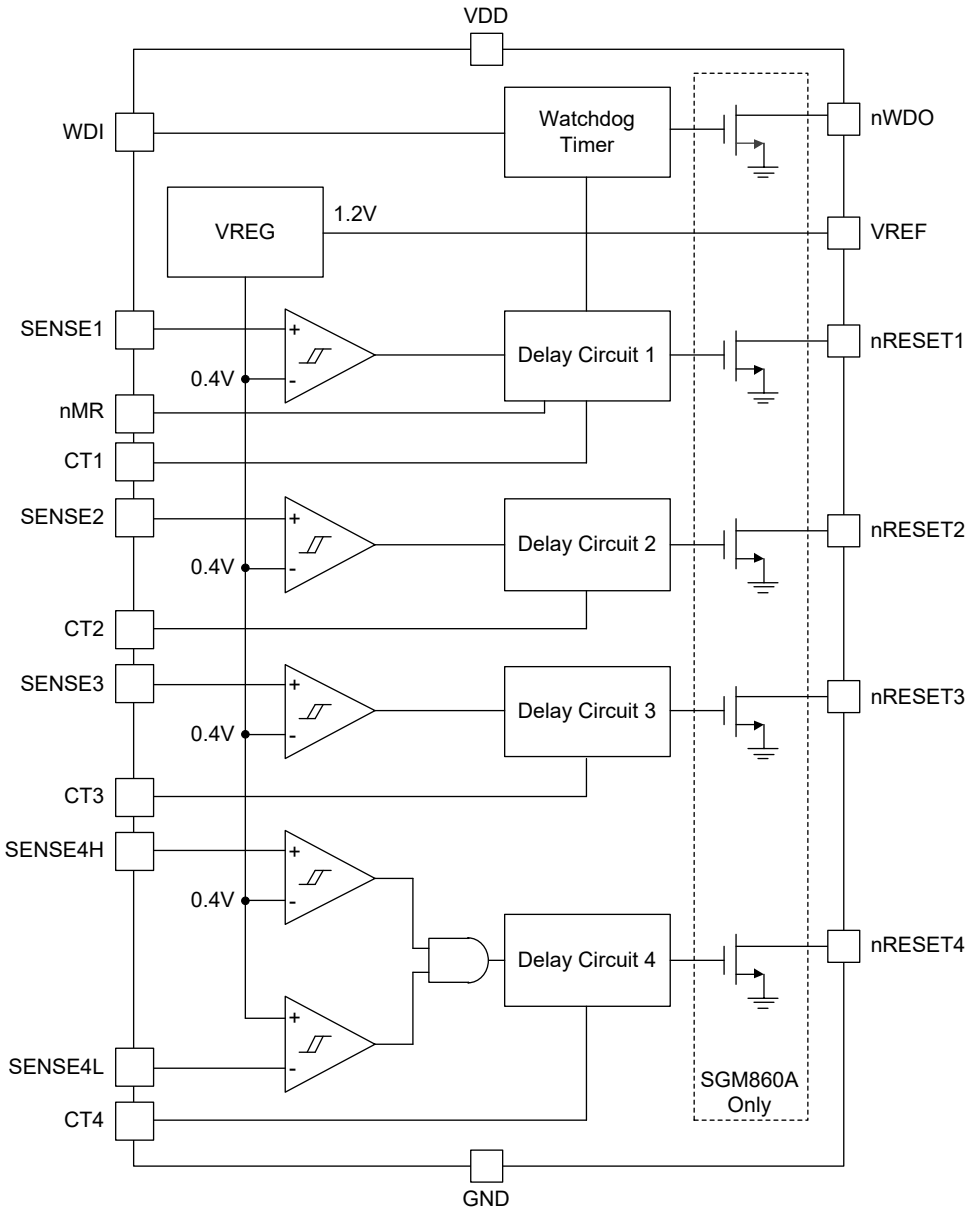


Figure 11. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM860 is a family of multi-channel voltage supervisors. It has four SVS function sets within one device, including a watchdog timer, a window comparator and negative voltage detection. The SGM860 will assert the nRESETx (x = 1, 2, 3, 4) signals as shown in Table 1 to Table 4. When the reset signal is released, the nRESETx remains asserted during the delay time programmed by the users. It also features very low quiescent current of 6μA (TYP).

Voltage Monitoring

With an external resistor divider, any voltage threshold over 0.4V can be monitored through each SENSEy (y = 1, 2, 3, 4L) pin. The SENSE4H pin can detect any over-voltage above 0.4V, or detect negative voltage through an external resistor divider. For more details, see the Sensing a Negative Voltage section. The SGM860 supports a wide range of voltage threshold detection and adjustable reset delay time, making these devices suitable for plenty of applications.

The SGM860 is not susceptible to short negative transients on SENSEy. The curve of SENSEy minimum pulse width vs. threshold overdrive voltage shows that the sensitivity to transients depends on threshold overdrive.

Manual Reset

The SGM860 provides a choice to use the manual reset (nMR) pin to initial the device reset. The nMR input is a logic signal provided externally from other processors, logic circuits, and/or discrete sensors. Because nMR is tied to SVS-1, nRESET1 is usually taken as the primary source to reset for the processor. When nMR goes low, nRESET1 is asserted. When nMR goes high and SENSE1 is above the reset threshold, nRESET1 is released when the delay time is configured by the users. Knowing that the nMR pin is pulled up internally through a 100kΩ resisitor, connect nMR to V_{DD} or just leave it floating once it is unnecessary to control it externally.

If more than one signal are used to control the nMR function, please use multiple N-MOS transistors and a pull-up resistor to combine the logic signals together by wire-OR.

Watchdog Timer

The SGM860 has a specialized watchdog error output named nWDO. The nWDO is very helpful to detect and fix the hang-up problems of a processor. The watchdog function is connected to SVS-1 as well. Details of timing diagram for WDT is shown in Figure 7. When nRESET1 is released, the WDT starts to count down. A logic level transition of WDI can reset the WDT and the timer starts to count down. However, if no transition of logic level is detected within t_{WDT}, then the WDT is timeout and will assert the nWDO. After the nWDO is asserted, the device is latched unless a reset of nRESET1 is activated. For example, a negative nMR pulse, SENSE1 voltage is below V_{ITN} or V_{DD} is off.

In order to reset the processor when the WDT timeout event occurs, the user can combine the nWDO with nRESET1 by wire-OR. In legacy applications, where the WDT timeout asserts nRESET1, connect the nWDO to nMR. Figure 15 shows the connections, and Figure 8 and Figure 9 show the timing diagram.

Reset Output

In a typical application for SGM860, the user can connect the nRESETx pin to a processor like DSP, ASIC, FPGA and CPU as the reset input pin, or connect it to a voltage regulator like DC/DC converter and LDO as the enable input signal.

The reset outputs of SGM860A are open-drain structure and pull-up resistors are needed to hold the lines high if nRESETx is not asserted. The nRESETx can be connected to other devices at correct voltage level by connecting the pull-up resistor to the proper voltage rails. Choose the pull-up resistor larger than 10kΩ for the safe operation of output transistors. Any combination of nRESETx can be combined into one logic signal with the wire-OR logic.

The SGM860B provides push-pull reset outputs and the logic high level is determined by V_{DD}. Hence, the pull-up resistor is not needed and the board area can be saved. However, users must ensure that all interface logic level are checked and all nRESETx connections must match the V_{DD} logic level.

DETAILED DESCRIPTION (continued)

The nRESET outputs are defined when the V_{DD} is higher than 0.9V. For the proper reset of the processor, V_{DD} should be provided as early as possible in the application circuits. The initial power-on state is shown in Figure 2. Table 1 to Table 4 describe how the outputs are asserted or released. Timing diagrams of SVS-x are shown in Figure 3 to Figure 6. Once the conditions are qualified, the SVS-x transfers from asserted to released after a delay time set by the user. But the SVS-x transfers from released to asserted immediately with minimum propagation delay. The relationship between threshold voltages (V_{ITN}, V_{HYSN}) and SENSEy voltage is depicted in Figure 5. SVS-1 to SVS-4 have the same behavior like Figure 5.

Device Functional Modes

Table 1 to Table 5 provide the state of different parts under specialized cases.

Table 1. SVS-1 Truth Table

Condition		nRESET1 Output	Reset Status
nMR Low	SENSE1 < V_{ITN}	Low	Asserted
nMR Low	SENSE1 > V_{ITN}	Low	Asserted
nMR High	SENSE1 < V_{ITN}	Low	Asserted
nMR High	SENSE1 > V_{ITN}	High	Released after delay

Table 2. SVS-2 Truth Table

Condition	nRESET2 Output	Reset Status
SENSE2 < V_{ITN}	Low	Asserted
SENSE2 > V_{ITN}	High	Released after delay

Table 3. SVS-3 Truth Table

Condition	nRESET3 Output	Reset Status
SENSE3 < V_{ITN}	Low	Asserted
SENSE3 > V_{ITN}	High	Released after delay

Table 4. SVS-4 Truth Table

Condition		nRESET4 Output	Reset Status
SENSE4L < V_{ITN}	SENSE4H > V_{ITP}	Low	Asserted
SENSE4L < V_{ITN}	SENSE4H < V_{ITP}	Low	Asserted
SENSE4L > V_{ITN}	SENSE4H > V_{ITP}	Low	Asserted
SENSE4L > V_{ITN}	SENSE4H < V_{ITP}	High	Released after delay

Table 5. Watchdog Timer (WDT) Truth Table

Condition				nWDO Output	Status
nWDO	WDO	nRESET1	WDI Pulse Input		
Low	High	Asserted	Toggling	low	Remain in WDT timeout
Low	High	Asserted	630ms after last WDI↑ or WDI↓	low	Remain in WDT timeout
Low	High	Released	Toggling	low	Remain in WDT timeout
Low	High	Released	630ms after last WDI↑ or WDI↓	low	Remain in WDT timeout
High	Low	Asserted	Toggling	high	Normal operation
High	Low	Asserted	630ms after last WDI↑ or WDI↓	high	Normal operation
High	Low	Released	Toggling	high	Normal operation
High	Low	Released	630ms after last WDI↑ or WDI↓	low	Enter WDT timeout

APPLICATION INFORMATION

Under-Voltage Detection

The SGM860 provides the SENSEy pins to monitor the system voltages. Once the voltage at SENSEy (y = 1, 2, 3, 4L) drops below V_{ITN}, the corresponding reset pin goes low. If the voltage at SENSE4H is higher than V_{ITP}, the nRESET4 is activated. In order to smooth the transitions between reset output assertion or deassertion, an internal hysteresis is added to the comparators. To suppress the noise caused by transients, layout parasitism and interference between power rails, place a bypass capacitor in the range of 1nF to 10nF at SENSEy. Figure 15 shows a typical connection of the resistor divider network. Voltage rails down to 0.4V can be detected by SENSEy and the threshold voltages can be obtained with Equation 1 to Equation 3.

$$V_{MON\_1} = \left(1 + \frac{R_{S1H}}{R_{S1L}}\right) \times 0.4(V) \quad (1)$$

$$V_{MON\_2} = \left(1 + \frac{R_{S2H}}{R_{S2L}}\right) \times 0.4(V) \quad (2)$$

$$V_{MON\_3} = \left(1 + \frac{R_{S3H}}{R_{S3L}}\right) \times 0.4(V) \quad (3)$$

Under-Voltage and Over-Voltage Detection

The comparison polarity of the comparator at SENSE4H is different from other SENSEy pins. As can be seen in Figure 12, this comparator supervises the over-voltage of V_{MON_4}, a window comparator of SVS-4 is formed with this comparator and SENSE4L.

$$V_{MON\_4,UV} = \left(1 + \frac{R_{S4H}}{(R_{S4M} + R_{S4L})}\right) \times 0.4(V) \quad (4)$$

$$V_{MON\_4,OV} = \left(1 + \frac{(R_{S4H} + R_{S4M})}{R_{S4L}}\right) \times 0.4(V) \quad (5)$$

Where:

$V_{MON\_4,UV}$ is the under-voltage threshold.

$V_{MON\_4,OV}$ is the over-voltage threshold.

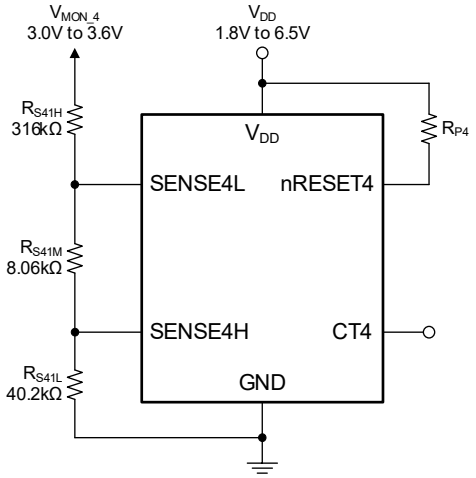


Figure 12. SVS-4: Window Comparator

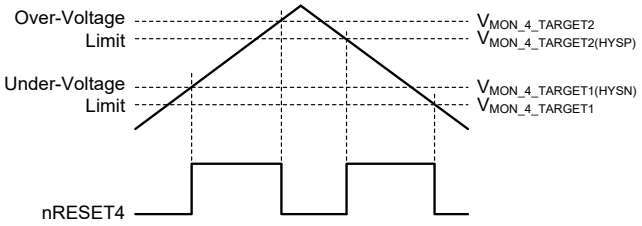


Figure 13. Window Comparator Operation

Sensing a Negative Voltage

To monitor a voltage less than 0.4V (either positive or negative), the SVS-4 comparator along with voltage reference output VREF is used and the diagram is depicted in Figure 14. Here, the SVS-4 monitors the positive voltage and negative voltage at the power rail (in Figure 14, that is the ±15V supply to an operation amplifier) and the status of nRESET4 changes as described in Table 4. R_{S42H} and R_{S42L} are placed at high and low voltage positions, respectively. Calculation of the voltage threshold is presented in Equation 6 and 7.

$$V_{MON\_4,POS} = \left(1 + \frac{R_{S41H}}{R_{S41L}}\right) \times 0.4(V) \quad (6)$$

$$V_{MON\_4,NEG} = \left(1 + \frac{R_{S42L}}{R_{S42H}}\right) \times 0.4 - \frac{R_{S42L}}{R_{S42H}} \times V_{REF}$$

$$= 0.4 - \left(\frac{R_{S42L}}{R_{S42H}} \times 0.8(V)\right) \quad (7)$$

APPLICATION INFORMATION (continued)

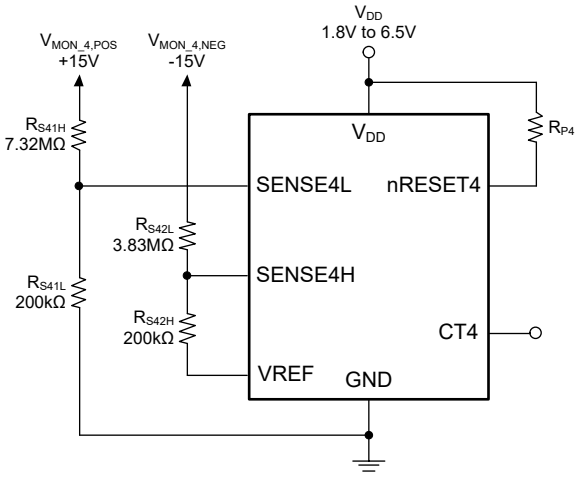


Figure 14. SVS4: Negative Voltage Sensing

Reset Delay Time

Each SVS channel can be programmed alone within three modes. The delay time settings are described in Table 6.

Table 6. Delay Timing Selection

CTx Connection	Delay Time
Pull up to V_{DD}	315ms (TYP)
Open	21ms (TYP)
Capacitor to GND	Programmable

In order to set the delay time as 315ms, a pull-up resistor in the range of 40kΩ to 200kΩ should be placed between the CTx pin and V_{DD}. When the device powers up, a pull-down transistor connected between CTx and GND turns on to decide and check the CTx status. Therefore, a large current flow is aroused for the direct connection between CTx and GND. As for setting a fixed delay time of 21ms, keep CTx pin floating. To set a delay time defined by the user, put a capacitor between CTx and GND and the delay time can be calculated as follows:

$$C_{CT}(nF) = \left[t_{DELAY}(ms) - 0.5(ms)\right] \times 0.23 \quad (8)$$

With Equation 8, a delay time from 1.45ms to 10s can be obtained. For the SGM860, to identify the capacitance between CTx and GND from a floating pin, choose the external capacitor greater than 220pF. The reset delay time is decided when the external capacitor voltage is charged to 1.24V by the on-chip and highly accurate current source of 285nA. Once the nRESET signal is asserted, the external capacitor is discharged. On the contrary, the internal current source is activated and starts to charge the external capacitor when the condition for releasing nRESETx occurs. If the CTx voltage rises up to 1.24V, the corresponding nRESET is released. As for the capacitor, choose a low leakage one such as ceramic capacitor. Note that the reset delay time may be different from the one set by users because of the stray capacitance at this pin. The CTx pins are susceptible to interference, and their routing should be as short as possible, requiring shielding treatment.

Typical Application

Design Requirements

The circuit provided in Figure 15 is designed to supervise the voltage condition in an FPGA. Detailed requirements are given in Table 7.

Table 7. Design Requirements

Parameter	Design Requirement
V_{DD}	5V
V_{MON_1}	1.8V, -5%
V_{MON_2}	1.5V, -5%
V_{MON_3}	1.2V, -5%
V_{MON_4}	1V, ±5%
Approximate startup time	100ms

APPLICATION INFORMATION (continued)

Detailed Design Procedure

To make sure V_{OL} is not higher than 0.4V, choose the pull-up resistors of 100kΩ.

The startup delay time of 100ms for all channels with C_T = 23nF can be calculated with Equation 8.

Choose a resistor of 10kΩ for R_{SxL} to guarantee a high DC accuracy.

The values of R_{SxH} and R_{S4M} can be calculated using Equation 1 to 5 with standard 1% resistors. Table 8 shows the results.

Table 8. Design Results

Resistor	Value (kΩ)
R_{S1H}	32.4
R_{S2H}	25.5
R_{S3H}	18.7
R_{S4H}	14.3
R_{S4M}	1

Due to the lack of a separate fault input of watchdog for FPGA, use a legacy connection of nWDO and nMR.

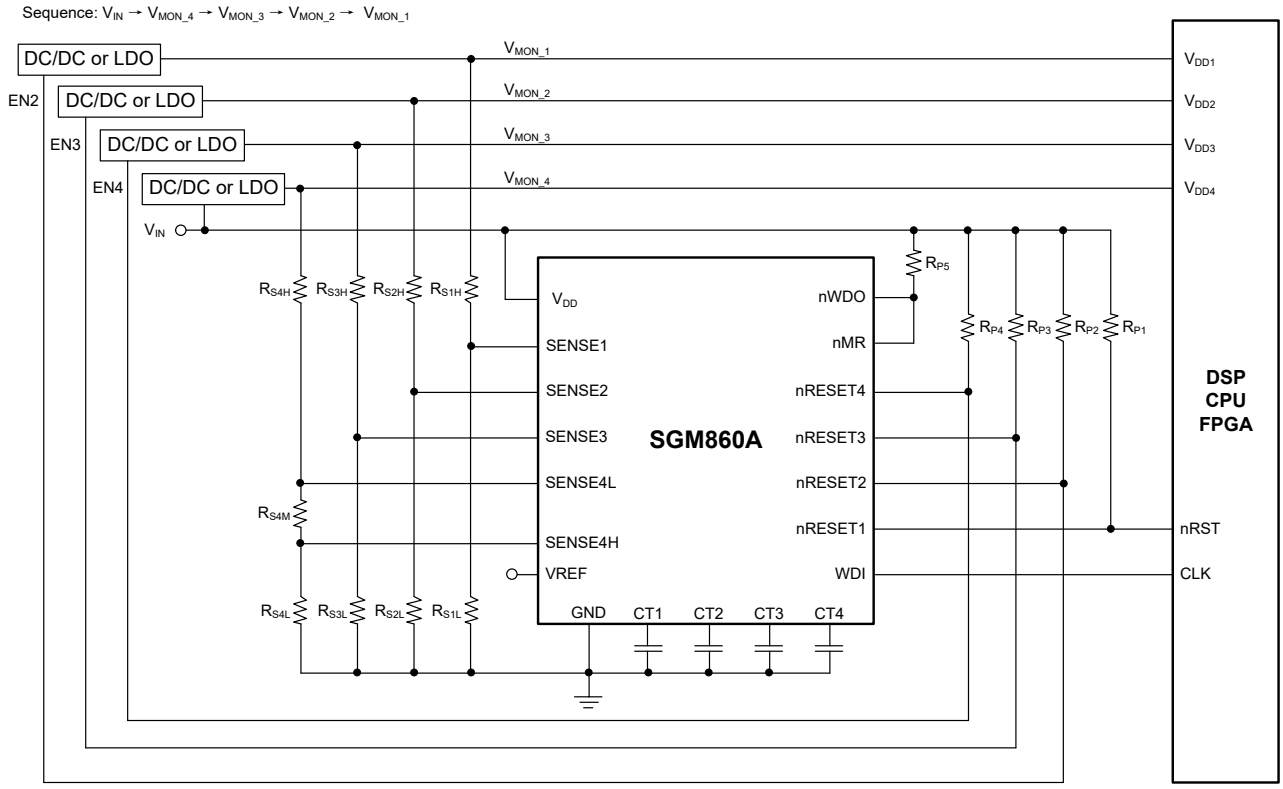


Figure 15. Typical Application Circuit

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM860 works from 1.8V to 6.5V input voltage. It is a good analog practice to place a 0.1μF capacitor between V_{DD} and GND. The input power supply must be higher than 1.8V normally to avoid reset activated by the internal UVLO circuit.

Layout

Some guidelines are given below to prepare the layout of the printed-circuit board (PCB) for SGM860.

1) CTx pins routing should be as short as possible to improve accuracy and require shielding treatment.

2) Take short traces from SENSEy to the resistor divider and long traces from R_{SxH} to $V_{MON\_x.}$

3) Connect V_{DD} capacitor as close as possible to the device.

4) Use short traces to connect V_{DD}. The parasitic inductance from the supply to the capacitor and the capacitor at V_{DD} form an LC tank and may lead to ring voltages that higher than the maximum allowed V_{DD} voltage.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

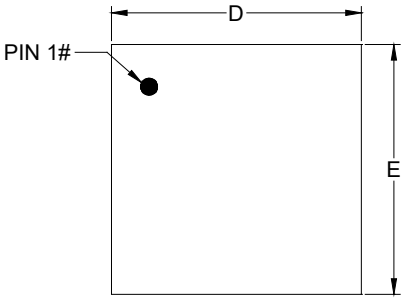
AUGUST 2024 – REV.A.1 to REV.A.2	Page
Updated Application Information section	16

JUNE 2024 – REV.A to REV.A.1	Page
Updated Application Information section	18

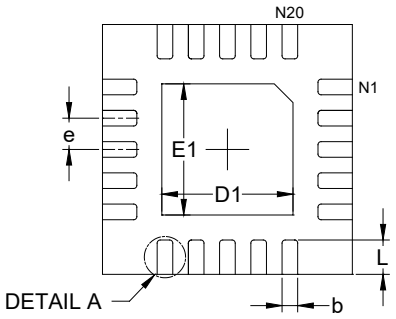
Changes from Original (NOVEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

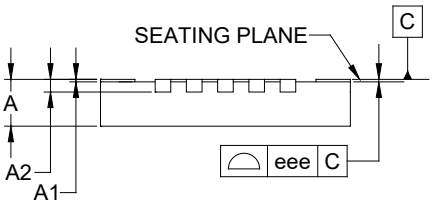
TQFN-4×4-20BL



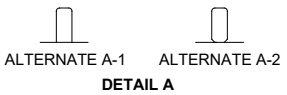
TOP VIEW



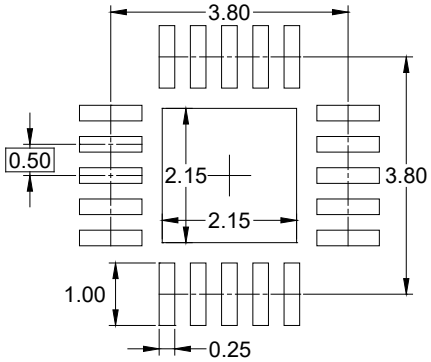
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



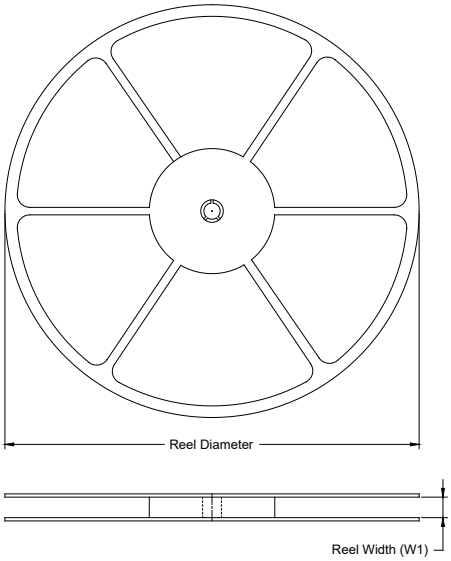
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.900	-	4.100
D1	2.000	-	2.200
E	3.900	-	4.100
E1	2.000	-	2.200
e	0.500 BSC		
L	0.450	-	0.650
eee	0.080		

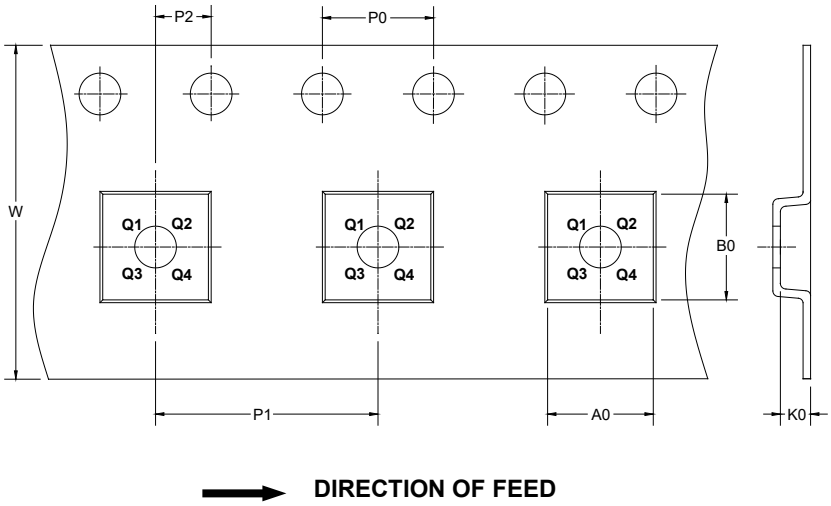
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



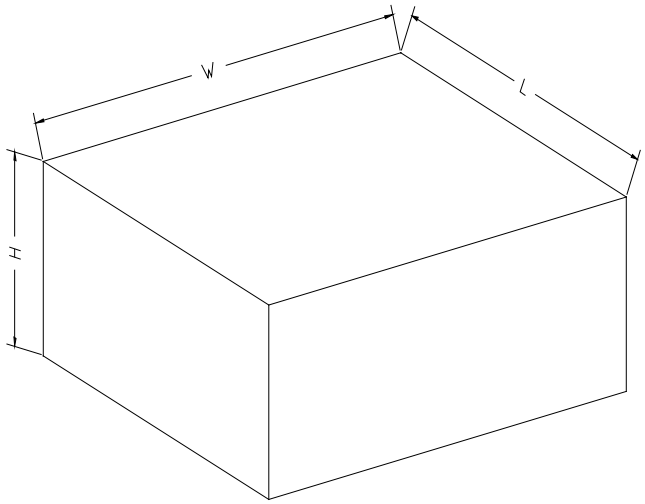
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-20BL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002