SGM864S
4-Channel
Adjustable Power Supply Sequencer

GENERAL DESCRIPTION

The SGM864S is an integrated, 4-rail power sequencer. It controls the power-up and power-down sequence of four power supplies by pulling their enable or shutdown pins high or low. Staggered start sequence can avoid the impact of latch conditions or large inrush current on system reliability.

The device has five open-drain outputs that are controled by five enable pins. When the EN pin is pulled high and the ENx pin is high, each of the four outputs (OUT1 to OUT4) is released after a fixed delay time, which can be adjusted by the NP0 capacitor outside the CDLYx pin. When EN remains high and any ENx is pulled low, the OUTx will be shut down correspondingly. When ENx remains high and EN is pulled low, the outputs are pulled low in reverse order (from OUT4 to OUT1) after CDLY programmable delay time. If the four OUTx all output high, the PG pin outputs high.

The SGM864S also includes an internal clamp voltage regulator that stabilizes the internal reference voltage at 5V with an accuracy of ±2.6% by using shunt resistors (R_{SHUNT}) on VCC. The maximum external supply voltage (V_{DD}) is 22V. The total value of the capacitor (C_{IN}) pulled down to GND should be limited to between 1μF and 10μF. When V_{CC} is 2V to 5.5V, set EN_REF to high or connect it to VCC, then the shunt voltage reference is disabled. VCC does not require any external resistor. Once V_{CC} rises above 6V, the shunt voltage reference is enabled. Set EN_REF to low or keep it floating (a 500kΩ built-in resistor). VCC requires the shunt resistors of 130Ω to 40kΩ.

The SGM864S is available in a Green TQFN-3.5×3.5-20L package. It operates over a junction temperature range of -40℃ to +125℃.

FEATURES

- **Sequence Four Voltage Rails**
- **Input Voltage Range: 2V to 5.5V**
- **Shunt Voltage Reference: 5V (±2.6% Accuracy)**
- **EN and ENx Threshold Voltage: 1.23V (TYP)**
- **Hysteresis: ≥ 0.2V**
- **Low Quiescent Current: 55μA (TYP)**
- **Capacitor-Adjustable Delay Time**
- **External Power Supply by VCC when Shunt Voltage Reference is Enabled: 15mA (MAX)**
- **Sequence Controlled by ENx and CDLYx Pins**
- **Power Good Function**
- **Open-Drain OUTx Outputs**
- **Available in a Green TQFN-3.5×3.5-20L Package**

APPLICATIONS

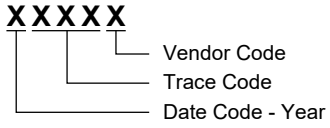
Communication Equipment
Enterprise Servers
5G Wireless Product
DC/DC Converters
Power Inverter

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM864S	TQFN-3.5×3.5-20L	-40℃ to +125℃	SGM864SXTRL20G/TR	0NJ XTRL20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{CC} ..... -0.3V to 6V
EN, ENx Voltages ..... -0.3V to 6V
OUTx Voltage ..... -0.3V to 6V
Input Current 15mA
Package Thermal Resistance
TQFN-3.5×3.5-20L, θ_{JA} ..... 41.6℃/W
TQFN-3.5×3.5-20L, θ_{JB} ..... 18.9℃/W
TQFN-3.5×3.5-20L, θ_{JC_TOP} ..... 41.5℃/W
TQFN-3.5×3.5-20L, θ_{JC_BOT} ..... 6.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{CC} ..... 2V to 5.5V
Shunt Resistor, R_{SHUNT} (1) ..... 130Ω to 40kΩ
Delay Capacitor, C_{DELAY} (2) ..... 100nF (MAX)
Total Capacitor on VCC, C_{IN} ..... 1μF to 10μF
Pull-up Resistor, $R_{PULL-UP}$ ..... 10kΩ to 100kΩ
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:
1. R_{SHUNT} should be power resistor.
2. C_{DELAY} should be NP0 capacitor.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

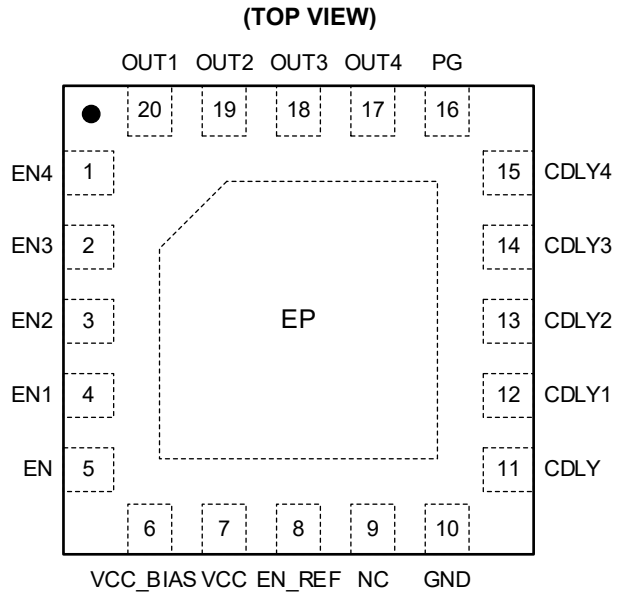
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



TQFN-3.5×3.5-20L

PIN DESCRIPTION

PIN	NAME	FUNCTION	
1	EN4	Voltage Rail 4 Enable Pin. 1.23V Threshold Voltage. A 500kΩ pull-down resistor is internally set.	
2	EN3	Voltage Rail 3 Enable Pin. 1.23V Threshold Voltage. A 500kΩ pull-down resistor is internally set.	
3	EN2	Voltage Rail 2 Enable Pin. 1.23V Threshold Voltage. A 500kΩ pull-down resistor is internally set.	
4	EN1	Voltage Rail 1 Enable Pin. 1.23V Threshold Voltage. A 500kΩ pull-down resistor is internally set.	
5	EN	ENx Controlled Pin. The ENx input flitering time is 600ns (TYP). If EN is set high (EN = 1), the ENx asserts after an adjustable CDLYx time. If EN is low (EN = 0), the OUTx asserts in reverse order (from OUT4 to OUT1). 1.23V threshold voltage. A 500kΩ pull-down resistor is internally set.	
6	VCC_BIAS	Low-Level Output Confirmed Pin. Connect a 1MΩ to 10MΩ resistor to the external power supply. The maximum current consumption flowing through this resistor is 22μA.	
7	VCC	2V to 5.5V Supply Voltage. If V_{DD} is higher than 6V, VCC has the drive capability to provide current externally and stabilizes the internal reference voltage at 5V.	
8	EN_REF	Active-Low Enable Input Pin. Pulling this pin logic low or keeping it floating enables the shunt voltage reference. Pulling this pin logic high or connecting it to VCC disables the shunt voltage reference. Use this pin to adjust the VCC shunt voltage reference to 5V. And a 500kΩ pull-down resistor is internally set.	
9	NC	No Connection. It is recommended to connect it to GND.	
10	GND	Ground.	
11	CDLY	Connecting an NP0 capacitor (100nF, MAX) between this pin and GND to select the programmable delay time. See Table 1 for more details.	
12	CDLY1	Connecting an NP0 capacitor (100nF, MAX) between this pin and GND to select the programmable delay time.	Capacitor-Adjustable Delay Pin for EN1.
13	CDLY2		Capacitor-Adjustable Delay Pin for EN2.
14	CDLY3		Capacitor-Adjustable Delay Pin for EN3.
15	CDLY4		Capacitor-Adjustable Delay Pin for EN4.
16	PG	Power Good Open-Drain Output. If the four OUTx all output high, the PG pin outputs high. If any OUTx outputs low, the PG pin outputs low. Before the VCC rises to 1V, Pull up a resistor of 10kΩ from OUTx, and the equivalent impedance of the OUTx to GND is 1kΩ.	
17	OUT4	Active-High Open-Drain Output Pin. Before the VCC rises to 1V, Pull up a resistor of 10kΩ from OUTx, and the equivalent impedance of the OUTx to GND is 1kΩ.	OUT4 is the output for EN4.
18	OUT3		OUT3 is the output for EN3.
19	OUT2		OUT2 is the output for EN2.
20	OUT1		OUT1 is the output for EN1.
—	EP	Exposed Pad.	

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2V to 5.5V, T_J = -40℃ to +125℃, typical values are measured at V_{CC} = 5V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Operating Voltage Range	V_{CC}		2		5.5	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{CC} falling	1.51	1.57	1.64	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	V_{CC} rising	170	230	280	mV
V_{CC} Supply Current	I_{CC}			55	110	μA
V_{CC} Shunt Voltage				5		V
Accuracy on VCC			-2.6		2.6	%
EN/ENx						
High-Level Input Voltage	V_{EN_H}, V_{ENx_H}	t_F = 600ns	1.18	1.23	1.28	V
Low-Level Input Voltage	V_{EN_L}, V_{ENx_L}		0.97	1.01	1.05	V
EN_REF						
EN_REF Low-Level Input Voltage	V_{IL}				0.3 × V_{CC}	V
EN_REF High-Level Input Voltage	V_{IH}		0.7 × V_{CC}			V
CDLY/CDLYx						
Charging Current	I_{CDELAY}			2		μA
Threshold Voltage				750		mV
Oscillator Power Consumption		V_{CC} = 5V (1)		110	220	μA
Parasitic Capacitance	ΔC			4		pF
OUT/OUTx						
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.2	V
Output Open-Drain Leakage Current	I_{LKG}				0.5	μA
OUT/OUTx Pull-Down Resistance (2)	R_{OUTx}	$R_{PULL-UP}$ = 10kΩ, V_{CC} = 600mV		1		kΩ
Switching						
Adjustable Delay Time	t_D				1.5	s
Adjustable Delay Time Accuracy		After 2ms delay	-11		11	%
EN Input Filtering Time	t_F		100	600	1200	ns

NOTES:

1. When V_{CC} is 5V, all four channels are in the judge process (the CDLY oscillator is on for each channel).
2. Connect a 10kΩ pull-up resisitor to OUTx. At the worst corner, the 1kΩ (TYP) pull-down resistor is provided by V_{CC} = 750mV.

TIMING DIAGRAM

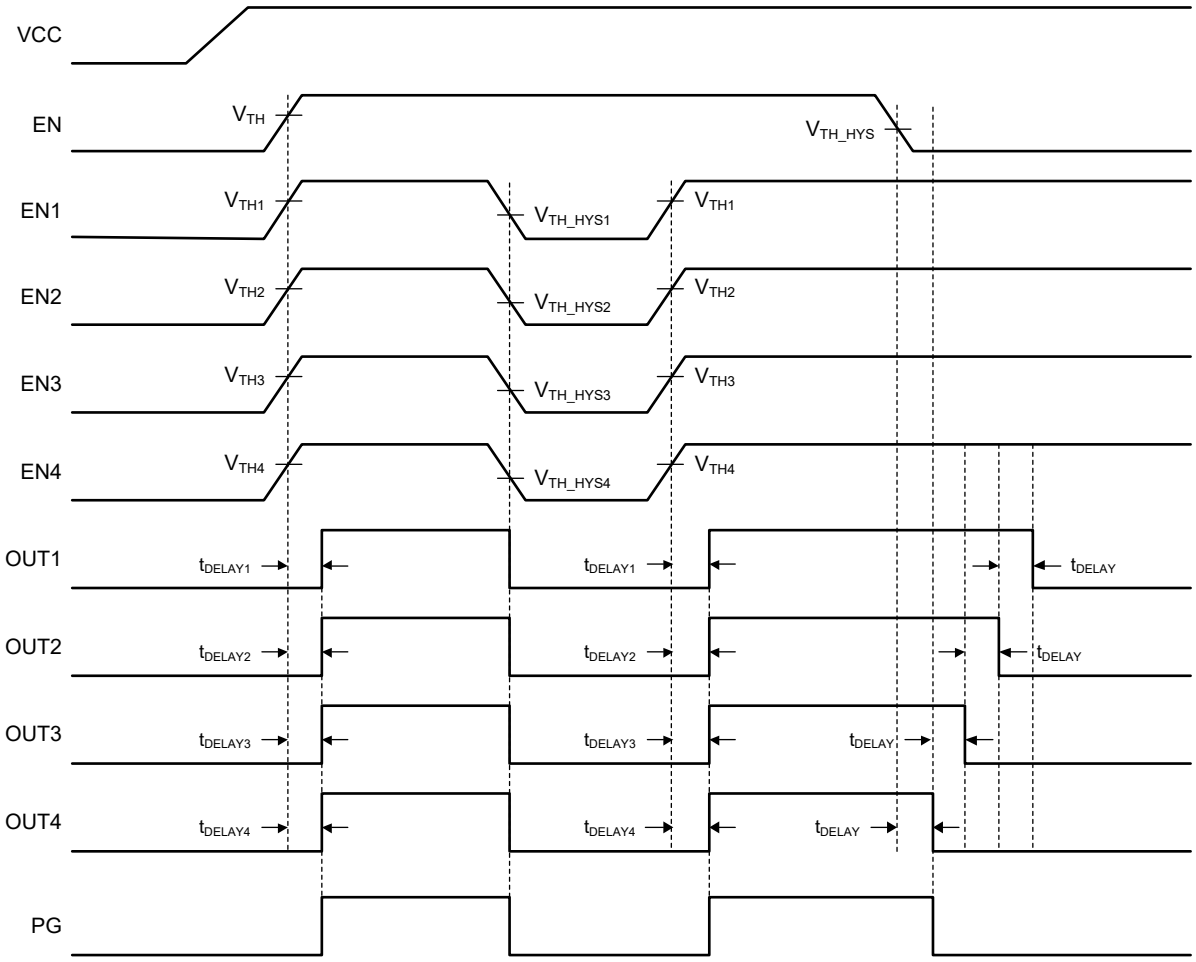
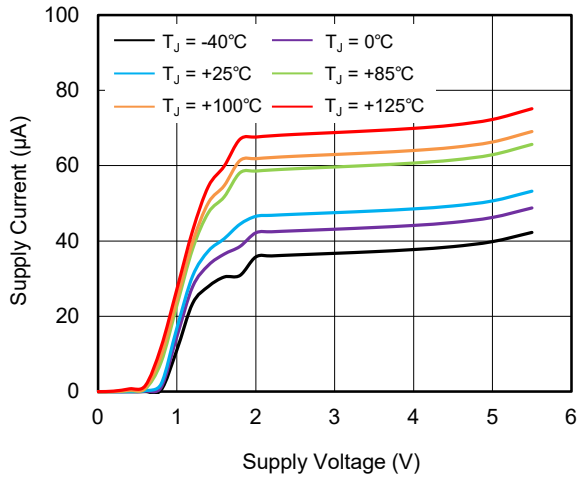


Figure 1. Timing Diagram

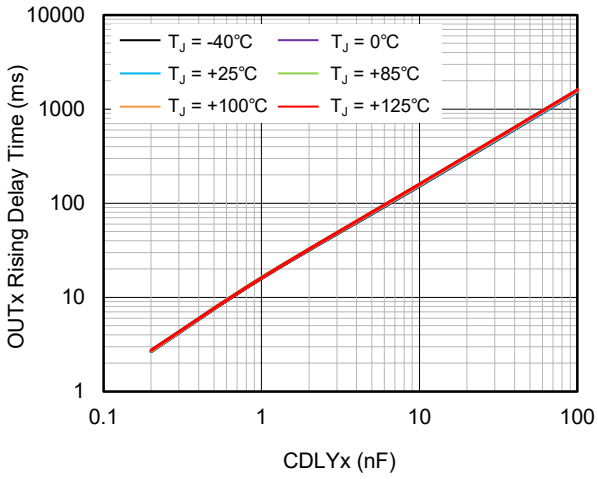
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃ and V_{CC} = 5V, unless otherwise noted.

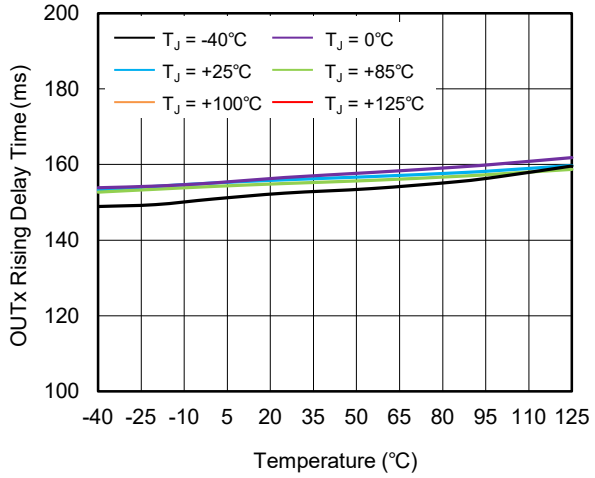
Supply Current vs. Supply Voltage



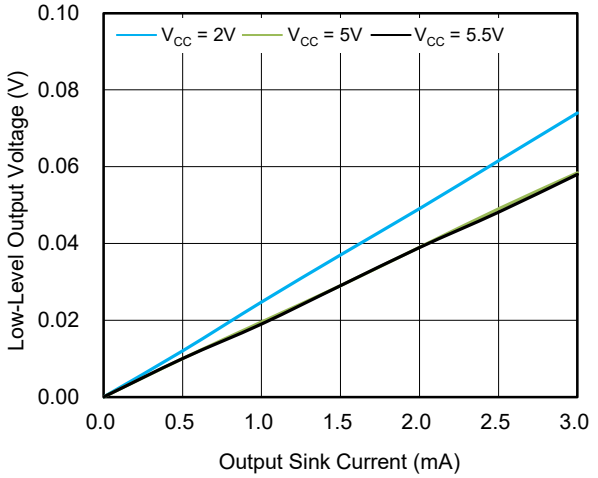
OUTx Rising Delay Time vs. CDLYx



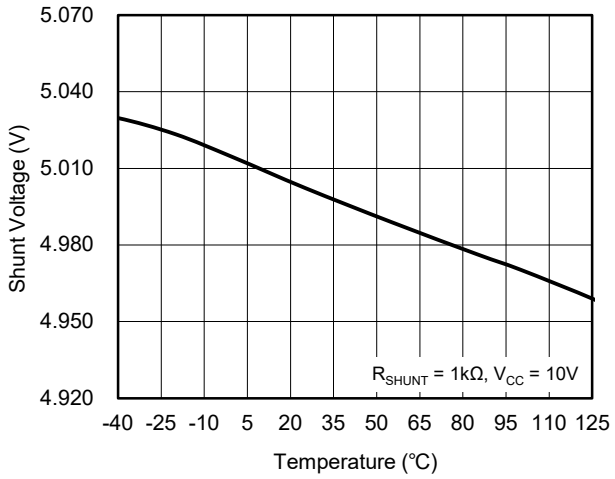
OUTx Rising Delay Time vs. Temperature



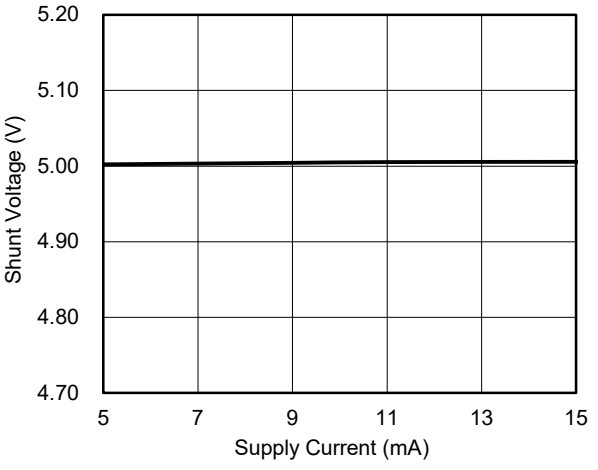
Low-Level Output Voltage vs. Output Sink Current



Shunt Voltage vs. Temperature



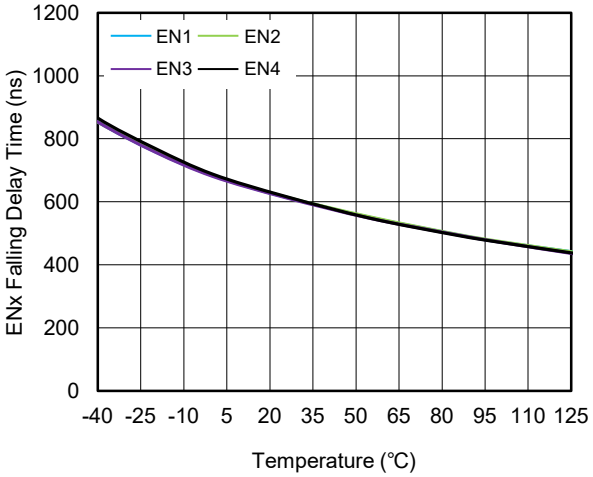
Shunt Voltage vs. Supply Current



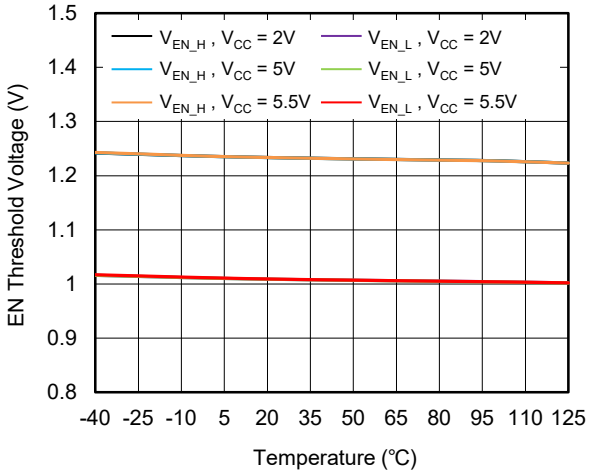
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃ and V_{CC} = 5V, unless otherwise noted.

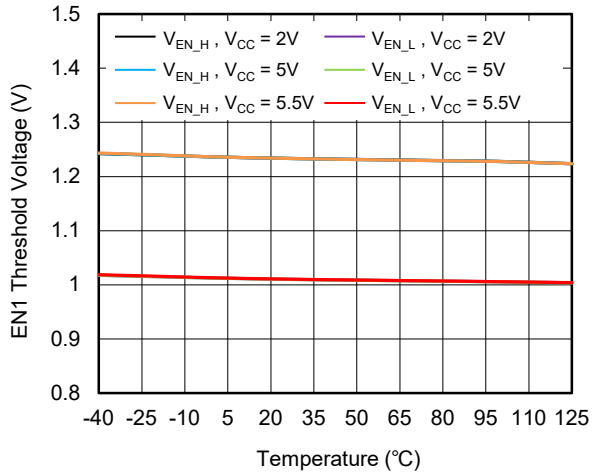
ENx Falling Delay Time vs. Temperature



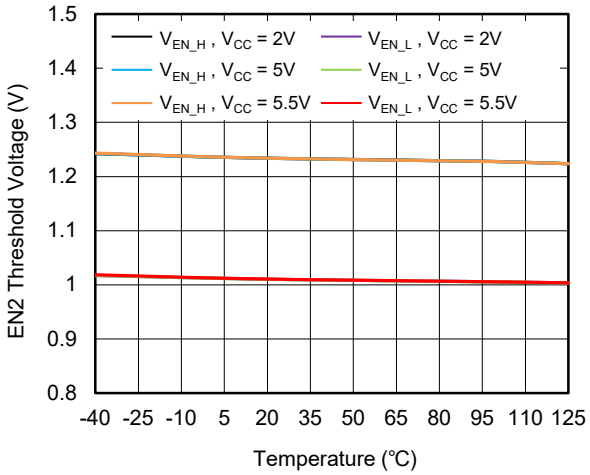
EN Threshold Voltage vs. Temperature



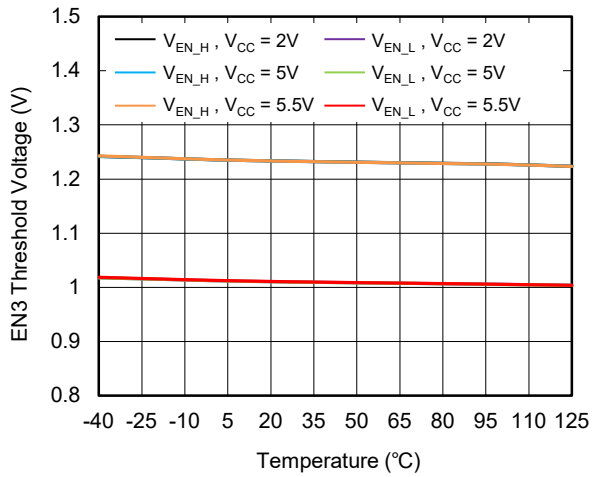
EN1 Threshold Voltage vs. Temperature



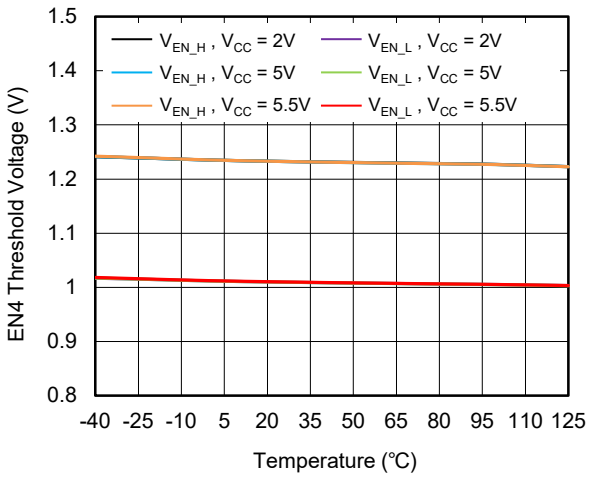
EN2 Threshold Voltage vs. Temperature



EN3 Threshold Voltage vs. Temperature



EN4 Threshold Voltage vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

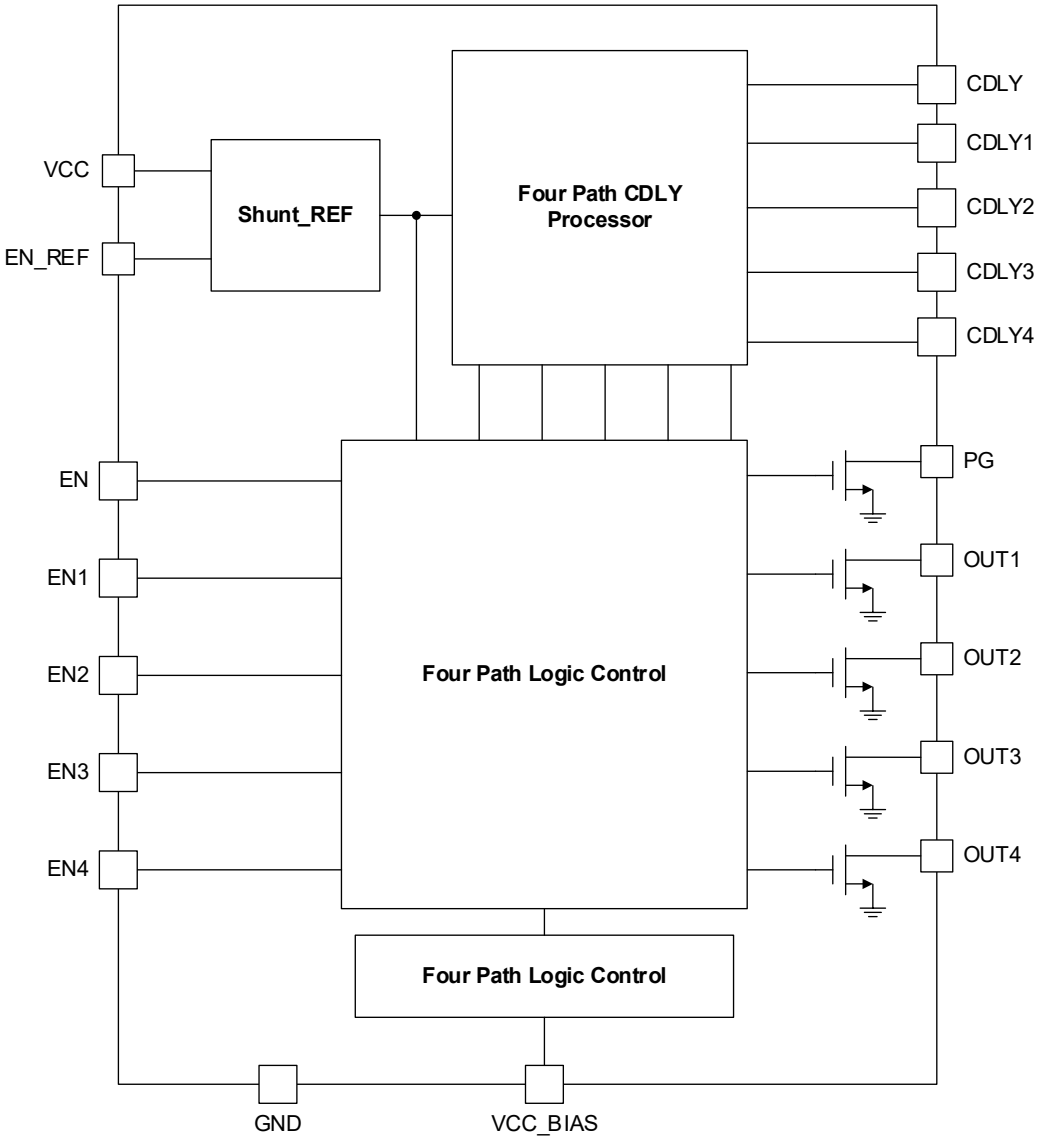


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM864S is an integrated, 4-rail power sequencer. It controls the power-up and power-down sequence of four power supplies by pulling their enable or shutdown pins high or low. Staggered start sequence can avoid the impact of latch conditions or large inrush current on system reliability. The integrated Shunt_REF function can stabilize the VCC at 5V with ±2.6% accuracy, and with different R_{SHUNT} options, the VCC can provide a maximum drive capacity of 15mA for external devices.

Voltage Monitoring

The SGM864S can be used for voltage detection. With an external resistance divider, any voltage threshold above 1.23V can be monitored by each ENx (x = 1, 2, 3, 4) pin. EN is used as an enable signal for the four channels of ENx. ENx can only determine the voltage of each channel when the voltage of EN exceeds 1.23V. And the four ENx channels trigger reset independently of each other. It is also possible to directly monitor the status of the target source through direct access to EN/ENx. The SGM864S supports a wide range of voltage threshold detection and adjustable power-up and power-down delay times, making it suitable for a lot of applications.

Output

In the typical application of the SGM864S, users can connect the OUTx/PG pin to the devices such as DSPS, ASIC, FPGA and CPU as a reset input pin, or connect it to DC/DC converter and LDO regulator as an enable input signal.

The outputs of SGM864S are open-drain structure and pull-up resistors are needed to hold the lines high if OUTx/PG is not asserted. The OUTx/PG can be connected to other devices at correct voltage level by connecting the pull-up resistor to the proper voltage rails. Choose the pull-up resistor larger than 10kΩ for the safe operation of output transistors. Any combination of OUTx/PG can be combined into one logic signal with the wire-OR logic.

Delay Time and Power-Off Delay Time

When the EN pin is pulled high and the ENx pin is high, each of the four outputs (OUT1 to OUT4) is released after a fixed delay time, which can be adjusted by the NP0 capacitor outside the CDLYx pin. Each channel of ENx can be individually programmed with a delay time by the corresponding CDLYx, and the delay time of each channel is expressed by Equation 1.

$$t_{DELAY} = \frac{(C_{DELAY} + \Delta C) \times 0.75 \times 40}{2 \times 10^{-6}} = 1.5 \times (C_{DELAY} + \Delta C) \times 10^{7} \quad (1)$$

where:

1.5 is the time constant.

ΔC is the parasitic capacitance of 4pF (TYP).

Note that the maximum value of C_{DELAY} is 100nF, and its temperature coefficient should be PPM level. The delay accuracy is considered only when t_{DELAY} exceeds 2ms.

Table 1 shows the examples of four delay times programmed by four typical NP0 capacitors.

Table 1. Different Delay Times Programmed by C_{DELAY}

C_{DELAY} (nF)	I_{SOURCE} (μA), TYP	t_{DELAY} (ms)
0.15	2	2.25
0.68	2	10.2
1	2	15
2.2	2	33

When the ENx is high and EN pin is pulled down, the outputs are asserted with a reverse sequence from OUT4 to OUT1 after CDLYx programmable delay time. The EN pin controls the falling sequence of OUTx. The falling delay time is programmed by a capacitor connected to CDLY. The delay time of each channel is also expressed by Equation 1.

Power-Down Sequence Priority

When EN becomes low and ENx remains high, the power-down sequence will execute. During the process of reverse power-down of OUTx, if ENx becomes low, the corresponding OUTx will be asserted immediately, while the OUTx corresponding to the high ENx will still maintain the original power-down delay time (Figure 4).

When EN becomes low and ENx remains high, the power-down sequence will execute. During the process of reverse power-down of OUTx, if the EN returns to high again, the asserted OUTx will be released again with a CDLYx time, and the OUTx that has not yet been asserted will remain in the released state (Figure 5).

DETAILED DESCRIPTION (Continued)

VCC_Bias Function

When the EN_REF pin of the SGM864S is low or floating, the shunt REF function is enabled. When the external supply voltage V_{DD} is powered on quickly, the internal VCC will be set up very slowly due to R_{SHUNT} and C_{IN}, which will result in the OUTx and PG not providing a strong enough pull-down capability for a long time. At this time, an external resistor of 1MΩ to 10MΩ can be connected between VCC_BIAS and the external power supply, which is used for current limiting. The rapid establishment of VCC_BIAS provides a fast pull-down capability for OUTx and PG, thus ensuring the determined output states for the OUTx and PG.

A brief description of the VCC_BIAS function is shown below. Before the internal VCC is built up, VCC_BIAS will be clamped up to a maximum of 1.9V. A current of $(V_{DD}$ - 1.9V)/R_{BIAS} will flow into the diode inside of the SGM864S. After the internal VCC is built up, the internal logic circuit pulls the voltage of the VCC_BIAS down to GND. A current of V_{DD}/R_{BIAS} will flow into the the SGM864S.

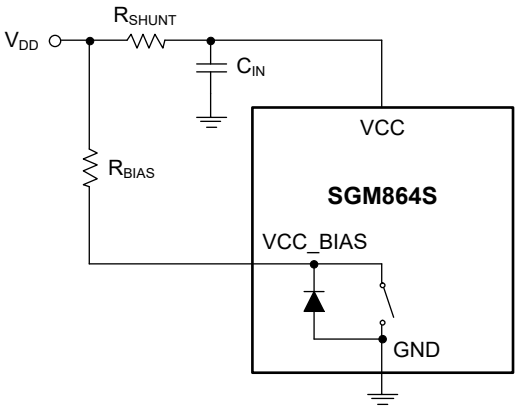


Figure 3. VCC_Bias Function Diagram

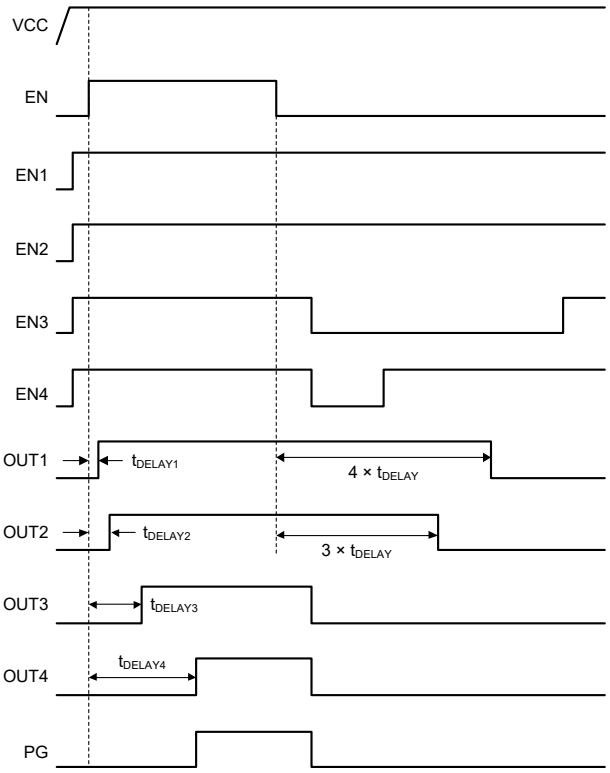


Figure 4. Power-Down Sequence 1

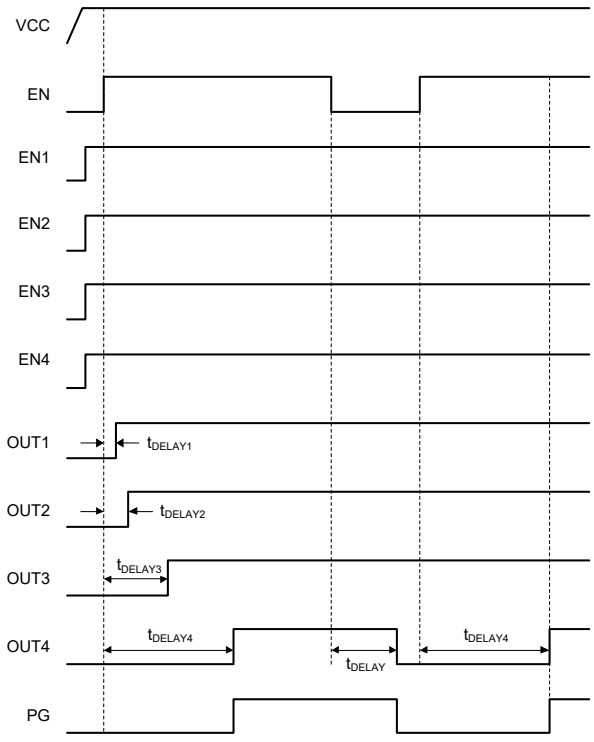


Figure 5. Power-Down Sequence 2

APPLICATION INFORMATION

Typical Application

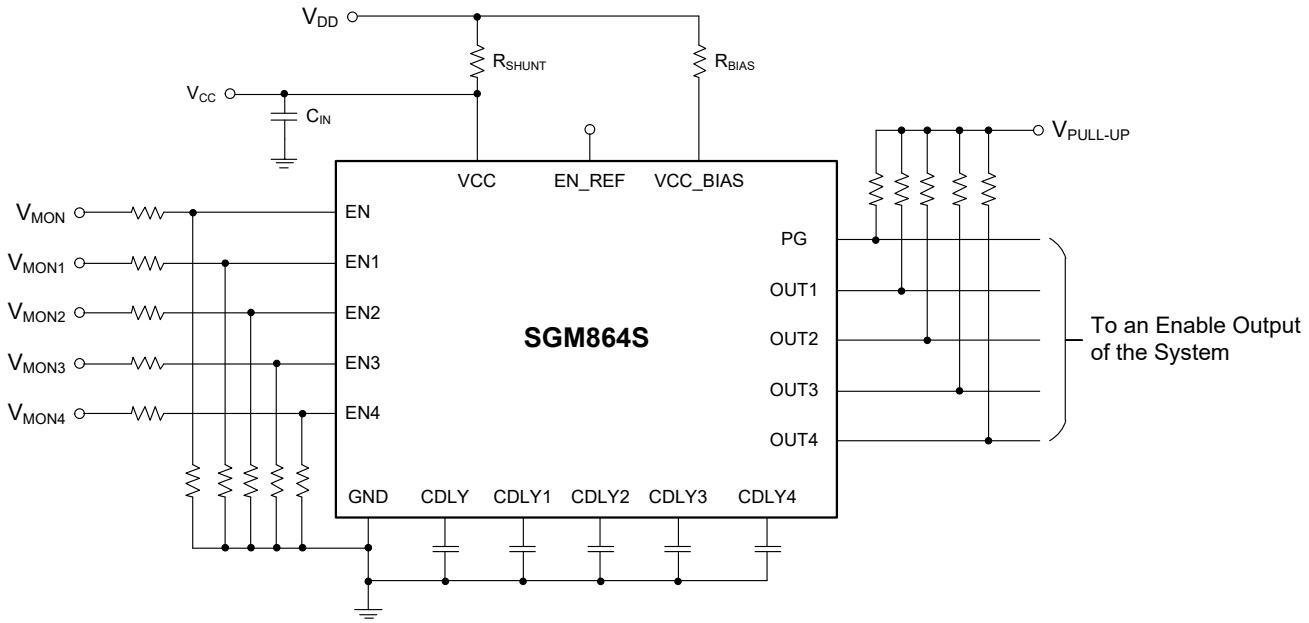


Figure 6. Typical Application Circuit

Application Guidelines

When the Shunt_REF function is enabled and the R_{SHUNT} is greater than 500Ω, the EN and ENx voltages are all above the rising thresholds of EN and ENx (V_{EN_H}, V_{ENx_H}) before SGM864S is powered on and stabilized, it is recommended that the user set the external supply voltage (V_{DD}) above the safe voltage (V_{SOA}) within 1ms, to ensure the normal establishment of the VCC during the power-up process. Otherwise, the power consumption will increase due to premature triggering of the internal CDLY oscillator, which will lower the VCC and trigger UVLO locking during the power-on process, resulting in oscillations near the UVLO during the VCC power-on process. See Table 2 for more details.

When EN_REF is low, and V_{DD} is above 6V, the VCC has the drive capability to provide current externally and stabilizes the internal reference voltage at 5V. Use Equation 2 to caculate the current flowing through the shunt resistor.

$$I_L = \frac{V_{DD} - 5V}{R_{SHUNT}} - I_{CC\_MAX} \quad (2)$$

where:

I_L is the drive current provided by VCC.

I_{CC_MAX} is the maximum current consumption of the IC.

If users want to obtain the maximum drive current (I_{L_MAX}) provided by VCC under different application situations, set R_{SHUNT} = 130Ω, V_{DD} = 7V, or R_{SHUNT} = 800Ω, V_{DD} = 17V, I_L = I_{L_MAX} = 15mA, or R_{SHUNT} = 1kΩ, V_{DD} = 20V.

Table 2. Design Parameters

V_{DD} (V)	Shunt Resistor R_{SHUNT} (kΩ)	EN_REF State	Total Capacitance on VCC, C_{IN} (μF)	V_{SOA}	Recommended Values	Recommended Values at I_{L_MAX} = 15mA
2V to 5.5V	-	High	1μF to 10μF	NA	C_{IN} = 2.2μF	-
4.5V to 7V	130Ω to 5kΩ	Low/Floating	1μF to 10μF	2.8V	R_{SHUNT} = 500Ω, C_{IN} = 2.2μF	R_{SHUNT} = 130Ω, V_{DD} = 7V
7V to 17V	800Ω to 10kΩ	Low/Floating	1μF to 10μF	3.8V	R_{SHUNT} = 1.5kΩ, C_{IN} = 2.2μF	R_{SHUNT} = 800Ω, V_{DD} = 17V
17V to 22V	1kΩ to 40kΩ	Low/Floating	1μF to 10μF	8.8V	R_{SHUNT} = 5kΩ, C_{IN} = 2.2μF	R_{SHUNT} = 1kΩ, V_{DD} = 20V

APPLICATION INFORMATION (Continued)

Cascade Application

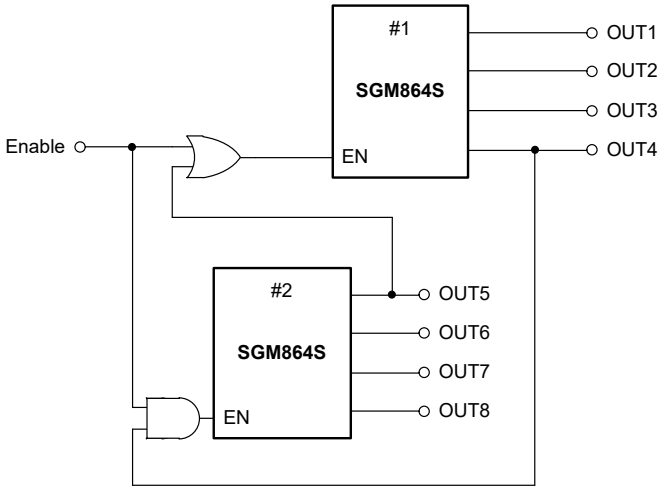


Figure 7. SGM864S Cascade Circuit

Layout Guidelines

Some guidelines are given below to prepare the layout of the PCB for SGM864S.

1) CDLY/CDLYx pins routing should be as short as possible to improve accuracy and require shielding treatment.
2) Take short traces from EN/ENx to the resistor divider and long traces from R_{SxH} to V_{MONx}.
3) Connect the VCC capacitor as close as possible to the device.
4) Use short traces to connect VCC. The parasitic inductance from the supply to the capacitor and the capacitor at VCC form an LC tank and may lead to ring voltages that higher than the maximum allowed VCC voltage.

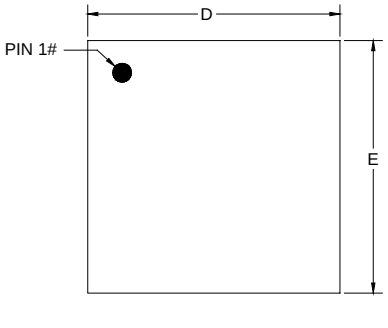
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

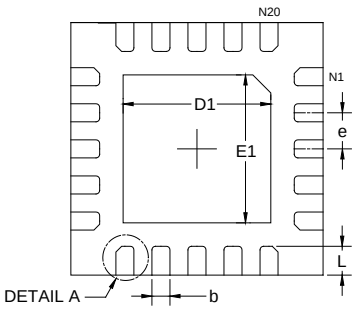
Changes from Original (APRIL 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

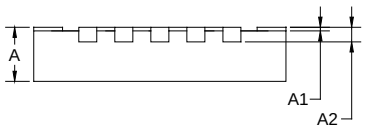
TQFN-3.5×3.5-20L



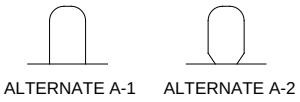
TOP VIEW



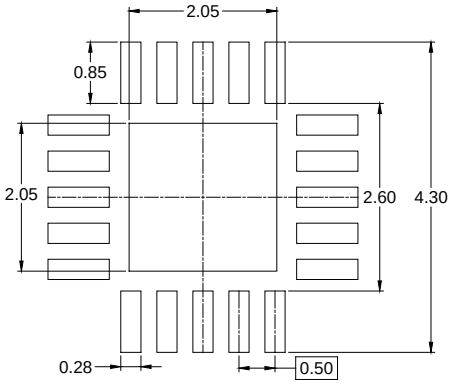
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



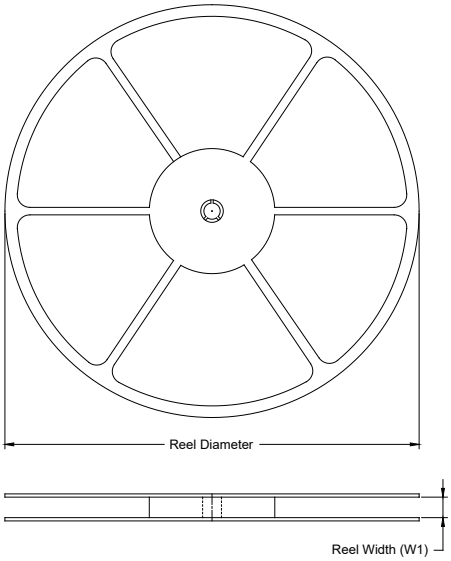
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	3.450	3.500	3.550
D1	2.000	2.050	2.100
E	3.450	3.500	3.550
E1	2.000	2.050	2.100
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450

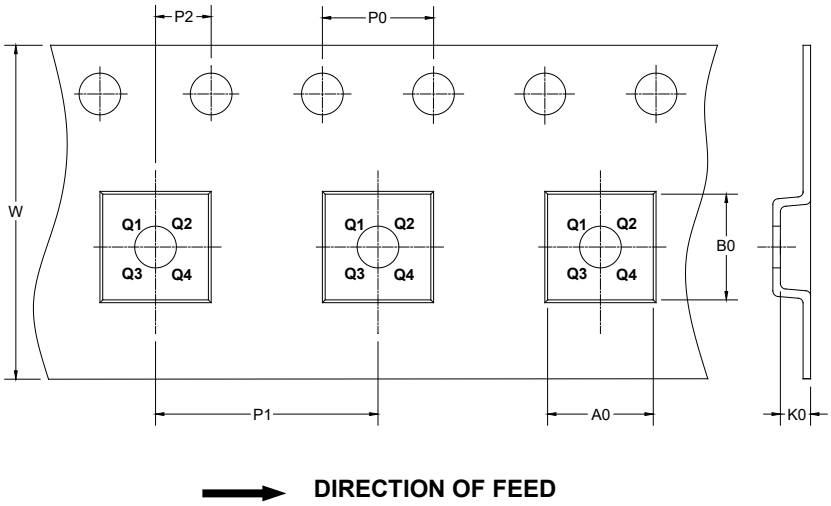
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



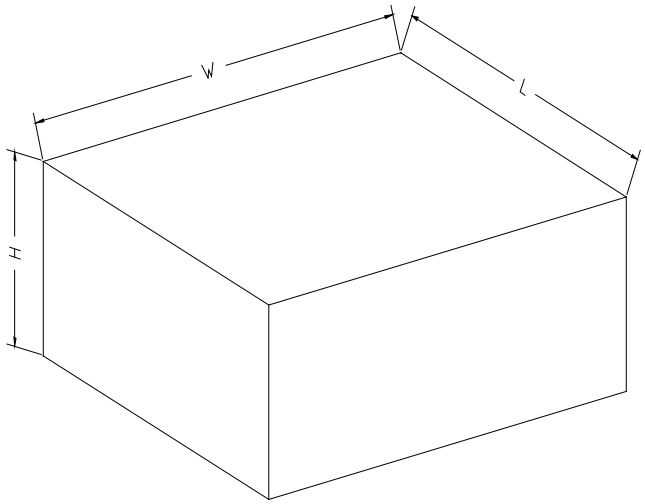
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-20L	13"	12.4	3.80	3.80	0.95	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002