SGN5210
2.4 GHz RF Transceiver

Production Data Sheet

Product Description:

The Signia SGN5210 IC is a low-cost, fully integrated CMOS radio frequency (RF) transceiver, optimized for applications in the globally available 2.4~2.5 GHz ISM band. It contains transmit, receive, VCO and PLL functions, including VCO resonator, thus minimizing the need for external components.

The synthesizer is designed for fast hopping and ease of use, requiring only an external RC loop filter. The on-chip reference divider accepts integer reference frequencies between 4~25 MHz, for 1 MHz channel spacing.

The transmit section features digitally adjustable output power, ranging from approx. +2 to -32 dBm. Nominal mark and space deviation is ±167 kHz. IQ modulation yields transmit data rates from DC up to 333 kbps (1 Mbps max.). Low in-band spurious signals, and internal Gaussian filtering of the transmit data, ease regulatory compliance.

The superhetrodyne receiver is comprised of LNA, active image-reject down-converter, and "low-IF" amplifier/limiter chain. IF bandwidth is typically 1.2 MHz. FM demodulation is completely internal, utilizing digital delay-line discriminator architecture. The receiver may be used in applications requiring data rates from DC to 333 kbps (1 Mbps max.). Symbol rate can be 3 or more µS, and is optimized for an integer number of µS per symbol.

The SGN5210 also features a fully digital baseband interface, greatly simplifying the interface to commonly used microprocessors and ASICs.

Internal DC block on the antenna pin means only a low-cost bandpass filter is needed between the antenna and the IC.

For longer battery life, power consumption is minimized by providing separate power controls for transmit, receive, PLL, VCO, and PA sections, as well as a sleep state to reduce standby battery usage.

This product is available in 48-lead 7x7 mm JEDEC standard QFN package, featuring an exposed pad on the bottom for best RF characteristics.

Ordering Information

SGN5210	2.4 GHz RF Transceiver IC

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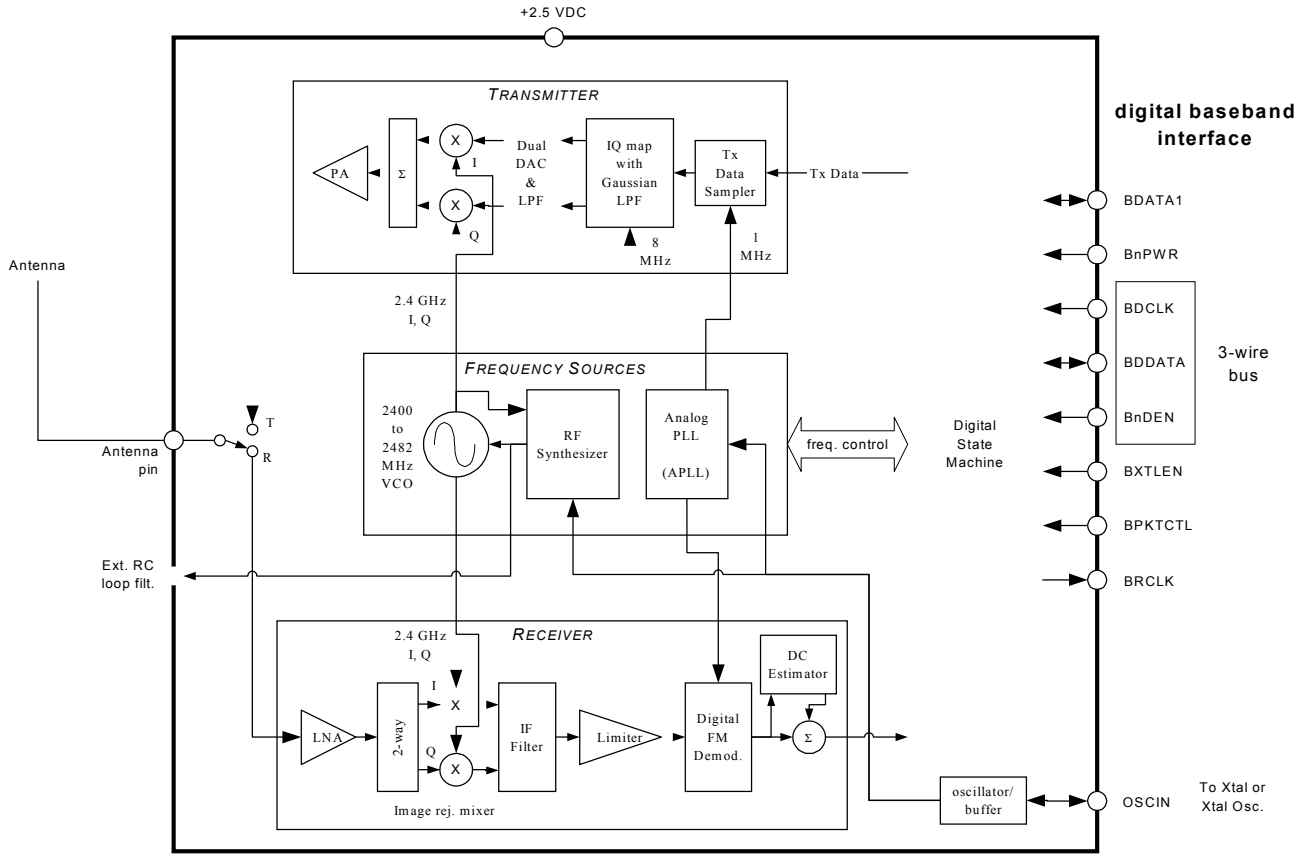
Key Features:

- Complete fully Integrated radio transceiver in lowest-cost silicon CMOS
- Low power consumption:
  - Tx 40mA
  - Rx 50mA
- Max. Transmit power: 1.6 mW (+2 dBm)
- Fast Hopping: up to 1600 hops per second
- Direct IQ up-conversion for stable PLL and modulation index
- Clean Transmit output needs minimum filtering
- Nominal Receiver sensitivity: -80 dBm
- Low-IF approach to minimize DC offset
- LO Leakage very low, << -60 dBm
- Built-in AutoTune circuitry for the internal receive IF filters
- No external RF balun or T/R switch required
- Fully digital baseband interface
- Flexible power management for minimizing current consumption
- 7x7mm QFN package with minimum RF parasitics
- A component of Signia's 2.4 GHz RFIC Transceiver family

Applications:

- Wireless Game controllers
- Wireless keyboard, mice
- Wireless headsets, audio
- Remote controls
- Home automation
- Industrial controls

Block Diagram



Ratings

Absolute Maximum Ratings					
Parameter	**Symbol**	**Rating**			**Unit**
		MIN	**TYP**	**MAX**	
Operating Temperature	T_{OP}	0		+60	°C
Storage Temperature	$T_{STORAGE}$	-55		+125	°C
Supply Voltage	V_{SUPPLY}			+3.0	Vdd
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.0	Vdd
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z_0=50Ω)	$VSWR_{OUT}$			10:1	VSWR

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.
2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover work benches with grounded conductive mats.

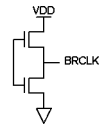
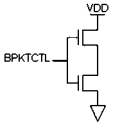
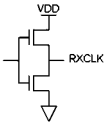
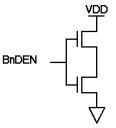
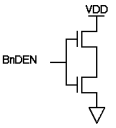
Electrical Characteristics

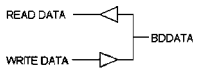
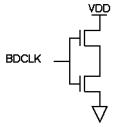
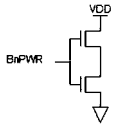
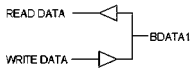
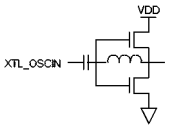
The following specifications are guaranteed for T_A = 25 °C, V_{DD} = 2.50 ± 0.25 VDC, unless otherwise noted:

Parameter	Symbol	Specification			Units	Test Condition and Notes
		MIN	TYP	MAX		
Current Consumption						
Current Consumption - TX	I_{DD_TX}		40		mA	P_{OUT} = nominal output power
Current Consumption - RX	I_{DD_RX}		50		mA	
Current Consumption - IDLE	I_{DD_SB}		3		mA	RF Synthesizer and VCO: OFF (see Reg. 21)
	I_{DD_SYNTH}		20		mA	RF Synthesizer and VCO: ON (see Reg. 21)
Current Consumption - SLEEP	I_{DD_SLP}		3		mA	Clock (pin 43) still applied
Current Consumption – STATE 0 (BnPWR=0)	I_{DD_ST0}		35		uA	Clock (pin 43) removed
	I_{DD_ST0n}		100		uA	Clock (pin 43) still applied
Digital Inputs						
Logic input high	V_{IH}	0.8 V_{DD}		V_{DD}	V	
Logic input low	V_{IL}	0		0.8	V	
Input Capacitance	C_{IN}			10	pF	
Input Leakage Current	I_{LEAK_IN}			10	uA	
Digital Outputs						
Logic output high	V_{OH}	.8 V_{DD}		V_{DD}	V	
Logic output low	V_{OL}	0		.8	V	
Output Capacitance	C_{OUT}			10	pF	
Output Leakage Current	I_{LEAK_OUT}			10	uA	
Rise/Fall Time	T_{RISE_OUT}		5		nS	
Clock Signals						
BRCLK output frequency	BRCLK		1 or 12		MHz	Depends on Register 9, bit 1 setting: Always either 1 MHz during Tx, or 12 MHz always.
BRCLK tolerance	T_BRCLK		--		ppm	Same as OSCIN frequency tolerance
BDCLK rise, fall time				10	nS	Required for error-free register reading, writing.
BDCLK frequency range	BDCLK	0		20	MHz	The serial (3-wire bus) clock freq. range.
Overall Transceiver						
Operating Frequency Range	F_{OP}	2400		2482	MHz	
Rx Input mismatch	$VSWR\_{I}$		<2:1		VSWR	Z_0=50Ω
Tx Output mismatch	$VSWR\_{O}$		<2:1		VSWR	Z_0=50Ω

Parameter	Symbol	Specification			Units	Test Condition and Notes
		MIN	TYP	MAX		
Receive Section						**Rx out on BDATA1 pin, using baseband clock recovery. For BER ≤ 0.1%:**
Receiver sensitivity			-80	-72	dBm	Meas. at antenna pin of IC
Maximum useable signal		-20			dBm	
Input 3rd order intercept point	IIP_3	-14	-11		dBm	
Data (Symbol) rate	Ts	3			µS	Must be integer number of microseconds. For BER ≤ 0.1%
Minimum Carrier to Interference ratio						
Co-Channel Interference	$CI_{cochannel}$	11			dB	-60 dBm desired signal.
Adjacent Ch. Interference, 1MHz offset	CI_{-1}		0		dB	-60 dBm desired signal.
Adjacent Ch. Interference, 2MHz offset	CI_{-2}		-30		dB	-60 dBm desired signal.
Adjacent Ch. Interference, ≥ 3MHz offset	CI_{-3}		-40		dB	-67 dBm desired signal.
Image Frequency Interference	CI_{Image}		-9		dB	-67 dBm desired signal. Image freq. is always 6 MHz higher than desired signal.
Adjacent (1MHz) interference to image	CI_{Image_11}		-20		dB	-67 dBm desired signal. Always 5, 6, or 7 MHz higher than desired signal.
Out-of-Band Blocking						Meas. with ACX ceramic filter on ant. pin:
30 MHz to 2000 MHz	OBB_{-1}	-10			dBm	
2000 MHz to 2400 MHz	OBB_{-2}	-27			dBm	
2500 MHz to 3000 MHz	OBB_{-3}	-27			dBm	
3000 MHz to 12.75 GHz	OBB_{-4}	-10			dBm	
Transmit Section						**Register 9 bits 9-7 set to 000 (Power level 0)**
RF Output Power	Pout		+2		dBm	Power Level 0. Meas. at antenna pin of IC.
Modulation Characteristics						
Frequency Deviation	F_{DEV}	115	166	175	kHz	Peak FM deviation
In-Band Spurious Emission						Integrated over a 1MHz channel.
2 MHz offset	IBS_{-2}			-20	dBm	
>3 MHz offset	IBS_{-3}			-40	dBm	
Out-of-Band Spurious Emission, Operation						
30MHz – 1GHz	OBS_{O_1}		< -60	-36	dBm	
1GHz – 12.75GHz	OBS_{O_2}		-45	-30	dBm	Excludes desired signal.
1.8GHz – 1.9GHz	OBS_{O_3}		< -60	-47	dBm	
5.15GHz – 5.3GHz	OBS_{O_3}		< -65	-47	dBm	
RF VCO and PLL Section						
Typical RF PLL Lock range	F_{VCO}	2330		2550	MHz	
Frequency Tolerance			--		ppm	Same as OSCIN frequency tolerance
Channel (Step) Size			1		MHz	
SSB Phase Noise			-95		dBc/Hz	550 kHz offset
			-115		dBc/Hz	2 MHz offset
OSCIN Reference Frequency		6	13	30	MHz	Pin 43. Must be integer multiple of 1 MHz.
OSCIN Voltage required						Min. voltage level needed for fully functional PLL's, AC or DC coupled into Pin 43:
6 to 11 MHz Sine wave		2.5			V_{p-p}	
Sq. wave		1.25			V_{p-p}	
11 to 15 MHz Sine wave		2.0			V_{p-p}	
Sq. wave		1.4			V_{p-p}	
15 to 20 MHz Sine or Sq. wave		1.4			V_{p-p}	
20 to 30 MHz Sine or Sq. wave		1.25			V_{p-p}	
RF PLL Settling Time	T_{HOP}		90	200	µS	80 MHz frequency change, settle to within 40 kHz.
Out-of-Band Spurious Emission						IDLE state. Synthesizer and VCO ON.
30MHz – 1GHz	OBS_{-1}		< -75	-57	dBm	
1GHz – 12.75GHz	OBS_{-2}		-68	-47	dBm	

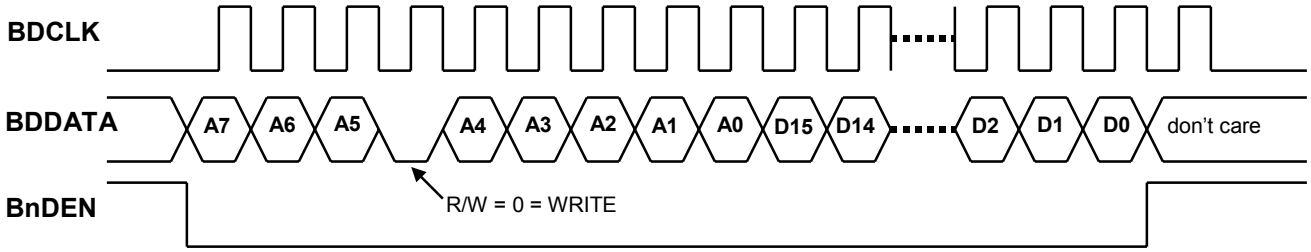
Pin Description

Pin No.	Pin Name	Type	Description	Interface
1	PA_EN	O	DO NOT CONNECT.	
2	VDD	PWR	Power supply voltage.	
3	GND	GND	Ground connection.	
4	VDD	PWR	Power supply voltage.	
5, 6, 7	GND	GND	Ground connections.	
8	TX/RX	50Ω RF	RF Input/output pin, to antenna.	
9	GND	GND	Ground connection.	
10, 11	VDD	PWR	Power supply voltage.	
12	GND	GND	Ground connection.	
13, 14	VDD	PWR	Power supply voltage.	
15	GND	GND	Ground Connection.	
16	VDD	PWR	Power supply voltage.	
17	GND	GND	Ground Connection.	
18 ~ 21	TEST	--	DO NOT CONNECT. Reserved for factory test.	
22, 23	GND	GND	Ground Connections	
24	BRCLK	O	Outputs either 1MHz Tx symbol clock, or 12 MHz APLL output.	
25	BPKTCTL	I	In transmit state this pin turns on PA_ON by receiving a high signal from the baseband. In receive state, this pin controls the DC estimation behavior in two different states: a low state is used to set the DC estimation for fast acquisition and a high state is used for slower or fixed DC estimation.	
26	(Reserved)	-	DO NOT CONNECT.	
27	RXCLK	O	Receiver symbol clock recovery output. Fixed at 1 MHz fundamental rate. Useful for over-sampling the BDATA1 Rx data output.	
28	TEST-SE	--	DO NOT CONNECT. Reserved for factory test.	
29	BXTLEN	I	This sets the chip into SLEEP state by supplying a low signal.	
30	TEST3	--	Reserved for factory test.	
31	BnDEN	I	Enable line for the 3-wire bus. Active low.	

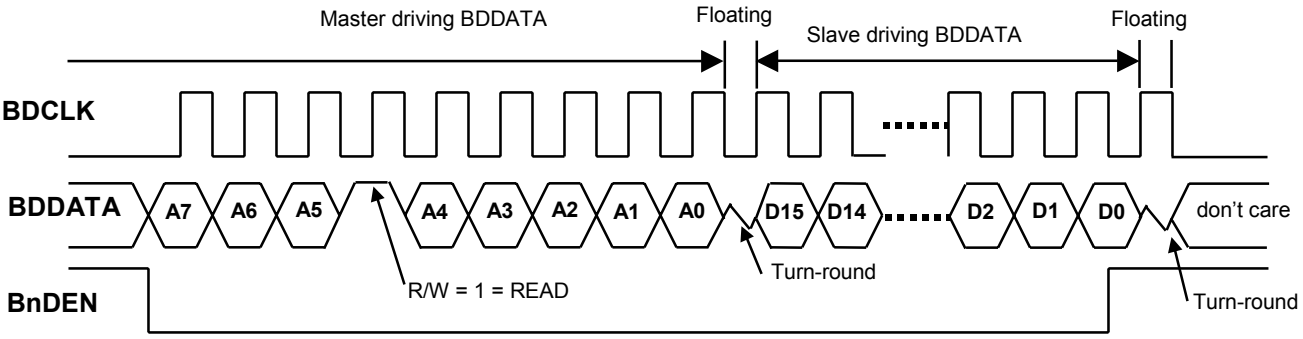
Pin No.	Pin Name	Type	Description	Interface
32	TEST4	--	DO NOT CONNECT. Reserved for factory test.	
33	BDDATA	I/O	Data line for the 3-wire bus.	
34	TEST5	--	DO NOT CONNECT. Reserved for factory test.	
35	BDCLK	I	Clock line for the 3-wire bus.	
36	BnPWR	I	When BnPWR is low, the RF chip will be in state 0, and power consumption is very low. When raised high, BnPWR is used to turn on the RF chip, restoring all registers to their default value.	
37	BDATA1	I/O	In transmit mode, this pin receives transmit data from the baseband. It will be sampled at 1 Mbps. Sample clock is derived from the pin 43 OSC_IN signal. Sampling begins with the Tx Data Sync pulse. In receive mode, this pin sends receive data to the baseband at up to 1 Mbps rate. This pin is also used to initialize the chip into IDLE.	
38	VDD	PWR	Power supply voltage.	
39	GND	GND	Ground connection.	
40	VDD	PWR	Power supply voltage.	
41, 42	TEST6, 7	--	DO NOT CONNECT. Reserved for factory test.	
43	XTL_OSCIN	A I	Crystal oscillator input, from a reference oscillator. Can be sine or square wave. If square wave, some rounding of the edges is preferable, to reduce transmit spurious products that are offset from the carrier by this frequency.	
44	VDD	PWR	Power supply voltage.	
45	GND	GND	Ground connection.	
46	PLL_LPF	A I/O	PLL loop filter.	
47	GND	GND	Ground connection.	
48	VDD	PWR	Power supply voltage.	
Exposed pad	GND	GND	Ground connection.	

Serial Register Interface

For additional information, please refer to Application Note AN5000.



3-wire bus
Write cycle



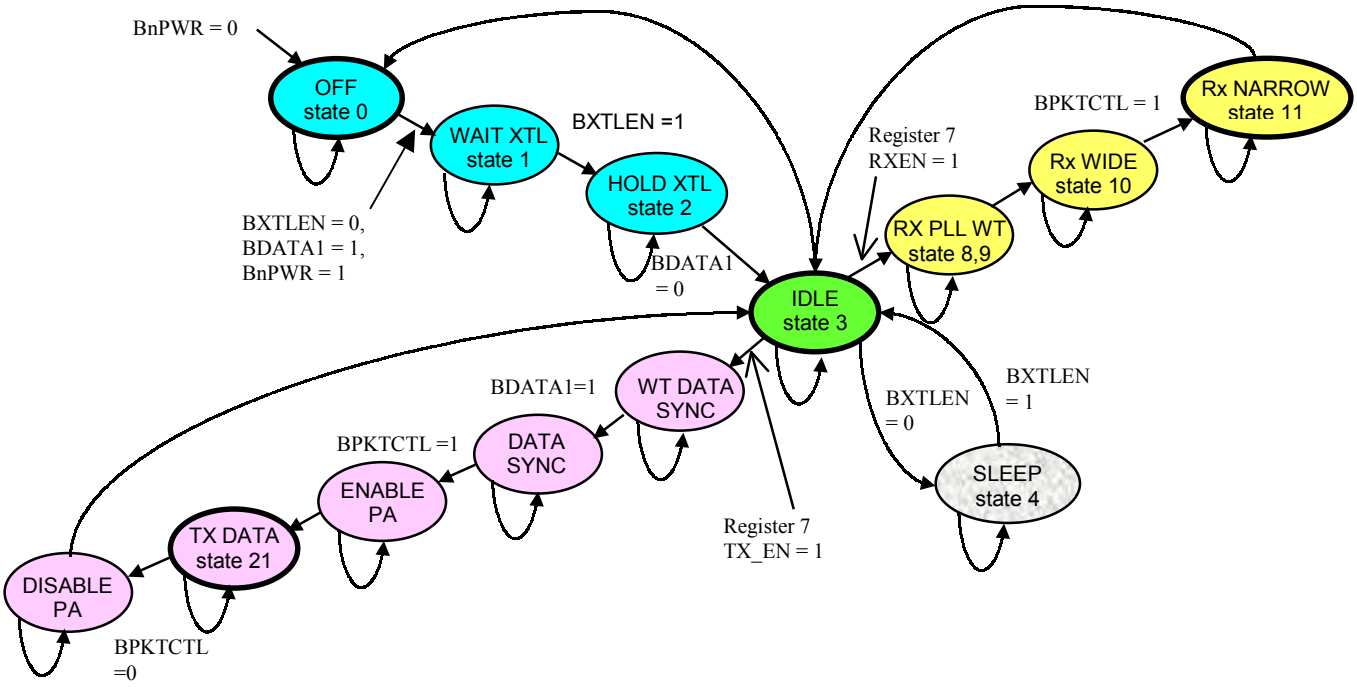
3-wire bus
Read cycle

No. Of Bits	Field	Comments
3 (A7:A5)	Device Address	Always 101
1	Read/Write	"0" Write, "1" Read.
5 (A4:A0)	Register Address	Up to 32 registers
16 (D15:D0)	Data Field	The IC is configured in "WRITE" mode, and outputs it's register contents in "READ" mode.

3-wire bus
Protocol

State Diagram

For additional information, please refer to Application Note AN5000.



Detailed Register Information

DC Estimator Control (Write/Read) – Register 0 (Default =0x1000)

Bit No.	Bit Name	Description
15 - 14	(reserved)	(reserved)
13 - 12	BPKTCTL_TC_DC [1:0]	Set time constant for DC estimation circuit, *after* BPKTCTL is asserted. Please note 00 setting is to select fixed DC offset value that was calculated before BPKTCTL was asserted. See register 18 also.
11 – 10	TC_DC [1:0]	Set time constant for DC estimation circuit, *before* BPKTCTL is asserted.
9 – 0	(reserved)	(reserved)

BPKTCTL_TC_DC [1:0]	Symbols
00	Fixed DC offset value (requires register 18 setting)
01	16
10	32
11	64

TC_DC [1:0]	Symbols
00	4
01	6
10	8
11	16

Rx and Synthesizer Status (Read only) – Register 1

Bit No.	Bit Name	Description
15 – 13	(reserved)	(reserved)
12 - 11	RD_LNA_GAIN	2-bit LNA Gain Control @ 10 dB/step. The Baseband can read back the LNA gain controlled by local PGA circuit.
10	RF_SYNTH_LOCK	RF_SYNTH_LOCK is the original output signal from the synthesizer to indicate the PLL lock status.
9 - 0	RD_DC_ADJ [9:0]	10-bit 2's compliment DC offset adjustment. The Baseband can read back the DC offset adjustment value estimated by local DC estimation circuit.

Rx Configure (Write/Read) – Register 2 (Default = 0x0406)

Bit No.	Bit Name	Description
15 - 10	(reserved)	(reserved)
9	PGA_PARA_OW	When 1 indicates the BBIC overwrites the PGA adjustment value
8 - 1	(reserved)	(reserved)
0	DC_PARA_OW	When 1 indicates the BBIC overwrites the DC adjustment value. Set DC_PARA_OW = 0 to allow the chip to track out frequency drift on the receive input signal.

RFIC State (Read only) – Register 3

Bit No.	Bit Name	Description
15 - 11	RF_STATE[4:0]	Read the status of finite state machine.
10 - 8	RD_PGA [2:0]	3-bit PGA control for 50 dB VGA (-10/+40 dB) dynamic range. The Baseband can read back the PGA setting, which is controlled by local PGA circuit.
7 - 0	RSSI_LTERM [7:0]	8-bit RSSI value with time constant set by baseband. The value can be read by BB for long term averaging to control transmit power

RF_STATE		STATE
Binary [4:0]	Decimal	
00000	0	Off
00001	1	PwrOnWaitXTL
00010	2	HoldXTL
00011	3	Idle
00100	4	Sleep
00101	5	SleepWaitXTL
01000	8	RXPLLWait1
01001	9	RXPLLWait2
01010	10	RXWideFilt
01011	11	RXNarrowFilt
10000	16	WaitDataSync1
10001	17	WaitDataSync2
10010	18	DataSync
10011	19	EnblePA1
10100	20	EnblePA2
10101	21	TXData
10110	22	DisablePA1
10111	23	DisablePA2
11000	24	DisablePA3

Receiver Control (Write/Read) – Register 4 (Default = 0x0030)

Bit No.	Bit Name	Description
15 - 5	(reserved)	(reserved)
4 - 3	WT_LNA_GAIN[1:0]	2-bit LNA Gain Control @ 10 dB/step. Active only when PGA_PARA_OW in register 2 is set. In normal operation, receive gains are controlled by local PGA circuit.
2 - 0	WT_PGA [2:0]	3-bit PGA control for 50 dB VGA (-10/+40 dB) dynamic range @ 2 dB/step. Active only when PGA_PARA_OW in register 2 is set. In normal operation, receive gain are controlled by local PGA circuit.

WT_LNA_GAIN [1:0]	LNA Gain (dB)
00	16
01	6
10	-4
11	Not Defined

WT_PGA [2:0]	PGA Gain (dB)
000	0
001	2
010	4
011	6
100	8
101	10
110	12
111	14

RFIC Control (Write/Read) – Register 5 (Default = 0x4D0C)

Bit No.	Bit Name	Description
15 - 11	SYNTH_ON_DELAY_CNT[4:0]	In the state WAIT DATA SYNC, RF oscillator will be enabled at first. There is time offset controlled by the counter SYNTH_ON_DELAY_CNT. When the counter counts to zero and SYNTH_IDLE_OFF = 0, the synthesizer will be enabled. Each time increment is 1 µS.
10 - 9	(reserved)	(reserved)
8	REG_PROTECT	The bit is used to protect registers from accidental change. If REG_PROTECT = 1 (default), only registers 7, 8, 9, and this REG_PROTECT bit, may be modified. If REG_PROTECT = 0, all the registers can be modified.
7 - 0	RX_DELAY [7:0]	8-bit Receive delays from receiving synthesizer program register to start transmit BDATA1 to BBIC. Each time increment is 1 µS.

DC Estimator (Read only) – Register 6

Bit No.	Bit Name	Description
15 - 0	DC_LONGTERM [15:0]	16-bits 2's compliment DC offset long-term averaged value. The Baseband can read back the DC offset long-term averaged value estimated by local DC estimator circuit.

RF Synthesizer, Tx/Rx Control (Write/Read) – Register 7 (Default = 0x0030)

Bit No.	Bit Name	Description
15 - 14	Reserved	
13 - 9	SWALLOW [4:0]	5-Bits Synthesizer Swallow counter. The synthesizer will be programmed directly with Register 7 [13:9] and Register 7 [6:0]. Valid only when the RF_PLL_DIRECT (register 21) is set to 1.
8	TX_EN	Enable the Transmit Sequence for state machine control. Note that TX_EN and RX_EN cannot be HIGH at the same time.
7	RX_EN	Enable the Receive Sequence for state machine control. Note that TX_EN and RX_EN cannot be HIGH at the same time.
6 - 0	RF_PLL[6:0]	When the RF_PLL_DIRECT (register 21) is set to 1, the synthesizer will be programmed directly, using both Register 7 [13-9] and Register 7 [6:0]. Register 7 [6:0] are used as 7-bit synthesizer program counter.
	RF_PLL_CH_NO [6:0]	When the RF_PLL_DIRECT (register 21) is set to 0, these 7 bits are the RF channel number. Transmit and receive carrier frequency will be : f = 2402+ PLL_CH_NO. In this case, SWALLOW bits will be ignored.

APLL Control (Write/Read) – Register 8 (Default = 0x1676)

Bit No.	Bit Name	Description
15 - 14	(reserved)	(reserved)
13 - 9	APLL_ID [4:0]	5-bit APLL input divider counter. Input divider = APLL_ID + 2
8 - 0	(reserved)	(reserved)

RFIC Control (Write/Read) – Register 9 (Default = 0x6803)

Bit No.	Bit Name	Description
15 – 11	SYNTH_ID [4:0]	RF Synthesizer input reference clock divider, ranging from 1 to 31 (0 is not valid)
10	(reserved)	(reserved)
9 - 7	PA_CTRL [2:0]	Transmit power level
6 - 3	(reserved)	(reserved)
2	APLL_PD	Analog PLL power-down mode. When 1, APLL is off.
1	BRCLK_SEL	Selects BRCLK pin output signal: If BRCLK_SEL = 1 (default), BRCLK always outputs the 12MHz APLL output. If BRCLK_SEL = 0, BRCLK outputs TXCLK (1 MHz).
0	(reserved)	(reserved)

PA_CTRL (Power level)		Typical Power Amplifier Output Level, dBm
Binary [2:0]	Decimal	
000	0	+2
001	1	-4
010	2	-10
011	3	-13
100	4	-18
101	5	-23
11x	6 or 7	-32

Reserved (Write/Read) – Register 10 (Default = 0x0004)

Bit No.	Bit Name	Description
15 - 0	(reserved)	(reserved)

On-chip Oscillator (Write/Read) – Register 11 (Default = 0x4040)

Bit No.	Bit Name	Description
15 - 1	(reserved)	(reserved)
0	XTAL_OSC_EN	When 1 is set, enable the internal negative resistance oscillator circuit.

On-chip Oscillator (Write/Read) – Register 12 (Default = 0x9000)

Bit No.	Bit Name	Description
15 - 13	XTAL_EX_TUNE[2:0]	Fine tune ppm for external Xtal.(default = 100)
12 - 11	(reserved)	(reserved)
10 - 8	XTAL_LOAD[2:0]	When > 0, set the on-chip xtal load.
7	XTAL_BIAS_EN	When 1 is set, switches on the bias point.
6:0	(reserved)	(reserved)

Reserved (Write/Read) – Register 13 (Default = 0x0000)

Bit No.	Bit Name	Description
15 - 0	(reserved)	(reserved)

Tx Timing (Write/Read) – Register 14 (Default = 0x0200)

Bit No.	Bit Name	Description
15 - 8	TX_MOD_OFF_DELAY	These registers are the initial value for the counter of the TX RF modulator power-off control. The counter begins to decrease to zero just after that PA was turn off in PA-OFF state, TX RF modulator is turn on when the zero is reached. Each time increment is 1 μS.
7 - 0	(reserved)	(reserved)

Reserved (Write/Read) – Register 15 (Default 0x7193)

Bit No.	Bit Name	Description
15 - 0	(reserved)	(reserved)

Reserved (Write/Read) – Register 16 (Default 0xC9CF)

Bit No.	Bit Name	Description
15-0	(reserved)	(reserved)

Reserved (Write/Read) – Register 17 (Default 0xD3D7)

Bit No.	Bit Name	Description
15 - 0	(reserved)	(reserved)

Tx, Rx Control (Write/Read) – Register 18 (Default 0x0000)

Bit No.	Bit Name	Description
15	SOFTWARE_CNTL	Set this bit to enable software to control the transmit sequencing of modulator, PA, and TR switch, based on the values of TX_MOD_ON_DELAY, TX_PA_ON_DELAY and TX_SW_ON_DELAY respectively. Default setting '0' is to select hardware state machine to control the sequencing.
14 - 13	DC_CNTL[1:0]	00: Select to use fixed DC offset value after BPKTCTL is asserted; however, this value is computed before preamble period as opposed to the 00 setting of bit 13-12 of Register 0. 01: Select to use 8 symbols as time constant to compute DC offset values after BPKTCTL is asserted. 1x: Select to enable BPKTCTL_DC_TC (bit 13-12 of Register 0) setting.
12 - 8	(reserved)	(reserved)
7-0	TX_MOD_ON_DELAY [7:0]	If SOFTWARE_CTRL = 0, this is the delay from rising edge of BPKTCTL, to Modulator turning on. If SOFTWARE_CTRL = 1, this sets the timing delay of the Modulator turning on, after BPKTCTL is asserted. Each time increment is1 µS.

Reserved (Write/Read) – Register 20 (Default 0x83E0)

Bit No.	Bit Name	Description
15 - 0	(reserved)	(reserved)

PLL Synthesizer Control (Write/Read) – Register 21 (Default 0x0962)

Bit No.	Bit Name	Description
15	(reserved)	(reserved)
14	RF_VCO_IDLE_OFF	If RF_VCO_IDLE_OFF = 1, the RF VCO will shutdown while the state machine is in Idle state. This saves power, but a longer PLL settling time may be required when the VCO is automatically powered up to Transmit or Receive. If RF_VCO_IDLE_OFF is 0, the RF VCO stays on even when the state machine is in Idle state. While this consumes more power, there is no extra PLL settling time required when transmit or receive is desired.
13	SYNTH_IDLE_OFF	If SYNTH_IDLE_OFF = 1, the RF synthesizer will shutdown while the state machine is in Idle state. This saves power, but a longer PLL settling time may be required when the synthesizer is automatically powered up to Transmit or Receive. If SYNTH_IDLE_OFF is 0, the synthesizer stays on even when the state machine is in Idle state. While this consumes more power, there is no extra PLL settling time required when transmit or receive is desired.
12	RF_PLL_DIRECT	If RF_PLL_DIRECT is set to 1, transmit and receive carrier frequency will be programmed in MHz, with Register 7 [6:0] and [13:9]. If RF_PLL_DIRECT is set to 0, transmit and receive carrier frequency will be programmed by channel number. Carrier frequency = PLL_RF_FREQ_BASE + PLL_CH_NO.
11 – 0	PLL_RF_FREQ_BASE	If RF_PLL_DIRECT is set to 0, this sets the frequency of channel 0. Default = 2402 MHz. If RF_PLL_DIRECT is set to 1, this value is ignored.

Tx RF Timing Control (Write/Read) – Register 22 (Default 0x0A02)

Bit No.	Bit Name	Description
15 – 8	TX_PA_ON_DELAY	If SOFTWARE_CTRL = 0, this is the delay from Modulator turning on, to PA turning on. If SOFTWARE_CTRL = 1, this sets the timing delay of the PA turning on, after BPKTCTL is asserted. Each time increment is1 µS.
7 – 0	TX_PA_OFF_DELAY	These registers are the initial value for the counter of the TX PA power-off control. When the RF state is in PA-OFF and the counter decreases to zero, TX PA will be turn OFF. Each time increment 1 µS.

Tx Timing Control (Write/Read) – Register 23 (Default 0x0302)

Bit No.	Bit Name	Description
15 – 8	TX_SW_ON_DELAY	If SOFTWARE_CTRL = 0, this is the delay from PA turning on, to TR switch set to the Tx position. If SOFTWARE_CTRL = 1, this sets the timing delay of the TR Switch after BPKTCTL is asserted. Each time increment is1 µS.
7 – 0	(reserved)	(reserved)

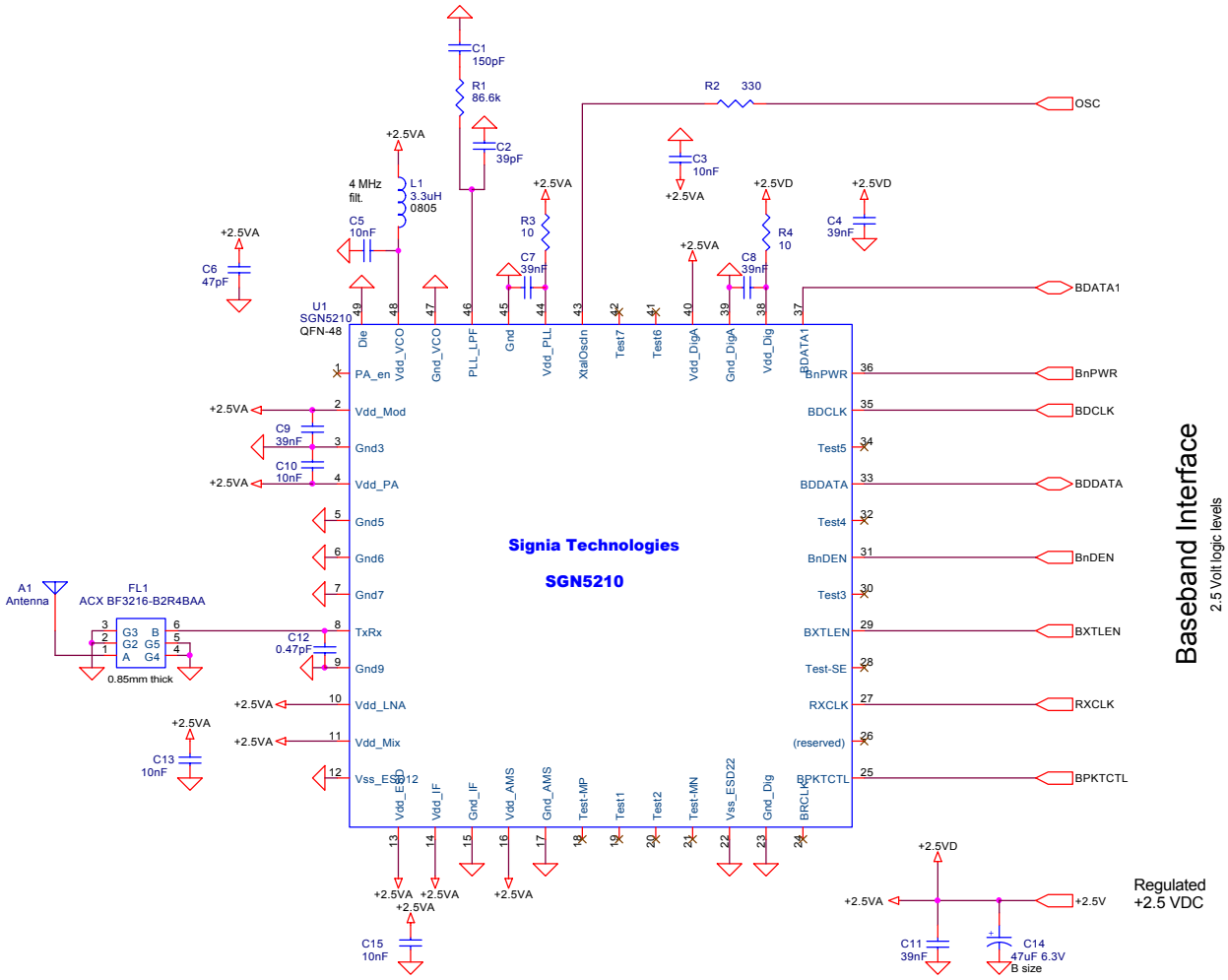
Manufacture's ID Code LSB (Read only) – Register 30(0x8E8E)

Bit No.	Bit Name	Description
15 - 0	ID_CODE_L [15:0]	Lower 16-bit of Manufacture's ID code.

Manufacture's ID Code MSB (Read only) – Register 31(0x10C0)

Bit No.	Bit Name	Description
15 - 0	ID_CODE_M [31:16]	Upper 16-bit of Manufacture's ID code.

Typical Application



Additional Development Resources

Programming and Applications

Please refer to AN5000.05 "*Wireless Solutions using Signia Technologies 2.4 GHz RF Transceiver chips*".

Reference Design

Please refer to AN5002.01 "*A Reference Design for Short-Range Wireless using the Signia Technologies SGN5210 2.4 GHz RF Transceiver IC*".

Evaluation Kit

Please ask your Signia sales representative for the "*SGN5210 RF Evaluation Kit*", including IBM PC compatible LPT interface and software.

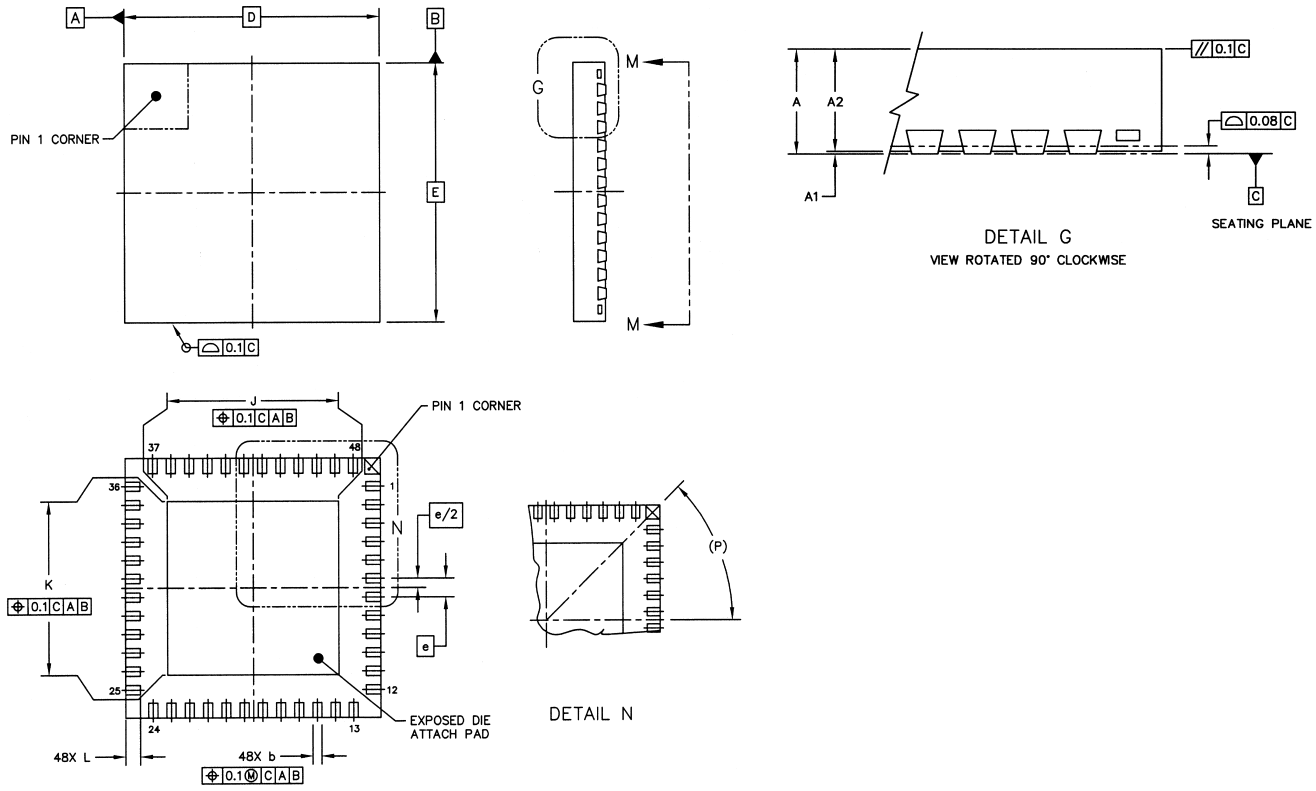
Manufacturing Kits

Various PCB layouts are available. Please see http://www.signiatech.com/products/vsr.html or contact your Signia sales representative.

Package Outline

QFN 48 Lead Exposed Pad Package, 7x7 x1mm Pkg. 0.5mm Pitch (JEDEC) MO-220-A

All dimensions are in millimeters:



VIEW M-M

Dim.	Min.		Max.	Dim.	Min.		Max.
A	0.8		1	e		0.5 BSC	
A1	0		0.05	J	4.55	4.7	5.25
A2	0.75		1	K	4.55	4.7	5.25
b	0.18	0.25	0.3	L	0.3	0.4	0.5
D		7 BSC		P		45° REF	
E		7 BSC					

Notes:

1.0 COPLANRITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

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