

**Ordering Information**

<b>Part Numbers</b>	<b>Description</b>	<b>Device Vendor</b>
SH5126SV351816-SE	512Mx64 (4GB), DDR3, 204-Pin Unbuffered SO-DIMM, Non-ECC, 512Mx8 Based, PC3L-12800, DDR3L-1600-11-11-11, 30.00mm, 1.35V/1.5V, Halogen-Free (RoHS Compliant).	Samsung, Rev. E K4B4G0846E-BYK0

(All specifications of this module are subject to change without notice.)

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**Part Number Decode**

<b>S</b>	<b>H</b>	<b>512</b>	<b>6</b>	<b>SV3</b>	<b>518</b>	<b>1</b>	<b>6</b>	<b>-</b>	<b>S</b>	<b>E</b>
1	2	3	4	5	6	7	8		9	10

<b>1</b>	<b>SMART Modular Technologies</b>
<b>2</b>	<b>Module Process Technology</b> H: Halogen-Free (RoHS Compliant)
<b>3</b>	<b>Module Address Depth</b> 512: 512M
<b>4</b>	<b>Module Data Bus Width</b> 6: x64
<b>5</b>	<b>Module Configuration</b> SV3: 1.35V/1.5V DDR3 204-Pin Unbuffered SO-DIMM
<b>6</b>	<b>Device Configuration</b> 518: 512Mx8 Based
<b>7</b>	<b>CAS Latency</b> 1: CL 11
<b>8</b>	<b>Device Speed</b> 6: DDR3L-1600
<b>9</b>	<b>Device Vendor</b> S: Samsung
<b>10</b>	<b>Device Revision</b> E: Revision E



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### Revision History

Date	Description
July 13, 2015	Datasheet released.

## 4GB (512Mx64) DDR3 SDRAM Module - 512Mx8 Based 204-Pin Unbuffered SO-DIMM, Non-ECC

### Features

- Standard = JEDEC
- Configuration = Non-ECC
- Number of Module Ranks = 1
- Number of Devices = 8
- $V_{DD} = V_{DDQ} = 1.35V/1.5V$
- $V_{DDSPD} = 3.0V$  to 3.6V
- Cycle Time = 1.25ns
- CAS Latency = 5, 6, 7, 8, 9, 10, 11
- Additive Latency = 0, CL-1, and CL-2
- CAS Write Latency (CWL) = 5, 6, 7, 8
- Burst Length = BC4, BL8, BC4 or BL8 (on the fly)
- Burst Type = Nibble Sequential & Interleave Mode
- Internal Banks per SDRAM = 8
- Refresh = 8K/64ms
- Device Package = FBGA
- Lead Finish = Gold
- Length x Height = 67.60mm x 30.00mm
- No. of sides = Double-sided
- Mating Connector (Examples)
  - Horizontal = Foxconn - AS0A626-UASN-7F
- ZQ calibration supported
- On chip DLL align DQ, DQS and  $\overline{DQS}$  transition with CK transition
- DM write data-in at both the rising and falling edges of the data strobe
- All addresses and control inputs latched on the rising edges of the clock
- Dynamic On Die Termination supported
- Driver strength selected by EMRS
- Asynchronous RESET pin supported
- Write Levelization supported
- 8-bit pre-fetch

### Addressing

Device Configuration	512Mx8
Number of Internal Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BC switch on the fly	A12/ $\overline{BC}$
Row Address	A0 - A15
Column Address	A0 - A9
Page size	1KB

### Pin Description Table

Symbol	Type	Polarity	Function
$\overline{CK0-CK1}$ , CK0-CK1	Input	Differential Crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM address/control inputs are sampled on the crossing of the positive edge of CK and the negative edge of $\overline{CK}$ . Output (read) data is referenced to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE0	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
ODT0	Input	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming this function is enabled on the DRAM.
BA0-BA2	Input	-	Selects which SDRAM bank of the eight is activated.

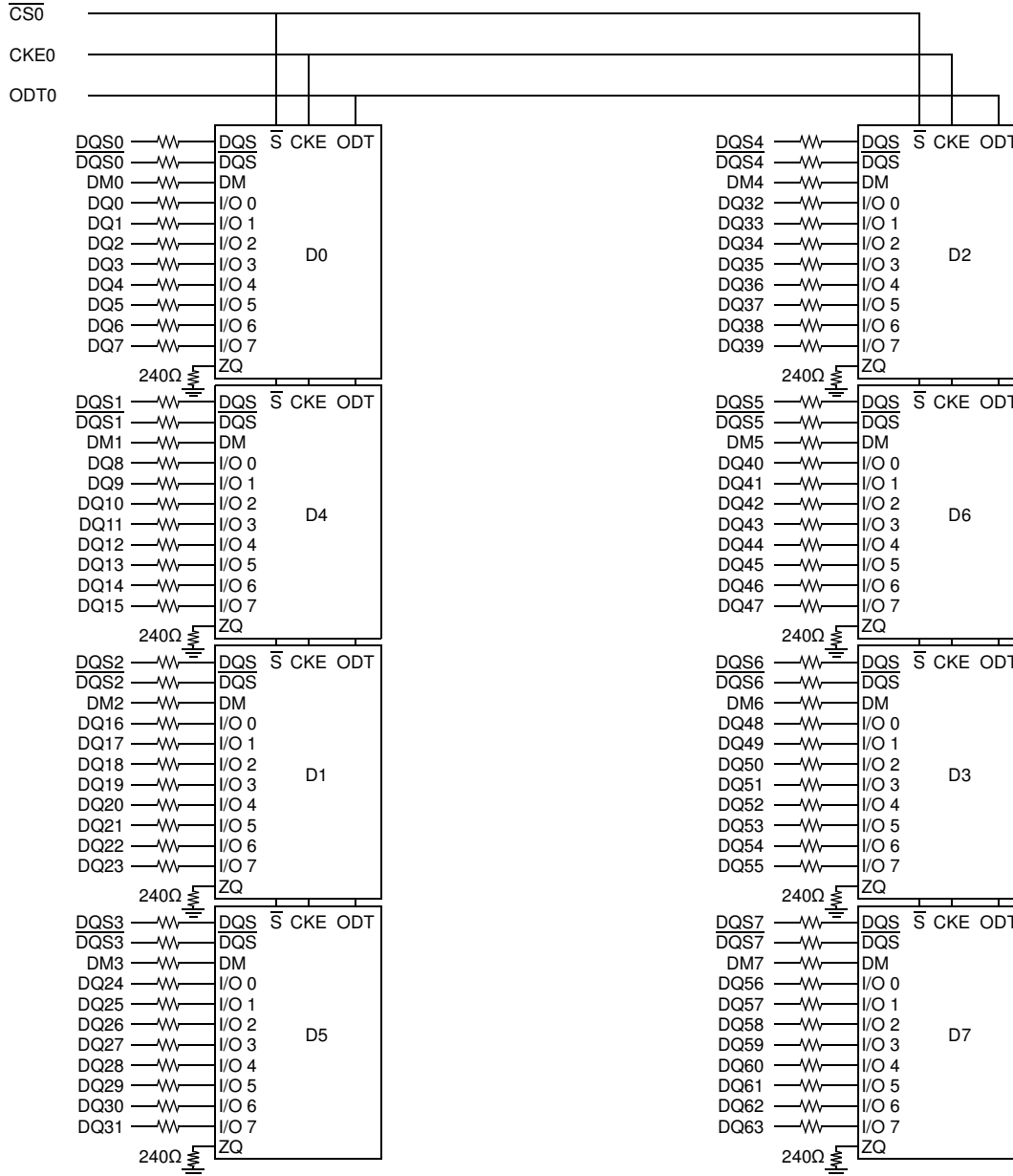
**Pin Description Table (Continued)**

Symbol	Type	Polarity	Function
A0-A15	Input	-	During a Bank Activate command cycle, address inputs define the row address (RA0-RA15). During a Read or Write command cycle, address inputs define the column address (CA0-CA9). In addition to the column address, AP is used to invoke auto-precharge operation at the end of the burst read or write cycle. If AP is high, auto-precharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12( $\overline{BC}$ ) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
RAS, CAS, WE	Input	Active Low	RAS, CAS, and WE (along with CS) define the command being entered.
DQ0-DQ63	Input/Output	-	Data Input/Output pins.
$\overline{DQS0-DQS7}$ DQS0-DQS7	Input/Output	Differential Crossing	Data strobe for input and output data.
DM0-DM7	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
SA0-SA1	Input	-	These signals are tied at the system to either $V_{SS}$ or $V_{DDSPD}$ to configure the serial SPD EEPROM address range.
SDA	Input/Output	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to $V_{DDSPD}$ to act as a pull-up on the system board.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus tied to $V_{DDSPD}$ to act as a pull-up on the system board.
$\overline{EVENT}$	Output	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part. No pull-up resistor is provided on DIMM.
$\overline{RESET}$	Input	Active Low	Asynchronous Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is CMOS rail to rail signal with DC high and low at 80% and 20% of $V_{DD}$ .
$V_{DD}, V_{SS}$	Supply	-	Power and ground for the DDR3 SDRAM input buffers, and core logic. $V_{DD}$ and $V_{DDQ}$ pins are tied to $V_{DD}/V_{DDQ}$ planes on these modules. $V_{SS}$ pins are tied to $V_{SS}$ planes on these modules.
$V_{DDQ}$	Supply	-	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. $V_{DDQ}$ shares the same power plane as $V_{DD}$ pins.
$V_{REFDQ}$	Supply	-	Reference voltage for I/O inputs.
$V_{REFCA}$	Supply	-	Reference voltage for address/command inputs.
$V_{DDSPD}$	Supply	-	Power supply for SPD EEPROM. This supply is separate from the $V_{DD}/V_{DDQ}$ power plane.
$V_{TT}$	Supply	-	Termination voltage for address/command/control/clock nets.
NC	-	-	No Connect.

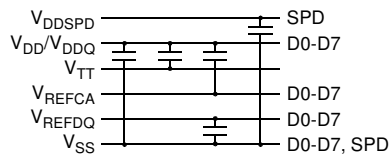
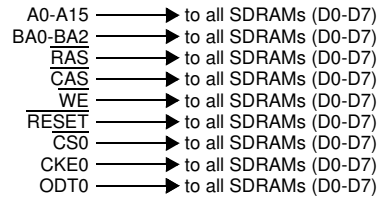
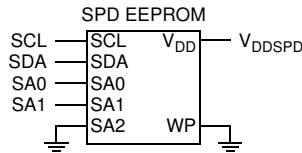


**DDR3 204-Pin Unbuffered SO-DIMM Pin List**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>REFDQ</sub>	2	V <sub>SS</sub>	53	DQ19	54	V <sub>SS</sub>	105	V <sub>DD</sub>	106	V <sub>DD</sub>	157	DQ42	158	DQ46
3	V <sub>SS</sub>	4	DQ4	55	V <sub>SS</sub>	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{\text{RAS}}$	161	V <sub>SS</sub>	162	V <sub>SS</sub>
7	DQ1	8	V <sub>SS</sub>	59	DQ25	60	V <sub>SS</sub>	111	V <sub>DD</sub>	112	V <sub>DD</sub>	163	DQ48	164	DQ52
9	V <sub>SS</sub>	10	$\overline{\text{DQS0}}$	61	V <sub>SS</sub>	62	$\overline{\text{DQS3}}$	113	$\overline{\text{WE}}$	114	$\overline{\text{CS0}}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{\text{CAS}}$	116	ODT0	167	V <sub>SS</sub>	168	V <sub>SS</sub>
13	V <sub>SS</sub>	14	V <sub>SS</sub>	65	V <sub>SS</sub>	66	V <sub>SS</sub>	117	V <sub>DD</sub>	118	V <sub>DD</sub>	169	$\overline{\text{DQS6}}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13	120	ODT1 (NC)	171	DQS6	172	V <sub>SS</sub>
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{\text{CS1}}$ (NC)	122	NC	173	V <sub>SS</sub>	174	DQ54
19	V <sub>SS</sub>	20	V <sub>SS</sub>	71	V <sub>SS</sub>	72	V <sub>SS</sub>	123	V <sub>DD</sub>	124	V <sub>DD</sub>	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1 (NC)	125	NC	126	V <sub>REFCA</sub>	177	DQ51	178	V <sub>SS</sub>
23	DQ9	24	DQ13	75	V <sub>DD</sub>	76	V <sub>DD</sub>	127	V <sub>SS</sub>	128	V <sub>SS</sub>	179	V <sub>SS</sub>	180	DQ60
25	V <sub>SS</sub>	26	V <sub>SS</sub>	77	NC	78	A15	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{\text{DQS1}}$	28	DM1	79	BA2	80	A14	131	DQ33	132	DQ37	183	DQ57	184	V <sub>SS</sub>
29	DQS1	30	$\overline{\text{RESET}}$	81	V <sub>DD</sub>	82	V <sub>DD</sub>	133	V <sub>SS</sub>	134	V <sub>SS</sub>	185	V <sub>SS</sub>	186	$\overline{\text{DQS7}}$
31	V <sub>SS</sub>	32	V <sub>SS</sub>	83	A12/ $\overline{\text{BC}}$	84	A11	135	$\overline{\text{DQS4}}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V <sub>SS</sub>	189	V <sub>SS</sub>	190	V <sub>SS</sub>
35	DQ11	36	DQ15	87	V <sub>DD</sub>	88	V <sub>DD</sub>	139	V <sub>SS</sub>	140	DQ38	191	DQ58	192	DQ62
37	V <sub>SS</sub>	38	V <sub>SS</sub>	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V <sub>SS</sub>	195	V <sub>SS</sub>	196	V <sub>SS</sub>
41	DQ17	42	DQ21	93	V <sub>DD</sub>	94	V <sub>DD</sub>	145	V <sub>SS</sub>	146	DQ44	197	SA0	198	$\overline{\text{EVENT}}$
43	V <sub>SS</sub>	44	V <sub>SS</sub>	95	A3	96	A2	147	DQ40	148	DQ45	199	V <sub>DDSPD</sub>	200	SDA
45	$\overline{\text{DQS2}}$	46	DM2	97	A1	98	A0	149	DQ41	150	V <sub>SS</sub>	201	SA1	202	SCL
47	DQS2	48	V <sub>SS</sub>	99	V <sub>DD</sub>	100	V <sub>DD</sub>	151	V <sub>SS</sub>	152	$\overline{\text{DQS5}}$	203	V <sub>TT</sub>	204	V <sub>TT</sub>
49	V <sub>SS</sub>	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{\text{CK0}}$	104	$\overline{\text{CK1}}$	155	V <sub>SS</sub>	156	V <sub>SS</sub>				

**Block Diagram**


Note: Unless otherwise noted, data resistor values are 15Ω ± 5%.

**Block Diagram (Continued)**

**Clock Wiring**

CK Signals	Clock Wiring
CK0/CK0	8 SDRAMs (D0-D7)
CK1/CK1	0 SDRAMs

**Notes:**

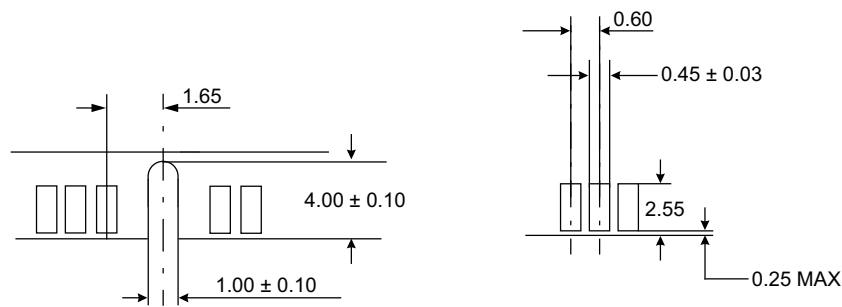
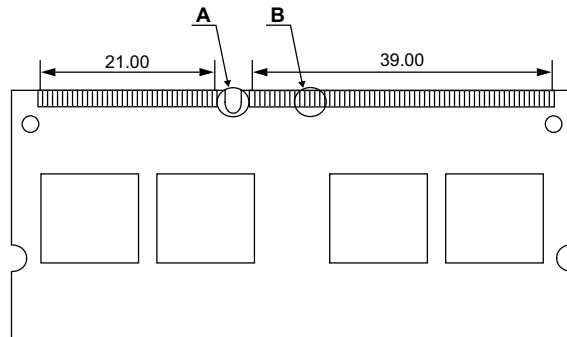
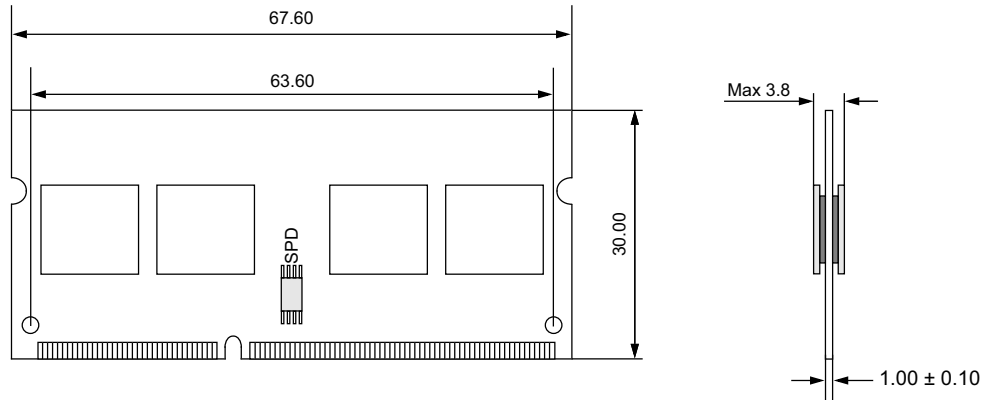
1. All address, command and control signal lines are terminated through a series resistor to V<sub>TT</sub>.
2. Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 7.



**Physical Dimensions**

204-Pin Unbuffered SO-DIMM Module

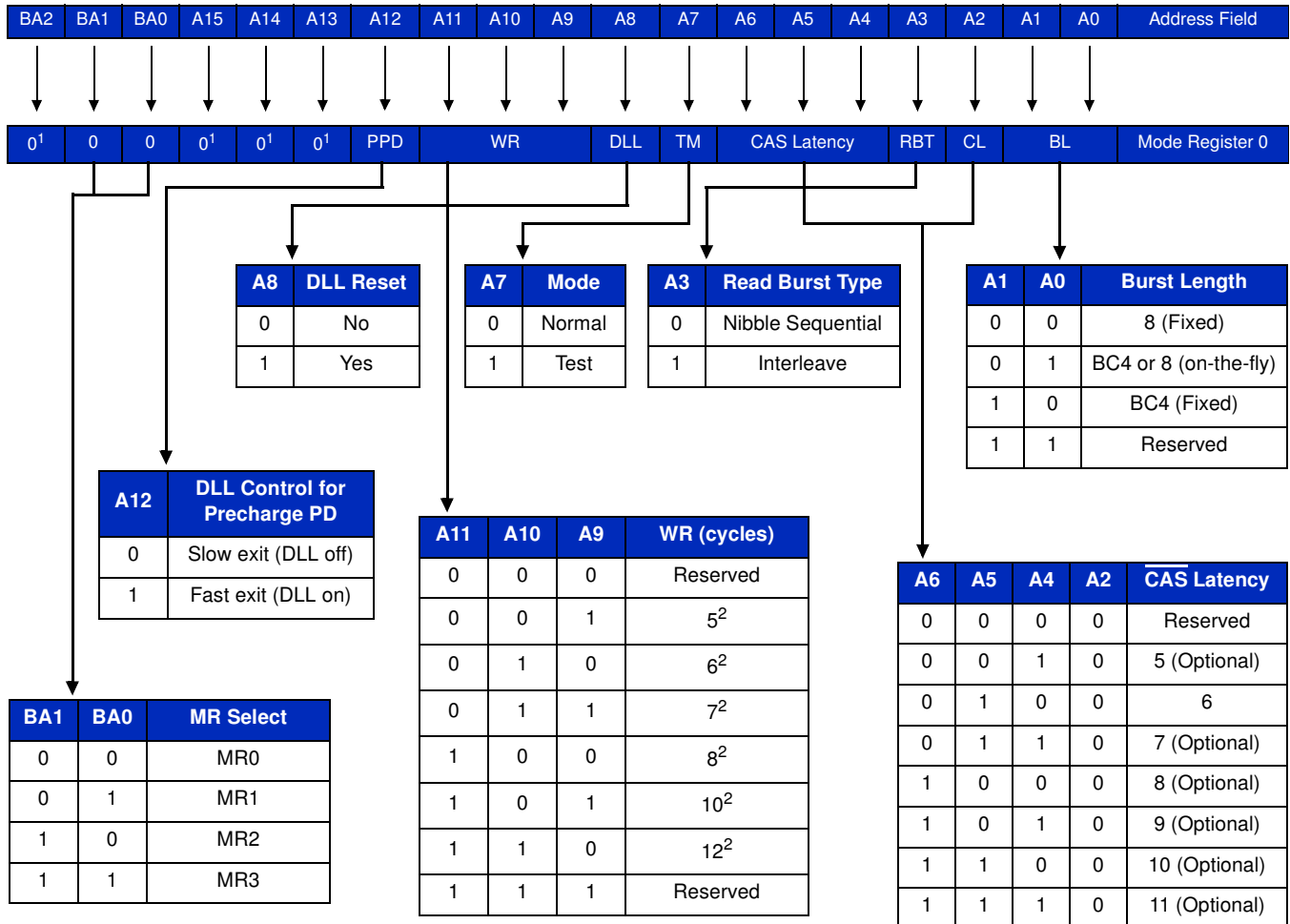
Units : Millimeters


**Detail A**
**Detail B**

 Tolerances on all dimensions  $\pm 0.15$  unless otherwise specified.

**Mode Register (MR0) Table Definition**

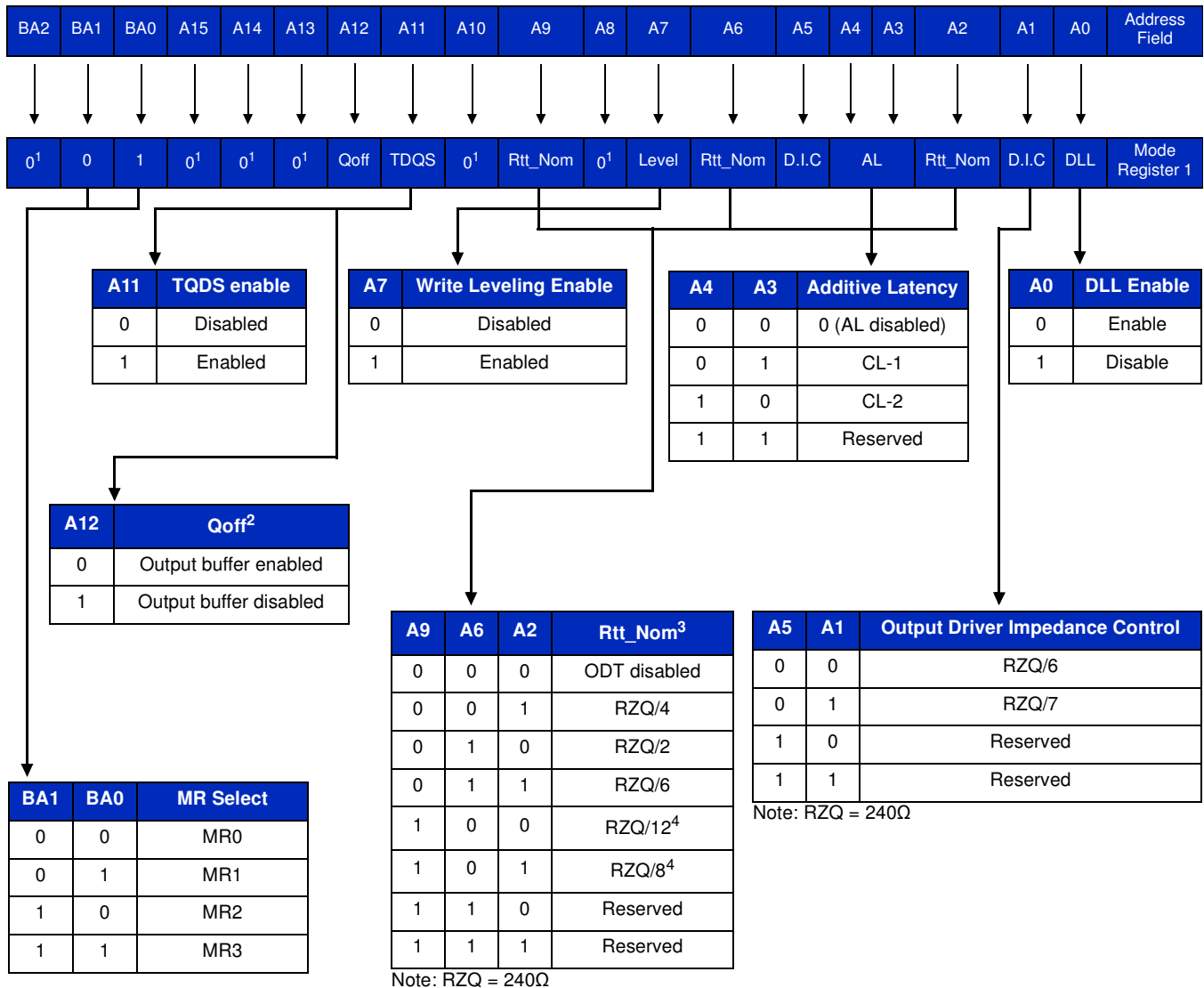
The mode register stores the data for controlling the various operating modes of DDR3 SDRAM. It controls CAS latency, burst length, burst chop, burst sequence, test mode, DLL reset,  $t_{WR}$  and various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , BA0, BA1 and BA2 while controlling the state of address pins A0~A15.


**Notes:**

- BA2 and A13~A15 are reserved for future use and must be programmed to 0 during MRS.
- $WR_{min}$  (write recovery for auto-precharge) in clock cycles is calculated by dividing  $t_{WR}$  (in ns) by  $t_{CK}$  (in ns) and rounding up to the next integer:  $WR_{min} [\text{cycles}] = \text{Round-up} (t_{WR}[\text{ns}] / t_{CK}[\text{ns}])$ . The WR value in the mode register must be programmed to be equal or larger than  $WR_{min}$ . The programmed WR value is used with  $t_{RP}$  to determine  $t_{DAL}$ .

### Mode Register (MR1) Table Definition

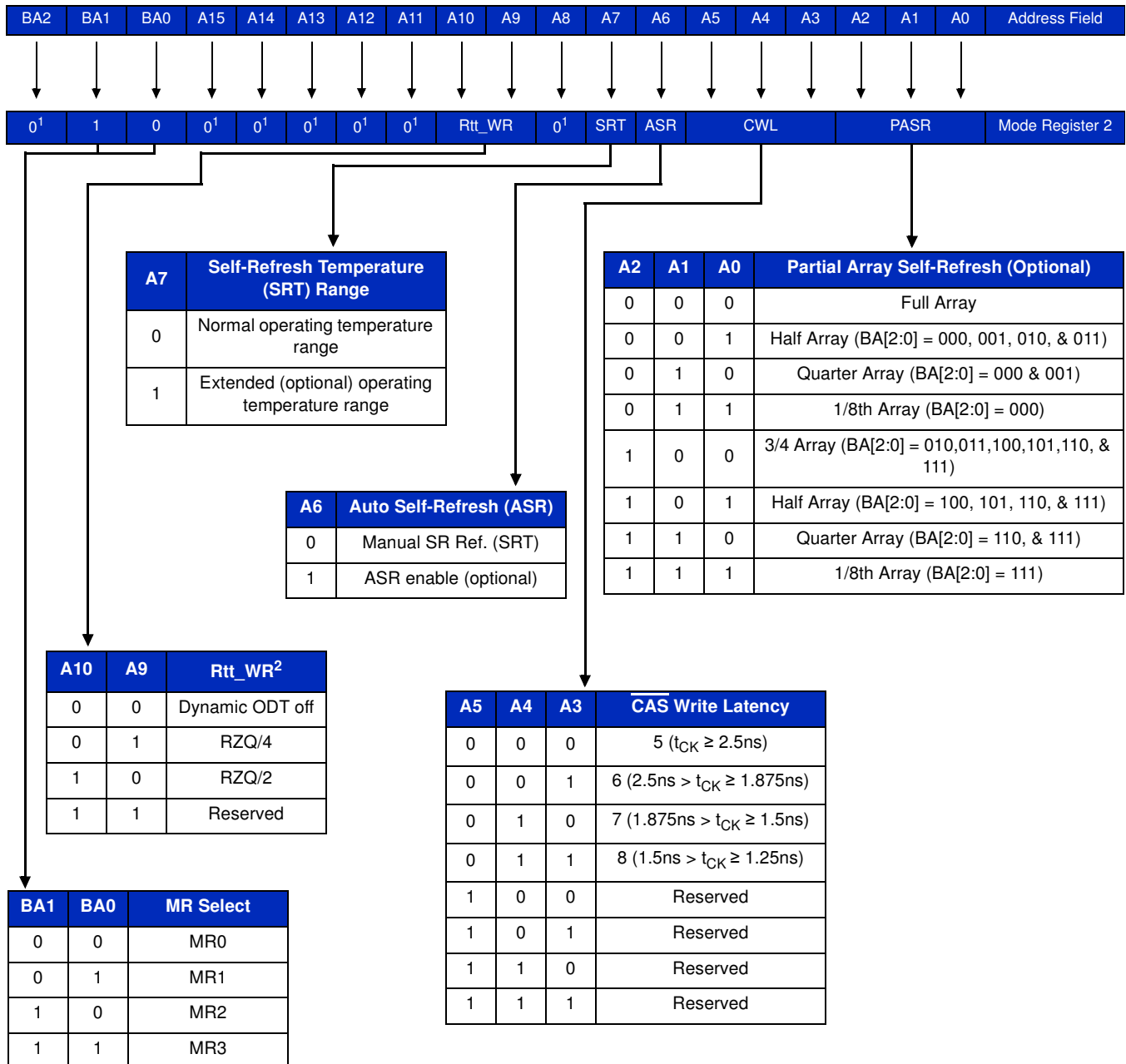
The Mode Registers MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt\_Nom impedance, additive latency, Write Leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS, RAS, CAS, WE, high on BA0 and low on BA1 and BA2, while controlling the state of address pins A0~A15.


**Notes:**

1. BA2 and A8, A10, A13~A15 are reserved for future use and must be programmed to 0 during MRS.
2. Outputs disabled - DQs, DQSs, DQSs.
3. In Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all Rtt\_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only Rtt\_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
4. If Rtt\_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

### Mode Register (MR2) Table Definition

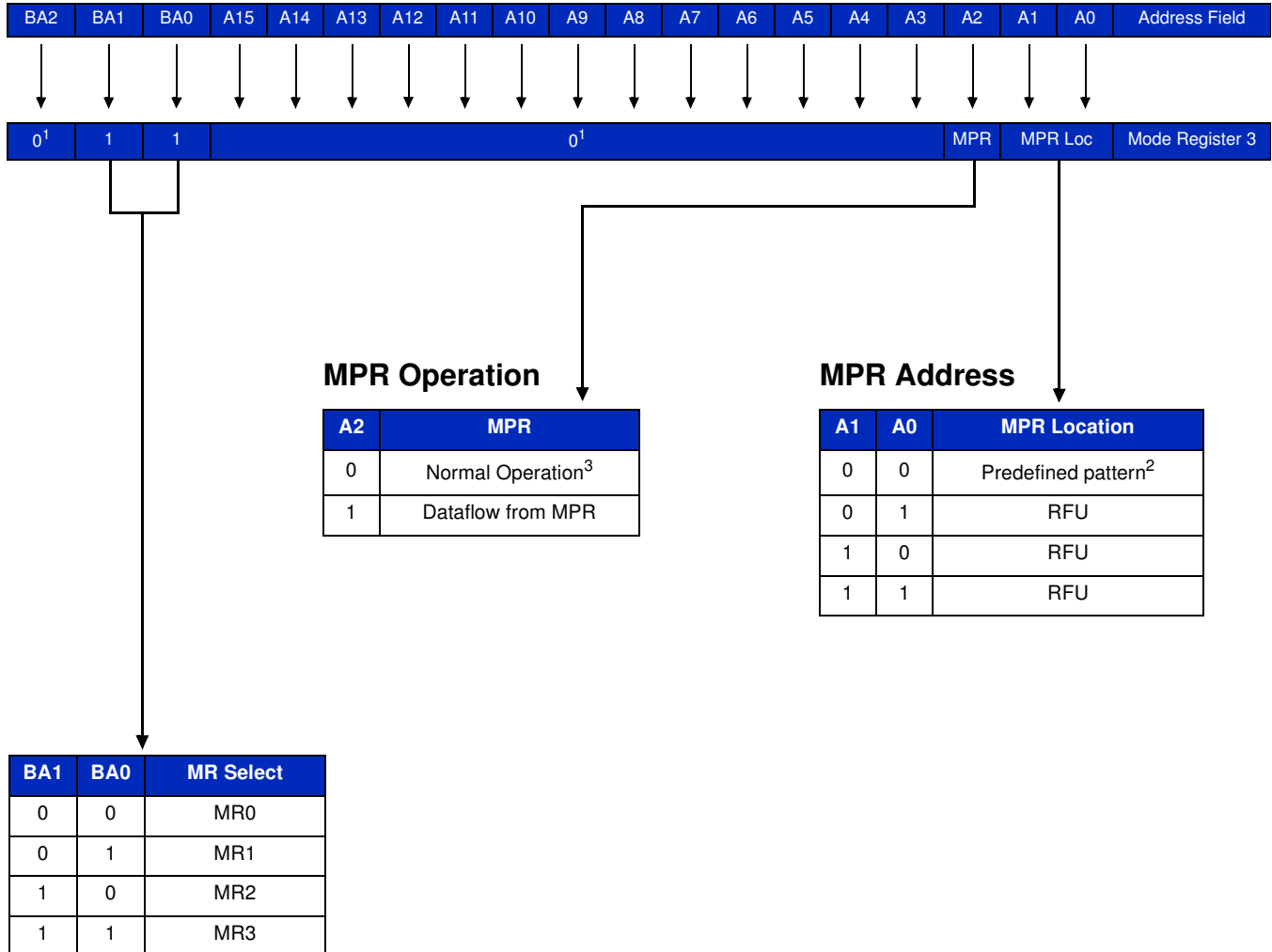
The Mode Registers MR2 stores the data for controlling refresh related features, Rtt\_WR impedance, and CAS Write Latency. The Mode Register 2 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and low on BA0 and BA2 while controlling the state of address pins A0~A15.


**Notes:**

- BA2, A8 and A11~A15 are reserved for future use and must be programmed to 0 during MRS.
- If Rtt\_WR value can be applied during writes even when Rtt\_Nom is disabled. During Write Leveling, Dynamic ODT is not available.

### Mode Register (MR3) Table Definition

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , high on BA1 and BA0, low on BA2 while controlling the state of address pins A0~A15.



#### Notes:

1. BA2, A3~A15 are reserved for future use and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0), then MR3 A[1:0] will be ignored.

## Command Truth Table

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

- Notes 1- 4 apply to the entire Command Truth Table.
- Note 5 applies to all Read/Write command.

[BA= Bank address, RA= row Address, CA = Column Address,  $\overline{BC}$  = Burst chop, X = Don't care, V = Valid]

## Command Truth Table

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA2	A13-A15	$\overline{A12/BC}$	A10/AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self-Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7, 9, 12
Self-Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7, 8, 9, 12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge All Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power-Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
Power-Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

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**Notes:**

1. All DDR3 SDRAM commands are defined by states of  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2.  $\overline{RESET}$  command is enabled when Low, which will be used only for asynchronous reset, so  $\overline{RESET}$  must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS, BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by the MRS.
6. The Power-Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
8. Self-Refresh Exit is asynchronous.
9.  $V_{REF}$  (Both  $V_{REFDQ}$  and  $V_{REFCA}$ ) must be maintained during Self-Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read and write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

**CKE Truth Table**

- Notes 1-7 apply to the entire CKE Truth Table.
- CKE low is allowed only if  $t_{MRD}$  and  $t_{MOD}$  are satisfied.

**CKE Truth Table**

Current State	CKE		Command (N) <sup>3</sup> RAS, CAS, WE, CS	Action (N) <sup>3</sup>	Notes
	Previous Cycle (N-1)	Current Cycle (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	Deselect or NOP	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	Deselect or NOP	Self-Refresh Exit	8, 12, 16
Bank Activate	H	L	Deselect or NOP	Active Power-Down Entry	11, 13, 14
Reading	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Writing	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	Deselect or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	11, 13, 14, 18
		L	Refresh	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on page 14.					10

**Notes:**

- CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
- COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
- All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
- CKE must be registered with the same value on  $t_{CKEmin}$  consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the  $t_{CKEmin}$  clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + t_{CKEmin} + t_{IH}$ .
- Deselect and NOP are defined in the Command Truth Table.
- On Self-Refresh Exit, Deselect or NOP commands must be issued on every clock edge occurring during the  $t_{XS}$  period. Read or ODT commands may be issued only after  $t_{XSDLL}$  is satisfied.
- Self-Refresh mode can only be entered from the All Banks Idle state.
- Must be a legal command as defined in the Command Truth Table.
- Valid commands for Power-Down Entry and Exit are NOP and Deselect only.
- Valid commands for Self-Refresh Exit are NOP and Deselect only.
- Self-Refresh can not be entered during Read or Write operations.
- The Power-Down does not perform any refresh operations.
- "X" means "don't care" (including floating around  $V_{REF}$ ) in Self-Refresh and Power-Down. It also applies to Address pins.
- $V_{REF}$  (Both  $V_{REFDQ}$  and  $V_{REFCA}$ ) must be maintained during Self-Refresh operation.
- If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
- "Idle state" is defined as all banks are closed ( $t_{RP}$ ,  $t_{DAL}$ , etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied ( $t_{MRD}$ ,  $t_{MOD}$ ,  $t_{RFC}$ ,  $t_{ZQinit}$ ,  $t_{ZQoper}$ ,  $t_{ZQCS}$ , etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied ( $t_{XS}$ ,  $t_{XP}$ ,  $t_{XPDLL}$ , etc.).



## Absolute Maximum Ratings

### Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
$V_{DD}$	Voltage on $V_{DD}$ relative to $V_{SS}$	-0.4 ~ 1.975	V	1, 3
$V_{DDQ}$	Voltage on $V_{DDQ}$ relative to $V_{SS}$	-0.4 ~ 1.975	V	1, 3
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.4 ~ 1.975	V	1
$T_{STG}$	Storage Temperature	-55 to +100	°C	1, 2

**Notes:**

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.
- $V_{DD}$  and  $V_{DDQ}$  must be within 300 mV of each other at all times and  $V_{REF}$  must be not greater than  $0.6 \cdot V_{DDQ}$ . When  $V_{DD}$  and  $V_{DDQ}$  are less than 500 mV;  $V_{REF}$  may be equal to or less than 300 mV.

### Recommended DC Operating Conditions

Symbol	Parameter	Voltage	Rating			Units	Notes
			Min	Typical	Max		
$V_{DD}$	Supply Voltage	1.35V	1.283	1.35	1.45	V	1, 2, 3
		1.5V	1.425	1.5	1.575	V	1, 2, 3
$V_{DDQ}$	Supply Voltage for Output	1.35V	1.283	1.35	1.45	V	1, 2, 3
		1.5V	1.425	1.5	1.575	V	1, 2, 3

**Notes:**

- Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$ .
- $V_{DDQ}$  tracks with  $V_{DD}$ . AC parameters are measured with  $V_{DD}$  and  $V_{DDQ}$  tied together.
- $V_{DD}$  &  $V_{DDQ}$  rating are determined by operation voltage.

### Operating Temperature Range

Symbol	Parameter	Range	Units	Notes
T <sub>OPER</sub>	Normal Operating Temperature Range (Case)	0 to 95	°C	1, 2, 3

**Notes:**

- Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 °C and 85 °C under all operating conditions.
- Some applications require operation of the DRAM between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
  - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t<sub>REFI</sub> to 3.9µs. It is also possible to specify a component with 1X refresh (t<sub>REFI</sub> to 7.8µs) in the Extended Temperature Range. Please refer to the SPD for option availability.
  - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the SPD for option availability.

### Temperature Sensor Characteristics

Symbol	Description	Test Condition	Typical	Max	Units
JEDEC B-Grade	Accuracy for corresponding range	+75 °C ≤ T <sub>AMB</sub> ≤ +95 °C	±0.5	±1	°C
		+40 °C ≤ T <sub>AMB</sub> ≤ +125 °C	±1	±2	°C
		-40 °C ≤ T <sub>AMB</sub> ≤ +125 °C	±2	±3	°C
Resolution			0.25		°C/LSB

### Refresh Parameters

Parameter	Symbol	4Gb	Units
REF command to ACT or REF command time	t <sub>RFC</sub>	260	ns
Average periodic refresh interval	t <sub>REFI</sub>	0 °C ≤ T <sub>CASE</sub> ≤ 85 °C	7.8
		85 °C ≤ T <sub>CASE</sub> ≤ 95 °C	3.9

**AC and DC Logic Input Levels for Single-Ended Signals**

Symbol	Parameter	DDR3L-1600		Units	Notes
		Min	Max		
<b>1.35V</b>					
$V_{IH}$ (DC90)	DC input logic high	$V_{REF} + 0.090$	$V_{DD}$	V	1
$V_{IL}$ (DC90)	DC input logic low	$V_{SS}$	$V_{REF} - 0.090$	V	1
$V_{IH}$ (AC160)	AC input logic high	$V_{REF} + 0.160$	Note 2	V	1, 4
$V_{IL}$ (AC160)	AC input logic low	Note 2	$V_{REF} - 0.160$	V	1, 4
$V_{IH}$ (AC135)	AC input logic high	$V_{REF} + 0.135$	Note 2	V	1
$V_{IL}$ (AC135)	AC input logic low	Note 2	$V_{REF} - 0.135$	V	1
$V_{REFCA}(DC)$	Reference voltage for ADD/CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3
<b>1.5V</b>					
$V_{IH}$ (DC100)	DC input logic high	$V_{REF} + 0.100$	$V_{DD}$	V	1
$V_{IL}$ (DC100)	DC input logic low	$V_{SS}$	$V_{REF} - 0.100$	V	1
$V_{IH}$ (AC175)	AC input logic high	$V_{REF} + 0.175$	Note 2	V	1, 4
$V_{IL}$ (AC175)	AC input logic low	Note 2	$V_{REF} - 0.175$	V	1, 4
$V_{IH}$ (AC150)	AC input logic high	$V_{REF} + 0.150$	Note 2	V	1
$V_{IL}$ (AC150)	AC input logic low	Note 2	$V_{REF} - 0.150$	V	1
$V_{REFCA}(DC)$	Reference voltage for ADD/CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3

**Notes:**

1. For Command and Address signals except  $\overline{RESET}$ ,  $V_{REF} = V_{REFCA}$ . For DQ and DM,  $V_{REF} = V_{REFDQ}$ .
2. Refer to AC Overshoot and Undershoot Specifications for Address/Control Pins on page 21.
3. The AC peak noise on  $V_{REF}$  may not allow  $V_{REF}$  to deviate from  $V_{REF(DC)}$  by more than  $\pm 1\% V_{DD}$  (for reference: approximately  $\pm 15mV$ ).
4. Applies to Command and Address signals only.

**Differential Swing Requirements for Clock (CK/ $\overline{\text{CK}}$ ) and Strobe (DQS/ $\overline{\text{DQS}}$ )**

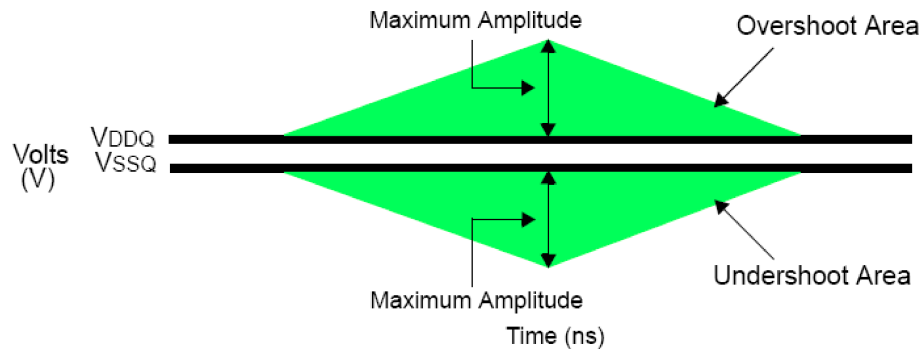
Symbol	Parameter	DDR3L-1600		Units	Notes
		Min	Max		
<b>1.35V</b>					
$V_{\text{IHDIFF}}$	Differential input logic high	0.180	Note 3	V	1
$V_{\text{ILDIFF}}$	Differential input logic high	Note 3	-0.180	V	1
$V_{\text{IHDIFF(AC)}}$	AC input logic high	$2 * (V_{\text{IH(AC)}} - V_{\text{REF}})$	Note 3	V	2
$V_{\text{ILDIFF(AC)}}$	AC input logic low	Note 3	$2 * (V_{\text{REF}} - V_{\text{IL(AC)}})$	V	2
<b>1.5V</b>					
$V_{\text{IHDIFF}}$	Differential input logic high	0.200	Note 3	V	1
$V_{\text{ILDIFF}}$	Differential input logic high	Note 3	-0.200	V	1
$V_{\text{IHDIFF(AC)}}$	AC input logic high	$2 * (V_{\text{IH(AC)}} - V_{\text{REF}})$	Note 3	V	2
$V_{\text{ILDIFF(AC)}}$	AC input logic low	Note 3	$2 * (V_{\text{REF}} - V_{\text{IL(AC)}})$	V	2

**Notes:**

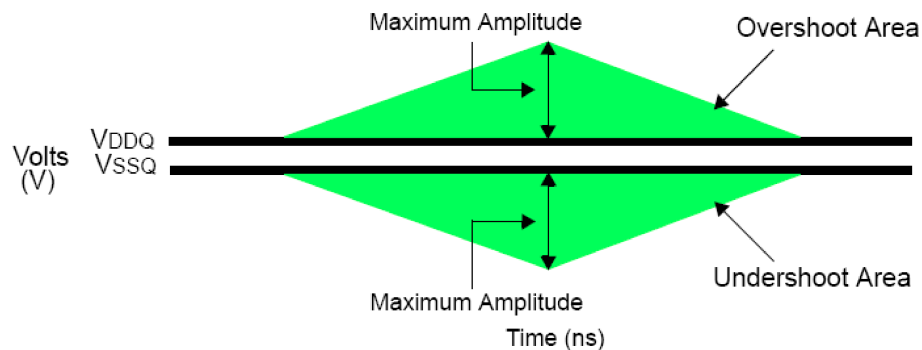
- Used to define a differential signal slew-rate.
- For CK/ $\overline{\text{CK}}$ , use  $V_{\text{IH}}/V_{\text{IL(AC)}}$  of ADD/CMD and  $V_{\text{REFCA}}$ ; for DQS/ $\overline{\text{DQS}}$ , use  $V_{\text{IH}}/V_{\text{IL(AC)}}$  of DQs and  $V_{\text{REFDQ}}$ ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended signals CK,  $\overline{\text{CK}}$ , DQS,  $\overline{\text{DQS}}$  need to be within the respective limits ( $V_{\text{IH(DC)max}}$ ,  $V_{\text{IL(DC)min}}$ ) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins on page 21.

**AC Overshoot/Undershoot Specification for Address/Control Pins**

Parameter	DDR3L-1600	Units
Maximum peak amplitude allowed for overshoot area.	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.4	V
Maximum overshoot area above $V_{DD}$ .	0.33	V-ns
Maximum undershoot area under $V_{SS}$ .	0.33	V-ns
(A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT)		


**AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins**

Parameter	DDR3L-1600	Units
Maximum peak amplitude allowed for overshoot area.	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.4	V
Maximum overshoot area above $V_{DD}$ .	0.13	V-ns
Maximum undershoot area under $V_{SS}$ .	0.13	V-ns
(CK, $\overline{CK}$ , DQ, DQS, $\overline{DQS}$ , DM)		



**Device Standard Speed Bins**

Speed Bin		DDR3L-1600		Units	Notes	
CL - nRCD - nRP		11-11-11				
Parameter	Symbol	Min	Max			
Internal read command to first data	$t_{AA}$	13.125	20	ns	6	
ACT to internal read or write delay time	$t_{RCD}$	13.125	-	ns	6	
Pre command period	$t_{RP}$	13.125	-	ns	6	
ACT to ACT or REF command period	$t_{RC}$	48.125	-	ns	6	
ACT to PRE command period	$t_{RAS}$	35	9 * $t_{REFI}$	ns		
CL = 5	CWL = 5	$t_{CK(avg)}$	3.0	3.3	ns	1, 2, 3, 5, 7
	CWL = 6, 7, 8		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	ns	1, 2, 3, 5
	CWL = 6, 7, 8		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 5
	CWL = 7, 8		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 5
	CWL = 7, 8		Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 7		1.5	< 1.875	ns	1, 2, 3, 5
	CWL = 8		Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 7		1.5	< 1.875	ns	1, 2, 3, 5
	CWL = 8		Reserved		ns	4
CL = 11	CWL = 5, 6, 7	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 8		1.25	< 1.5	ns	1, 2, 3, 5
Supported CL Settings			5, 6, 7, 8, 9, 10, 11		$n_{CK}$	
Supported CWL Settings			5, 6, 7, 8		$n_{CK}$	

### Speed Bin Tables Notes

1. The CL setting and CWL setting result in  $t_{CK(AVG)min}$  and  $t_{CK(AVG)max}$  requirements. When making a selection of  $t_{CK(AVG)}$ , both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2.  $t_{CK(AVG)min}$  limits: Since  $\overline{CAS}$  Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard  $t_{CK(AVG)}$  value (3.0ns, 2.5ns, 1.875ns, 1.5ns, or 1.25ns) when calculating CL [nCK] =  $t_{AA}$  [ns] /  $t_{CK(AVG)}$  [ns], rounding up to the next 'Supported CL', where  $t_{CK(AVG)} = 3.0ns$  should only be used for CL = 5 calculation.
3.  $t_{CK(AVG)max}$  limits: Calculate  $t_{CK(AVG)} = t_{AA,max} / CL$  SELECTED and round the resulting  $t_{CK(AVG)}$  down to the next valid speed bin (i.e. 3.0ns, 2.5ns, 1.875ns, 1.5ns, or 1.25ns). This result is  $t_{CK(AVG)max}$  corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. In order to support down binning to CL=7 and CL=9,  $t_{AA}/t_{RCD}/t_{RPmin}$  must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1600-11-11-11 devices supporting down binning to DDR3-1333-9-9-9 or DDR3-1066-7-7-7 should program 13.125 ns in SPD bytes for  $t_{AAmin}$  (Byte16),  $t_{RCDmin}$  (Byte 18), and  $t_{RPmin}$  (Byte 20). Once  $t_{RP}$  (Byte 20) is programmed to 13.125ns,  $t_{RCmin}$  (Bytes 21 & 23) also should be programmed accordingly ( $t_{RASmin} + t_{RPmin} = 35 \text{ ns} + 13.125 \text{ ns} = 48.125ns$ ).
7. DDR3-800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.

**Device Timing Parameters by Speed Bin**

Parameter	Symbol	DDR3L-1600		Units	Notes
		Min	Max		
<b>Clock Timing</b>					
Minimum clock cycle time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	$t_{CK}$	6
Average clock period	$t_{CK(avg)}$	Refer to Speed Bin on page 22.		ps	
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	$t_{CK(avg)}$	
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	$t_{CK(avg)}$	
Absolute clock period	$t_{CK(abs)}$	$t_{CK(avg)min} + t_{JIT(per)min}$	$t_{CK(avg)max} + t_{JIT(per)max}$	ps	
Absolute clock high pulse width	$t_{CH(abs)}$	0.43	-	$t_{CK(avg)}$	25
Absolute clock low pulse width	$t_{CL(abs)}$	0.43	-	$t_{CK(avg)}$	26
Clock period jitter	$t_{JIT(per)}$	-70	70	ps	
Clock period jitter during DLL locking period	$t_{JIT(per, lck)}$	-60	60	ps	
Cycle to cycle period jitter	$t_{JIT(CC)}$	140		ps	
Cycle to cycle period jitter during DLL locking period	$t_{JIT(CC, lck)}$	120		ps	
Duty cycle jitter	$t_{JIT(duty)}$	-	-	ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	-103	103	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	-122	122	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	-136	136	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	-147	147	ps	
Cumulative error across 6 cycles	$t_{ERR(6per)}$	-155	155	ps	
Cumulative error across 7 cycles	$t_{ERR(7per)}$	-163	163	ps	
Cumulative error across 8 cycles	$t_{ERR(8per)}$	-169	169	ps	
Cumulative error across 9 cycles	$t_{ERR(9per)}$	-175	175	ps	
Cumulative error across 10 cycles	$t_{ERR(10per)}$	-180	180	ps	
Cumulative error across 11 cycles	$t_{ERR(11per)}$	-184	184	ps	
Cumulative error across 12 cycles	$t_{ERR(12per)}$	-188	188	ps	
Cumulative error across n = 13-50 cycles	$t_{ERR(nper)}$	$t_{ERR(nper)min} = (1 + 0.68\ln(n)) * t_{JIT(per)min}$ $t_{ERR(nper)max} = (1 + 0.68\ln(n)) * t_{JIT(per)max}$		ps	24



**Device Timing Parameters by Speed Bin (Continued)**

Parameter	Symbol	DDR3L-1600		Units	Notes
		Min	Max		
<b>Data Timing</b>					
DQS, $\overline{\text{DQS}}$ to DQ skew, per group, per access	$t_{\text{DQSQ}}$	-	100	ps	13
DQ output hold time from DQS, $\overline{\text{DQS}}$	$t_{\text{QH}}$	0.38	-	$t_{\text{CK(avg)}}$	13, b
DQ low-impedance from CK, $\overline{\text{CK}}$	$t_{\text{LZ(DQ)}}$	-450	225	ps	13, 14, a
DQ high-impedance from CK, $\overline{\text{CK}}$	$t_{\text{HZ(DQ)}}$	-	225	ps	13, 14, a
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to $V_{\text{IH(AC)}} / V_{\text{IL(AC)}}$ levels	1.35V $t_{\text{DS(base) AC160}}$	-	-	ps	17, d
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to $V_{\text{IH(AC)}} / V_{\text{IL(AC)}}$ levels	1.35V $t_{\text{DS(base) AC135}}$	25	-	ps	17, 27, d
Data hold time from DQS, $\overline{\text{DQS}}$ referenced to $V_{\text{IH(DC)}} / V_{\text{IL(DC)}}$ levels	1.35V $t_{\text{DH(base) DC90}}$	55	-	ps	17, d
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to $V_{\text{IH(AC)}} / V_{\text{IL(AC)}}$ levels	1.5V $t_{\text{DS(base) AC175}}$	-	-	ps	17, d
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to $V_{\text{IH(AC)}} / V_{\text{IL(AC)}}$ levels	1.5V $t_{\text{DS(base) AC150}}$	10	-	ps	17, 27, d
Data hold time from DQS, $\overline{\text{DQS}}$ referenced to $V_{\text{IH(DC)}} / V_{\text{IL(DC)}}$ levels	1.5V $t_{\text{DH(base) DC100}}$	45	-	ps	17, d
DQ and DM input pulse width for each input	$t_{\text{DIPW}}$	360	-	ps	28
<b>Data Strobe Timing</b>					
DQS, $\overline{\text{DQS}}$ differential READ preamble	$t_{\text{RPRE}}$	0.9	Note 19	$t_{\text{CK(avg)}}$	13, 19, b
DQS, $\overline{\text{DQS}}$ differential READ postamble	$t_{\text{RPST}}$	0.3	Note 11	$t_{\text{CK(avg)}}$	11, 13, b
DQS, $\overline{\text{DQS}}$ differential output high time	$t_{\text{QSH}}$	0.4	-	$t_{\text{CK(avg)}}$	13, b
DQS, $\overline{\text{DQS}}$ differential output low time	$t_{\text{QSL}}$	0.4	-	$t_{\text{CK(avg)}}$	13, b
DQS, $\overline{\text{DQS}}$ differential WRITE preamble	$t_{\text{WPRE}}$	0.9	-	$t_{\text{CK(avg)}}$	
DQS, $\overline{\text{DQS}}$ differential WRITE postamble	$t_{\text{WPST}}$	0.3	-	$t_{\text{CK(avg)}}$	
DQS, $\overline{\text{DQS}}$ rising edge output access time from rising CK, $\overline{\text{CK}}$	$t_{\text{DQSCK}}$	-225	225	ps	13, a
DQS and $\overline{\text{DQS}}$ low-impedance time (Referenced from RL - 1)	$t_{\text{LZ(DQS)}}$	-450	225	ps	13, 14, a
DQS and $\overline{\text{DQS}}$ low-impedance time (Referenced from RL + BL / 2)	$t_{\text{HZ(DQS)}}$	-	225	ps	13, 14, a

**Device Timing Parameters by Speed Bin (Continued)**

Parameter	Symbol	DDR3L-1600		Units	Notes
		Min	Max		
DQS, $\overline{\text{DQS}}$ differential input low pulse width	$t_{\text{DQSL}}$	0.45	0.55	$t_{\text{CK(avg)}}$	
DQS, $\overline{\text{DQS}}$ differential input high pulse width	$t_{\text{DQSH}}$	0.45	0.55	$t_{\text{CK(avg)}}$	
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	$t_{\text{DQSS}}$	-0.27	0.27	$t_{\text{CK(avg)}}$	c
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	$t_{\text{DSS}}$	0.18	-	$t_{\text{CK(avg)}}$	c
DQS, $\overline{\text{DQS}}$ falling edge hold time from CK, $\overline{\text{CK}}$ rising edge	$t_{\text{DSH}}$	0.18	-	$t_{\text{CK(avg)}}$	c
<b>Command and Address Timing</b>					
DLL locking time	$t_{\text{DLLK}}$	512	-	nCK	
Internal READ command to PRECHARGE command delay	$t_{\text{RTP}}$	max (4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal READ command	$t_{\text{WTR}}$	max (4nCK, 7.5ns)	-		18, e
WRITE recovery time	$t_{\text{WR}}$	15	-	ns	e
Mode Register Set command cycle time	$t_{\text{MRD}}$	4	-	nCK	
Mode Register Set command update delay	$t_{\text{MOD}}$	max (12nCK, 15ns)	-		
ACT to internal read or write delay time	$t_{\text{RCD}}$	Refer to Speed Bin on page 22.			e
PRECHARGE command period	$t_{\text{RP}}$	Refer to Speed Bin on page 22.			e
ACT to ACT or REF command period	$t_{\text{RC}}$	Refer to Speed Bin on page 22.			e
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	$t_{\text{CCD}}$	4	-	nCK	
Auto-precharge write recovery + precharge time	$t_{\text{DAL(min)}}$	WR + roundup ( $t_{\text{RP}} / t_{\text{CK(avg)}}$ )		nCK	
Multi-purpose register recovery time	$t_{\text{MPRR}}$	1	-	nCK	22
ACTIVE to PRECHARGE command period	$t_{\text{RAS}}$	Refer to Speed Bin on page 22.			e
ACTIVE to ACTIVE command period for 1KB page size	$t_{\text{RRD}}$	max (4nCK, 6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	$t_{\text{RRD}}$	max (4nCK, 7.5ns)	-		e
Four activate window for 1KB page size	$t_{\text{FAW}}$	30	-	ns	e
Four activate window for 2KB page size	$t_{\text{FAW}}$	40	-	ns	e



**Device Timing Parameters by Speed Bin (Continued)**

Parameter	Symbol	DDR3L-1600		Units	Notes	
		Min	Max			
Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	1.35V	$t_{IS(base)}$ AC160	60	-	ps	16, b
Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	1.35V	$t_{IS(base)}$ AC135	185	-	ps	16, b
Command and Address hold time to CK, $\overline{CK}$ referenced to $V_{IH(DC)}$ / $V_{IL(DC)}$ levels	1.35V	$t_{IS(base)}$ DC90	130	-	ps	16, b
Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	1.5V	$t_{IS(base)}$ AC175	45	-	ps	16, b
Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	1.5V	$t_{IS(base)}$ AC150	170	-	ps	16, b
Command and Address hold time to CK, $\overline{CK}$ referenced to $V_{IH(DC)}$ / $V_{IL(DC)}$ levels	1.5V	$t_{IS(base)}$ DC100	120	-	ps	16, b
Control and Address input pulse width for each input		$t_{IPW}$	560	-	ps	28
<b>Calibration Timing</b>						
Power-up and RESET calibration time		$t_{ZQinit}$	max (512nCK, 640ns)	-		
Normal operation Full calibration time		$t_{ZQoper}$	max (256nCK, 320ns)	-		
Normal operation Short calibration time		$t_{ZQCS}$	max (64nCK, 80ns)	-		23
<b>Reset Timing</b>						
Exit Reset from CKE HIGH to a valid command		$t_{XPR}$	max (5nCK, $t_{RFCmin} + 10ns$ )	-		
<b>Self Refresh Timing</b>						
Exit Self Refresh from to commands not requiring a locked DLL		$t_{XS}$	max (5nCK, $t_{RFCmin} + 10ns$ )	-		
Exit Self Refresh from to commands requiring a locked DLL		$t_{XSDLL}$	$t_{DLLKmin}$	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing		$t_{CKESR}$	$t_{CKEmin} + 1nCK$	-		

**Device Timing Parameters by Speed Bin (Continued)**

Parameter	Symbol	DDR3L-1600		Units	Notes
		Min	Max		
Valid clock requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	$t_{CKSRE}$	max (5nCK, 10ns)	-		
Valid clock requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	$t_{CKSRX}$	max (5nCK, 10ns)	-		
<b>Power Down Timing</b>					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	$t_{XP}$	max (3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	$t_{XPDLL}$	max (10nCK, 24ns)	-		2
CKE minimum pulse width	$t_{CKE}$	max (3nCK, 5ns)	-	nCK	
Command pass disable delay	$t_{CPDED}$	1	-	nCK	
Power Down Entry to Exit Timing	$t_{PD}$	$t_{CKEmin}$	$9 * t_{REFI}$		15
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	$t_{PRPDEN}$	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	$t_{RDPDEN}$	$RL + 4 + 1$	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRPDEN}$	$WL + 4 + (t_{WR} / t_{CK(avg)})$	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	$WL + 4 + WR + 1$	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	$t_{WRPDEN}$	$WL + 2 + (t_{WR} / t_{CK(avg)})$	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPDEN}$	$WL + 2 + WR + 1$	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	nCK	20, 21
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	$t_{MODmin}$	-		

**Device Timing Parameters by Speed Bin (Continued)**

Parameter	Symbol	DDR3L-1600		Units	Notes
		Min	Max		
<b>ODT Timing</b>					
ODT turn on latency	ODTLon	WL-2 = CWL + AL -2		nCK	
ODT turn off latency	ODTLoff	WL-2 = CWL + AL -2		nCK	
ODT high time without Write command or with Write command and BC4	ODTH4	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t <sub>AONPD</sub>	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t <sub>AOFPD</sub>	2	8.5	ns	
RTT turn-on	t <sub>AON</sub>	-225	225	ps	7, a
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t <sub>AOF</sub>	0.3	0.7	t <sub>CK(avg)</sub>	8, a
RTT dynamic change skew	t <sub>ADC</sub>	0.3	0.7	t <sub>CK(avg)</sub>	a
<b>Write Leveling Timing</b>					
First DQS/DQS rising edge after write leveling mode is programmed	t <sub>WLMRD</sub>	40	-	nCK	3
DQS/DQS delay after write leveling mode is programmed	t <sub>WLDQSEN</sub>	25	-	nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	t <sub>WLS</sub>	165	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t <sub>WLH</sub>	165	-	ps	
Write leveling output delay	t <sub>WLO</sub>	0	7.5	ns	
Write leveling output error	t <sub>WLOE</sub>	0	2	ns	

## Device Timing Parameters Notes

- Actual value dependant upon measurement level definitions. See "Device Operation & Timing Diagram Datasheet".
  - Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
  - The max values are system dependent.
  - WR as programmed in the Mode Register.
  - Value must be rounded-up to next higher integer value.
  - There is no maximum cycle time limit besides the need to satisfy the refresh interval,  $t_{REFI}$ .
  - For definition of RTT turn-on time  $t_{AON}$ , see "Device Operation & Timing Diagram Datasheet"
  - For definition of RTT turn-off time  $t_{AOF}$ , see "Device Operation & Timing Diagram Datasheet".
  - $t_{WR}$  is defined in ns, for calculation of  $t_{WRPDEN}$  it is necessary to round up  $t_{WR} / t_{CK}$  to the next integer.
  - WR is in clock cycles as programmed in MR0.
  - The maximum read postamble is bound by  $t_{DQSCk}(min)$  plus  $t_{QSH}(min)$  on the left side and  $t_{HZ(DQS)max}$  on the right side. See "Device Operation & Timing Diagram Datasheet".
  - Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by Jitter Notes on page 31.
  - Value is only valid for RON34.
  - Single ended signal parameter.
  - $t_{REFI}$  depends on  $T_{OPER}$ .
  - $t_{IS(base)}$  and  $t_{IH(base)}$  values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK,  $\overline{CK}$  differential slew rate. Note for DQ and DM signals,  $V_{REF(DC)} = V_{REFDQ(DC)}$ . For input only pins except  $\overline{RESET}$ ,  $V_{REF(DC)} = V_{REFCA(DC)}$ .
  - $t_{DS(base)}$  and  $t_{DH(base)}$  values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS,  $\overline{DQS}$  differential slew rate. Note for DQ and DM signals,  $V_{REF(DC)} = V_{REFDQ(DC)}$ . For input only pins except  $\overline{RESET}$ ,  $V_{REF(DC)} = V_{REFCA(DC)}$ .
  - Start of internal write transaction is defined as follows:  
 For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.  
 For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.  
 For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
  - The maximum read preamble is bound by  $t_{LZDQS}(min)$  on the left side and  $t_{DQSCk}(max)$  on the right side. See "Device Operation & Timing Diagram Datasheet".
  - CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
  - Although CKE is allowed to be registered LOW after a REFRESH command once  $t_{REFPDEN}(min)$  is satisfied, there are cases where additional time such as  $t_{XPDLL}(min)$  is also required. See "Device Operation & Timing Diagram Datasheet".
  - Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
  - One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.  
 One method for calculating the interval between ZQCS commands, given the temperature ( $Tdriftrate$ ) and voltage ( $Vdriftrate$ ) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:
- $$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$
- where  $TSens = \max(dRTTdT, dRONdTM)$  and  $VSens = \max(dRTTdV, dRONdVM)$  define the SDRAM temperature and voltage sensitivities.  
 For example, if  $TSens = 1.5\% / ^\circ C$ ,  $VSens = 0.15\% / mV$ ,  $Tdriftrate = 1 ^\circ C / sec$  and  $Vdriftrate = 15 mV / sec$ , then the interval between ZQCS commands is calculated as:
- $$\frac{0.5}{(1.5 \times 1) + (0.15 + 15)} = 0.133 \approx 128ms$$
- $n =$  from 13 cycles to 50 cycles. This row defines 38 parameters.
  - $t_{CH(abs)}$  is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
  - $t_{CL(abs)}$  is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
  - The  $t_{IS(base)}$  AC150 specifications are adjusted from the  $t_{IS(base)}$  specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175mv - 150mV) / 1 V/ns].
  - Pulse width of a input signal is defined as the width between the first crossing of  $V_{REFDC}$  and the consecutive crossing of  $V_{REFDC}$ .

29.  $t_{DQSL}$  describes the instantaneous differential input low pulse width on  $\overline{DQS-DQS}$ , as measured from one falling edge to the next consecutive rising edge.
30.  $t_{DQSH}$  describes the instantaneous differential input high pulse width on  $\overline{DQS-DQS}$ , as measured from one rising edge to the next consecutive falling edge.
31.  $t_{DQSH, act} + t_{DQSL, act} = 1 t_{CK, act}$ ; with  $t_{XYZ, act}$  being the actual measured value of the respective timing parameter in the application.
32.  $t_{DSH, act} + t_{DSS, act} = 1 t_{CK, act}$ ; with  $t_{XYZ, act}$  being the actual measured value of the respective timing parameter in the application.

## Jitter Notes

- a. Unit ' $t_{CK(avg)}$ ' represents the actual  $t_{CK(avg)}$  of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. (ex)  $t_{MRD} = 4 [nCK]$  means; if one Mode Register Set command is registered at  $T_m$ , another Mode Register Set command may be registered at  $T_{m+4}$ , even if  $(T_{m+4} - T_m)$  is  $4 \times t_{CK(avg)} + t_{ERR(4per), min}$ .
- b. These parameters are measured from a command/address signal ( $\overline{CKE}$ ,  $\overline{CS}$ ,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ , ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT(per)}$ ,  $t_{JIT(cc)}$ , etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- c. These parameters are measured from a data strobe signal (DQS,  $\overline{DQS}$ ) crossing to its respective clock signal (CK,  $\overline{CK}$ ) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT(per)}$ ,  $t_{JIT(cc)}$ , etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- d. These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal ( $\overline{DQS}$ ,  $\overline{DQS}$ ) crossing.
- e. For these parameters, the DDR3 SDRAM device supports  $t_{nPARAM} [nCK] = RU \{t_{PARAM} [ns] / t_{CK(avg)} [ns]\}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support  $t_{nRP} = RU \{t_{RP} / t_{CK(avg)}\}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which  $t_{RP} = 15ns$ , the device will support  $t_{nRP} = RU \{t_{RP} / t_{CK(avg)}\} = 6$ , as long as the input clock jitter specifications are met, i.e. Precharge command at  $T_m$  and Active command at  $T_{m+6}$  is valid even if  $(T_{m+6} - T_m)$  is less than 15ns due to input clock jitter.
- f. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{ERR(mper), act}$  of the input clock, where  $2 \leq m \leq 12$ . (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{ERR(mper), act, min} = -172 ps$  and  $t_{ERR(mper), act, max} = +193 ps$ , then  $t_{DQSCK, min(derated)} = t_{DQSCK, min} - t_{ERR(mper), act, max} = -400 ps - 193 ps = -593 ps$  and  $t_{DQSCK, max(derated)} = t_{DQSCK, max} - t_{ERR(mper), act, min} = 400 ps + 172 ps = +572 ps$ . Similarly,  $t_{LZ(DQ)}$  for DDR3-800 derates to  $t_{LZ(DQ), min(derated)} = -800 ps - 193 ps = -993 ps$  and  $t_{LZ(DQ), max(derated)} = 400 ps + 172 ps = +572 ps$ . (Caution on the min/max usage!) Note that  $t_{ERR(mper), act, min}$  is the minimum measured value of  $t_{ERR(nper)}$  where  $2 \leq n \leq 12$ , and  $t_{ERR(mper), act, max}$  is the maximum measured value of  $t_{ERR(nper)}$  where  $2 \leq n \leq 12$ .
- g. When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT(per), act}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has  $t_{CK(avg), act} = 2500 ps$ ,  $t_{JIT(per), act, min} = -72 ps$  and  $t_{JIT(per), act, max} = +93 ps$ , then  $t_{RPRE, min(derated)} = t_{RPRE, min} + n t_{JIT(per), act, min} = 0.9 \times t_{CK(avg), act} + t_{JIT(per), act, min} = 0.9 \times 2500 ps - 72 ps = +2178 ps$ . Similarly,  $t_{QH, min(derated)} = t_{QH, min} + t_{JIT(per), act, min} = 0.38 \times t_{CK(avg), act} + t_{JIT(per), act, min} = 0.38 \times 2500 ps - 72 ps = +878 ps$ . (Caution on the min/max usage!)

## IDD and IDDQ Measurement-Loop Patterns Timing

Speed Bin		DDR3L-1600	Units
Parameter		11-11-11	
t <sub>CKmin</sub> (IDD)		1.25	ns
CL(IDD)		11	nCK
nRCD		11	nCK
nRC		39	nCK
nRAS		28	nCK
nRP		11	nCK
nFAW	1KB page size	24	nCK
nFAW	2KB page size	32	nCK
nRRD	1KB page size	5	nCK
nRRD	2KB page size	6	nCK
nRFC		208	nCK

## Definitions for IDD Measurement Conditions

- “0” and “LOW” is defined as  $V_{IN} \leq V_{ILAC(max)}$ .
- “1” and “HIGH” is defined as  $V_{IN} \geq V_{IHAC(min)}$ .
- “MID-LEVEL” is defined as inputs that are  $V_{REF} = V_{DD}/2$ .
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in IDD and IDDQ Measurement-Loop Patterns Timing above.
- Basic IDD and IDDQ Measurement Conditions are described in IDD Measurement Conditions on pages 33-34.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in IDD Measurement-Loop Patterns on pages 36-41.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting:
  - RON = RZQ/7 (34 Ohm in MR1);
  - Qoff = 0<sub>B</sub> (Output Buffer enabled in MR1);
  - RTT\_Nom = RZQ/6 (40 Ohm in MR1);
  - RTT\_Wr = RZQ/2 (120 Ohm in MR2);
  - TDQS Feature disabled in MR1.
- **Attention:** The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define  $\underline{D} = \{\underline{CS}, \underline{RAS}, \underline{CAS}, \underline{WE}\} = \{\text{HIGH}, \text{LOW}, \text{LOW}, \text{LOW}\}$
- Define  $\underline{D} = \{\underline{CS}, \underline{RAS}, \underline{CAS}, \underline{WE}\} = \{\text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}\}$





**IDD Measurement Conditions**

Symbol	Description	Conditions
$I_{DD0}$	Operating One Bank Active-Precharge Current	CKE: High; External clock: On; $t_{CK}$ , nRC, nRAS, CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to IDD0 Measurement-Loop Pattern on page 36; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (See IDD0 Measurement-Loop Pattern on page 36); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD0 Measurement-Loop Pattern on page 36.
$I_{DD1}$	Operating One Bank Active-Read-Precharge Current	CKE: High; External clock: On; $t_{CK}$ , nRC, nRAS, nRCD, CL: See IDD and IDDQ Timings on page 32; BL: $8^1, 6$ ; AL: 0; $\overline{CS}$ : High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data I/O: partially toggling according to IDD1 Measurement-Loop Pattern on page 37; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (See IDD1 Measurement-Loop Pattern on page 37); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD1 Measurement-Loop Pattern on page 37.
$I_{DD2P0}$	Precharge Power-Down Current Slow Exit	CKE: Low; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit <sup>3</sup> .
$I_{DD2P1}$	Precharge Power-Down Current Fast Exit	CKE: Low; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit <sup>3</sup> .
$I_{DD2N}$	Precharge Standby Current	CKE: High; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to IDD2N and IDD3N Measurement-Loop Pattern on page 38; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD2N and IDD3N Measurement-Loop Pattern on page 38.
$I_{DD2Q}$	Precharge Quiet Standby Current	CKE: High; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0.



**IDD Measurement Conditions (Continued)**

Symbol	Description	Conditions
$I_{DD3P}$	Active Power Down Current	CKE: Low; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0.
$I_{DD3N}$	Active Standby Current	CKE: High; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to IDD2N and IDD3N Measurement-Loop Pattern on page 38; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD2N and IDD3N Measurement-Loop Pattern on page 38.
$I_{DD4R}$	Operating Burst Read Current	CKE: High; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1, 6$ ; AL: 0; $\overline{CS}$ : High between RD; Command, Address, Bank Address Inputs: partially toggling according to IDD4R Measurement-Loop Pattern on page 39; Data I/O: seamless read data burst with different data between one burst and the next one according to IDD4R Measurement-Loop Pattern on page 39; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (See IDD4R Measurement-Loop Pattern on page 39); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD4R Measurement-Loop Pattern on page 39.
$I_{DD4W}$	Operating Burst Write Current	CKE: High; External clock: On; $t_{CK}$ , CL: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : High between WR; Command, Address, Bank Address Inputs: partially toggling according to IDD4W Measurement-Loop Pattern on page 39; Data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern on page 39; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (See IDD4W Measurement-Loop Pattern on page 39); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at HIGH; Pattern Details: See IDD4W Measurement-Loop Pattern on page 39.
$I_{DD5B}$	Burst Refresh Current	CKE: High; External clock: On; $t_{CK}$ , CL, nRFC: See IDD and IDDQ Timings on page 32; BL: $8^1$ ; AL: 0; $\overline{CS}$ : High between REF; Command, Address, Bank Address Inputs: partially toggling according to IDD5B Measurement-Loop Pattern on page 40; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nRFC (See IDD5B Measurement-Loop Pattern on page 40); Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD5B Measurement-Loop Pattern on page 40.



**IDD Measurement Conditions (Continued)**

Symbol	Description	Conditions
$I_{DD6}$	Self-Refresh Current: Normal Temperature Range	$T_{CASE}$ : 0 °C - 85 °C; Auto Self-Refresh (ASR): Disabled <sup>4</sup> ; Self-Refresh Temperature Range (SRT): Normal <sup>5</sup> ; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: See IDD and IDDQ Timings on page 32; BL: 8 <sup>1</sup> ; AL: 0; $\overline{CS}$ , Command, Address, Bank Address, Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: MID-LEVEL.
$I_{DD7}$	All Bank Interleave Read Current	CKE: High; External clock: On; $t_{CK}$ , nRC, nRAS, nRCD, nRRD, nFAW, CL: See IDD and IDDQ Timings on page 32; BL: 8 <sup>1, 6</sup> ; AL: CL-1; $\overline{CS}$ : High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to IDD7 Measurement-Loop Pattern on pages 40-41; Data I/O: read data bursts with different data between one burst and the next one according to IDD7 Measurement-Loop Pattern on pages 40-41; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, See IDD7 Measurement-Loop Pattern on pages 40-41; Output Buffer and RTT: Enabled in Mode Registers <sup>2</sup> ; ODT Signal: stable at 0; Pattern Details: See IDD7 Measurement-Loop Pattern on pages 40-41.
$I_{DD8}$	$\overline{RESET}$ Low Current	$\overline{RESET}$ : Low; External clock: Off; CK and $\overline{CK}$ : Low; CKE: FLOATING; $\overline{CS}$ , Command, Address, Bank Address, Data IO: FLOATING; ODT Signal: FLOATING; $\overline{RESET}$ Low current reading is valid once power is stable and $\overline{RESET}$ has been LOW for at least 1ms.

**Notes:**

- Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B.
- Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B; RTT\_Wr enable: set MR2 A[10,9] = 10B.
- Precharge Power Down Mode: set MR0 A[12] = 0B for Slow Exit or MR0 A[12]=1B for Fast Exit.
- Auto Self-Refresh (ASR): set MR2 A[6] = 0B to disable or 1B to enable feature.
- Self-Refresh Temperature Range (SRT): set MR2 A[7] = 0B for normal or 1B for extended temperature range.
- Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B.



**IDD Measurement Conditions (Continued)**

**IDD0 Measurement-Loop Pattern<sup>1</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>			
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-			
			1, 2	D, D	1	0	0	0	0	0	0	00	0	0	0	0	-		
			3, 4	D, D	1	1	1	1	0	0	0	00	0	0	0	0	-		
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if necessary															
			nRAS	PRE	0	0	1	0	0	0	0	00	0	0	0	0	-		
			...	Repeat pattern 1-4 until nRC - 1. Truncate if necessary															
			1*nRC + 0	ACT	0	0	1	1	0	0	0	00	0	0	F	0	-		
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	00	0	0	F	0	-		
			1*nRC + 3, 4	D, D	1	1	1	1	0	0	0	00	0	0	F	0	-		
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRAS - 1. Truncate if necessary															
			1*nRC + nRAS	PRE	0	0	1	0	0	0	0	00	0	0	F	0	-		
			...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if necessary															
			1	2*nRC	Repeat Sub-Loop 0, but BA[2:0] = 1														
			2	4*nRC	Repeat Sub-Loop 0, but BA[2:0] = 2														
3	6*nRC	Repeat Sub-Loop 0, but BA[2:0] = 3																	
4	8*nRC	Repeat Sub-Loop 0, but BA[2:0] = 4																	
5	10*nRC	Repeat Sub-Loop 0, but BA[2:0] = 5																	
6	12*nRC	Repeat Sub-Loop 0, but BA[2:0] = 6																	
7	14*nRC	Repeat Sub-Loop 0, but BA[2:0] = 7																	



**IDD Measurement Conditions (Continued)**

**IDD1 Measurement-Loop Pattern<sup>1</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>		
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-		
			1-2	D, D	1	0	0	0	0	0	0	00	0	0	0	0	-	
			3-4	D, D	1	1	1	1	0	0	0	00	0	0	0	0	-	
			...	Repeat pattern 1-4 until nRCD - 1. Truncate if necessary														
			nRCD	RD	0	1	0	1	0	0	0	0	00	0	0	0	0	00000000
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if necessary														
			nRAS	PRE	0	0	1	0	0	0	0	0	00	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if necessary														
			1*nRC + 0	ACT	0	0	1	1	0	0	0	0	00	0	0	F	0	-
			1*nRC + 1-2	D, D	1	0	0	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3-4	D, D	1	1	1	1	0	0	0	0	00	0	0	F	0	-
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRCD - 1. Truncate if necessary														
			1*nRC + nRCD	RD	0	1	0	1	0	0	0	0	00	0	0	F	0	00110011
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRAS - 1. Truncate if necessary														
		1*nRC + nRAS	PRE	0	0	1	0	0	0	0	0	00	0	0	F	0	-	
		...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if necessary															
		1	2*nRC	Repeat Sub-Loop 0, but BA[2:0] = 1														
		2	4*nRC	Repeat Sub-Loop 0, but BA[2:0] = 2														
		3	6*nRC	Repeat Sub-Loop 0, but BA[2:0] = 3														
		4	8*nRC	Repeat Sub-Loop 0, but BA[2:0] = 4														
		5	10*nRC	Repeat Sub-Loop 0, but BA[2:0] = 5														
		6	12*nRC	Repeat Sub-Loop 0, but BA[2:0] = 6														
		7	14*nRC	Repeat Sub-Loop 0, but BA[2:0] = 7														



**IDD Measurement Conditions (Continued)**

**IDD2N and IDD3N Measurement-Loop Pattern**

$\overline{\text{CK}}$ , $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>		
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-		
			1	D	1	0	0	0	0	0	0	00	0	0	0	0	-	
			2	D	1	1	1	1	1	0	0	00	0	0	F	0	-	
			3	D	1	1	1	1	1	0	0	00	0	0	F	0	-	
		1	4-7	Repeat Sub-Loop 0, but BA[2:0] = 1														
		2	8-11	Repeat Sub-Loop 0, but BA[2:0] = 2														
		3	12-15	Repeat Sub-Loop 0, but BA[2:0] = 3														
		4	16-19	Repeat Sub-Loop 0, but BA[2:0] = 4														
		5	20-23	Repeat Sub-Loop 0, but BA[2:0] = 5														
		6	24-27	Repeat Sub-Loop 0, but BA[2:0] = 6														
		7	28-31	Repeat Sub-Loop 0, but BA[2:0] = 7														



**IDD Measurement Conditions (Continued)**

**IDD4R Measurement-Loop Pattern<sup>1</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>	
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000	
			1	D	1	0	0	0	0	0	0	00	0	0	0	0	-
			2-3	D, D	1	1	1	1	0	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	00	0	0	F	0	-
			6-7	D, D	1	1	1	1	0	0	0	00	0	0	F	0	-
		1	8-15	Repeat Sub-Loop 0, but BA[2:0] = 1													
		2	16-23	Repeat Sub-Loop 0, but BA[2:0] = 2													
		3	24-31	Repeat Sub-Loop 0, but BA[2:0] = 3													
		4	32-39	Repeat Sub-Loop 0, but BA[2:0] = 4													
		5	40-47	Repeat Sub-Loop 0, but BA[2:0] = 5													
		6	48-55	Repeat Sub-Loop 0, but BA[2:0] = 6													
		7	56-63	Repeat Sub-Loop 0, but BA[2:0] = 7													

**IDD4W Measurement-Loop Pattern<sup>1</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>	
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000	
			1	D	1	0	0	0	1	0	00	0	0	0	0	-	
			2-3	D, D	1	1	1	1	1	0	0	00	0	0	0	0	-
			4	WR	0	1	0	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	1	0	00	0	0	F	0	-
			6-7	D, D	1	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	Repeat Sub-Loop 0, but BA[2:0] = 1													
		2	16-23	Repeat Sub-Loop 0, but BA[2:0] = 2													
		3	24-31	Repeat Sub-Loop 0, but BA[2:0] = 3													
		4	32-39	Repeat Sub-Loop 0, but BA[2:0] = 4													
		5	40-47	Repeat Sub-Loop 0, but BA[2:0] = 5													
		6	48-55	Repeat Sub-Loop 0, but BA[2:0] = 6													
		7	56-63	Repeat Sub-Loop 0, but BA[2:0] = 7													

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**IDD Measurement Conditions (Continued)**

**IDD5B Measurement-Loop Pattern<sup>1</sup>**

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>	
toggling	Static High	0	0	REF	0	0	0	1	0	0	00	0	0	0	0	-	
		1	1-2	D	1	0	0	0	0	0	0	00	0	0	0	0	-
			3-4	D	1	1	1	1	1	0	0	00	0	0	F	0	-
			5-8	Repeat cycles 1-4, but BA[2:0] = 1													
			9-12	Repeat cycles 1-4, but BA[2:0] = 2													
			13-16	Repeat cycles 1-4, but BA[2:0] = 3													
			17-20	Repeat cycles 1-4, but BA[2:0] = 4													
			21-24	Repeat cycles 1-4, but BA[2:0] = 5													
			25-28	Repeat cycles 1-4, but BA[2:0] = 6													
			29-32	Repeat cycles 1-4, but BA[2:0] = 7													
		2	33-nRFC - 1	Repeat Sub-Loop 1 until nRFC - 1. Truncate if necessary													

**IDD7 Measurement-Loop Pattern<sup>1</sup>**

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>	
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-	
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000	
			2	D	1	0	0	0	0	0	0	00	0	0	0	0	-
			...	Repeat above D Command until nRRD - 1													
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	F	0	0	00110011
			nRRD + 2	D	1	0	0	0	0	0	1	00	0	0	F	0	-
			...	Repeat above D Command until 2*nRRD - 1													
		2	2*nRRD	Repeat Sub-Loop 0, but BA[2:0] = 2													
		3	3*nRRD	Repeat Sub-Loop 1, but BA[2:0] = 3													
		4	4*nRRD	D	1	0	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary													
		5	nFAW	Repeat Sub-Loop 0, but BA[2:0] = 4													
6	nFAW + nRRD	Repeat Sub-Loop 1, but BA[2:0] = 5															





**IDD7 Measurement-Loop Pattern<sup>1</sup> (Continued)**

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	RAS	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data <sup>2</sup>		
toggling	Static High	7	nFAW + 2*nRRD	Repeat Sub-Loop 0, but BA[2:0] = 6														
		8	nFAW + 3*nRRD	Repeat Sub-Loop 1, but BA[2:0] = 7														
		9	nFAW + 4*nRRD	D	1	0	0	0	0	0	7	00	0	0	F	0	-	
				Assert and repeat above D Command until 2*nFAW - 1, if necessary														
		10	2*nFAW	ACT	0	0	1	1	0	0	0	00	0	0	F	0	-	
				2*nFAW + 1	RDA	0	1	0	1	0	0	0	00	1	0	F	0	00110011
				2*nFAW + 2	D	1	0	0	0	0	0	0	00	0	0	F	0	-
					Repeat above D Command until 2*nFAW + nRRD - 1													
		11	2*nFAW + nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	0	-	
				2*nFAW + nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000	
				2*nFAW + nRRD + 2	D	1	0	0	0	0	1	00	0	0	0	0	0	-
					Repeat above D Command until 2*nFAW + 2*nRRD - 1													
		12	2*nFAW + 2*nRRD	Repeat Sub-Loop 10, but BA[2:0] = 2														
		13	2*nFAW + 3*nRRD	Repeat Sub-Loop 11, but BA[2:0] = 3														
		14	2*nFAW + 4*nRRD	D	1	0	0	0	0	0	3	00	0	0	0	0	-	
				Assert and repeat above D Command until 3*nFAW - 1, if necessary														
		15	3*nFAW	Repeat Sub-Loop 10, but BA[2:0] = 4														
		16	3*nFAW + nRRD	Repeat Sub-Loop 11, but BA[2:0] = 5														
		17	3*nFAW + 2*nRRD	Repeat Sub-Loop 10, but BA[2:0] = 6														
18	3*nFAW + 3*nRRD	Repeat Sub-Loop 11, but BA[2:0] = 7																
19	3*nFAW + 4*nRRD	D	1	0	0	0	0	0	7	00	0	0	0	0	-			
		Assert and repeat above D Command until 4*nFAW - 1, if necessary																

**Notes:**

- DM must be driven LOW all the time. DQS,  $\overline{\text{DQS}}$  are used according to RD Commands, otherwise MID-LEVEL
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.



**IDD Specifications**

Parameter	PC3L-12800		Units
	11-11-11		
	1.35V	1.5V	
I <sub>DD0</sub>	200	230	mA
I <sub>DD1</sub>	280	320	mA
I <sub>DD2P0</sub>	60	90	mA
I <sub>DD2P1</sub>	60	90	mA
I <sub>DD2N</sub>	90	100	mA
I <sub>DD2Q</sub>	80	100	mA
I <sub>DD3P</sub>	80	90	mA
I <sub>DD3N</sub>	170	180	mA
I <sub>DD4R</sub>	510	570	mA
I <sub>DD4W</sub>	510	570	mA
I <sub>DD5B</sub>	1520	1600	mA
I <sub>DD6</sub>	100	120	mA
I <sub>DD7</sub>	970	1040	mA
I <sub>DD8</sub>	120	120	mA

**Notes:**

1. IDD values are calculated with non-active ranks (IDLE) in the IDD2N state.

### Input/Output Capacitance

Parameter	Symbol	PC3L-12800				Units	Notes
		1.35V		1.5V			
		Min	Max	Min	Max		
Input/output capacitance, (DQ, DM, DQS, $\overline{\text{DQS}}$ , TDQS, $\overline{\text{TDQS}}$ )	$C_{\text{IO}}$	1.4	2.2	1.4	2.3	pF	1, 2
Input/output capacitance delta, (DQ, DM, DQS, $\overline{\text{DQS}}$ , TDQS, $\overline{\text{TDQS}}$ )	$C_{\text{DIO}}$	-0.5	0.3	-0.5	0.3	pF	2, 10
Input/output capacitance delta, (DQS and $\overline{\text{DQS}}$ )	$C_{\text{DDQS}}$	0	0.15	0	0.15	pF	2, 4
Input capacitance, (CK and $\overline{\text{CK}}$ )	$C_{\text{CK}}$	6.4	11.2	6.4	11.2	pF	2
Input capacitance delta, (CK and $\overline{\text{CK}}$ )	$C_{\text{DCK}}$	0	1.2	0	1.2	pF	2, 3
Input capacitance, (ADD/CMD/CTRL input-only pins)	$C_{\text{I}}$	6	9.6	6	10.4	pF	2, 5
Input capacitance delta, (All ADD/CMD input-only pins)	$C_{\text{DI\_ADD\_CM}}_{\text{D}}$	-3.2	3.2	-3.2	3.2		2, 6, 7
Input capacitance delta, (All CTRL input-only pins)	$C_{\text{DI\_CTRL}}$	-3.2	1.6	-3.2	1.6	pF	2, 8, 9

**Notes:**

- Although the DM, TDQS and  $\overline{\text{TDQS}}$  pins have different functions, the loading matches DQ and DQS.
- This parameter is not subject to production test. It is verified by design and characterization.
- Absolute value of  $C_{\text{CK}} - C_{\overline{\text{CK}}}$ .
- Absolute value of  $C_{\text{IO}}(\text{DQS}) - C_{\text{IO}}(\overline{\text{DQS}})$ .
- $C_{\text{I}}$  applies to ODT,  $\overline{\text{CS}}$ , CKE, A0-A15, BA0-BA2,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ .
- $C_{\text{DI\_ADD\_CMD}}$  applies to A0-A15, BA0-BA2,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and  $\overline{\text{WE}}$ .
- $C_{\text{DI\_ADD\_CMD}} = C_{\text{I}}(\text{ADD\_CMD}) - 0.5 * (C_{\text{I}}(\text{CK}) + C_{\text{I}}(\overline{\text{CK}}))$ .
- $C_{\text{DI\_CTRL}}$  applies to ODT,  $\overline{\text{CS}}$  and CKE.
- $C_{\text{DI\_CTRL}} = C_{\text{I}}(\text{CTRL}) - 0.5 * (C_{\text{I}}(\text{CK}) + C_{\text{I}}(\overline{\text{CK}}))$ .
- $C_{\text{DIO}} = C_{\text{IO}}(\text{DQ,DM}) - 0.5 * (C_{\text{IO}}(\text{DQS}) + C_{\text{IO}}(\overline{\text{DQS}}))$ .

## Serial Presence Detect (SPD)

### Serial Presence Detect Table

Byte No.	Byte Description	Supported Value	Hex Value
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	0-116Byte / 256Byte / 176Byte	92h
1	SPD Revision	Version 1.2	12h
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0Bh
3	Key Byte / Module Type	Unbuffered SoDIMM	03h
4	SDRAM Density and Banks	4Gb 8banks	04h
5	SDRAM Addressing	Row: 16 / Column : 10	21h
6	Module Nominal Voltage VDD	1.35 and 1.5V	02h
7	Module Organization	1 Rank / x8	01h
8	Module Memory Bus Width	Non-ECC / 64bit	03h
9	Fine Timebase Dividend and Divisor	1ps	11h
10	Medium Timebase Dividend	1/8 (0.125ns)	01h
11	Medium Timebase Divisor	1/8 (0.125ns)	08h
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0Ah
13	Reserved	Reserved	00h
14	CAS Latencies Supported (LSB)	5 / 6 / 7 / 8 / 9 / 10 / 11	FEh
15	CAS Latencies Supported (MSB)	5 / 6 / 7 / 8 / 9 / 10 / 11	00h
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69h
17	Minimum Write Recovery Time (tWRmin)	15ns	78h
18	Minimum RAS# to CAS# Delat Time (tRCDmin)	13.125ns	69h
19	Minimum Row Active to Row Active Delay Time (tRRD-min)	6ns	30h
20	Minimum Row Precharge Delay Time (tRPmin)	13.125ns	69h
21	Upper Nibbles for tRASmin and tRCmin	-	11h
22	Minimum Active to Precharge Delay Time (tRASmin) (LSB)	35ns	18h
23	Minimum Active to Active/Refresh Delay Time (tRCmin) (LSB)	48.125ns	81h
24	Minimum Refresh Recovery Delay Time (tRFCmin) (LSB)	260ns	20h
25	Minimum Refresh Recovery Delay Time (tRFCmin) (MSB)	260ns	08h

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Byte No.	Byte Description	Supported Value	Hex Value
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns	3Ch
27	Minimum Internal Read to Precharge Command Delay (tRTPmin)	7.5ns	3Ch
28	Upper Nibbles for tFAWmin	30ns	00h
29	Minimum four Active window delay (tFAWmin) (LSB)	30ns	F0h
30	SDRAM Output Drivers supported	DLL off Mode / RZQ/6 / RZQ/7	83h
31	SDRAM Thermal and Refresh Options	No ODTS / No ASR	01h
32	Module Thermal Sensor	without TS	00h
33	SDRAM Device Type	Standard Monolithic	00h
34	Fine Offset for SDRAM Minimum Cycle Time (tCKmin)	1.25ns	00h
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	13.125ns	00h
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns	00h
37	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	13.125ns	00h
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	48.125ns	00h
39-40	Reserved	Reserved	00h
41	SDRAM Maximum Activate Count (MAC) Value	Unlimited MAC_pTRR Compliant	88h
42-59	Reserved	Reserved	00h
60	Module Nominal Height	30mm / R/C B 4.0	2Fh
61	Module Maximum Thickness	Planar Double sides	11h
62	Reference Raw Card Used	R/C B / 4.0 (compatible to 2.0)	41h
63	Address Mapping from Edge Connector to DRAM	Standard	00h
64-116	Reserved	-	00h
117	Module Manufacturer ID Code (LSB)	Samsung	80h
118	Module Manufacturer ID Code (MSB)	Samsung	CEh
119	Module ID: Module Manufacturing Location	Onyang Korea	01h
120	Module ID: Module Manufacturing Date (Year)	-	00h
121	Module ID: Module Manufacturing Date (Week)	-	00h

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Byte No.	Byte Description	Supported Value	Hex Value
122-125	Module ID: Module Serial Number	-	00h
126	Cyclical Redundancy Code		FFh
127	Cyclical Redundancy Code		43h
128	Module Part Number	M	4Dh
129	Module Part Number	4	34h
130	Module Part Number	7	37h
131	Module Part Number	1	31h
132	Module Part Number	B	42h
133	Module Part Number	5	35h
134	Module Part Number	1	31h
135	Module Part Number	7	37h
136	Module Part Number	3	33h
137	Module Part Number	E-die	45h
138	Module Part Number	B	42h
139	Module Part Number	0	30h
140	Module Part Number	-	2Dh
141	Module Part Number	Y	59h
142	Module Part Number	K	4Bh
143	Module Part Number	0	30h
144	Module Part Number	Blank	20h
145	Module Part Number	Blank	20h
146-147	Module Revision Code	-	00h
148	SDRAM Manufacturer's JEDEC ID Code (LSB)	Samsung	80h
149	SDRAM Manufacturer's JEDEC ID Code (MSB)	Samsung	CEh
150-175	Manufacturer's Specific Data	-	00h
176-255	Open for Customer Use	-	00h

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