SH57K11

Preliminary

High Performance Codec with controller

Features

- Up to 24 MHz operating frequency
- Power Down Mode provided
- 2 Channel Codec
- SSDC

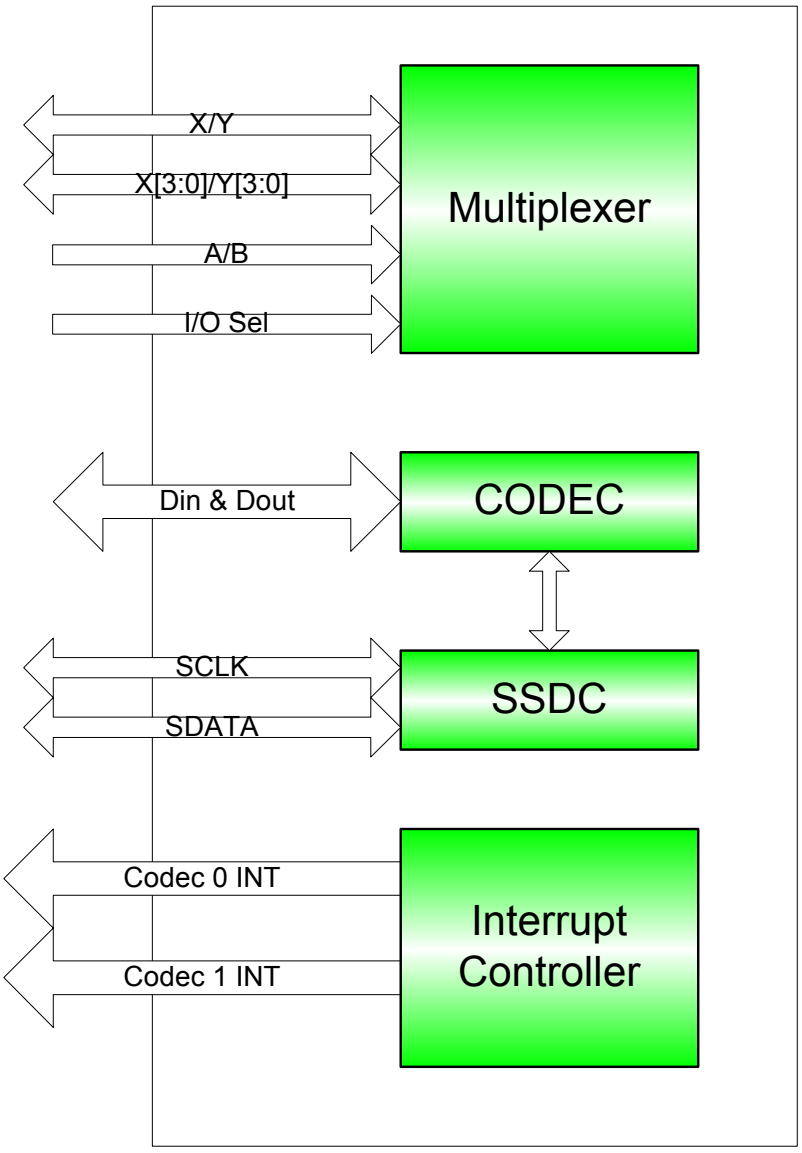
General Description

The SH57K11 is a low-voltage, high performance CODEC. The SH57K11 includes SSDC and CODEC controller.

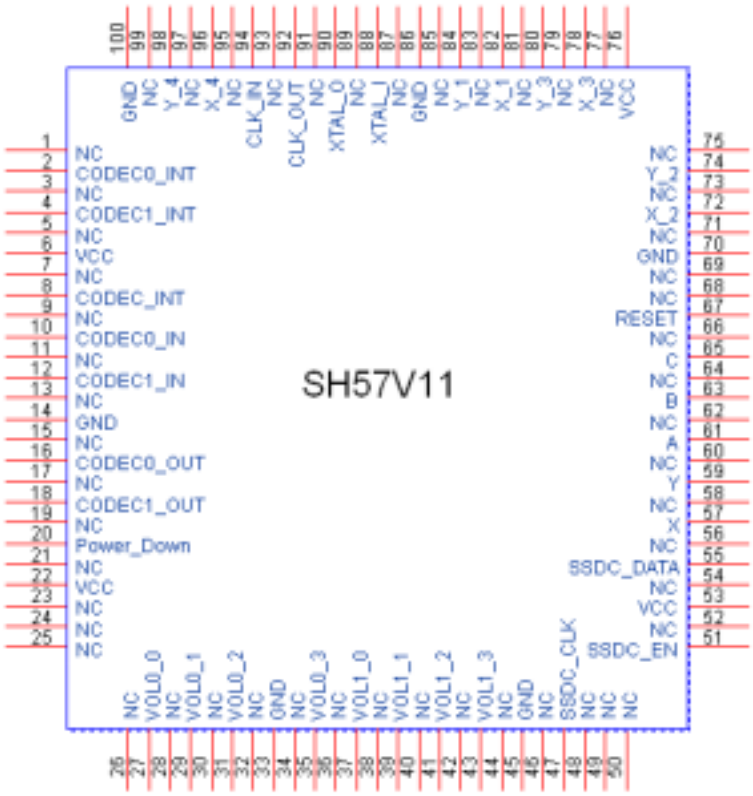
SH57K11 Feature Table

Item	SH57K11
SSDC	1set
Codec	2 channels
Volume Control	Yes
Interrupt Controller	Yes
Power	2.4V ~ 6V
Power Down Mode	Yes

Block Diagram



Pin Configuration



Pad Description

Pad No.	Designation	I/O	Description
1	NC	-	-
2	CODEC0_INT	O	CODEC 0 Interrupt flag
3	NC	-	-
4	CODEC1_INT	O	CODEC 1 Interrupt flag
5	NC	-	-
6	VCC	P	Power
7	NC	-	-
8	CODEC_INT	O	CODEC 0 and CODEC 1 Interrupt flag
9	NC	-	-
10	CODEC0_IN	I	CODEC 0 A/D input
11	NC	-	-
12	CODEC1_IN	I	CODEC 1 A/D input
13	NC	-	-
14	GND	P	GND
15	NC	-	-
16	CODEC0_OUT	O	CODEC 0 D/A output
17	NC	-	-
18	CODEC1_OUT	O	CODEC 1 D/A output
19	NC	-	-
20	Power_Down	I	1: Power Down Enable 0: Power Down Disable
21	NC	-	-
22	VCC	P	Power
23	NC	-	-
24	NC	-	-
25	NC	-	-
26	NC	-	-
27	VOL0_0	O	CODEC 0 Volume output
28	NC	-	-
29	VOL0_1	O	CODEC 0 Volume output
30	NC	-	-
31	VOL0_2	O	CODEC 0 Volume output
32	NC	-	-
33	GND	P	GND
34	NC	-	-
35	VOL0_3	O	CODEC 0 Volume output
36	NC	-	-

37	Vol1_0	O	CODEC 1 Volume output
38	NC	-	-
39	VOL1_1	O	CODEC 1 Volume output
40	NC	-	-
41	VOL1_2	O	CODEC 1 Volume output
42	NC	-	-
43	VOL1_2	O	CODEC 1 Volume output
44	NC	-	-
45	GND	P	GND
46	NC	-	-
47	SSDC_CLK	I	SSDC Clock Input
48	NC	-	-
49	NC	-	-
50	NC	-	-
51	SSDC_EN	I	SSDC Enable
52	NC	-	-
53	VCC	P	Power
54	NC	-	-
55	SSDC_DATA	I/O	SSDC Data
56	NC	-	-
57	X	I	Switch common input X
58	NC	-	-
59	Y	I/O	Switch common input/output Y
60	NC	-	-
61	A	I	Switch select A (B:A) 00: X_1, Y_1 (B:A) 10: X_3, Y_3
62	NC	-	-
63	B	I	Switch select B (B:A) 01: X_2, Y_2 (B:A) 11: X_4, Y_4
64	NC	-	-
65	C	I	Switch I/O select 0: output 1: input
66	NC	-	-
67	RESET	I	1: RESET 0: Active
68	NC	-	-
69	NC	-	-
70	GND	P	GND
71	NC	-	-
72	X_2	O	Switch common X output 2
73	NC	-	-
74	Y_2	I	Switch common Y input 2

75	NC	-	-
76	VCC	P	Power
77	NC	-	-
78	X_3	O	Switch common X output 3
79	NC	-	-
80	Y_3	O	Switch common Y output 3
81	NC	-	-
82	X_1	O	Switch common X output 3
83	NC	-	-
84	Y_1	I/O	Switch common Y I/O 3
85	NC	-	-
86	GND	P	GND
87	NC	-	-
88	XTAL_I	I	Crystal input
89	NC	-	-
90	XTAL_O	O	Crystal output
91	NC	-	-
92	CLK_OUT	O	CLOCK OUTPUT
93	NC	-	-
94	CLK_IN	I	System clock input
95	NC	-	-
96	X_4	O	Switch common X output 4
97	NC	-	-
98	Y_4	I/O	Switch common Y I/O 4
99	NC	-	-
100	GND	P	GND

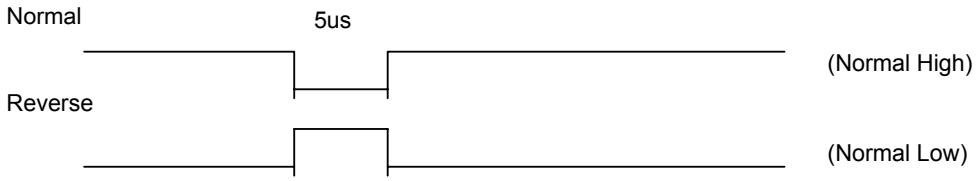
RAM Mapped System Register Summary

System Control Register											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00H	SYS_CTL	00	R/W	INV_INT1	INV_INT0	INV_INT	-	CLK_DIV	CLK_DIV	-	-
Volume Control Register											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
04H	VOL0_CTL	00H	R/W	VOL_EN	-	-	-	VOL_3	VOL_2	VOL_1	VOL_0
05H	VOL1_CTL	00H	R/W	VOL_EN	-	-	-	VOL_3	VOL_2	VOL_1	VOL_0
CODEC Control Register											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
06H	CODEC0_CTL	00H	R/W	-	-	SR_SEL1	SR_SEL0	BEEP_EN	CODECZ	RECB	START
07H	CODEC0_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
08H	CODEC0_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
09H	CODEC1_CTL	00H	R/W	-	-	SR_SEL1	SR_SEL0	BEEP_EN	CODECZ	RECB	START
0AH	CODEC1_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0BH	CODEC1_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

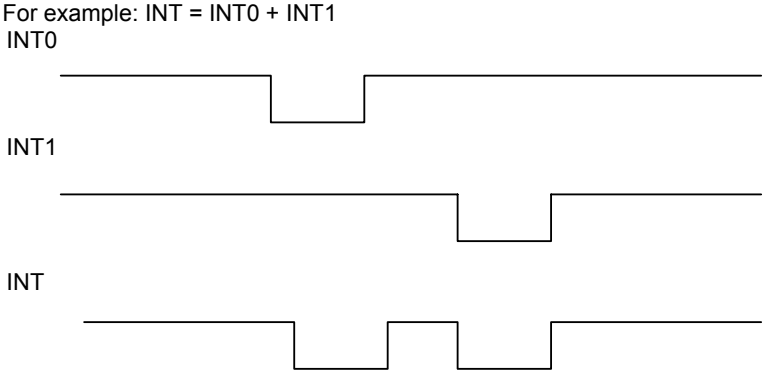
Note: Accessing these reserved control registers may cause some unexpected results. These registers are reserved for future usage.

SYS_CTL: System Control Register		
B7	INV_INT1	Reverse Codec1 interrupt. 1: Reverse
B6	INV_INT0	Reverse Codec0 interrupt. 1: Reverse
B5	INV_INT	Reverse Codec Interrupt. 1: Reverse
B3~B2	CLK_DIV1~0	Clock division rate 00: CLK/1 01: CLK/2 10: CLK/3 11: CLK/4

Interrupt Signal



Note: CODEC_INT is resulted by Codec0_INT or Codec1_INT.
For example: INT = INT0 + INT1



CODEC Controller

CODEC_CTL: CODEC Control Register		
B5~B4	SR_SEL1~0	Sampling rate selection
B3	BEEP_EN	1: enable beeper output; 0: disable beeper
B2	CODECZ	CODEC output enable
B1	RECB	0: record; 1: playback
B0	START	1: start sampling clock; 0: stop sampling clock

SR_SEL	Sampling rate selection
00	32K
01	64K
10	96K
11	128K

Volume Controller

The volume controller is to output to pin VOL3~VOL0. Setting VOL_EN will enable the volume controller.

Volume Control Register

VOL_CTL: Volume Control Register		
B7	VOL_EN	Set to 1 to enable volume controller
B3~0	VOL.3~0	Volume control bits 3~0

SSDC data format

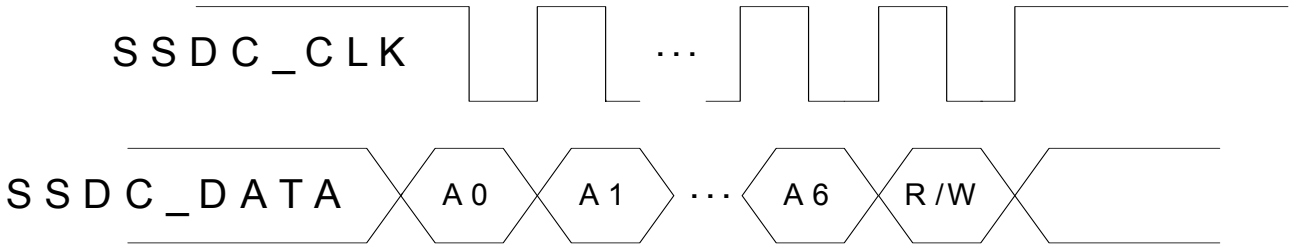
R/W	-	-	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

R/W: 1 = Write, 0 = Read
Address: please refer **RAM Mapped System Register Summary**

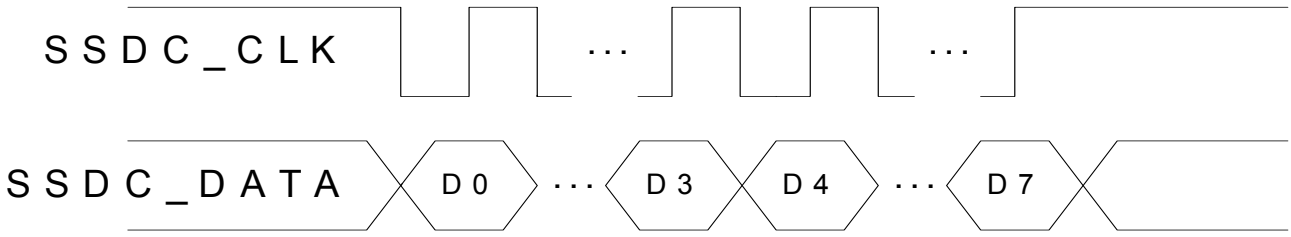
SSDC (Synchronous Serial Data Communication)

This is a Three-wire communication interface. It seems like standard 8051 UART mode 0 and SPI_CS mixed.

Receive Timing

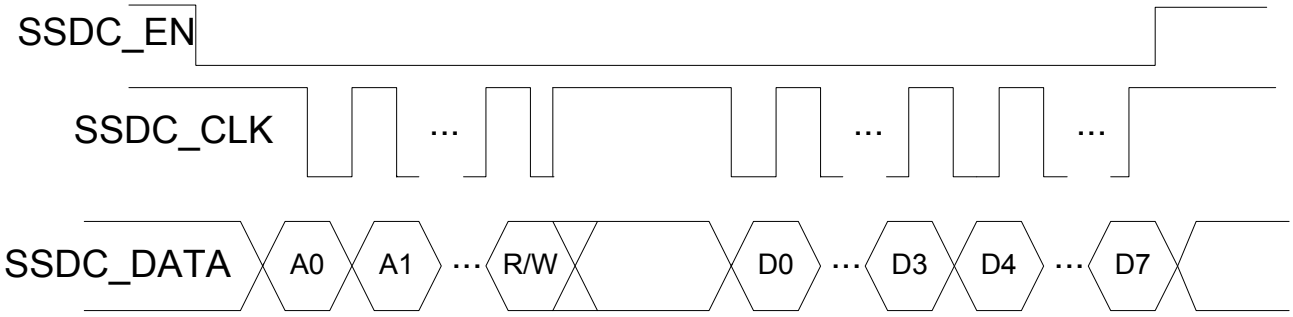


Transmit Timing

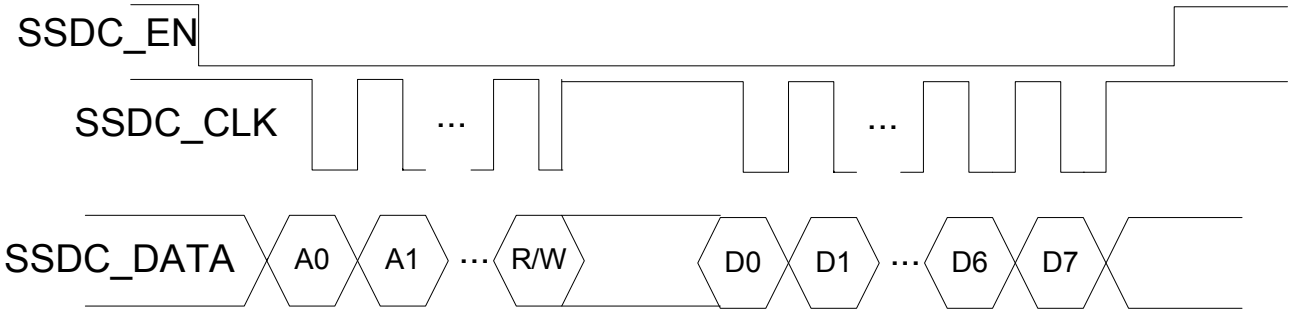


The full timing chart

When R/W = 0



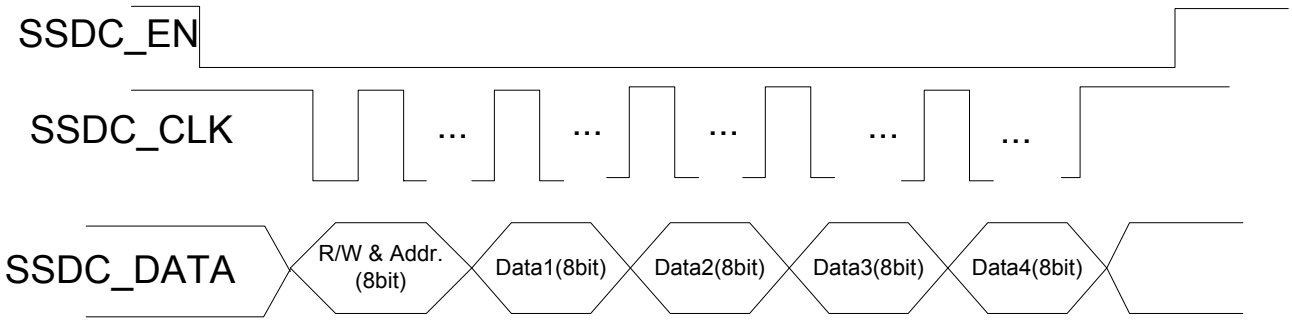
When R/W = 1



Codec Data Buffer

SSDC

When Addr. = (07H or 0AH)



Revision History

Version 0.1

- **General Description**

  The SH57K11 is a low-voltage, high performance CODEC. The SH57K11 includes a watchdog timer, 1-set SPI, 1-set SSDC and a CODEC controller.

- **System Controller**

- **Serial Peripheral Interface (SPI)**

- **SSDC (Synchronous Serial Data Communication)**

Version 0.2

Power	2.4V ~ 3.3V

- **Volume Controller**

  The volume controller is to output VOL.3~0 (B1H.3~0) to pin VOL3~VOL0. Setting VOL_EN will enable the volume controller.

- **System Controller**

B3~B2	CLK_DIV1~0	Clock division rate 00: CLK/2 01: CLK/4 10: CLK/6 11: CLK/12

Version 0.3

- **Pin Configuration**
- **Pad Description**

5	SPI_MISO	O	SPI data output
6	SPI_MOSI.	I	SPI data input

29	SSDC_EN	I	SSDC Enable 1: Disable 0: Enable
30	Power_down	I	1: Power Down Enable 0: Power Down Disable

- **RAM Mapped System Register Summary**

System Control Register											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00H	SYS_CTL	00	R/W	INV_INT1	INV_INT0	INV_INT	-	CLK_DIV	CLK_DIV	Power_Down	RESET

- **SSDC (Synchronous Serial Data Communication)**

  SSDC Timing chart relpenish

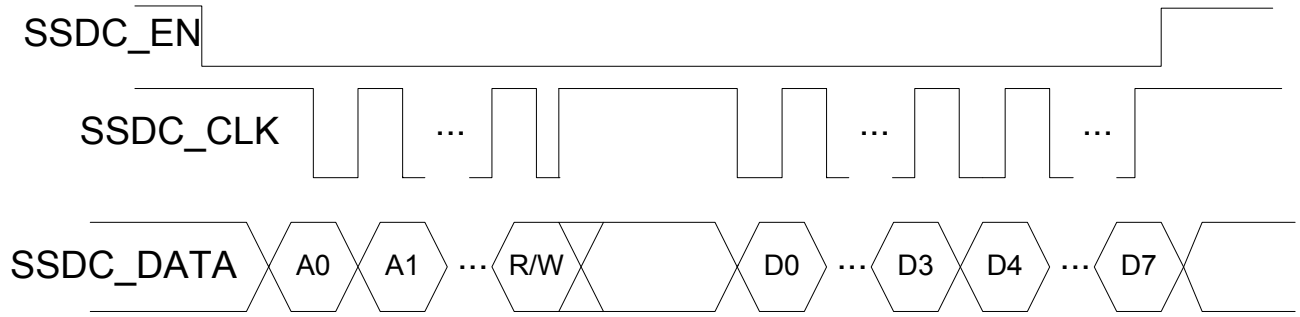
- **Feature Table**

Power	2.4V ~ 6V

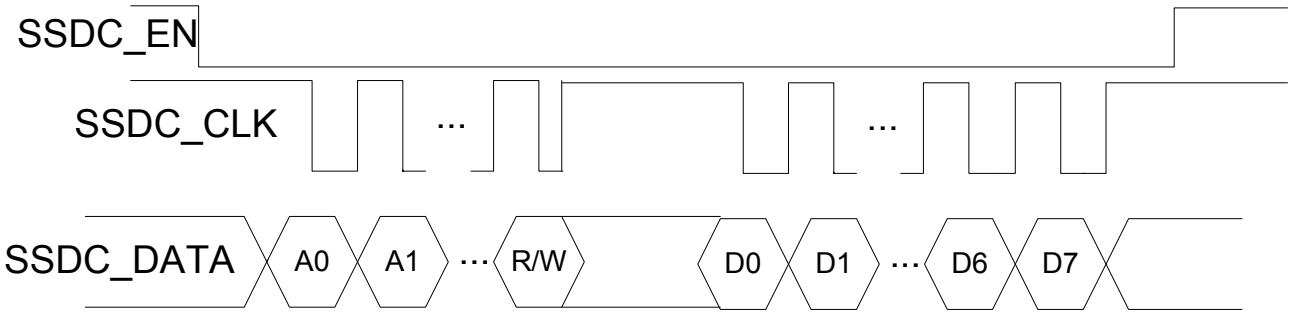
Version 0.4

- **SSDC (Synchronous Serial Data Communication)**

When R/W = 0



When R/W = 1



Version 0.5

- **RAM Mapped System Register Summary**

CODEC Control Register											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
06H	CODEC0_CTL	00H	R/W	SR_SEL3	SR_SEL2	SR_SEL1	SR_SEL0	BEEP_EN	CODECZ	RECB	START
07H	CODEC0_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
08H	CODEC0_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
09H	CODEC1_CTL	00H	R/W	SR_SEL3	SR_SEL2	SR_SEL1	SR_SEL0	BEEP_EN	CODECZ	RECB	START
0AH	CODEC1_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0BH	CODEC1_Data	00H	R/W	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

- **Codec Data Buffer**

Version 0.5

- **Remove SPI relative**

Version 0.7

- **Update PIN Configuration**
- **Update Pad Description**

- **RAM Mapped System Register Summary**

Version 0.8

- **Update PIN Configuration**
- **Update Pad Description**
- **RAM Mapped System Register Summary**