SH57K12

Preliminary

High Performance 8031 Microcontroller

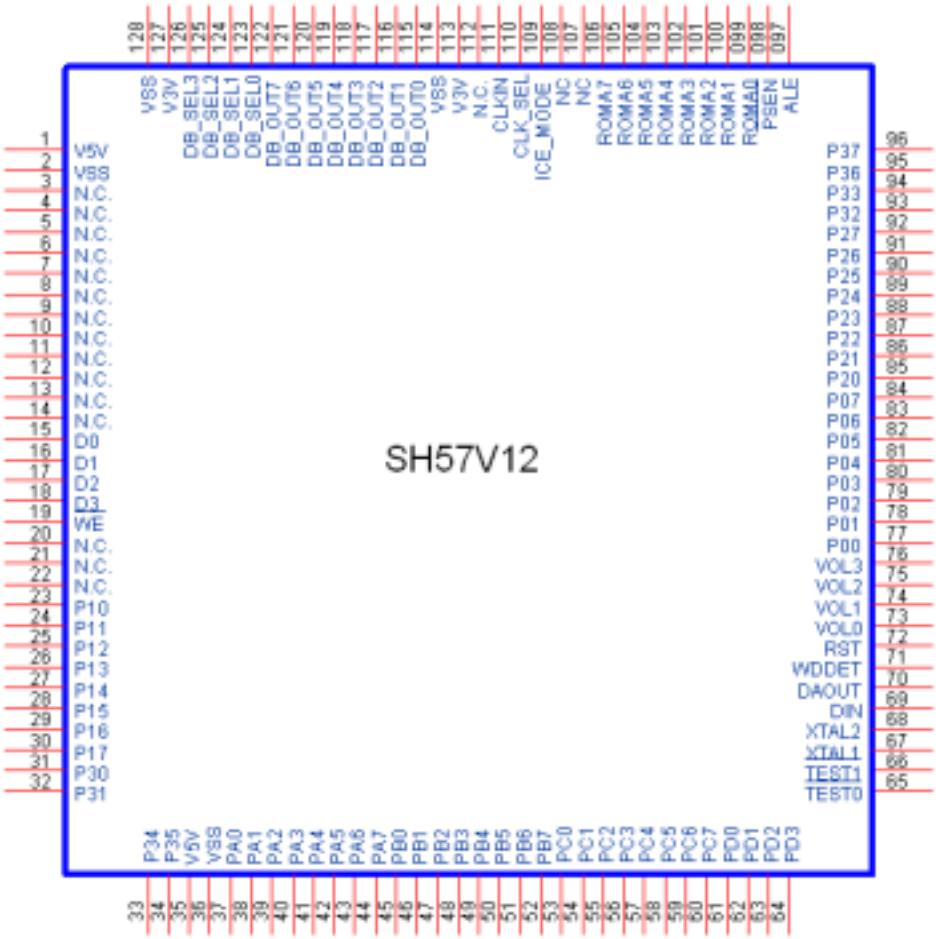
Features

- 8031 MCU core embedded
- DC to 24 MHz operating frequency
- EV: ROM-less
- 16 KB MASK ROM for program storage
- 384 bytes on-chip data RAM:
  - 256 bytes accessed as in the 8031
  - 128 bytes accessed via “MOVX @DPTR”
- RAM mapped system control registers
- 5 interrupt sources (Timer0, Timer1, UART, CODEC RAM Check, CODEC RAM Read/Write)
- 40 GPIO ports with internal pull-up resistors
- Two 16-bit programmable timers/counters
- Watchdog timer (pin option)
- Power Down Mode provided
- CODEC controller
- Dual Power
  - MCU and peripherals operate from 2.4 to 3.6V (V3V)
  - Input/output voltage range from 2.4 to 5.5V (V5V)
- Standby current 10μA for V3V = 3.3V, V5V=5V
- Package Type
  - EV128 - pin QFP package
  - Chip form 80 pin

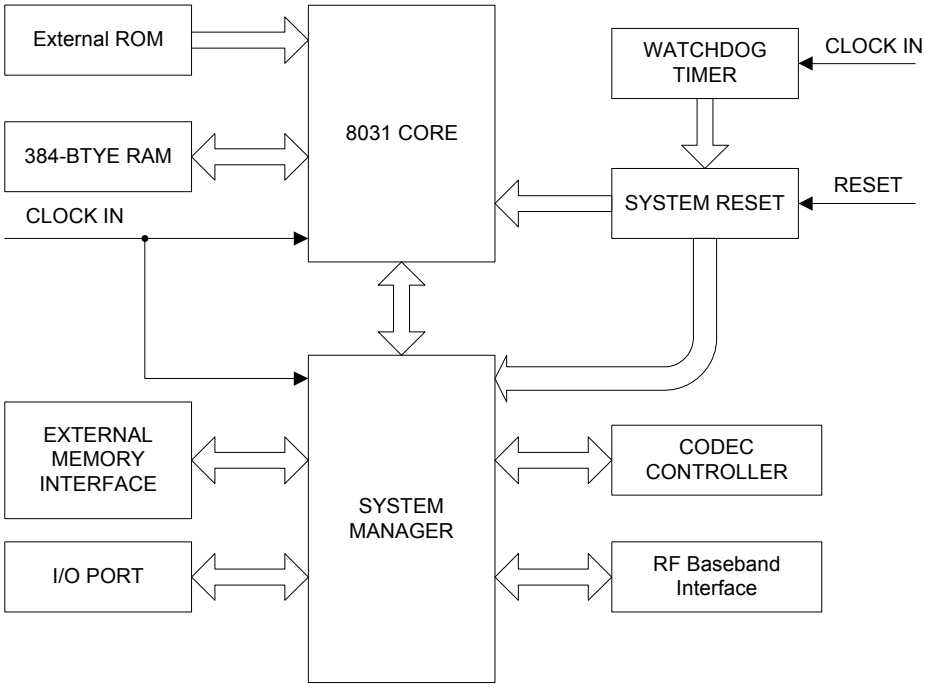
General Description

The SH57K12 is a low-voltage, high performance 8031 embedded microcontroller with 384 bytes on chip RAM. The SH57K12 includes a watchdog timer, and a CODEC controller.

SH57K12 EV Pin Configuration



SH57K12 Block Diagram



SH57K12 EV Pad Description

Pad No.	Designation	I/O	Description
1	VCC	P	Power, positive supply
2	VSS	P	Power, chip ground
3	N.C.		
4	N.C.		
5	N.C.		
6	N.C.		
7	N.C.		
8	N.C.		
9	N.C.		
10	N.C.		
11	N.C.		
12	N.C.		
13	N.C.		
14	N.C.		
15	D0	I/O	CODEC data I/O D0
16	D1	I/O	CODEC data I/O D1
17	D2	I/O	CODEC data I/O D2
18	D3	I/O	CODEC data I/O D3
19	WE	O	Write Strobe for CODEC
20	N.C.		
21	N.C.		
22	N.C.		
23	P10	I/O	8031 Port 1.0
24	P11	I/O	8031 Port 1.1
25	P12	I/O	8031 Port 1.2
26	P13	I/O	8031 Port 1.3
27	P14	I/O	8031 Port 1.4
28	P15	I/O	8031 Port 1.5
29	P16	I/O	8031 Port 1.6
30	P17	I/O	8031 Port 1.7
31	P30	I/O	8031 Port 3.0, RXD

SH57K12 EV Pad Description (continued)

Pad No.	Designation	I/O	Description
32	P31	I/O	8031 Port 3.1, TXD
33	P34	I/O	8031 Port 3.4, T0
34	P35	I/O	8031 Port 3.5, T1
35	VCC	P	Power, positive supply
36	VSS	P	Power, chip ground
37	PA0	I/O	Input/output Port A.0 with high current
38	PA1	I/O	Input/output Port A.1 with high current
39	PA2	I/O	Input/output Port A.2 with high current
40	PA3	I/O	Input/output Port A.3 with high current
41	PA4	I/O	Input/output Port A.4 with high current
42	PA5	I/O	Input/output Port A.5 with high current
43	PA6	I/O	Input/output Port A.6 with high current
44	PA7	I/O	Input/output Port A.7 with high current
45	PB0	I/O	Input/output Port B.0
46	PB1	I/O	Input/output Port B.1
47	PB2	I/O	Input/output Port B.2
48	PB3	I/O	Input/output Port B.3
49	PB4	I/O	Input/output Port B.4
50	PB5	I/O	Input/output Port B.5
51	PB6	I/O	Input/output Port B.6
52	PB7	I/O	Input/output Port B.7
53	PC0	I/O	Input/output Port C.0
54	PC1	I/O	Input/output Port C.1
55	PC2	I/O	Input/output Port C.2
56	PC3	I/O	Input/output Port C.3
57	PC4	I/O	Input/output Port C.4
58	PC5	I/O	Input/output Port C.5
59	PC6	I/O	Input/output Port C.6
60	PC7	I/O	Input/output Port C.7
61	PD0	I/O	Input/output Port D.0
62	PD1	I/O	Input/output Port D.1

SH57K12 EV Pad Description (continued)

Pad No.	Designation	I/O	Description
63	PD2	I/O	Input/output Port D.2
64	PD3	I/O	Input/output Port D.3
65	$\overline{\text{TEST0}}$	I	Enable TEST Mode0 when low (For factory used only)
66	$\overline{\text{TEST1}}$	I	Enable TEST Mode1 when low (For factory used only)
67	XTAL1	O	Crystal oscillator output
68	XTAL2	I	Crystal oscillator input
69	DIN	I	CODEC data input
70	DAOUT	O	CODEC output control
71	WDDET	I/O	Output: watchdog timer status output Input: disable watchdog timer while low
72	RST	I	8031 and system reset input (active high)
73	VOL0	O	Volume control output 0
74	VOL1	O	Volume control output 1
75	VOL2	O	Volume control output 2
76	VOL3	O	Volume control output 3
77	P00	I/O	8031 Port 0.0
78	P01	I/O	8031 Port 0.1
79	P02	I/O	8031 Port 0.2
80	P03	I/O	8031 Port 0.3
81	P04	I/O	8031 Port 0.4
82	P05	I/O	8031 Port 0.5
83	P06	I/O	8031 Port 0.6
84	P07	I/O	8031 Port 0.7
85	P20	I/O	8031 Port 2.0
86	P21	I/O	8031 Port 2.1
87	P22	I/O	8031 Port 2.2
88	P23	I/O	8031 Port 2.3
89	P24	I/O	8031 Port 2.4
90	P25	I/O	8031 Port 2.5
91	P26	I/O	8031 Port 2.6
92	P27	I/O	8031 Port 2.7
93	P32	I/O	8031 Port 3.2
94	P33	I/O	8031 Port 3.3`

SH57K12 EV Pad Description (continued)

Pad No.	Designation	I/O	Description
95	P36	I/O	8031 Port 3.6
96	P37	I/O	8031 Port 3.7
97	ALE	I/O	8031 address latch enable
98	PSEN	I/O	8031 program store enable
99	ROMA0	O	External program ROM address bit 0
100	ROMA1	O	External program ROM address bit 1
101	ROMA2	O	External program ROM address bit 2
102	ROMA3	O	External program ROM address bit 3
103	ROMA4	O	External program ROM address bit 4
104	ROMA5	O	External program ROM address bit 5
105	ROMA6	O	External program ROM address bit 6
106	ROMA7	O	External program ROM address bit 7
107,108	NC		No connection
109	ICE_MODE	I	1: external 8031; 0: built-in 8031
110	CLK_SEL	I	1: oscillator; 0: crystal
111	CLKIN	I	Oscillator clock input
112	n/a		
113	VCC	P	Power, positive supply
114	VSS	P	Power, chip ground
115	DB_OUT0	O	Debug output
116	DB_OUT1	O	Debug output
117	DB_OUT2	O	Debug output
118	DB_OUT3	O	Debug output
119	DB_OUT4	O	Debug output
120	DB_OUT5	O	Debug output
121	DB_OUT6	O	Debug output
122	DB_OUT7	O	Debug output
123	DB_SEL0	I	Debug select
124	DB_SEL1	I	Debug select
125	DB_SEL2	I	Debug select
126	DB_SEL3	I	Debug select
127	VCC	P	Power, positive supply
128	VSS	P	Power, chip ground

SH57K12 Pad Description

Pad No.	Designation	I/O	Description
1	N.C.	O	
2	N.C.	O	
3	N.C.	O	
4	N.C.	O	
5	N.C.	O	
6	N.C.	O	
7	GND	P	GND
8	N.C.	O	
9	N.C.	O	
10	N.C.	O	
11	N.C.	O	
12	VCC	P	VCC
13	N.C.	O	
14	N.C.	O	
15	D0	I/O	CODEC data I/O D0
16	D1	I/O	CODEC data I/O D1
17	D2	I/O	CODEC data I/O D2
18	D3	I/O	CODEC data I/O D3
19	WE	O	Write Strobe for CODEC
20	N.C.	O	
21	N.C.	O	
22	N.C.	O	
23	P10	I/O	8031 Port 1.0
24	P11	I/O	8031 Port 1.1
25	P12	I/O	8031 Port 1.2
26	P13	I/O	8031 Port 1.3
27	P14	I/O	8031 Port 1.4
28	P15	I/O	8031 Port 1.5
29	P16	I/O	8031 Port 1.6
30	P17	I/O	8031 Port 1.7
31	P30/RXD	I/O	8031 Port 3.0, RXD
32	P31/TXD	I/O	8031 Port 3.1, TXD

SH57K12 Pad Description (continued)

Pad No.	Designation	I/O	Description
33	P32	I/O	8031 Port 3.4, T0
34	P33	I/O	8031 Port 3.5, T1
35	PA0	I/O	Input/output Port A.0 with high current
36	PA1	I/O	Input/output Port A.1 with high current
37	PA2	I/O	Input/output Port A.2 with high current
38	PA3	I/O	Input/output Port A.3 with high current
39	PA4	I/O	Input/output Port A.4 with high current
40	GND	P	GND
41	PA5	I/O	Input/output Port A.5 with high current
42	PA6	I/O	Input/output Port A.6 with high current
43	PA7	I/O	Input/output Port A.7 with high current
44	PB0	I/O	Input/output Port B.0
45	PB1	I/O	Input/output Port B.1
46	PB2	I/O	Input/output Port B.2
47	PB3	I/O	Input/output Port B.3
48	PB4	I/O	Input/output Port B.4
49	PB5	I/O	Input/output Port B.5
50	PB6	I/O	Input/output Port B.6
51	PB7	I/O	Input/output Port B.7
52	PC0	I/O	Input/output Port C.0
53	PC1	I/O	Input/output Port C.1
54	PC2	I/O	Input/output Port C.2
55	PC3	I/O	Input/output Port C.3
56	PC4	I/O	Input/output Port C.4
57	PC5	I/O	Input/output Port C.5
58	PC6	I/O	Input/output Port C.6
59	PC7	I/O	Input/output Port C.7
60	PD0	I/O	Input/output Port D.0

SH57K12 Pad Description (continued)

Pad No.	Designation	I/O	Description
61	PD1	I/O	Input/output Port D.1
62	PD2	I/O	Input/output Port D.2
63	PD3	I/O	Input/output Port D.3
64	$\overline{\text{TEST0}}$	I	Enable TEST Mode0 when low (For factory used only)
65	$\overline{\text{TEST1}}$	I	Enable TEST Mode1 when low (For factory used only)
66	VCC	P	VCC
67	XTAL1	O	Crystal oscillator output
68	XTAL2	I	Crystal oscillator input
69	VCC	P	VCC
70	DIN	I	CODEC data input
71	DAOUT	O	CODEC output control
72	WDDET	I/O	Output: watchdog timer status output Input: disable watchdog timer while low
73	RST	I	8031 and system reset input (active high)
74	GND	P	GND
75	VCC	P	VCC
76	VOL0	O	Volume control output 0
77	VOL1	O	Volume control output 1
78	VOL2	O	Volume control output 2
79	VOL3	O	Volume control output 3
80	N.C.	I/O	

Memory Allocation

The 8031 is a ROM-less MCU with 256 bytes SRAM. It can support up to 64 Kbytes external program memory and 64 Kbytes external data memory.

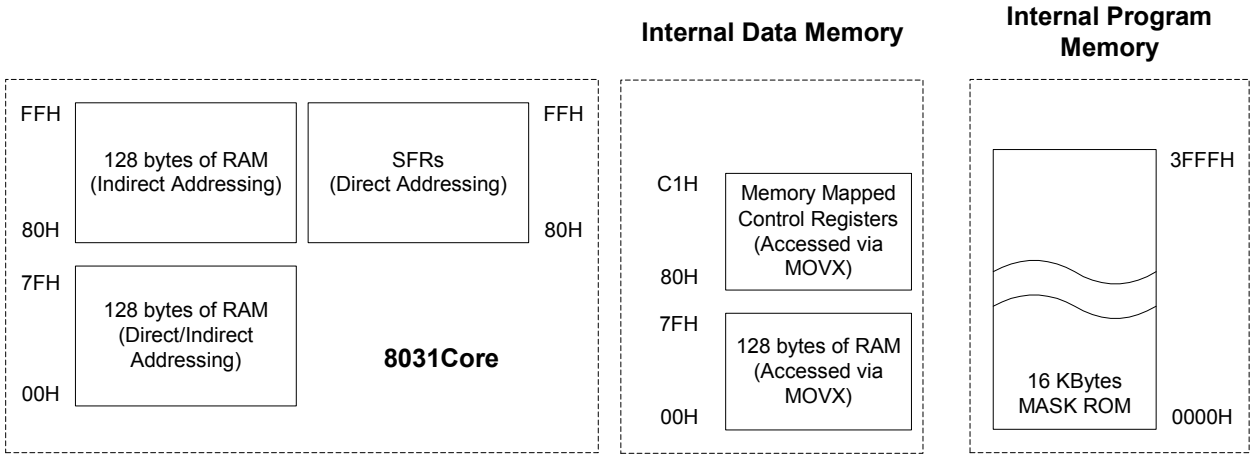
Data Memory

– Internal RAM of 8031: There are 256 bytes of internal data memory in 8031
– Special Function Registers (SFR): There are 128-byte SFRs in 8031
– System control registers of SH57K12: There are 128 bytes of system control registers to configure and control the peripherals of SH57K12
– Built-in Data RAM: There are 128 bytes of RAM, which can be accessed via MOVX instruction

Memory Map

The data memory spaces of 8031 are divided into three blocks, which are generally referred to as the lower 128 direct/indirect addressing bytes, the upper 128 Indirect addressing bytes and SFR space. Please refer to the Intel MCS-51 User's Manual for detail memory operation of 8031.

The Internal Memory Map



RAM Mapped System Register Summary (using MOVX, 00H-7FH is for 128byte SRAM)

I/O Ports Control and Data Registers											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
80H	PMODA	FFH	R/W	PMODA.7	PMODA.6	PMODA.5	PMODA.4	PMODA.3	PMODA.2	PMODA.1	PMODA.0
81H	PA	00H	R/W	PA.7	PA.6	PA.5	PA.4	PA.3	PA.2	PA.1	PA.0
82H	PMODB	FFH	R/W	PMODB.7	PMODB.6	PMODB.5	PMODB.4	PMODB.3	PMODB.2	PMODB.1	PMODB.0
83H	PB	00H	R/W	PB.7	PB.6	PB.5	PB.4	PB.3	PB.2	PB.1	PB.0
84H	PMODC	FFH	R/W	PMODC.7	PMODC.6	PMODC.5	PMODC.4	PMODC.3	PMODC.2	PMODC.1	PMODC.0
85H	PC	00H	R/W	PC.7	PC.6	PC.5	PC.4	PC.3	PC.2	PC.1	PC.0
86H	PMODD	00H	R/W	-	-	-	-	PMODD.3	PMODD.2	PMODD.1	PMODD.0
87H	PD	00H	R/W	-	-	-	-	PD.3	PD.2	PD.1	PD.0
Watch-Dog Timer Control Register											

Addr.	Register	Reset	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
88H	WDT_CTRL	-	W	-	-	-	-	-	-	-	WD_RST
CODEC Control Register											
Addr.	**Register**	**Reset**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A0H	CODEC_MEM_CTL	00H	R/W	-	-	-	MEM_CHK	PAGE_WR	PAGE_RD	S_WTITE	S_READ
C0H	CODEC_CTL	00H	R/W	SR_SEL3	SR_SEL2	SR_SEL1	SR_SEL0	BEEP_EN	CODECZ	RECB	START
Volume Control Register											
B1H	VOL_CTL	00H	R/W	VOL_EN	-	-	-	VOL.3	VOL.2	VOL.1	VOL.0

Note: Accessing these reserved control registers may cause some unexpected results. These registers are reserved for future usage.

Microprocessor 8031

Features
Intel 8031 architecture
- 8-Bit CPU optimized for control applications
- Extensive Boolean processing capabilities
- Maximum 64K External Program Memory ability
- Maximum 64K External Program Memory ability
- 256 Bytes of on-chip Data RAM
- 32 bi-directional and individually addressable I/O lines
- Two 16-bit timer/counters
- 5-vector interrupt structure with two programmable priority levels

General Description

The 8031 is an 8-bit microprocessor optimized for control applications. Byte-processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for Internal RAM. The instruction set provides several byte instructions including multiply and divide instructions. In additional several bit-oriented instructions are also provided. This allows direct bit manipulation and testing in control and logic systems that require Boolean processing.

Special Function Registers (SFRs)

The 8031 core has a total of 20 SFRs, as shown in the table below, SFR Map for 8031. Note that not all the addresses are occupied by SFRs. The unoccupied addresses are not implemented and should not be used by the customer. Read access from these unoccupied locations will return unpredictable data, while write accesses will have no effect on the chip.

SFR Map for 8031									
F8H									FFH
F0H	B								F7H
E8H									EFH
E0H	ACC								E7H
D8H									DFH
D0H	PSW								D7H
C8H									CFH
C0H									C7H
B8H	IP								BFH
B0H	P3								B7H
A8H	IE								AFH
A0H	P2								A7H
98H	SCON	SBUF							9FH
90H	P1								97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H	P0	SP	DPL	DPH				PCON	87H

Note: SFRs in 80H, 88H, 90H, 98H, A0H, A8H, B0H, B8H, C0H, C8H, D0H, D8H, E0H, E8H, F0H and F8H are bit-addressable.

Accumulator (E0H)

ACC is the accumulator register used for most of the arithmetic and logical instructions.

B Register (F0H)

The B register is an SFR which is used primarily in the multiply and divide instructions. It can however be used as a temporary scratch pad register for the other instructions.

Program Status Word (PSW) (D0H)

The PSW is the register that holds information about the status of the Accumulator, the selected register banks and other information. This register is detailed in the following table.

PSW: Program Status Word Register (D0H)		
B7	CY	Carry flag
B6	AC	Auxiliary Carry flag (for BCD operations)
B5	F0	Flag 0(Available to the user for general purposes)
B4	RS1	Register Bank select control bit 1 & 0 Set/cleared by software to determine working bank. (RS1, RS0): (00) – Bank 0 ⇔ Address → (00H ~ 07H) (01) – Bank 1 ⇔ Address → (08H ~ 0FH) (10) – Bank 2 ⇔ Address → (10H ~ 17H) (11) – Bank 3 ⇔ Address → (18H ~ 1FH)
B3	RS0	
B2	OV	Overflow Flag
B1	X	User definable flag
B0	P	Parity Flag Set/Cleared by hardware each instruction cycle to indicate an odd/even number of “one” bit I the Accumulator, i.e., even parity.

Stack Pointer (81H)

The Stack Pointer is an 8-bit wide register that is used to point to the top of the stack where addresses are stored. After a reset, the stack pointer is initialized to 07H, and so the stack begins at 08H. However the stack can reside at any location in the Internal RAM and stack pointer can be programmed to suit the user’s needs.

Data Pointer (82H, 83H)

The Data Pointer (DPTR) consists of a high byte (DPH) and low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Port 0,1,2,3 (80H, 90H, A0H, B0H)

The four ports have four SFRs associated with them. Data to be brought out onto the port pins is written to the latches.

Timer Registers (8AH, 8BH, 8CH, 8DH)

The 8031 has two 16-bit timers, Timer/Counter 0 and Timer/Counter 1. The TH0, TL0 and TH1, TL1 register pairs are the 16-bit counting registers for the two timer/counters respectively. The TCON and TMOD registers provide control functions for timer 0 and timer 1.

Control Registers
The SFRs TCON, TMOD, SCON, IE, IP and PCON are the registers, which contain the control and status bits for the Timer/Counters, the Serial Port and the Interrupt system.
For more details please refer to the MCS-51 Programmer’s Guide and Data Sheet of INTEL MCS-51 family.

Port Structure and Operation

All four ports in the 8031 are bi-directional. Each consists of a latch, an output driver, and input buffer.
The output drivers of Port 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read.

Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the port 2 pins continue to emit the P2 SFR content.
All the Port 3 pins are multi-functional. They are not only port pins, but also serve the functions of various special features as listed on the following table.

Port 3 Function Descriptions

Alternate Function of Port 3		
Port Pin	Alternate Function	Assigned Function for SH57K12
P3.7	RD (external Data Memory read strobe)	Internal signal of SH57K12
P3.6	WR (external Data Memory write strobe)	Internal signal of SH57K12
P3.5	T1 (Timer/Counter 1 external pin)	GPIO
P3.4	T0 (Timer/Counter 0 external pin)	GPIO
P3.3	INT1 (external interrupt 1)	Internal signal of SH57K12
P3.2	INT0 (external interrupt 0)	Internal signal of SH57K12
P3.1	TXD (serial output port)	GPIO
P3.0	RXD (serial input port)	GPIO

In order to make the alternate functions activate correctly, the corresponding bit latch must be held at value 1. If this is not done then the corresponding port pin is stuck at 0, and external or internal inputs will have no effect on the pin value.

Serial Port

The UART operates in all of the usual modes that are the same as the normal 8051. For more details please refer to the MCS-51 Programmer's Guide and Data Sheet of INTEL MCS-51 family.

Clock

The 8031 can use either a crystal oscillator or an external clock. Internally, the clock is divided by 2 before it is used. This makes 8031 relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The 8031 incorporate a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

Reset

The external RST signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all the other SFR registers except SBUF to 00H. SBUF is not reset.

Interrupt Vectors
The 8031 provides 5 interrupts: 2 external interrupts, 2 timer interrupts and 1 UART interrupt. There are six interrupt vectors provided by the 8031. The descriptions are as followed.

Address	Interrupt Source	Description
0000H	**Reset**	**System Reset**
0003H	**IE0**	**External INT0 Interrupt of the 8031**
000BH	**TF0**	**Timer/Counter0 Overflow Interrupt of the 8031**
0013H	**IE1**	**External INT1 Interrupt the of the 8031**
001BH	**TF1**	**Timer/Counter1 Overflow Interrupt of the 8031**
0023H	**TI+RI**	**UART Interrupt**

Interrupt Enable

Each of the interrupt sources can be individually enabled or disabled by programming IE register. This register also contains a global disable bit, which can be clear to disable all interrupts at once. The following table shows the IE definition.

IE (Interrupt Enable) Register in the 8031 core (A8H)		
B7	EA	Disable all interrupts. If EA=0, no interrupt will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
B6~B5	X	Unused
B4	ES	Serial port (UART) interrupt enable bit
B3	ET1	Timer 1 Overflow Interrupt enable bit
B2	EX1	External Interrupt 1 enable bit
B1	ET0	Timer 0 Overflow Interrupt enable bit
B0	EX0	External Interrupt 0 enable bit

Enable bit = 1, enables the interrupt

Enable bit = 0, disables the interrupt

Interrupt Priority

Each interrupt source can also be individually programmed to one of the two priority levels by setting or clearing a bit in the IP register. The Following table shows the IP definition.

IP Register in the 8031 core (B8H)		
B7~B5	X	Unused
B4	PS	Serial port interrupt priority bit
B3	PT1	Timer1 overflow interrupt priority bit
B2	PX1	External interrupt1 priority bit
B1	PT0	Timer0 overflow interrupt priority bit
B0	PX0	External interrupt0 priority bit
Priority bit = 1, assign higher priority Priority bit = 0, assign lower priority		

A low-priority interrupt can be interrupted by a high-priority interrupt, but cannot be interrupted by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.
If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by software polling sequence.
In operation, all the interrupt flags are latched into the interrupt control system every machine cycle. The samples are polled during the following machine cycle. If the flag for an enabled interrupt is found to be set 1, The interrupt system generates an LCALL to the appropriate location in Program Memory, unless some other condition block an interrupt, among them that an interrupt of equal or higher priority level is already in progress.
The hardware-generated LCALL accesses the contents of the Program Counter to push onto the stack, and reloads the PC with the beginning address of the service routine.
As previously noted, the service routine for each interrupt begins at a fixed location.
Only the Program Counter is automatically pushed onto the stack, and other registers are pushed onto the stack by software if necessary. This enhances the interrupt response time, albeit at expense of increasing the programmer's burden of responsibility. As a result, many interrupt functions that are typical in control applications – toggling a port pin, for example, or reloading a timer, or unloading a serial buffer – can often be completed in less time than it takes other architectures to commence them.

Power-Down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stop. The only way to exit power-down mode is by a reset.

PCON: Power Control Register (87H)		
B7	SMOD	Double baud rate bit
B6	-	Reserved
B5	-	Reserved
B4	-	Reserved
B3	GF1	General-purpose flag bit
B2	GF0	General-purpose flag bit
B1	PD	Power down mode bit
B0	IDL	Idle mode bit

Machine Cycles

In the 8031, a machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two systems clock periods. Thus a machine cycle takes 12 system clock periods.

Each state is divided into a Phase 1 half and a Phase 2 half. Fig. 1 shows the fetch/execute sequences in states and phases for various kinds of instructions. Normally two program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code byte, the CPU simply ignores the extra fetch, and the Program Counter is not increment. The fetch/execute sequences in states and phases for various kinds of instructions are show in Fig. 1.

The fetch/execute sequences are the same whether the Program Memory is internal or external to the chip. Execution times do not depend on whether the Program Memory is internal or external.

Fig. 2 shows the signals and timing involved in program fetches when the Program Memory is external. If Program Memory is external, then the Program Memory read strobe PSEN is normally activated twice per machine cycle, as shown in Fig. 2(a).

If an access to external Data Memory occurs, as shown in Fig. 2(b), two PSEN are skipped, because the address and data bus are being used for the Data Memory access.

Note that a Data Memory bus cycle takes twice as much time as a Program Memory bus cycle. Fig. 2 shows the relative timing of the addresses being emitted at Ports 0 and 2, and of ALE and PSEN. ALE is used to latch the low address byte from P0 into the address latch. (PSEN is active low)

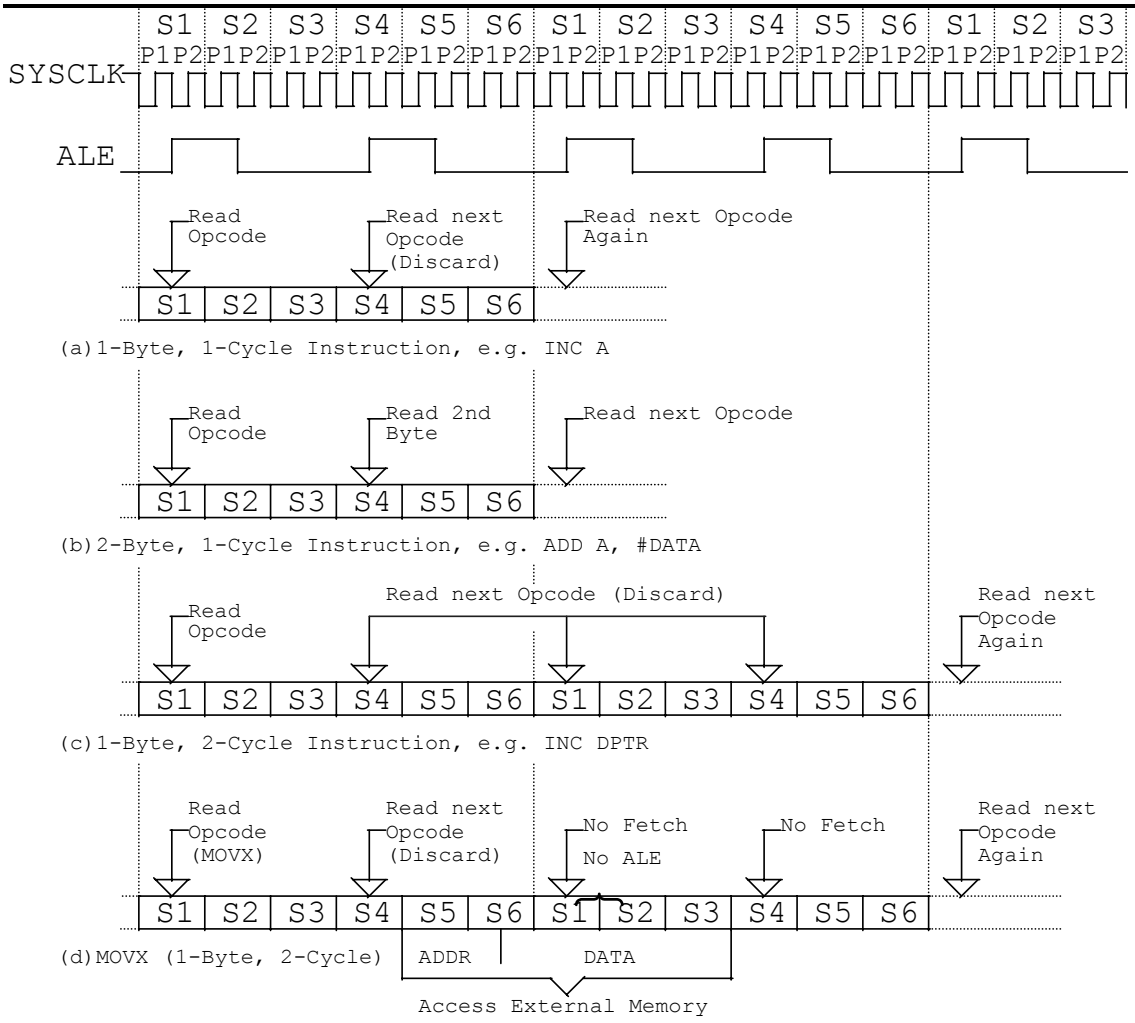
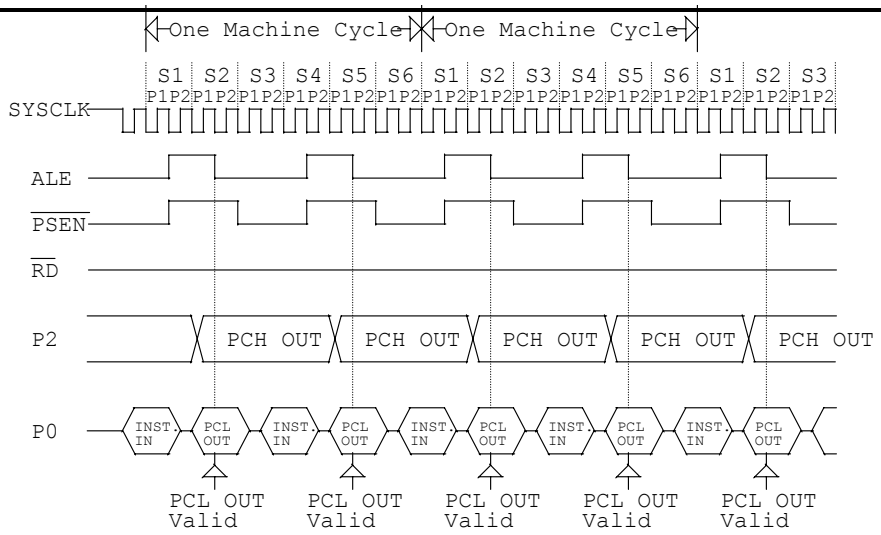
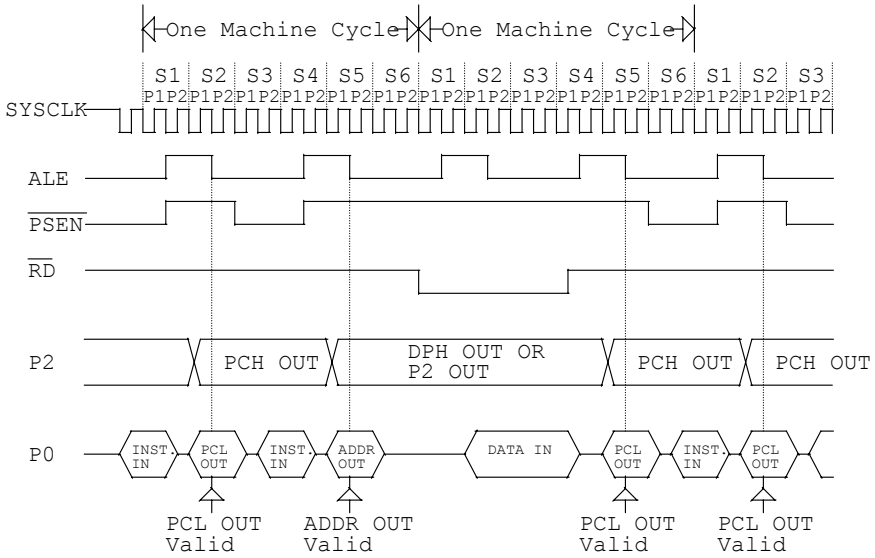

S1 S2 S3 S4 S5 S6 S1 S2 S3 S4 S5 S6 S1 S2 S3
P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2 P1P2
SYSCLK
ALE
Read Opcode
Read next Opcode (Discard)
Read next Opcode Again
S1 S2 S3 S4 S5 S6
(a)1-Byte, 1-Cycle Instruction, e.g. INC A
Read Opcode
Read 2nd Byte
Read next Opcode
S1 S2 S3 S4 S5 S6
(b)2-Byte, 1-Cycle Instruction, e.g. ADD A, #DATA
Read next Opcode (Discard)
Read Opcode
Read next Opcode Again
S1 S2 S3 S4 S5 S6 S1 S2 S3 S4 S5 S6
(c)1-Byte, 2-Cycle Instruction, e.g. INC DPTR
Read Opcode (MOVX)
Read next Opcode (Discard)
No Fetch
No ALE
No Fetch
Read next Opcode Again
S1 S2 S3 S4 S5 S6 S1 S2 S3 S4 S5 S6
(d)MOVX (1-Byte, 2-Cycle)
ADDR
DATA
Access External Memory

Fig. 1



(a) Without MOVX



(b) With MOVX

Fig. 2

Features of SH57K12

Reset

There are two reset sources for SH57K12:

- External reset
- Watchdog timer internal reset

External RST Pin

The reset signal is the same as described in the 8031. A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles.

Watchdog Timer Reset

This MCU implements a Watchdog timer reset to avoid system malfunction. If the watchdog timer is not cleared in time, it will generate a pulse to reset the whole system and the MCU.

Input/Output Ports

The SH57K12 has 36 GPIO ports. Port1 [7:0] and Port3 [5,4,1,0] are the same as in the 8031. Others are extended I/Os. Port A, Port B and Port C are bi-directional general-purpose I/O ports. The I/O status of each port can be configured individually. PMODA, PMODB and PMODC registers are used to configure I/O status. Each port is corresponding to one bit in these registers. The PMODA.7 bit is for PA.7 port, PMODA.6 bit is for PA.6 port and so on. We can configure these 26 ports in this rule. If we set the bit value to '1', the corresponding port is configured as input port. And if the bit is clear to '0', the port is configured as output port. The I/O value can be set or fetched by these registers PA, PB and PC. These I/O ports don't support bit operation.

I/O port Registers

PMODA — Port A Control Register (80H)			
B7~B0	PMODA7~ PMODA0	R/W	Port A direction select, 1: Input port, 0: Output port
PMODB — Port B Control Register (82H)			
B7~B0	PMODB7~ PMODB0	R/W	Port B direction select, 1: Input port, 0: Output port
PMODC — Port C Control Register (84H)			
B7~B0	PMODC7~ PMODC0	R/W	Port C direction select, 1: Input port, 0: Output port
PMODD — Port D Control Register (86H)			
B3~B0	PMODD3~ PMODD0	R/W	Port D direction select, 1: Input port, o: Output port
PA — Port A Data Register (81H)			
B7~B0	PA.7~PA.0	R/W	Port A data
PB — Port B Data Register (83H)			
B7~B0	PB.7~PB.0	R/W	Port B data
PC — Port C Data Register (85H)			

B7~B0	PC.7~PC.0	R/W	Port C data
PD — Port D Data Register (87H)			
B3~B0	PD.3~PD.0	R/W	Port D data

Interrupts

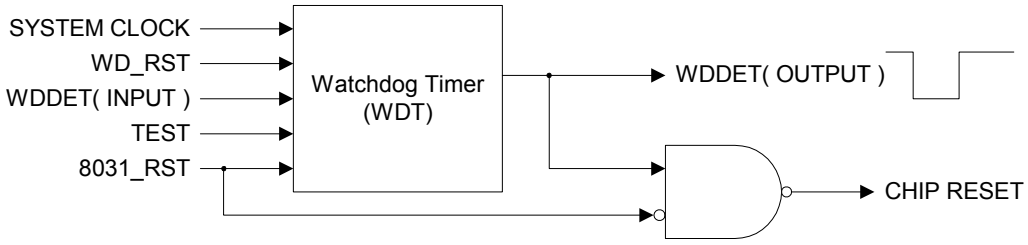
The 8031 core has 5 interrupt vectors. In SH57K12, these five interrupt vectors are expanded. The interrupts of Timer0, Timer1, and TI/RI are single-level interrupts as for 8031 core. The interrupt INT1 is triggered by external interrupt INT_EX in Normal Mode. In Power Down Mode, a falling edge of INT_EX wakes up the MCU and generate an INT1 interrupt. User must read the status of I/Os to determine that which interrupt sources cause INT1. All the interrupt sources can be controlled or enabled by SFRs of 8031 and system control registers of SH57K12.

Interrupt Controller of SH57K12

INT1 is dedicated to RAM error checking and RAM ROW read/write routine. INT1 is triggered when RAM checking operation is finished or a ROW read/write is finished.

Watchdog Timer Operation

SH57K12 implements a watchdog timer reset to avoid system shutdown or malfunction. To disable the watchdog timer, connect WDDET pin to ground. The watchdog timer must be cleared by set the bit WD_RST to 1 before time-out. Otherwise the WDT will send out a pulse signal to reset the whole system. The structure of watchdog timer is shown below. For system clock is 12MHz, the length of the watchdog timer is 5.6 seconds.



Watchdog Timer Control Register

WDT_CTL: Watchdog Timer Control Register (88H)		
B0	WD_RST	Watchdog timer reset bit. 1: Reset watchdog timer, 0: No use

CODEC Controller

The CODEC controller is built in SH57K12.

CODEC Controller Registers

CODEC_MEM_CTL: RAM Control Register (A0H)		
B4	MEM_CHK	Activate memory checking
B3	PAGE_WR	Activate row (page) writing
B2	PAGE_RD	Activate row (page) reading
B1	S_WRITE	Activate single writing
B0	S_READ	Activate single reading
CODEC_CTL: CODEC Control Register (C0H)		
B7~B4	SR_SEL3~0	Sampling rate selection
B3	BEEP_EN	1: enable beeper output; 0: disable beeper
B2	CODECZ	CODEC output enable
B1	RECB	0: record; 1: playback
B0	START	1: start sampling clock; 0: stop sampling clock

Volume Controller

The volume controller is to output VOL.3~0 (B1H.3~0) to pin VOL3~VOL0. Setting VOL_EN will enable the volume controller.

Volume Control Register

VOL_CTL: Volume Control Register (B1H)		
B7	VOL_EN	Set to 1 to enable volume controller
B3~0	VOL.3~0	Volume control bits 3~0

Absolute Maximum Ratings

Power Supply Voltage……-0.5V to 5.5V
Input Voltage……..…..-0.3V to V5V+0.3V
Output Voltage…….……...-0.3V to V5V+0.3V
Power Dissipation……..0.03W
Operating Temperature……0°C to 70°C
Storage Temperature……-55°C to 135°C

Comments

Stresses above those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these of any other conditions above specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics **(Temperature = 0°C to 70°C, GND = 0V)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply voltage	V3V	2.4		3.6	V	
Supply voltage	V5V	2.4		5.5	V	
Operating current	IDD		4		mA	

DC Electrical Characteristics (Temperature = 0°C to 70°C, V5V = 3.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions

Input high voltage	VIH1	0.9V5V		V5V+0.3	V	RESET
	VIH2	V5V-0.3		V5V+0.3	V	XTALI
	VIH3	0.8V5V		V5V+0.3	V	All pins except RESET, XTALI
Input low voltage	VIL1	-0.3		0.1V5V	V	RESET
	VIL2	-0.3		0.3	V	XTALI
	VIL3	-0.3		0.2V5V	V	All pins except RESET, XTALI
Output high voltage	VOH	V5V-0.7			V	Output pin without loading
Output low voltage	VOL			0.4	V	Output pin without loading
Drive/Sink current	IOH		2		mA	V_{OH} = 2.6V, V_{OL} = 0.4V
	IOL		-2		mA	P1, P3 [0,1,4,5], PB, PC, PD
Drive/Sink current	IOH		10		mA	V_{OH} = 2.6V, V_{OL} = 0.4V
	IOL		-10		mA	PA
Drive/Sink current	IOH		16		mA	V_{OH} = 2.6V, V_{OL} = 0.4V
	IOL		-16		mA	DAOUT, VOL[3..0]
Sink current	IOL		-16		mA	V_{OL} = 0.4V
Pull-up resistance	RUP	130	180	230	KΩ	P1, P3 [0,1,4,5], PA, PB, PC, PD

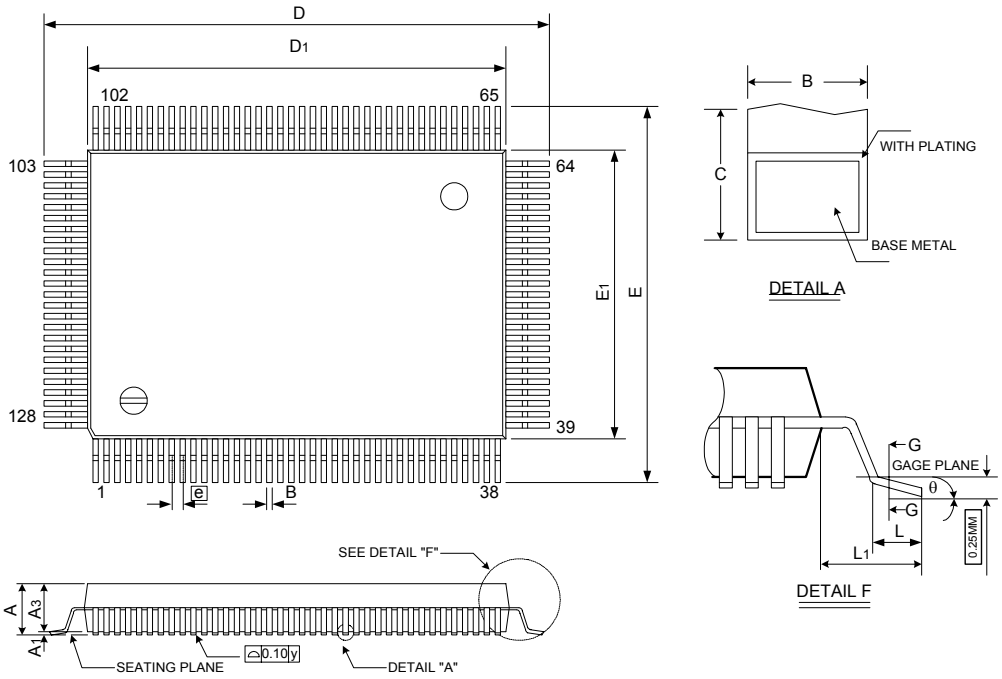
AC Electrical Characteristics (Temperature = 0°C to 70°C, V3V = 3.0V±10%, GND = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Execution cycle time	TCYC	1			μs	Fmain = 12 MHz
Hardware Reset duration	TRES	2			TCYC	Fmain = 12 MHz
CPU start up time from Reset or Power-down	TCPU		2.5	10	ms	Fmain = 12 MHz by crystal oscillator
External crystal frequency	Fxtal		12	24	MHz	Crystal oscillator
External crystal start up time	T_{WS}			1	sec	

SH57K12 EV Package Information

QFP 128L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.134	--	--	3.40
A_1	0.010	--	--	0.25	--	--
A_2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	--	0.008	0.09	--	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.667	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
Y	--	--	0.004	--	--	0.10
θ	0°	--	7°	0°	--	7°

Notes:
1.Dimensions D & E do not include resin fins.
2.Dimensions F are for reference of surface mount PC Board design only.

SH57K12 Bonding Diagram

Chip Size (um): 2345.40 2475.9

X Cord	Y Cord	PIN Name
-1099.71	1049.23	N.C.
-1099.71	934.21	N.C.
-1099.71	819.19	N.C.
-1099.71	704.17	N.C.
-1099.71	589.15	N.C.
-1099.71	472.67	N.C.
-1099.71	367.64	GND
-1099.71	262.61	N.C.
-1099.71	157.58	N.C.
-1099.71	52.55	N.C.
-1099.71	-52.48	N.C.
-1099.71	-157.51	VCC
-1099.71	-262.54	N.C.
-1099.71	-367.57	N.C.
-1099.71	-472.60	D0
-1099.71	-587.62	D1
-1099.71	-702.64	D2
-1099.71	-817.66	D3
-1099.71	-932.68	WE
-1099.71	-1047.70	N.C.
-1066.37	-1164.27	N.C.
-951.35	-1164.27	N.C.
-836.33	-1164.27	P10
-721.31	-1164.27	P11
-606.28	-1164.27	P12
-491.27	-1164.27	P13
-386.24	-1164.27	P14
-281.20	-1164.27	P15
-176.18	-1164.27	P16
-71.14	-1164.27	P17
33.88	-1164.27	P30

138.91	-1164.27	P31
243.95	-1164.27	P32
348.98	-1164.27	P33
454.00	-1164.27	PA0
570.40	-1164.27	PA1
685.42	-1164.27	PA2
800.44	-1164.27	PA3
915.46	-1164.27	PA4
1030.48	-1164.27	GND

X Cord	Y Cord	PIN Name
1100.12	-1048.27	PA5
1100.12	-933.25	PA6
1100.12	-818.23	PA7
1100.12	-703.21	PB0
1100.12	-588.19	PB1
1100.12	-473.17	PB2
1100.12	-368.14	PB3
1100.12	-263.11	PB4
1100.12	-158.08	PB5
1100.12	-53.05	PB6
1100.12	51.98	PB7
1100.12	157.01	PC0
1100.12	262.04	PC1
1100.12	367.07	PC2
1100.12	472.10	PC3
1100.12	589.72	PC4
1100.12	704.74	PC5
1100.12	819.76	PC6
1100.12	934.78	PC7

1100.12	1049.8	PD0
1029.91	1165.60	PD1
914.89	1165.60	PD2
799.88	1165.60	PD3
684.86	1165.60	TEST0
569.84	1165.60	TEST1
454.00	1165.60	VCC
348.98	1165.60	XTAL1
243.95	1165.60	XTAL2
138.91	1165.60	VCC
33.88	1165.60	DIN
-71.14	1165.60	DAOUT
-176.18	1165.60	WDDET
-281.20	1165.60	RESET
-386.24	1165.60	GND
-491.27	1165.60	VCC
-606.28	1165.60	VOL_0
-721.31	1165.60	VOL_1
-836.33	1165.60	VOL_2
-951.35	1165.60	VOL_3
-1066.37	1165.60	N.C.

Ordering Information

Part No.	Package
SH57V12	QFP128
SH57K12	Chip 80