SH66N12

2K OTP 4-bit Microcontroller with LCD Driver

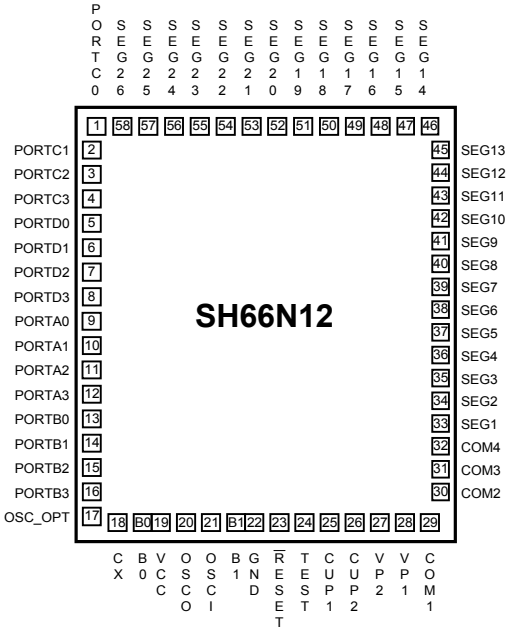
Features

- The SH6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 2048 X 16 bits
- RAM: 256 X 4 bits (data memory)
- Operation Voltage Range: 1.2V - 1.7V
- 16 CMOS I/O pins (PORTC, D can switch to segment.)
- 4-level subroutine nesting (including interrupts)
- Two 8-bit timers with pre-divider circuit
- Oscillator warm-up timer
- 4 priority interrupt sources:
  - External interrupt (falling edge)
  - Timer0 interrupt
  - Timer1 interrupt
  - PortB & PortC interrupt (falling edge)
- Clock source:
  - 32.768KHz crystal or 131K RC (pad option)
- Instruction cycle time:
  - 4/32.768KHz (≈ 122μs) for 32.768KHz crystal
  - 4/131KHz (≈ 31μs) for 131KHz RC
- LCD driver: 4 X 34 (1/4 duty, 1/3 bias or 1/3 duty, 1/2 bias, 8 segments shared with PORTC, D)
- Built-in voltage doubler and tripler charge pump circuit
- Built-in EL-light driver
- Built-in Resistor to Frequency converter circuit
- Built-in alarm generator (carrier frequency: 4KHz.)
- Two low power operation modes - HALT or STOP mode
- Low power consumption
- Bonding option for multi-code software
- Available in CHIP FORM

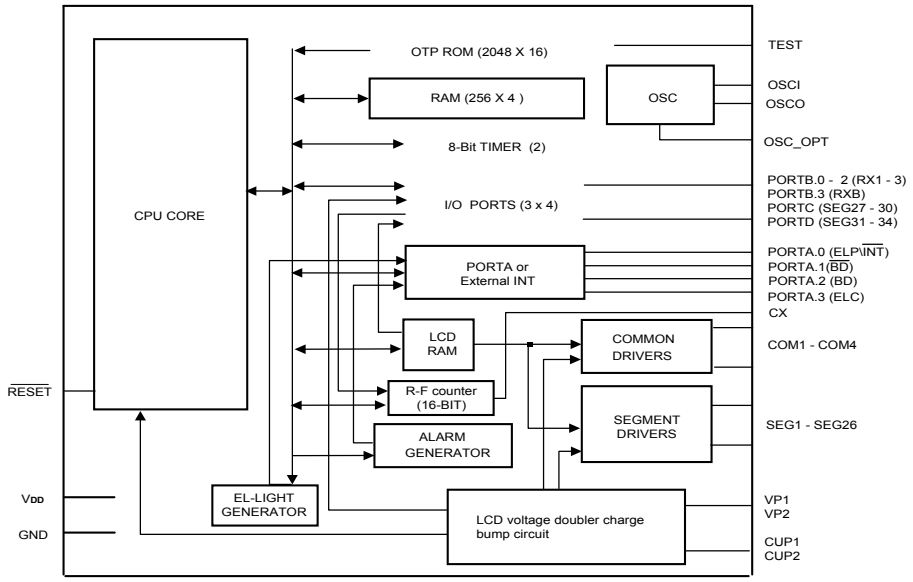
General Description

The SH66N12 is a single-chip microcontroller integrated with an SH6610C CPU core, SRAM, timer, alarm generator, LCD driver, I/O port, voltage pump, El-light driver, R-F converter and one-time program ROM.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
33 - 58	SEG1 - 26	O	Segment signal output for LCD display
29 - 32	COM1 - 4	O	Common signal output for LCD display
28, 27	VP1, VP2	P	Power supply pin for LCD driver
25, 26	CUP1 - 2	P	Connection for voltage doubler capacitor
24	TEST	I	Test pin internally pull-down. (No connect for user)
23	$\overline{\text{RESET}}$	I	Pad reset input
19	V_{DD}	P	Power supply pin for CPU
	B0	I	Bonding option, internally pull-low
	B1	I	Bonding option, internally pull-high
22	GND	P	Ground pin
17	OSC_OPT	I	Clock source selection Pull low: 32K crystal. Pull high: 131K RC (internal pull high)
20	OSCO	O	Oscillator output pin, connected to crystal oscillator
21	OSCI	I	Oscillator input pin, connected to crystal or external resistor
9 - 12	PORTA0 - 3	I/O	Bit programmable I/O, PA.0 could be external interrupt input ($\overline{\text{INT}}$) PA.0, PA.3 could be EL-light output PA.0 (ELP), PA.3 (ELC) PA.1, PA.2 could be buzzer output PA.1 (BD), PA.2 ($\overline{\text{BD}}$)
13 - 16	PORTB0 - 3	I/O	Bit programmable I/O, vector interrupt (active falling edge) PB.0 - 2 shared with RX1 - 3, PB.3 shared with RXB
1 - 4	PORTC0 - 3	I/O	Bit programmable I/O, Vector interrupt (active falling edge) Shared with SEG27 - 30
5 - 8	PORTD0 - 3	I/O	Bit programmable I/O. shared with SEG31 - 34
18	CX	I	R-F converter counter input pin

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and the Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 2K program ROM. It consists of 11-bits: the Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, and PC0).The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BNC),
(2) When executing a subroutine call instruction (CALL),
(3) When an interrupt occurs,
(4) When the chip is in the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2. ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BNZ, and BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and retrieved back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfer between the accumulator and system register or data memory can be performed.

1.4. Stack

A group of registers are used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized into 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed for subroutine calls and interrupts.

The contents of the Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). The stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter into an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of the stack will be shifted out.

2. ROM

The ROM can address 2048 words X 16 bits of program area from $000 to $7FF.

There is an area from address $0 through $4 reserved for special interrupt service routines, such as starting at vector address.

Address	Instruction	Remarks
000H	JMP Instruction	Jump to RESET service routine
001H	JMP Instruction	Jump to External interrupt service routine
002H	JMP Instruction	Jump to TIMER0 service routine
003H	JMP Instruction	Jump to TIMER1 service routine
004H	JMP Instruction	Jump to PB,PC service routine (PORTB, PORTC)

*JMP instruction can be replaced by any instruction.

3. RAM

Built-in RAM contains of general-purpose data memory, LCD RAM, and system register.

The following is the memory allocation map:

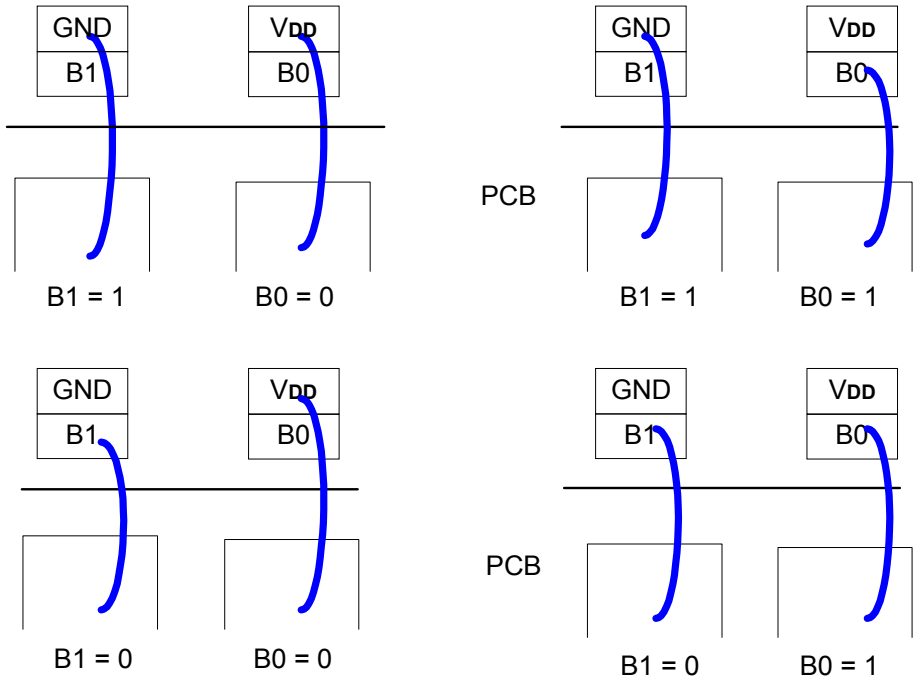
$000 - $01F: System register and I/O
$020 - $11F: Data memory (256 X 4 bits, divided into 2 banks)
$300 - $321: LCD RAM space (34 X 4 bits)

The Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power on
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags	0000
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags	0000
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0-2: Timer0 Mode register	000
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0-2: Timer1 Mode register	000
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble	0000
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble	0000
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble	0000
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	0000
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	0000
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	0000
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD	0000
$0C	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit0: count resister1 Bit1: count resister2 Bit2: count resister3 Bit3: set PORTB as R-F converter	0000
$0D	-	ELON	B1	B0	R R/W	Bit0, 1: Bonding option Bit2: EL-LIGHT on/off control	010
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register	-
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register	-
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble	-
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble	-
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble	-
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mod Bit2: LCD off Bit3: R-F convert counter on	0100
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control	0000
$15	PPULL	O/S2	O/S1	DUTY	R/W	Bit0: change LCD duty to 1/4 duty, 1/3 bias Bit1: set PORTC as LCD segment output Bit2: set PORTD as LCD segment output Bit3: Port pull-up control	0000
$16	ELF	ELPF	-	-	R/W	EL-LIGHT mode control Bit2: ELP driver output frequency control Bit3: EL-LIGHT driver frequency select	0000
$17	RFL.3	RFL.2	RFL.1	RFL.0	R/W	R-F counter register low nibble	0000
$18	RFML.3	RFML2	RFML.1	RFML.0	R/W	R-F counter register middle_low nibble	0000
$19	RFMH.3	RFMH.2	RFMH.1	RFMH.0	R/W	R-F counter register middle_high nibble	0000
$1A	RFH.3	RFH.2	RFH.1	RFH.0	R/W	R-F counter register high nibble	0000
$1B	PACR.3	PACR.2	PACR.1	PACR.0	R/W	Set PORTA to be output port	0000
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	Set PORTB to be output port	0000
$1D	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	Set PORTC to be output port	0000
$1E	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	Set PORTD to be output port	0000
$1F	-	-	-	-	-	Reserved	-

System Register 0DH

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0DH	-	ELON	B1	B0	R R/W	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive Bit2: EL-LIGHT on	Pull low Pull high 0
	X	X	1	0			Yes
	X	X	0	0		B1 bond to GND	
	X	X	1	1		B0 bond to V_{DD}	
	X	X	0	1		B1 bond to GND & B0 bond to V_{DD}	



SH66N12 Bonding Option

Up to 4 different bonding options are available for user's choices. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

System Register 13

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power on
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as ALARM output Bit1: heavy load mode Bit2: LCD display Control Bit3: R-F convert counter on	0100
	X	X	X	0		PORTA.1, PORTA.2 as I/O port	Yes
	X	X	X	1		PORTA.1, PORTA.2 as ALARM output	
	X	X	0	X		No heavy load	Yes
	X	X	1	X		HEAVY LOAD mode	
	X	0	X	X		LCD signal on	
	X	1	X	X		LCD signal off	Yes
	0	X	X	X		R-F convert counter off	Yes
	1	X	X	X		R-F convert counter on	

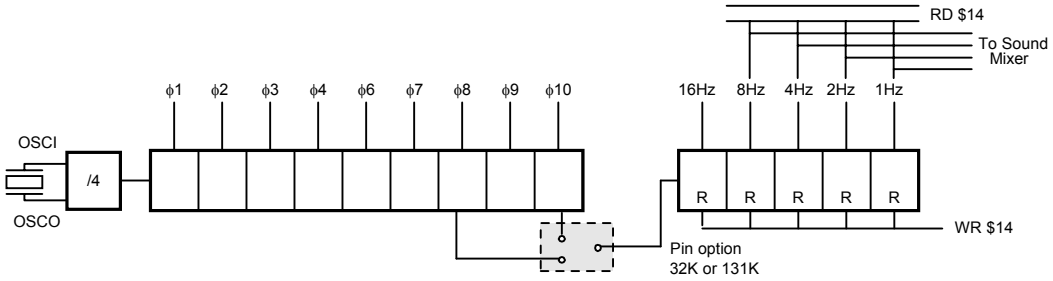
HEAVY LOAD Mode (HLM): This mode is designed for the 32KHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

System Register 14, AEC:

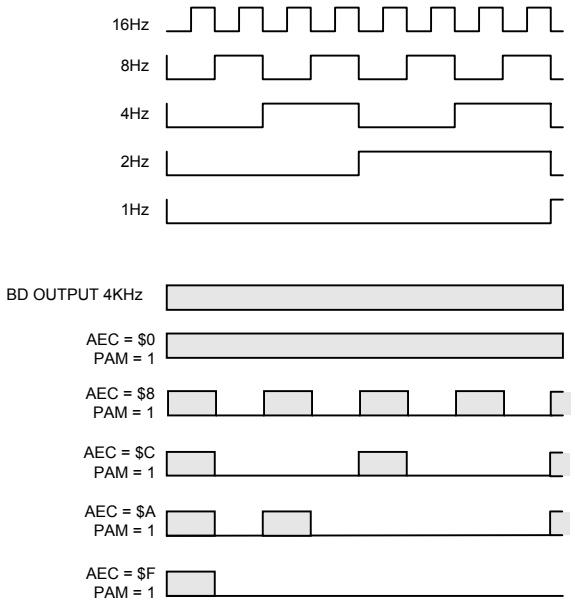
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control	
	0	0	0	0		DC envelope	Yes
	X	X	X	1		1Hz envelope	
	X	X	1	X		2Hz envelope	
	X	1	X	X		4Hz envelope	
	1	X	X	X		8Hz envelope	

The alarm carrier frequency is 4KHz.
WRITE mode: control the envelope selection.
READ mode can read out current envelope waveforms.

Below is the ALARM functional block equivalent circuit diagram. To activate the ALARM function, first to switch the PAM to ALARM OUTPUT mode. After setting PAM equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time. The programmer can read back the envelope from AEC register and make any pattern changes as needed by the programmer. The Read operation will not affect the alarm output waveform.



The programming alarm waveform is shown below:



System Register 15

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description	Power on
$15	PPULL	O/S2	O/S1	DUTY	R/W		0000
	X	X	X	0		LCD driver = 1/3 duty, 1/2 bias	Yes
	X	X	X	1		LCD driver = 1/4 duty, 1/3 bias	
	X	X	0	X		PORTC as I/O ports	Yes
	X	X	1	X		PORTC as LCD segment27 - 30	
	X	0	X	X		PORTD as I/O ports	Yes
	X	1	X	X		PORTD as LCD segment31 - 34	

4. LCD Driver

The LCD driver contains a controller, voltage generator, 4 common signal pins, and 34 segment driver pins. There are two different driving modes that are programmable, one is 1/4 duty and 1/3 bias, the other is 1/3 duty and 1/2 bias (COM4 same as COM1). DRIVING mode is controlled by register 15 and the power-on status is 1/3 duty, 1/2 bias. The controller consists of display data RAM and a duty generator.

The LCD data RAM is a dual port RAM that transfers data to segment pins automatically without a program control.

PORTC, PORTD can be used as LCD SEG27 - 34. It's selected by bit2 and bit1 of the system register 15. When used as I/O ports, the data in LCD RAM won't affect the I/O input and output data. Also, when used as LCD output, the data of I/O RAM won't affect LCD output. LCD RAM can be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM is the same as before executing the "STOP" instruction.

When the LCD is off, both COMMON and SEGMENT output low.

Configuration of LCD RAM Area: (Segments 1 - 34, 1/4duty)

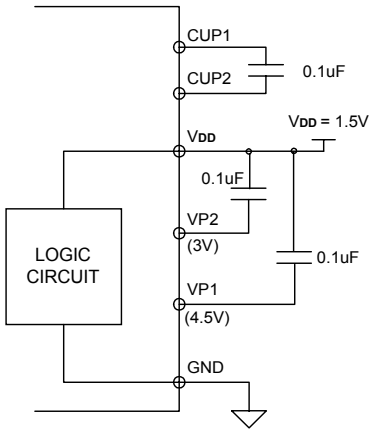
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	311H	SEG18	SEG18	SEG18	SEG18
301H	SEG2	SEG2	SEG2	SEG2	312H	SEG19	SEG19	SEG19	SEG19
302H	SEG3	SEG3	SEG3	SEG3	313H	SEG20	SEG20	SEG20	SEG20
303H	SEG4	SEG4	SEG4	SEG4	314H	SEG21	SEG21	SEG21	SEG21
304H	SEG5	SEG5	SEG5	SEG5	315H	SEG22	SEG22	SEG22	SEG22
305H	SEG6	SEG6	SEG6	SEG6	316H	SEG23	SEG23	SEG23	SEG23
306H	SEG7	SEG7	SEG7	SEG7	317H	SEG24	SEG24	SEG24	SEG24
307H	SEG8	SEG8	SEG8	SEG8	318H	SEG25	SEG25	SEG25	SEG25
308H	SEG9	SEG9	SEG9	SEG9	319H	SEG26	SEG26	SEG26	SEG26
309H	SEG10	SEG10	SEG10	SEG10	31AH	SEG27	SEG27	SEG27	SEG27
30AH	SEG11	SEG11	SEG11	SEG11	31BH	SEG28	SEG28	SEG28	SEG28
30BH	SEG12	SEG12	SEG12	SEG12	31CH	SEG29	SEG29	SEG29	SEG29
30CH	SEG13	SEG13	SEG13	SEG13	31DH	SEG30	SEG30	SEG30	SEG30
30DH	SEG14	SEG14	SEG14	SEG14	31EH	SEG31	SEG31	SEG31	SEG31
30EH	SEG15	SEG15	SEG15	SEG15	31FH	SEG32	SEG32	SEG32	SEG32
30FH	SEG16	SEG16	SEG16	SEG16	320H	SEG33	SEG33	SEG33	SEG33
310H	SEG17	SEG17	SEG17	SEG17	321H	SEG34	SEG34	SEG34	SEG34

Configuration of LCD RAM Area: (Segments 1 - 34, 1/3duty)

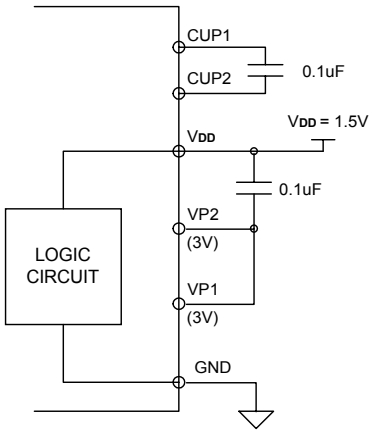
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
300H	-	SEG1	SEG1	SEG1	311H	-	SEG18	SEG18	SEG18
301H	-	SEG2	SEG2	SEG2	312H	-	SEG19	SEG19	SEG19
302H	-	SEG3	SEG3	SEG3	313H	-	SEG20	SEG20	SEG20
303H	-	SEG4	SEG4	SEG4	314H	-	SEG21	SEG21	SEG21
304H	-	SEG5	SEG5	SEG5	315H	-	SEG22	SEG22	SEG22
305H	-	SEG6	SEG6	SEG6	316H	-	SEG23	SEG23	SEG23
306H	-	SEG7	SEG7	SEG7	317H	-	SEG24	SEG24	SEG24
307H	-	SEG8	SEG8	SEG8	318H	-	SEG25	SEG25	SEG25
308H	-	SEG9	SEG9	SEG9	319H	-	SEG26	SEG26	SEG26
309H	-	SEG10	SEG10	SEG10	31AH	-	SEG27	SEG27	SEG27
30AH	-	SEG11	SEG11	SEG11	31BH	-	SEG28	SEG28	SEG28
30BH	-	SEG12	SEG12	SEG12	31CH	-	SEG29	SEG29	SEG29
30CH	-	SEG13	SEG13	SEG13	31DH	-	SEG30	SEG30	SEG30
30DH	-	SEG14	SEG14	SEG14	31EH	-	SEG31	SEG31	SEG31
30EH	-	SEG15	SEG15	SEG15	31FH	-	SEG32	SEG32	SEG32
30FH	-	SEG16	SEG16	SEG16	320H	-	SEG33	SEG33	SEG33
310H	-	SEG17	SEG17	SEG17	321H	-	SEG34	SEG34	SEG34

Connection Diagram

1. V_{DD} = 1.5V, 4.5V LCD, 1/4 duty, 1/3bias



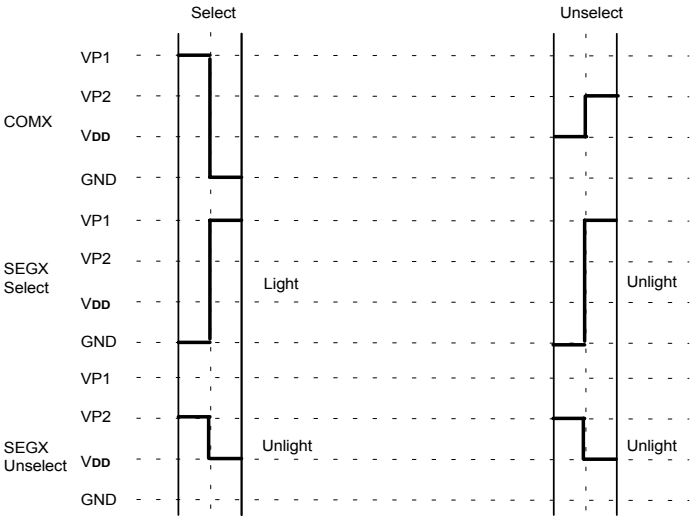
2. V_{DD} = 1.5V, 3V LCD, 1/3 duty, 1/2bias

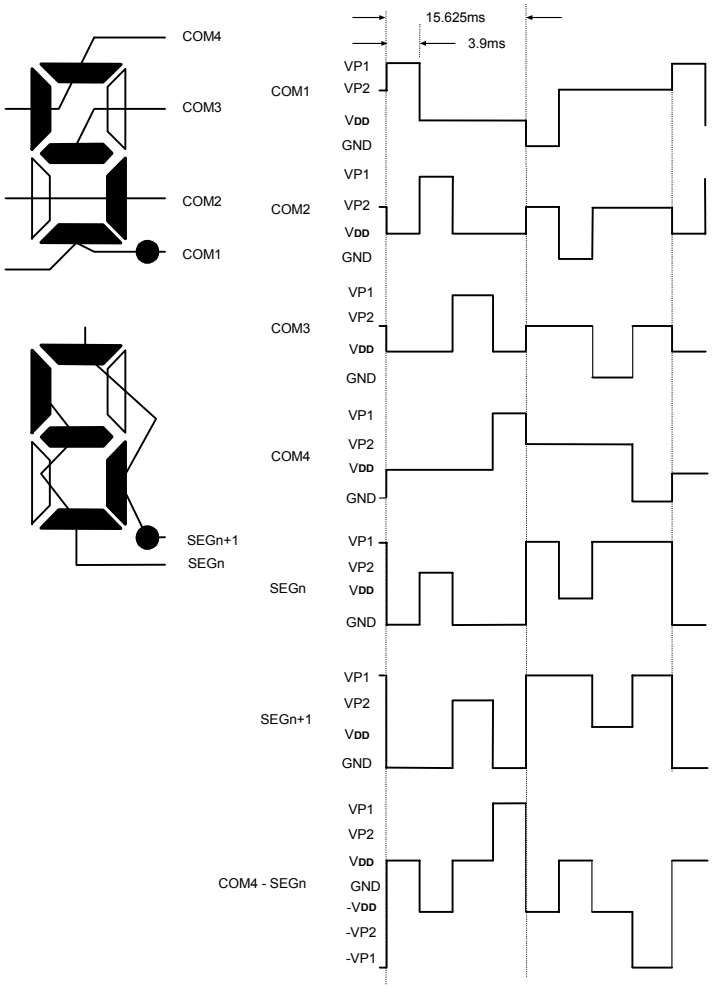


Notice:

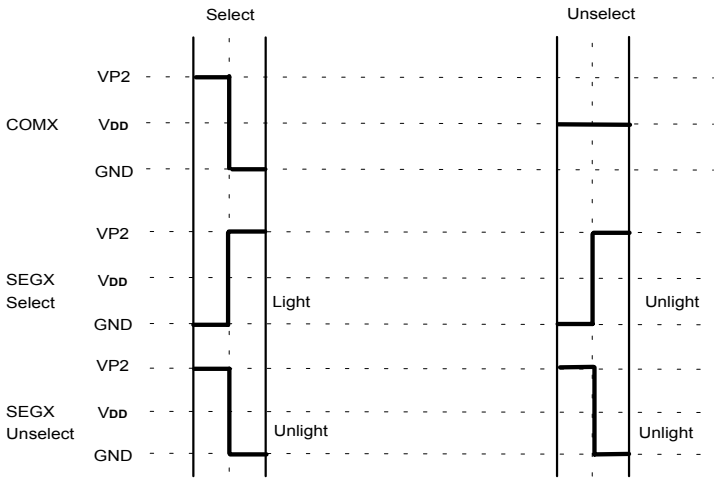
The pump circuit frequency would be 8KHz under 32768Hz Crystal or 131KHz RC oscillator.
The pump circuit will always work, whenever the LCD display is ON or OFF. (The pump circuit only stops at STOP mode)

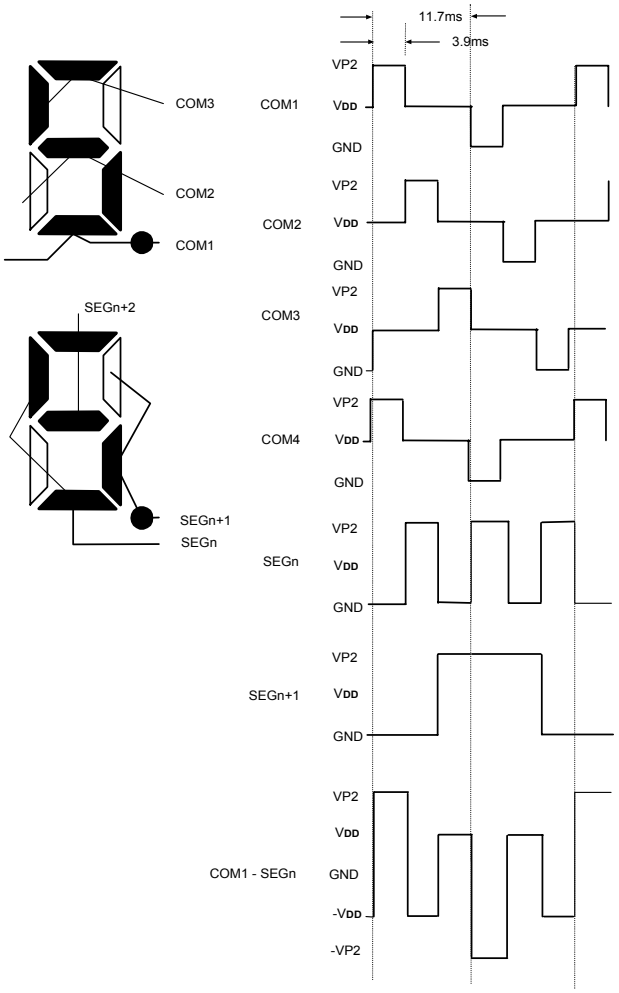
1/4 Duty, 1/3 Bias LCD Waveform (V_{DD} = 1.5V, VP1 = 4.5V, VP2 = 3V)





1/3 Duty, 1/2 Bias LCD Waveform (V_{DD} = 1.5V, VP1 = VP2 = 3V)

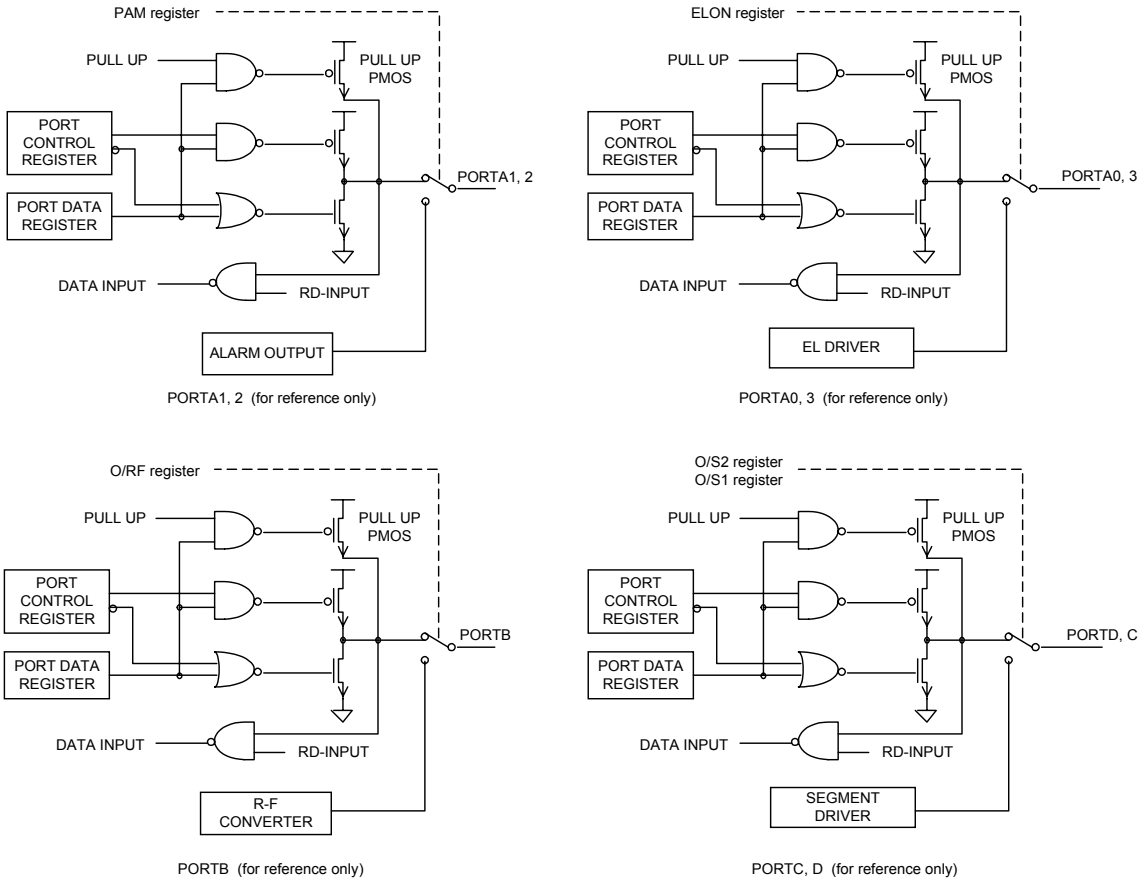




I/O Port

The SH66N12 has 16 CMOS I/O ports: PORTA, PORTB, PORTC and PORTD. Each I/O pins contains pull-up MOS controllable by program. The PORT control register (PACR, PBCR, PCCR, and PDCR) controls ON/OFF buffer of the output buffer. These I/O ports can be accessed by read/write system register. And users can output any value to any I/O port bit at any time.

PORTA, B, C, D



When PAM = 1 (system register 13H bit0) is set, the PA.0 & PA.1 are used as alarm outputs. When ELON = 1 (system register 0DH bit2) is set, the PA.0 & PA.1 are used as EL-LIGHT drivers. When O/S1 (system register 15H bit1) and O/S2 (system register 15H bit2) = 1 are set, the PORTC & PORTD are used as LCD SEGMENT outputs, and writing data into PC.X (system register 0AH), PD.X (system register 0BH) won't affect LCD output data. Writing O/RF (system register 13H bit3) = 1, and PORTB is used as R-F converter.

Controlling the Pull-up MOS

These ports contain pull-up MOS controlled by program. System register 15H bit3 (PPULL) controls ON/OFF of all pull-up MOS simultaneously. The pull-up MOS is also controlled by the port data registers (PA, PB, PC, and PD) of each port. (Writtng 0 could turn off the pull-up MOS) So, the pull-up MOS can be turned ON/OFF individually.

Port Interrupt

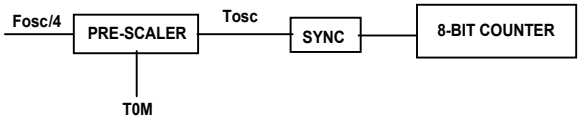
PORTB, PORTC interrupts (falling edge) are not controlled by Port I/O register. It means that if an interrupt request (IEx is set to 1 & one port bit high go low) has been touched and that the condition of the other port bits are high level whenever the port bit is output or input. When the PORTB is used as a R-F converter (O/RF = 1), the PORTB interrupt is disabled. And when PORTC is used as an LCD output (O/S1 = 1), the PORTC interrupt is also disabled.

External $\overline{\text{INT}}$

PortA.0 is shared by external interrupts (active low). When PortA.0 is used as ELP, the External $\overline{\text{INT}}$ is disabled even the IEX is set to 1.

Timer

The SH66N12 has two 8-bit timers. Their operation is counting - up. The timers consist of an 8-bit counter and an 8-bit preload register.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

Timer0 and Timer1 Configuration and Operation

Both of the Timer0 and Timer1 consist an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H), and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

Timer Mode Register:

The low-order digit should be written first, and then the high-order digit. The timer counter is loaded with contents of the load register automatically when the high order digit is written or count overflow happens. The timer overflow will generate an interrupt if the interrupt enable flag is set.

The timer can be programmed in several different system clock sources by setting the Timer Mode register (TM0, TM1).

Timer Load Register:

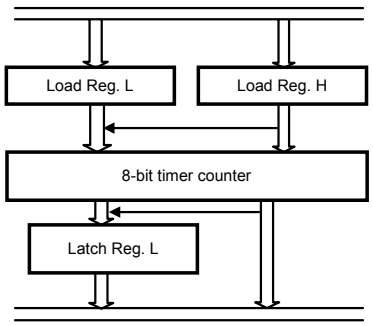
Since the register H controls the physical READ and WRITE operations, please follow these steps:

Write Operation:

Low nibble first;
High nibble to update the counter

Read Operation:

High Nibble first;
Low nibble followed.



The 8-bit counter counts prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 4-bit registers used for the timer control as shown in table1 and table 2. These mode registers select the input pulse sources into the timer.

Table 1: Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

Table 2: Timer1 Mode Register ($03)

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

Interrupt

Four interrupt sources are available on SH66N12:

- External interrupt ($\overline{INT}$ share with PA.0)
- Timer0 interrupt
- Timer1 interrupt
- Port's falling edge detection interrupt ($\overline{PBC}$)

The Configuration of System Register $00:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags

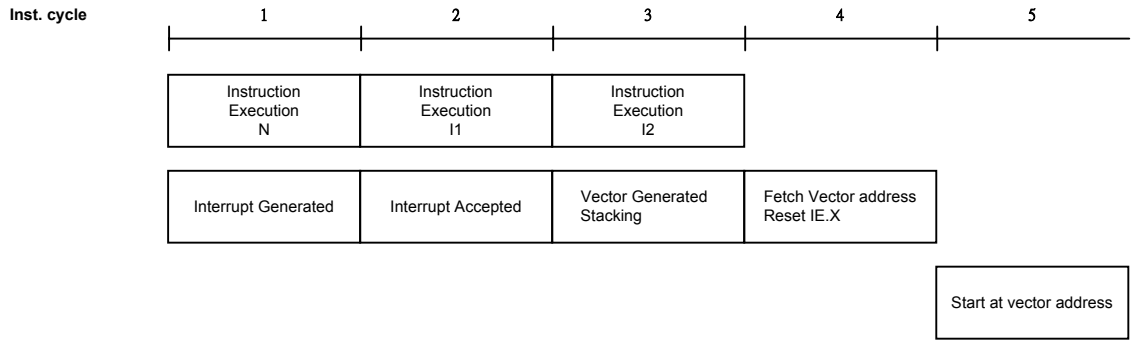
External Interrupt ($\overline{INT}$)

External interrupt is shared with the bit0 of PORTA. When bit3 of system register 0 (IEX) is set to 1, the external interrupt will be enabled, and a falling edge signal on PA.0 will generate an external interrupt. (Note: while external interrupt is enabled, writing a "0" to bit0 of PORTA will generate an external interrupt.)

Timer0, Timer1 Interrupt, Port Interrupt and I/O Ports

The input clock of Timer0 and Timer1 are based on OSC clock. The programming of Timer interrupt, Port interrupts and I/O ports refer to SH6610C SPEC.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, users can enable any INTERRUPT enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the execution of the next two instructions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

System Clock

The SH66N12 has one clock source. OSC1 is 32.768KHz crystal or 131KHz RC determined by OSC_OPT pad option.

Default is 131K RC oscillation. And 32k crystal oscillation is selected by OSC_OPT pad connects to GND.

The OSC generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals (TIMER0, TIMER1, LCD).

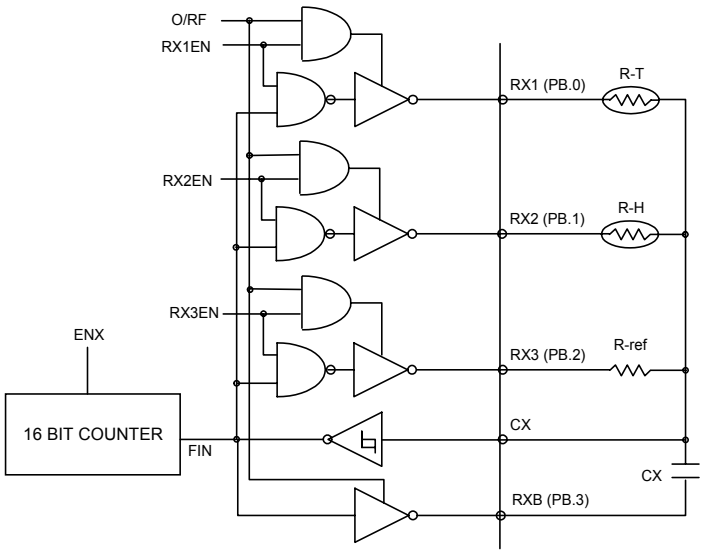
Resistor to Frequency Converter

System Register 0CH & 15H

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$0C	O/RF	RX3EN	RX2EN	RX1EN	R/W	Bit0: count resister1 Bit1: count resister2 Bit2: count resister3 Bit3: set PORTB.0 - 3 as R-F converter	0000
$13	ENX	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mode Bit2: LCD off Bit3: R-F convert counter on	0100
$17	RFL.3	RFL.2	RFL.1	RFL.0	R/W	R-F counter register low nibble	0000
$18	RFML.3	RFML.2	RFML.1	RFML.0	R/W	R-F counter register middle_low nibble	0000
$19	RFMH.3	RFMH.2	RFMH.1	RFMH.0	R/W	R-F counter register middle_high nibble	0000
$1A	RFH.3	RFH.2	RFH.1	RFH.0	R/W	R-F counter register high nibble	0000

When the settings of O/RF = 1, PORTB are used as R-F converter. It's like a RC oscillation circuit, and uses the 16-bit counter to get the resistive value of the sensor. First to set RX1EN = 1 (enable RX1-F convert), and then start timer1 or timer0 counter and set ENX = 1 (start R-F counter). When timer1 or timer0 INT occurs, we can get the value of the RX1-F counter. So, we can get different count values of R-T, R-H, R-ref by setting the RX1EN, RX2EN, RX3EN = 1 in turn.

The R-F converter could keep on working in the HALT mode, and would stop automatically when the "STOP" instruction is executed. (Keep the last state of RX1-3 ports and stop the R-F counter.)



R-F CONVERTER

Temperature sensor resistor: 10K - 50K @25℃ (for reference only)
Humidity sensor: 60K @25℃, 50%RH (for reference only)

Notice:

1. When O/RF is set to 1, the PORTB interrupt is disabled.
2. Connect CX to V_{DD} or GND when the R-F converter is not used.
3. The 16-bit counter can be used as an event counter when the R-F converter is not used.
4. Max-frequency of R-F converter should be less than 2MHz.

EL-LIGHT

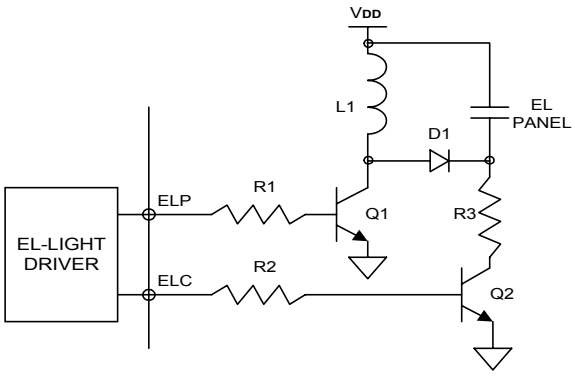
System Register 0DH, 16H

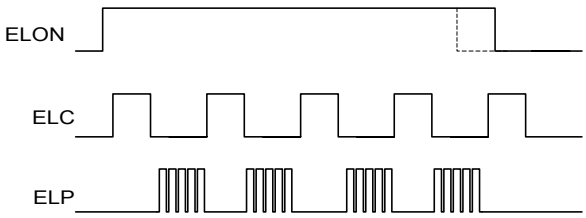
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$0D	-	ELON	B1	B0	R R/W	Bit0,1: Bonding option Bit2: EL-LIGHT on/off control. (initial off)	010
$16	ELF	ELPF	-	-	R/W	EL-LIGHT mode control Bit2: ELP driver output frequency control Bit3: EL-LIGHT driver frequency select	00

ELPF: (frequency of ELP pin charge waveform)
0 ELCLK
1 ELCLK/2
(ELCLK = 32KHz @32KHz Oscillator or 131KHz/4 @131KHz RC Oscillator by code option.)

ELF: (frequency of ELC pin discharge waveform)
0 ELCLK/64
1 ELCLK/32

Set the system register 0DH to select the EL-LIGHT driver waveform. Setting ELON = 1 will turn on the EL-LIGHT driver. ELC and ELP will output driver waveform automatically as shown in the diagram below. With external transistor, diode, inductance and resistor, we can pump the EL panel to AC 100 - 250V.





ELP: Output for EL charge
ELC: Output for EL discharge

While the EL-LIGHT is turned on, the ELC will be turned on before the ELP is on. When EL-LIGHT is turned off, the ELP will turn off first, then ELC will still work for one cycle to make sure that there is no voltage left on EL panel.

EL-LIGHT would keep on working in the HALT mode. But it will be turned off after the "STOP" instruction is executed (ELC & ELP keep low).

Notice:

1. When PORTA.0 and PORTA.3 are used as the EL driver, the data of PA.0 & PA.3 ($08H bit0 & 3) must be set to 0.
2. Please turn on the HLM (heavy-load mode) before turning on the EL-LIGHT.
3. Please turn off the EL-LIGHT before executing the “STOP” instruction.

One Time PROM (OTP) Pin Assignment

Name	I/O	Description
V_{DD}	P	+5.0V System Power Supply
V_{PP}	P	+12.0V Programming voltage supply shared with TEST
CE	I	Chip enable. Shared with $\overline{\text{RESET}}$
OE	I	Data Output enables. Shared with PORTD [3]
PGMB	I	Programming pulse control. Shared with PORTD [2]
OSCI	I	Clock for address increasing, Data latching and shifting clock for data verification
DATA	I/O	Data input for programming and data output for verification Shared with PORTD [1]
GND	P	Ground pin

Instructions

All instructions are one-cycle and one-word instructions, having the characteristic of the memory-oriented operation.
Arithmetic and Logical Instruction.

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM memonic is EORI. However, EORI has the operation identical with EORIM. Same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC;Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC;Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC,Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage. . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	
Operating Current	I_{OP}		6	9	μA	All output pins unload execute NOP instruction, exclude LCD, EL, R-F & Alarm current.
Standby Current	I_{SB1}		2	4	μA	All output pins unload (HALT mode) exclude LCD current. (Not heavy load mode)
Standby Current	I_{SB2}			0.5	μA	All output pins unload (STOP mode), LCD off
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3		0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input Low Voltage	V_{IL2}	GND - 0.3		0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}			V	PORTC, PORTD (I_{OH} = -8μA)
Output Low Voltage	V_{OL1}			0.2 X V_{DD}	V	PORTC, PORTD (I_{OL} = 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}			V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC,ELP (set PA.0, PA.3 to be EL driver), I_{OH} = -0.3mA
Output Low Voltage	V_{OL2}			0.2 X V_{DD}	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC,ELP (set PA.0, PA.3 to be EL driver), I_{OL} = 0.3mA
Output High Voltage	V_{OH3}	0.8 X V_{DD}			V	PORTB (I_{OH} = -2.4mA) @1.2V
Output Low Voltage	V_{OL3}			0.2 X V_{DD}	V	PORTB (I_{OH} = 2.4mA) @1.2V
Output High Voltage	V_{OH4}	V_{P1} - 0.2			V	SEGx, I_{OH} = -3μA
Output Low Voltage	V_{OL4}			0.2	V	SEGx, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P2} - 0.2			V	COMx, I_{OH} = -8μA
Output Low Voltage	V_{OL5}			0.2	V	COMx, I_{OL} = 8μA
Pull-up Resistor	R_P		150		KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
LCD Lighting	I_{LCD}			1	μA	No panel loaded

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, F_{OSC} = 131KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	
Operating Current	I_{OP}		25	40	μA	All output pins unload execute NOP instruction, exclude LCD, EL, R-F & Alarm current
Standby Current	I_{SB1}		10	15	μA	All output pins unload (HALT mode) exclude LCD current. (Not heavy load mode.)
Standby Current	I_{SB2}			0.5	μA	All output pins unload (STOP mode), LCD off, no current
Reset Current	I_{REST}			20	μA	Reset current.
Input High Voltage	V_{IH1}	0.8 X V_{DD}		V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input High Voltage	V_{IH2}	0.85 X V_{DD}		V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Input Low Voltage	V_{IL1}	GND - 0.3		0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD OSCI (Driven by external clock) (reference only)
Input Low Voltage	V_{IL2}	GND - 0.3		0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST, CX (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}			V	PORTC, PORTD (I_{OH} = -8μA)
Output Low Voltage	V_{OL1}			0.2 X V_{DD}	V	PORTC, PORTD (I_{OL} = 0.3mA)
Output High Voltage	V_{OH2}	0.8 X V_{DD}			V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC, ELP (set PA.0, PA.3 to be EL driver), I_{OH} = - 0.3mA
Output Low Voltage	V_{OL2}			0.2 X V_{DD}	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), ELC, ELP (set PA.0, PA.3 to be EL driver), I_{OL} = 0.3mA
Output High Voltage	V_{OH3}	0.8 X V_{DD}			V	PORTB (I_{OH} = -2.4mA) @1.2V
Output Low Voltage	V_{OL3}			0.2 X V_{DD}	V	PORTB (I_{OH} = 2.4mA) @1.2V
Output High Voltage	V_{OH4}	V_{P1} - 0.2			V	SEGx, I_{OH} = -3μA
Output Low Voltage	V_{OL4}			0.2	V	SEGx, I_{OL} = 3μA
Output High Voltage	V_{OH5}	V_{P1} - 0.2			V	COMx, I_{OH} = -8μA
Output Low Voltage	V_{OL5}			0.2	V	COMx, I_{OL} = 8μA
Pull-up Resistor	R_P		150		KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
LCD Lighting	I_{LCD}			1	μA	No panel loaded

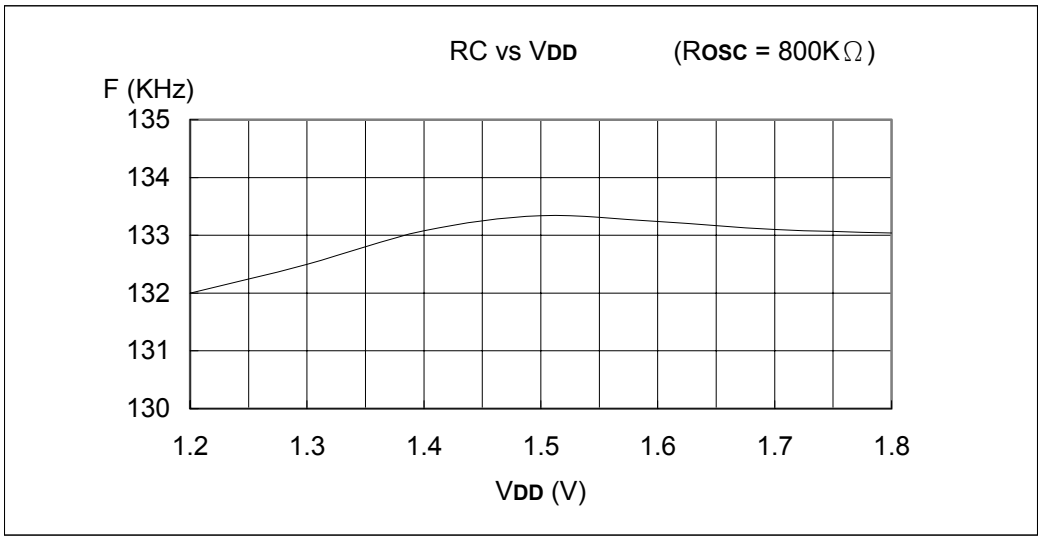
AC Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	T_{STT}		1	2	S	

AC Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, F_{OSC} = 131KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Variation (RC)	Δ F/F			±30	%	Include supply voltage and chip to chip variation

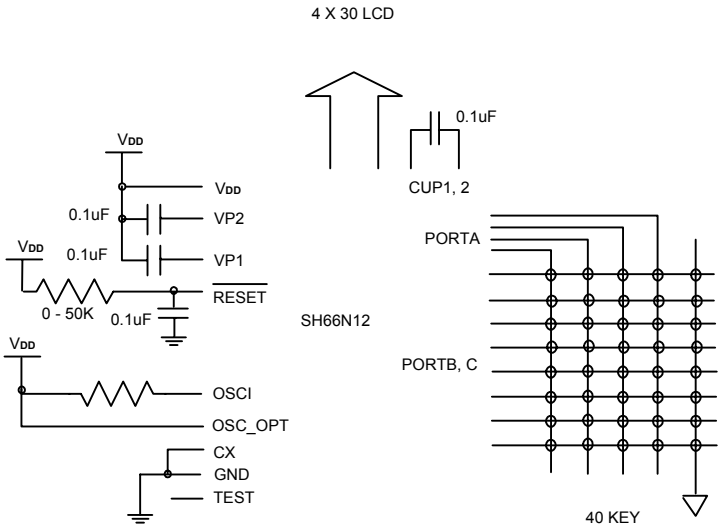
Typical V_{DD} vs. Frequency of RC Oscillator (OSC): (for reference only)



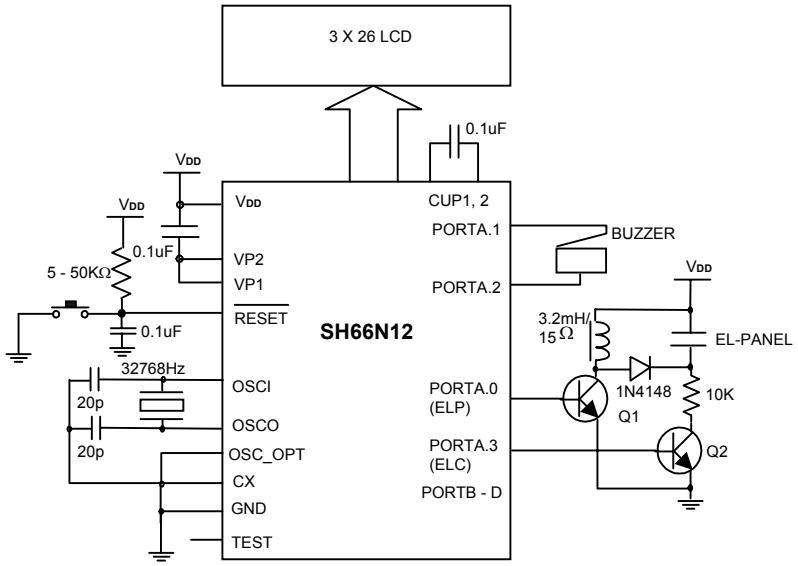
Application Circuits (for reference only)

SH66N12 chip substrate connects to system ground.

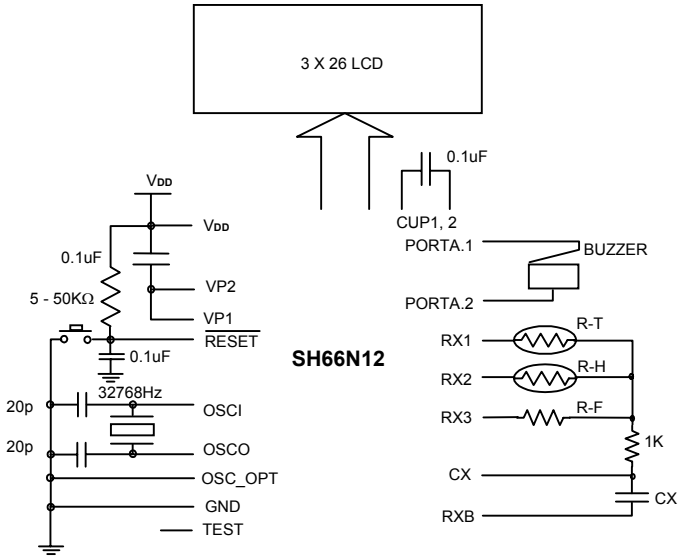
AP1: V_{DD} = 1.5V
OSC: RC: 131K (pad option)
LCD: 4.5V, 1/4 duty, 1/3 bias, PORTD used as segment
PORTA - C: I/O



AP2: V_{DD} = 1.5V
OSC: 32.768KHz crystal (pad option)
LCD: 3V, 1/3 duty, 1/2 bias
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2KHz or 4KHz selected by code option)
PORTA.0, PORTA.3: EL-LIGHT driver.
PORTB - D: I/O

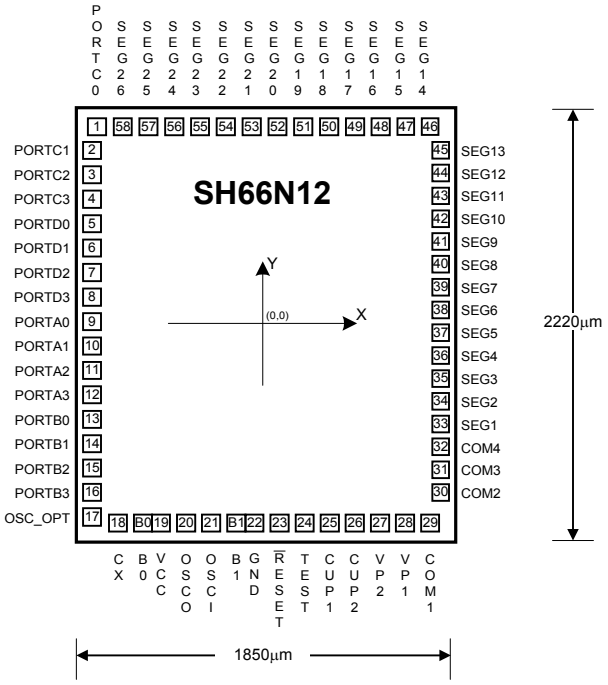


AP3: V_{DD} = 1.5V
OSC: 32.768KHz crystal (pad option)
LCD: 3V, 1/3 duty, 1/2 bias
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2KHz or 4KHz selected by code option)
PORTA.0, PORTA.3 & PORTC, D: I/O
PORTB: R-F Converter



R-T: Temperature Sensor
R-H: Humidity Sensor
R-F: Reference Resister
CX: R-F converter capacitor

Bonding Diagram



Pad Location

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTC0	-791.2	982.5	20	OSCO	-341.4	-982.5
2	PORTC1	-799	847.45	21	OSCI	-231.4	-982.5
3	PORTC2	-799	717.45		B1	-121.4	-982.5
4	PORTC3	-799	592.45	22	GND	-33.9	-982.5
5	PORTD0	-799	472.45	23	$\overline{\text{RESET}}$	76.1	-982.5
6	PORTD1	-799	357.45	24	TEST	193.2	-982.5
7	PORTD2	-799	242.45	25	CUP1	310.3	-982.5
8	PORTD3	-799	127.45	26	CUP2	420.3	-982.5
9	PORTA0	-799	12.45	27	VP2	530.3	-982.5
10	PORTA1	-799	-102.55	28	VP1	648.8	-982.5
11	PORTA2	-799	-217.55	29	COM1	773.8	-982.5
12	PORTA3	-799	-332.55	30	COM2	799	-827.5
13	PORTB0	-799	-447.55	31	COM3	799	-707.5
14	PORTB1	-799	-567.55	32	COM4	799	-592.5
15	PORTB2	-799	-692.55	33	SEG1	799	-482.5
16	PORTB3	-799	-817.55	34	SEG2	799	-372.5
17	OSC_OPT	-799	-947.55	35	SEG3	799	-262.5
18	CX	-669	-982.5	36	SEG4	799	-152.5
	B0	-548.45	-982.5	37	SEG5	799	-42.5
19	VCC	-460.95	-982.5	38	SEG6	799	67.5

Pad Location (Continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
39	SEG7	799	177.5	49	SEG17	394.8	982.5
40	SEG8	799	287.5	50	SEG18	279.8	982.5
41	SEG9	799	397.5	51	SEG19	164.8	982.5
42	SEG10	799	507.5	52	SEG20	49.8	982.5
43	SEG11	799	617.5	53	SEG21	-65.2	982.5
44	SEG12	799	732.5	54	SEG22	-180.2	982.5
45	SEG13	799	852.5	55	SEG23	-295.2	982.5
46	SEG14	775.8	982.5	56	SEG24	-410.2	982.5
47	SEG15	645.8	982.5	57	SEG25	-531.2	982.5
48	SEG16	515.8	982.5	58	SEG26	-661.2	982.5

Ordering Information

Part No.	Package	Packing
SH66N12H-yyxxx/000HR	Chip Form	Tray

Note:

(1) "-yyxxx": "yy" means 2 bits option and "xxx" means 3 bits code seriary number. If the product is OTP type and in blank order, those bits should be none.
(2) The data after mark "/" in Part No. block is the package and packing information for ordering.
(3) Any other package or packing request, please refer to following table.

Package		Packing	
D	DIP	**R**	Normal package size and in tray packing
F	QFP	**U**	Normal package size and in tube packing
H	CHIP	**A**	Normal package size and in tape & reel packing
J	CER-DIP	**D**	Larger package size and in tray packing
K	SKINNY	**L**	Larger package size and in tube packing
L	PLCC	**B**	Larger package size and in tape & reel packing
M	SOP	**T**	Smaller package size and in tray packing
N	OTHER	**S**	Smaller package size and in tube packing
Q	GOOD DIE ON WAFER	**N**	Smaller package size and in tape & reel packing
S	SOJ		
T	TO92		
V	VSOP/TSOP		
W	WAFER		
X	TSSOP		

Data Sheet Revision History

Version	Content	Date
2.0	Add package and packing information in ordering information	Jul.2004
1.0	Original	Jan. 2004