# SH66P13A

## OTP 4-bit Microcontroller with LCD Driver

### Features

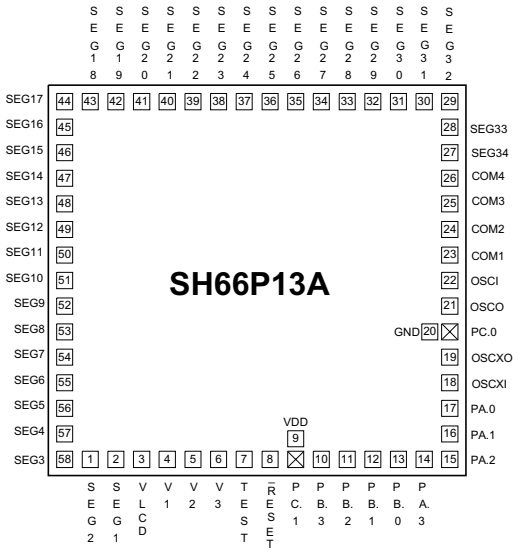
- SH6610C-based single-chip 4-bit microcontroller
- OTPROM: 4096 X 16 bits
- RAM: 512 X 4 bits (System & Data memory)
- Operation voltage: 2.5V - 6.0V
- 8 CMOS bi-directional I/O pins
- 4-Level subroutine nesting (include interrupts)
- One 8-bit auto re-load timer/counter
- 8-bit Base timer
- Powerful interrupt sources:
  - External interrupts ($\overline{INT0}$)
  - Internal interrupt (Timer0)
  - Internal interrupt (Base Timer)
  - Port's falling edge interrupt: PORTB ($\overline{INT1}$)
- LCD driver:
  - 240 dots (1/8 duty 1/4 bias)
  - 136 dots (1/4 duty 1/3 bias)
- LCD used as scan output
- Built-in dual tone PSG with one noise generator
- 2 Clock source
  OSC: (code option)
  - Crystal oscillator 32.768K
  - RC oscillator: 262K

  OSCX: (system register select)
  - Ceramic oscillator 455K
  - RC oscillator 1.8M or 2M
- Instruction cycle time:
  - 122.07μs for 32.768 KHz crystal
  - 15.27μs for 262 KHz RC
  - 8.79μs for 455KHz ceramic
  - 2.22μs for 1.8 MHz RC
  - 2μs for 2.0 MHz RC
- Two low power operation mode: HALT and STOP
- Low power consumption
- Warm up timer for power on reset

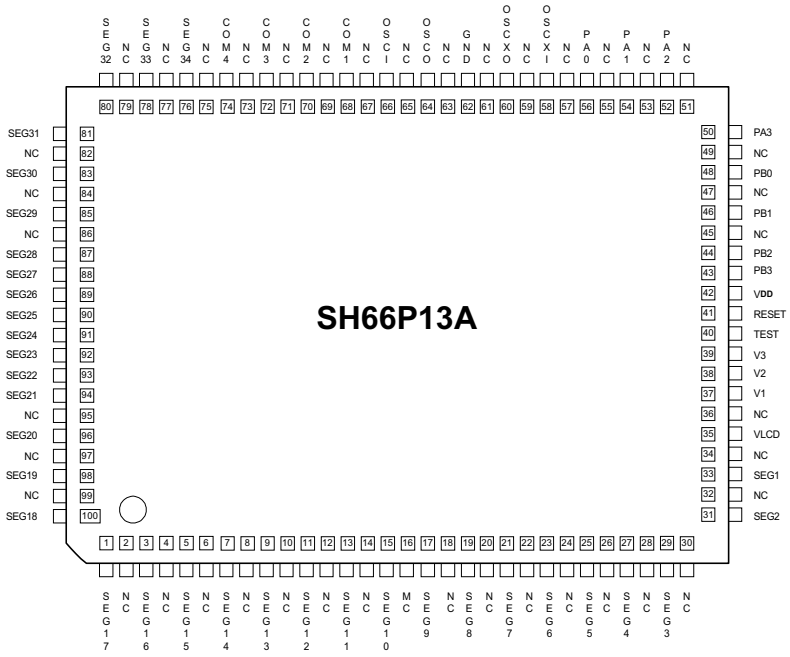
### General Description

SH66P13A is a single chip microcontroller integrated with SRAM, OTP ROM, Timer and Dual-tone PSG, LCD driver and I/O port. This chip builds in a dual-oscillator to enhance the total chip performance.

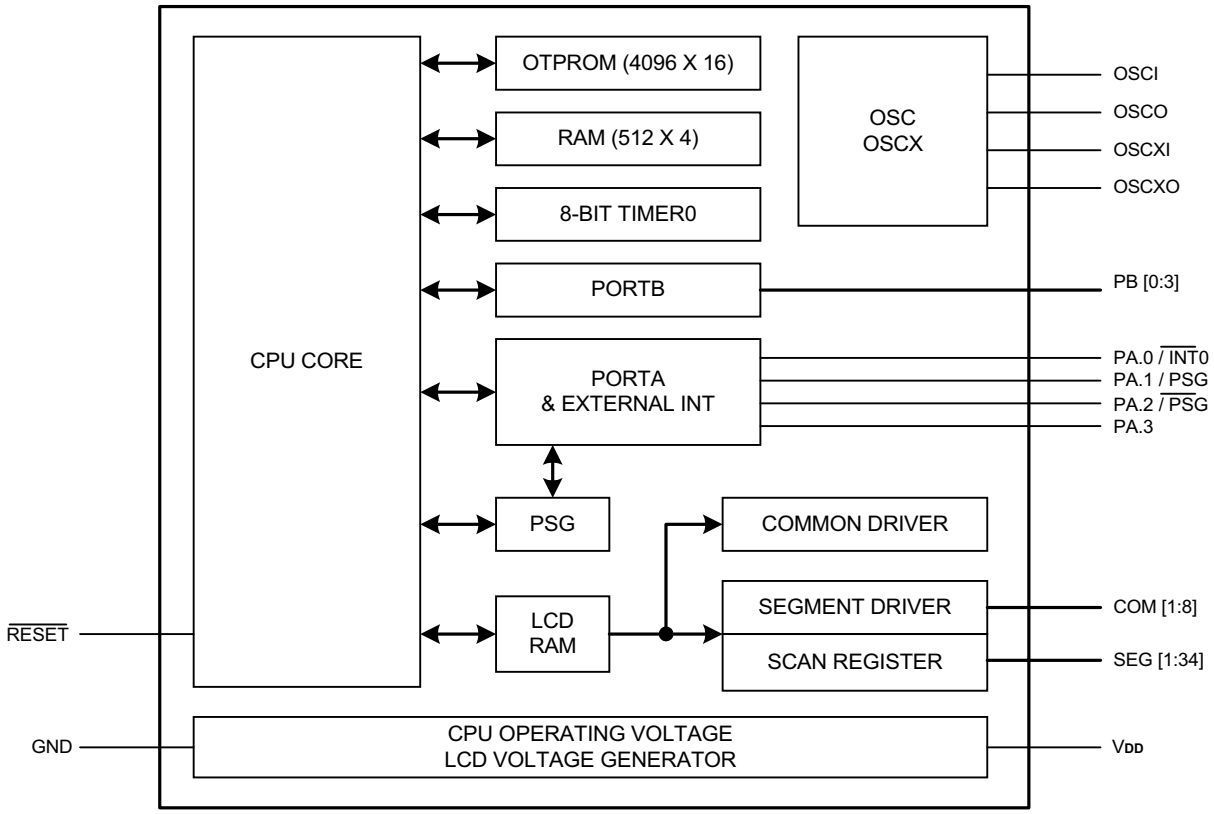
### Pad Configuration



## Pin Configuration




## Block Diagram



## Pad Description

| Pad No. | Designation | I/O | Description |
|---|---|---|---|
| 1, 2, 31 - 58 | SEG1 - SEG30 | O | Segment signal output for LCD display;<br>Share with scan output |
| 3 - 6 | $V_{LCD}$, V1, V2, V3 | I | Connect with external LCD divided resistance |
| 7 | TEST | I | Test pin (Internal pull-low). No connect for user |
| 8 | $\overline{RESET}$ | I | Reset input (No internal pull-up) |
| 9 | $V_{DD}$ | P | Power supply |
| 10 - 13 | Port B.3 - Port B.0 | I/O | Bit programmable I/O, Vector interrupt ( $\overline{INT1}$ ) |
| 14 - 17 | Port A.3 - Port A.0 | I/O | Bit programmable I/O, PA.0 shared with $\overline{INT0}$<br>PA.1, PA.2shared with PSG output<br>In the program mode, PA.1 shared with DATA, PA. 2 shared with PINPGMB, PA. 3 shared with PINOE |
| 18 | OSCXI | I | Oscillator X input pin |
| 19 | OSCXO | O | Oscillator X output pin |
| 20 | GND | P | Ground pin |
| 21 | OSCO | O | Oscillator output pin |
| 22 | OSCI | I | Oscillator input pin |
| 23 - 26 | COM1 - COM4 | O | Common signal output for LCD display |
| 27 - 30 | COM5 - COM8/SEG34 - SEG31 | O | Common/segment signal output for LCD display |

## Pin Description

| PIN No. | Designation | I/O | Description |
|---|---|---|---|
| 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33 | SEG17 - SEG1 | O | Segment signal output for LCD display;<br>share with scan output |
| 83, 85, 87 - 94, 96, 98, 100 | SEG30 - SEG18 | O | Segment signal output for LCD display;<br>share with scan output |
| 35, 37 - 39 | $V_{LCD}$, V1, V2, V3 | I | Connect with external LCD divided resistance |
| 40 | TEST | I | Test pin (Internal pull-low). No connect for user |
| 41 | $\overline{RESET}$ | I | Reset input (No internal pull-up) |
| 42 | $V_{DD}$ | P | Power supply |
| 43, 44, 46, 48 | Port B.3 - Port B.0 | I/O | Bit programmable I/O, Vector interrupt ( $\overline{INT1}$ ) |
| 50, 52, 54, 56 | Port A.3 - Port A.0 | I/O | Bit programmable I/O, PA.0 shared with $\overline{INT0}$<br>PA.1, PA.2 shared with PSG output<br>In the program mode, PA.1 shared with DATA, PA. 2 shared with PINPGMB, PA. 3 shared with PINOE |
| 58 | OSCXI | I | Oscillator X input pin |
| 60 | OSCXO | O | Oscillator X output pin |
| 62 | GND | P | Ground pin |
| 64 | OSCO | O | Oscillator output pin |
| 66 | OSCI | I | Oscillator input pin |
| 68, 70, 72, 74 | COM1 - COM4 | O | Common signal output for LCD display |
| 76, 78, 80, 81 | COM5 - COM8/SEG34 - SEG31 | O | Common/segment signal output for LCD display |

## Functional Description

### 1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

(a) PC (Program Counter)

The Program Counter is used to address the 4K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BC);
(2) When executing a subroutine call instruction (CALL);
(3) When an interrupt occurs;
(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

(b) ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decision (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

(c) Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfers between the accumulator and system register, LCD RAM, or data memory can be performed.

(d) Stack

A group of registers used to save the contents of CY & PC (10-0) sequentially with each subroutine call or interrupt. It is organized 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed total for subroutine calls and interrupts.
The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceeds 4, and the bottom of stack will be shifted out.

### 2. OTPROM

The OTPROM can address 4096 words X 16 bits of program area from $000 to $FFF.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

| Address | Instruction | Function |
|---|---|---|
| $000H | JMP Instruction | Jump to RESET service routine |
| $001H | JMP Instruction | Jump to $\overline{\text{INT0}}$ service routine |
| $002H | JMP Instruction | Jump to Timer0 service routine |
| $003H | JMP Instruction | Jump to Base Timer service routine |
| $004H | JMP Instruction | Jump to $\overline{\text{INT1}}$ service routine |

(b) Table Data Reference

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (AC) are placed by an offset address in program ROM. TJMP instruction branches into address ((PC11 - PC8) X ($2^8$) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

### 3. RAM

Built-in SRAM contains general-purpose data memory, LCD RAM, and system registers. They can be directly accessed in one instruction cycle. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(a) Data Memory, LCD RAM, and System Register

The following is the memory allocation map:
$000 - $01F: System register and I/O
$020 - $1FF: Data memory (480 X 4bits, divided into 4 banks)
$300 - $321, $328 - $345, $350 - $36D: LCD RAM space ( 34 X 4 bits)

(b) Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPM (3-bits) and DPL (4-bits). The addressing range can have 128 locations. Pseudo index address (INX) is used to read or write Data memory, and then RAM address bit9-bit0 comes from DPH, DPM and DPL.

(c) Configuration of System Register

| Address | Bit3 | Bit2 | Bit1 | Bit0 | Function | Initial Value | R/W |
|---|---|---|---|---|---|---|---|
| $00 | IEX | IET0 | IEBT | IEP | Interrupt enable flags | 0000 | R/W |
| $01 | IRQX | IRQT0 | IRQBT | IRQP | Interrupt request flags | 0000 | R/W |
| $02 | TM0.3 | TM0.2 | TM0.1 | TM0.0 | Timer0 mode register | 0000 | R/W |
| $03 | BTM.3 | BTM.2 | BTM.1 | BTM.0 | Base timer mode register | 0000 | R/W |
| $04 | T0L.3 | T0L.2 | T0L.1 | T0L.0 | Timer0 load/counter low nibble | 0000 | R/W |
| $05 | T0H.3 | T0H.2 | T0H.1 | T0H.0 | Timer0 load/counter high nibble | 0000 | R/W |
| $06 - $07 | - | - | - | - | Reserved | - | - |
| $08 | PA.3 | PA.2 | PA.1 | PA.0 | PORTA | 0000 | R/W |
| $09 | PB.3 | PB.2 | PB.1 | PB.0 | PORTB | 0000 | R/W |
| $0A | - | - | PC.1 | PC.0 | Bonding option | 01 (default) | R |
| $0B | PACR.3 | PACR.2 | PACR.1 | PACR.0 | Set PORTA to be output port | 0000 | W |
| $0C | PBCR.3 | PBCR.2 | PBCR.1 | PBCR.0 | Set PORTB to be output port | 0000 | W |
| $0D | LPD3 | LPD2 | LPD1 | LPD0 | LPD Enable Control (LPD3 - 0):<br>0101: LPD Enable (Default);<br>1010: LPD Disable | 0101 | W |
| $0E | TBR.3 | TBR.2 | TBR.1 | TBR.0 | Table branch register | 0000 | R/W |
| $0F | INX.3 | INX.2 | INX1 | INX.0 | Index register (INX) | 0000 | R/W |
| $10 | DPL3 | DPL2 | DPL1 | DPL0 | Data pointer for INX low nibble | 0000 | R/W |
| $11 | - | DPM.2 | DPM.1 | DPM.0 | Data pointer for INX middle nibble | 0000 | R/W |
| $12 | - | DPH.2 | DPH.1 | DPH.0 | Data pointer for INX high nibble | 0000 | R/W |
| $13 | PPULL | PAM2 | PAM1 | HLM | Bit1, 2: PA.1 & PA.2 as PSG output or I/O PORT<br>Bit0: Heavy load mode<br>Bit3: Port pull-up control | 0000 | R/W |
| $14 | OXS | - | OXM | OXON | Bit0: Turn on OSCX oscillator<br>Bit1: CPU clocks select (1: OSCX/0: OSC)<br>Bit3: OSCX type selection | 0000 | R/W |

| Address | Bit3 | Bit2 | Bit1 | Bit0 | Function | Initial Value | R/W |
|---|---|---|---|---|---|---|---|
| $15 | LPS1 | LPS0 | LCDOFF | **Should be set to "1"** | **Bit0: Should be set to "1"**<br>Bit1: LCD off<br>Bit2, 3: LCD frequency control | 0000 | R/W |
| $16 | LPD | O/S | - | - | Bit2: Set LCD segment as output<br>Bit3: LCD Power degrade | 0000 | R/W |
| $17 | C1.3 | C1.2 | C1.1 | C1.0 | PSG channel 1 low nibble | 0000 | W |
| $18 | OCT1 | C1.6 | C1.5 | C1.4 | PSG channel 1high nibble<br>Bit3: channel 1 octave shift control | 0000 | W |
| $19 | C2.3 | C2.2 | C2.1 | C2.0 | PSG channel 2 nibble 1 or alarm output | 0000 | W |
| $1A | C2.7 | C2.6 | C2.5 | C2.4 | PSG channel 2 nibble 2 | 0000 | W |
| $1B | C2.11 | C2.10 | C2.9 | C2.8 | PSG channel 2 nibble 3 | 0000 | W |
| $1C | OCT2 | C2.14 | C2.13 | C2.12 | PSG channel 2 nibble 4<br>Bit3: channel 2 octave shift control | 0000 | W |
| $1D | VOL1 | VOL0 | CH2EN | CH1EN | Bit0, Bit1: Channel 1, 2 enable<br>Bit2, Bit3: volume control | 0000 | W |
| $1E | SEL1 | SEL0 | C2M | C1M | Bit0, 1: PSG1, PSG2 mode control<br>Bit2, 3: PSG1, PSG2 clock source selection | 0000 | W |
| $1F | - | - | - | - | Reserved | - | - |

## 4. Oscillator Circuit

(a) Circuit Configuration

SH66P13A has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ. 32.768KHz) or RC (Typ.262KHz) determined by the code option. This is designed for low frequency operation. OSCX also has two types: ceramic (Typ.455KHz) or RC (1.8M or 2MHz) determined by software option. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC clock is automatically selected as the system clock input source.

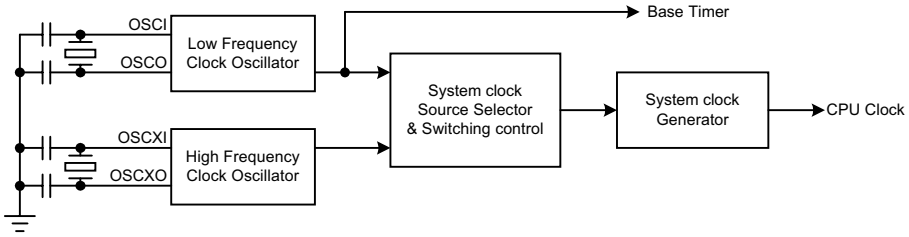



**Figure 1. Oscillator Block Diagram**

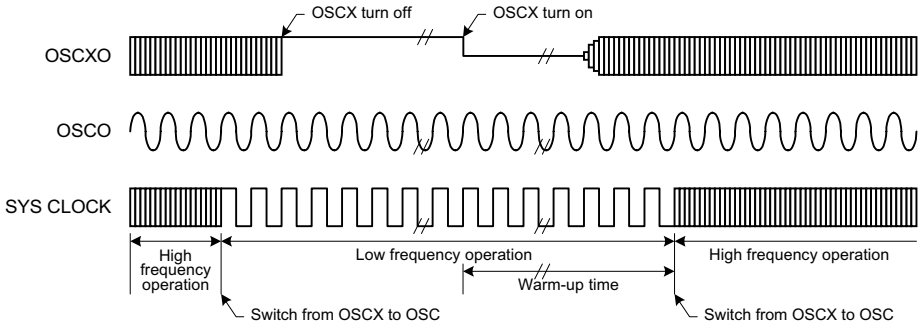
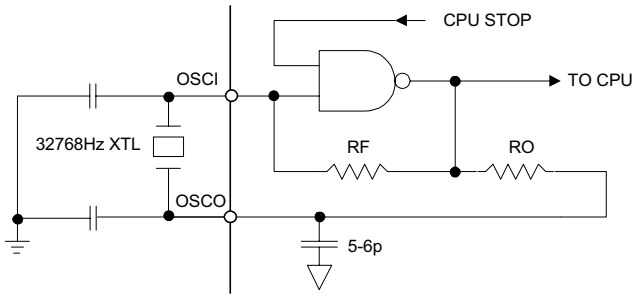



**Figure 2. Timing of System Clock Switching**

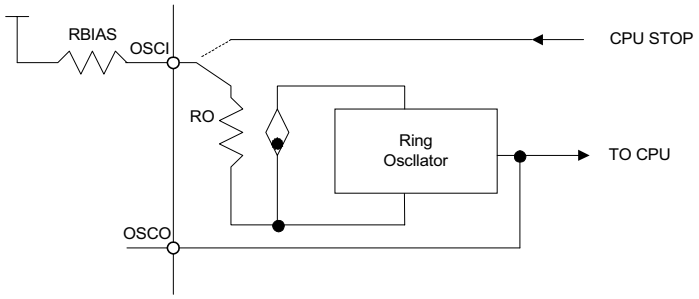
(b) OSC Oscillation

The OSC generates the basic clock pulses that provide the CPU and peripherals (Timer0, LCD) with an operating clock.

(1) OSC Crystal Oscillator Type



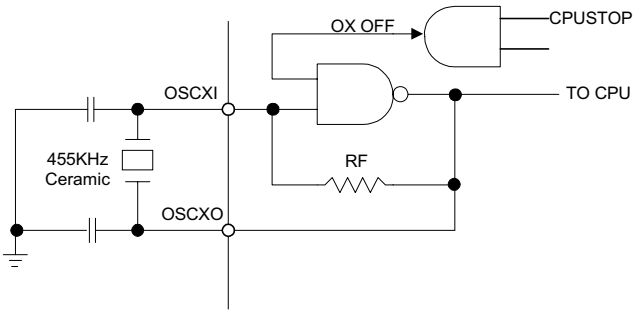
(2) OSC RC Oscillator Type



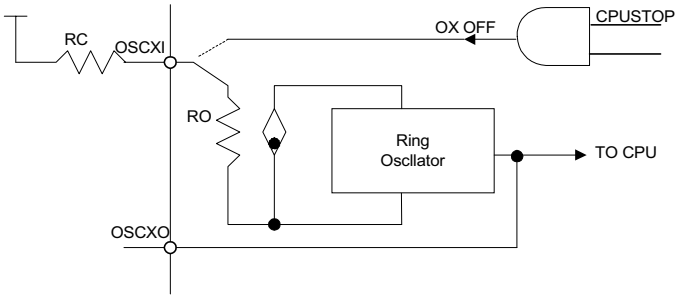

(c) OSCX Oscillation

OSCX has two clock oscillators. The software options select the ceramic or RC as the CPU's clock.
If the OSCX is not used, it must be masked to be Ceramic resonator and the OSCXI must be connected to GND.

(1) OSCX Ceramic Oscillator Type




(2) OSCX RC Oscillator Type




(d) Control of Oscillator

The oscillator control register configuration is shown as blow.

| Address | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|
| $14 | OXS | - | OXM | OXON |

OXON: OSCX oscillation on/off.
0:Turn off OSCX oscillation
1:Turn on OSCX oscillation
OXM: switching system clock.
0:select OSC as system clock
1:select OSCX as system clock
OXS: OSCX oscillator type selection
0:OSCX set as ceramic oscillator
1:OSCX set as RC oscillator

(e) Programming Notes

It takes at least 5 ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, one must wait a minimum of 5ms till the OSCX oscillation is active. However, the start time varies a lot with respect to oscillator characteristics and operational conditions. Therefore the waiting time depends on applications. When switching from OSCX to OSC, and turning off OSCX in one instruction, the OSCX turn off control would be delayed for one instruction cycle automatically to prevent CPU operation error.

### 5. System Clock

The system clock varies as the clock source changes. The following table shows the instruction execution time according to each frequency of the system clock source.

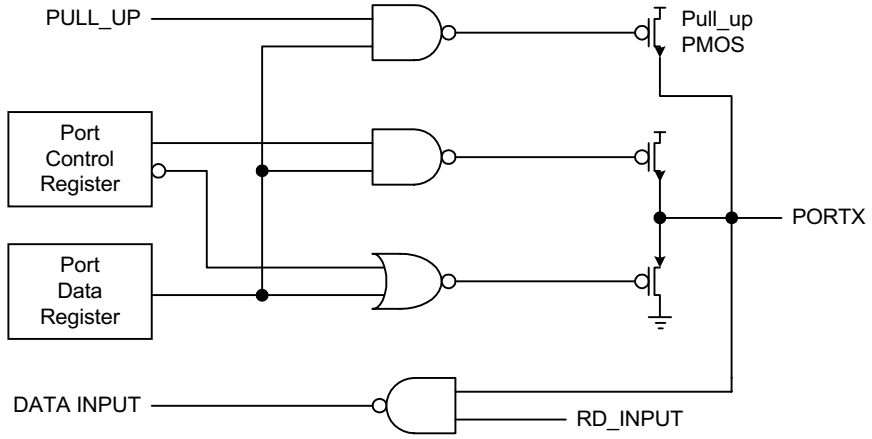
| | 32.768 Xtal (OSC ) | 262K RC (OSC ) | 455K ceramic Xtal (OSCX) | 1.8M RC (OSCX) | 2M RC (OSCX) |
|---|---|---|---|---|---|
| **Cycle time** | 122.07 μs | 17.778 μs | 8.79 μs | 2.22 μs | 2μs |

### 6. I/O PORT

The MCU provides 8-bidirectional I/O pins. Each I/O pin contains pull-up MOS controllable by program. When all I/O is used as input, the PORT control register (PACR, PBCR) controls ON/OFF of the output buffer.

(a) PORTA - B

These ports contain 8-bidirectional I/O ports.
The circuit configuration of PORTA - B is shown below.




I/O ports of SH66P13A can be accessed by read/write system register. User can output any value to any I/O port bit at any time. Bit3 of the PMOD register controls On/Off of all pull-ups MOS simultaneously. Pull-up MOS is also controlled by the port data registers (PA, PB) of each port also. So the pull-up MOS can be turned On/Off.

**Memory Map Addresses are Listed as Follow:**

| Address | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|
| $08 | PORTA.3 | PORTA.2 | PORTA.1 | PORTA.0 |
| $09 | PORTB.3 | PORTB.2 | PORTB.1 | PORTB.0 |

**Port I/O Control Register:**

| Address | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|
| $0B | PACR.3 | PACR.2 | PACR.1 | PACR.0 |
| $0C | PBCR.3 | PBCR.2 | PBCR.1 | PBCR.0 |

I/O control register: PACR.X, PBCR.X (X = 0, 1, 2, 3)
1: Use as an output buffer.
0: Use as input buffer (Power on initial).

**Port Mode Register (PMOD)**

| Address | Bit3 | Bit2 | Bit1 | Bit0 | Function | R/W |
|---|---|---|---|---|---|---|
| $13 | PPULL | PAM2 | PAM1 | HLM | Bit1, 2: Select PA.1, PA.2 as I/O port or PSG output<br>Bit0: Hevey load mode<br>Bit3: Port pull-up control | R/W |

PAM1, PAM2: Please sees the PSG
HLM: Enable heavy load mode 0: Disable 1: Enable
PPULL: Port pull-up 0: Disable pull-up 1: Enable pull-up

(b) Port Interrupt

PORTB interrupt (falling edge) is not controlled by Port I/O register. It means that if an interrupt request (IEx is set to 1 & one port bit high goes low) is been activated touched and the conditions at the other port bits are high level at any time the port bit is either output or input.

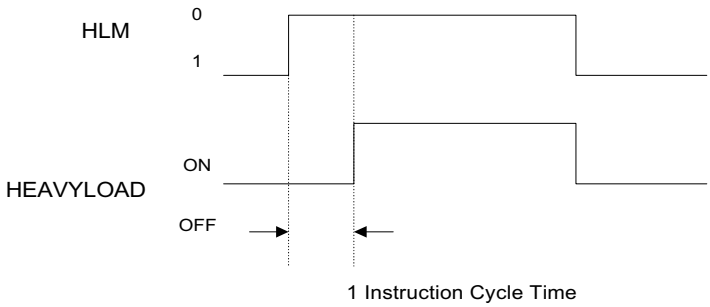
(c) External $\overline{INT}$

PortA.0 is shared by external interrupts (active low).

**7. Heavy Load Mode (HLM)**

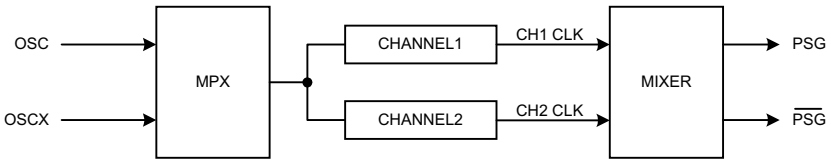
The MCU has a heavy load protection circuit for when the battery load becomes heavy. For examples, when an external buzzer sound or an external speaker is turned on. In this mode, the crystal oscillator circuit has been backed up for high gain. When setup this mode, more power would be provided to oscillator circuit. Unless it is necessary, be careful not to set this mode with software. Since the mode enter would delay for one instruction, please activate heavy load driving at least one instruction wait cycle after setting HLM through the software. The following shows the programming setting.

HLM: 0 = Heavy load protection mode is released
1 = Heavy load protection mode is set.




**8. Programmable Sound Generator (PSG)**

PSG has channel1 and channel2. The functional block diagram is as follows:




The PSG function provides four subfunctions for wide applications.

**Programmable Sound**

Program sound is created by two channels. Each channel can be programmed as follows.
Enable/Disable each channel sounds.
Select each channel sound frequency.
Two channel sounds are mixed into one PSG output.
The PSG output can be controlled at 4 volume levels.

**Fine Noise**

PSG can provide wide-band noise.
The wide-band noise volume can be controlled at 4 volume levels.

**Alarm**

PSG can provide many alarm functions through software.
The alarm carrier frequency can be programmed individually.
The alarm volume can be controlled at 4 volume levels.

**Remote Control**

The remote control is the only expandable application for PSG sound. Since the remote control frequency is 56.13KHz or 37.92KHz, the software could select sound frequency.

PSG subblock diagram:

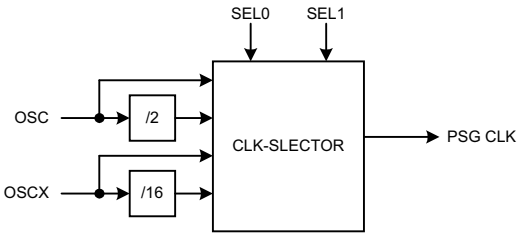
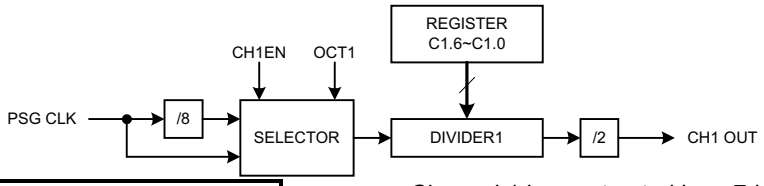



**Figure 3. MPX block diagram**

| SEL1 | SEL0 | Clk source | | PSG clk |
|---|---|---|---|---|
| 0 | 0 | OSC | OSC = 32.768K | 32.768K |
| | | | OSC = 262K | 262K |
| 0 | 1 | OSC/2 | OSC = 32.768K | 16.384K |
| | | | OSC = 262K | 131K |
| 1 | 0 | OSCX | OSCX = 1.8M | 1.8M |
| | | | OSCX = 455K | 455K |
| 1 | 1 | OSCX/16 | OSCX = 1.8M | 112.5K |
| | | | OSCX = 455K | 28.4K |

The MPX block selects 4 clock sources as PSG clk that provides for the two channel clk sources.

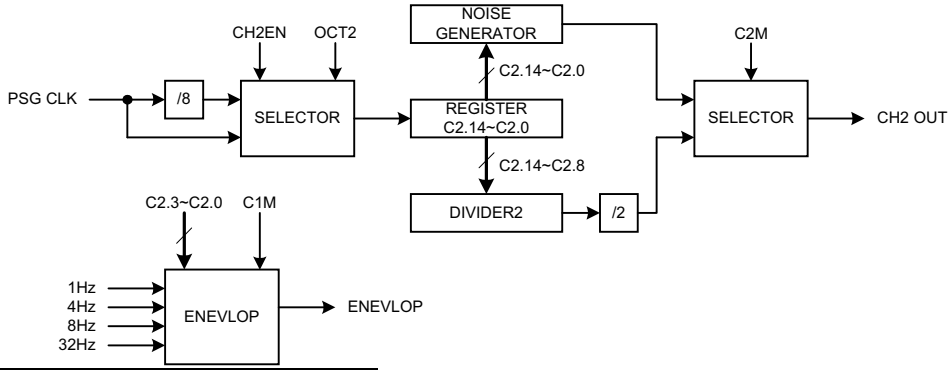
**Channel 1.**




| OCT1 | Scaling ratio |
|---|---|
| 0 | 1 |
| 1 | 1/8 |

Channel 1 is constructed by a 7-bit pseudo random counter. Channel 1 is enabled/disabled by CH1EN. It creates either a sound frequency or an alarm carrier frequency or a remote carrier frequency.

**Channel 2.**

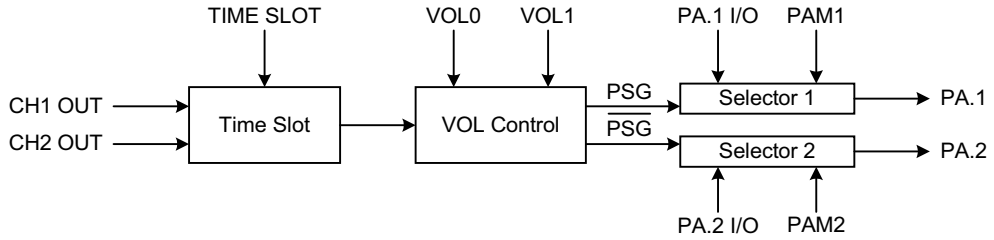



| OCT2 | Scaling ratio |
|---|---|
| 0 | 1 |
| 1 | 1/8 |

Channel 2 is constructed by a 15-bit pseudo random counter. Channel 2 is enabled/disabled by CH2EN
It can be a 15-bit wide-band noise generator or a 7-bit sound generator. It can also create an alarm envelope signal.

| C2M | C1M | Function | |
|---|---|---|---|
| 0 | 0 | CH1 is Sound generator. | CH2 is Sound generator. |
| 1 | 0 | CH1 is Sound generator. | CH2 is Noise generator. |
| x | 1 | CH1 is Sound generator. | CH2 is Alarm mode register. |

**Mixer**




The MIXER mixes CH1-OUT and CH2-OUT into one single tone output to PA.1、PA.2, when PAM1 = 1、PAM2 = 1. Then the tone output is controlled by the volume control bit into 4 volume levels and in the end outputted by PSG.

PA.1 & PA.2 are controlled by PAM1 & PAM2

| PAM2 | PAM1 | Function |
|---|---|---|
| 0 | 0 | PA.1: I/O PORT. PA.2: I/O PORT |
| 0 | 1 | PA.1: PSG output. PA.2: I/O PORT |
| 1 | 0 | PA.1: I/O PORT. PA.2: $\overline{PSG}$ output |
| 1 | 1 | PA.1: PSG output. PA.2: $\overline{PSG}$ output |

| SEL1 | SEL0 | Vol. control |
|---|---|---|
| 0 | 0 | NO |
| 0 | 1 | YES |
| 1 | 0 | YES |
| 1 | 1 | YES |

| VOL1 | VOL0 | Vol. Level |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

**Note:**

Don’t enable two PSG channels together to produce one tone, or it will produce some unpredicted errors. If it is necessary to use 2 channels together (e.g. to play two different melodies from two channels), don’t let the score always be the same tone as we can do, then the unpredicted errors will not occur or it will be ignore through user hearing.

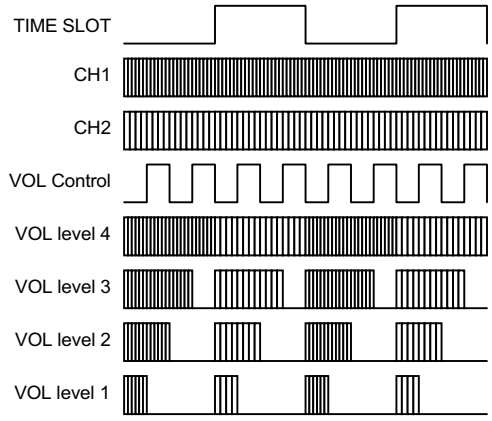
**The Value N of Divider is Corresponding to the REG C1.6 - C1.0 or REG C2.14 - C2.8 as Shown in the Following Table:**

| LSFR (C1.6 ~ C1.0) (C2.14 ~ C2.8) | N | LSFR (C1.6 ~ C1.0) (C2.14 ~ C2.8) | N | LSFR (C1.6 ~ C1.0) (C2.14 ~ C2.8) | N | LSFR (C1.6 ~ C1.0) (C2.14 ~ C2.8) | N |
|---|---|---|---|---|---|---|---|
| 01 | 127 | 16 | 95 | 12 | 63 | 4B | 31 |
| 02 | 126 | 2C | 94 | 24 | 62 | 17 | 30 |
| 04 | 125 | 59 | 93 | 49 | 61 | 2E | 29 |
| 08 | 124 | 33 | 92 | 13 | 60 | 5D | 28 |
| 10 | 123 | 67 | 91 | 26 | 59 | 3B | 27 |
| 20 | 122 | 4E | 90 | 4D | 58 | 77 | 26 |
| 41 | 121 | 1D | 89 | 1B | 57 | 6E | 25 |
| 03 | 120 | 3A | 88 | 36 | 56 | 5C | 24 |
| 06 | 119 | 75 | 87 | 6D | 55 | 39 | 23 |
| 0C | 118 | 6A | 86 | 5A | 54 | 73 | 22 |
| 18 | 117 | 54 | 85 | 35 | 53 | 66 | 21 |
| 30 | 116 | 29 | 84 | 6B | 52 | 4C | 20 |
| 61 | 115 | 53 | 83 | 56 | 51 | 19 | 19 |
| 42 | 114 | 27 | 82 | 2D | 50 | 32 | 18 |
| 05 | 113 | 4F | 81 | 5B | 49 | 65 | 17 |
| 0A | 112 | 1F | 80 | 37 | 48 | 4A | 16 |
| 14 | 111 | 3E | 79 | 6F | 47 | 15 | 15 |
| 28 | 110 | 7D | 78 | 5E | 46 | 2A | 14 |
| 51 | 109 | 7A | 77 | 3D | 45 | 55 | 13 |
| 23 | 108 | 74 | 76 | 7B | 44 | 2B | 12 |
| 47 | 107 | 68 | 75 | 76 | 43 | 57 | 11 |
| 0F | 106 | 50 | 74 | 6C | 42 | 2F | 10 |
| 1E | 105 | 21 | 73 | 58 | 41 | 5F | 9 |
| 3C | 104 | 43 | 72 | 31 | 40 | 3F | 8 |
| 79 | 103 | 07 | 71 | 63 | 39 | 7F | 7 |
| 72 | 102 | 0E | 70 | 46 | 38 | 7E | 6 |
| 64 | 101 | 1C | 69 | 0D | 37 | 7C | 5 |
| 48 | 100 | 38 | 68 | 1A | 36 | 78 | 4 |
| 11 | 99 | 71 | 67 | 34 | 35 | 70 | 3 |
| 22 | 98 | 62 | 66 | 69 | 34 | 60 | 2 |
| 45 | 97 | 44 | 65 | 52 | 33 | 40 | 1 |
| 0B | 96 | 09 | 64 | 25 | 32 | | |

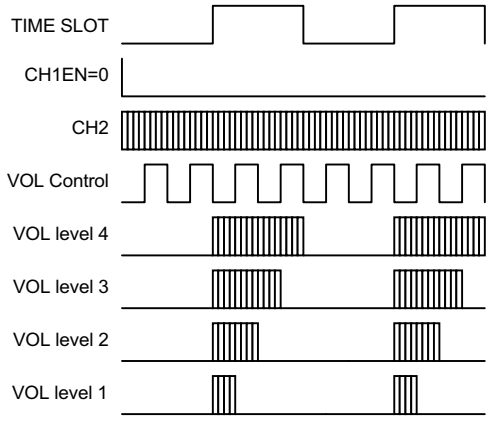
(a) PSG as sound generator

The programmable sound is one of the 4 working modes. The software designer can select up to 16 clock sources as PSG clk. And then select the CH1 and CH2 frequency divided value that is controlled by the value of REG C1.6 ~ C1.0 or C2.14 ~ C2.8.In the end we can select the 4 volume level controlled by VOL0, VOL1. The music tone can output both PSG and $\overline{PSG}$. We also can control the OCT1, OCT2 bit that shifts the music tone 3 octaves.

Example1: CH1EN = CH2EN = 1
OSCX = 1.8M, SEL0 = SEL1 = 1
So PSG clk = 112kHz; Switch clk = 28kHz
Vol. Clk = 112kHz

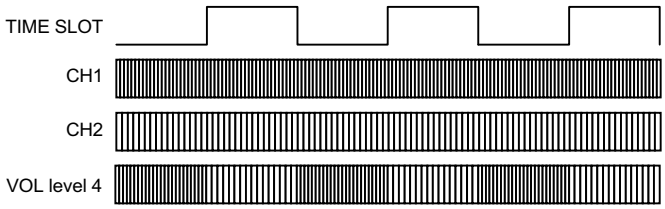



Example2: CH1EN = 0; CH2EN = 1
OSCX = 1.8M, SEL0 = SEL1 = 1
So PSG clk = 112kHz; Switch clk = 28kHz;
Vol. Clk = 112kHz




Example3: CH1EN = CH2EN = 1
OSC = 32k, SEL0 = SEL1 = 0
So PSG clk = 32kHz; Switch clk = 32kHz

No vol. control, the VOL level is set to 4 by hardware, so software should set VOL0 = VOL1 = 1.




**Note:**

For 32KHz operations, the volume control cannot be used, because the PWM multiplexing frequency is not high enough to switch sound! If a user wants to turn off the PSG completely, the software must disable both channels. User should not turn off the PSG by zero wave from output. Both the CH1EN and CH2EN should be set to "0" for the low power operation mode.

Example 4

If software designer wants to create C2 (channel 1) mixed with F5 (channel 2) sound (the C2, F5 sound frequency, please see the Music table1 and Music table2), VOL level = 3.He can select the suggestion as follows.

(1) Select CH1EN = CH2EN = 1, C1M = C2M = 0.
(2) Select OSCX = 1.8M and SEL0 = SEL1 = 1, so the PSG CLK = 112.5KHz.
(3) Select OCT1 = 1 and the value of channel 1 LSFR (C1.6 ~ C1.0) = 23, so the N = 108. Please see the Music table1.So the channel 1 sound frequency = 112.5Khz/8/(2 X 108) = 64.10Hz ≒ the C2 sound frequency.
(4) Select OCT2= 0 and the value of channel 2 LSFR (C2.8 ~ C2.14) = 4F, so the N = 81. Please see the Music table1.So the channel 1 sound frequency = 112.5Khz/1/(2 X 81) = 694.4Hz ≒ the F5 sound frequency .
(5) Lastly, select the VOL1 = 1 and VOL0 = 0, so the VOL level = 3.

**Note:**

The designer provides two crossing tables as an appendix that is what the designer prefers PSG clk = 32.768K or PSG clk = 112.5K.

(b) PSG as noise generator

The fine noise is created by CH2. If we want to create the single noise, we can make the CH1 music tone output. Otherwise we can mix the wide-band noise and the CH1 music tone into one single output through the MIXER. Lastly we can select 4 volume levels controlled by VOL0, VOL1.

(c) PSG as an Alarm Generator

When PSG is in the alarm mode, the CH1 provides the alarm carrier frequency and the CH2 provides the alarm envelope signal. Lastly we can select 4 volume levels controlled by VOL0, VOL1. The channel 2 low nibble C2.0 ~ C2.3 will be the alarm control register. Channel 1 output would modulate with an ALARM envelope control for 32KHz or 262KHz. The carrier frequency can be programmed by PSG channel 1.In reading this alarm control register, we can read the corresponding output envelope frequency (the 1Hz, 4Hz, 8Hz, 32Hz).

Alarm Control Register (OSC = 32KHz or 262KHz)

| $19 | C2.3 | C2.2 | C2.1 | C2.0 | Alarm output control |
|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | DC envelop |
| | X | X | X | 1 | 1Hz output |
| | X | X | 1 | X | 4Hz output |
| | X | 1 | X | X | 8Hz output |
| | 1 | X | X | X | 32Hz output |

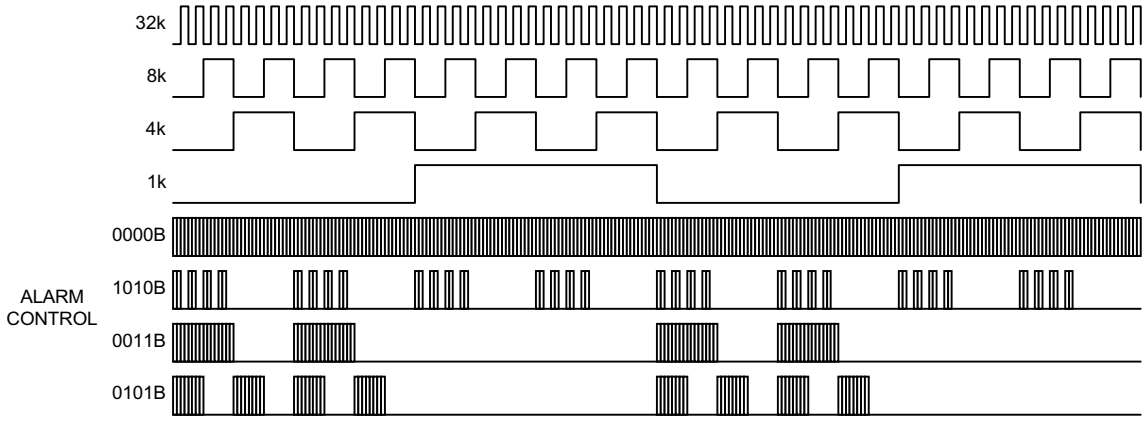



**Figure 4. Alarm Modulation Output for OSC = 32.768KHz or OSC = 262KHz**

(d) PSG as remote control

The remote control is only an expandable application for PSG sound. We can select the CH1 as tone output and the CH2 will create alarm frequency envelope signal.

When PSG channel is programmed in the ALARM mode. Programmer can set ALARM mode register to "0000B". Program the adequate frequency output to PSG output. Then use PAM1 or PAM2 to control the envelope of code. In this way, remote control function can be implemented easily.

The remote frequency = 56.73KHz or 37.92KHz.

The software should select OSCX = 455KHz, SEL1 = 1 and SEL0 = 0, so that the PSG CLK = 455KHz.

Then select channel 2 alarm mode (C1M = 1), and OCT1 = 0, C2.0 ~ C2.3 are set to 00H. VOL1, VOL2 = 1, 1.

Then select C1.6 ~ C1.0 = 7E, so that N = 6 and the PSG output frequency = 455KHz/1/(2 X 6) = 37.92KHz.

Or select C1.6 ~ C1.0 = 78, so that N = 4 and the PSG output frequency = 455KHz/1/(2 X 4) = 56.87KHz.

## 9. Timer

SH66P13A has one 8-bit timer. The timer consists of an 8-bit up counter and an 8-bit preload register.
The timers provide the following functions:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-bit prescaler.
- Interrupt on overflow from $FF to $00.

(a) Configuration and Operation

Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digit and high order digit. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

Load register programming: The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since register H would control the physical READ and WRITE operations.

Please follow these rules:

Write Operation:

Low nibble first
High nibble to update the counter

Read Operation:

High nibble first;
Low nibble followed.

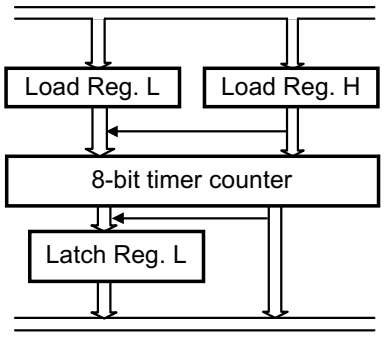



**Figure 5. Timer Load Register Configure**

(b) Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will start. This can also be used to wake CPU from HALT mode.

(c) Timer0 mode register (TM0)

The 8-bit counter prescaler overflow output pulses. TM0 are 4-bit registers used for timer control as shown in Table1. The register selects the input clock sources in the timer.

**Table 1. Timer0 Mode Registers ($02)**

| TM0.3 | TM0.2 | TM0.1 | TM0.0 | Prescaler | Clock Source |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | /2048 | System clock |
| 0 | 0 | 0 | 1 | /512 | System clock |
| 0 | 0 | 1 | 0 | /128 | System clock |
| 0 | 0 | 1 | 1 | /32 | System clock |
| 0 | 1 | 0 | 0 | /8 | System clock |
| 0 | 1 | 0 | 1 | /4 | System clock |
| 0 | 1 | 1 | 0 | /2 | System clock |
| 0 | 1 | 1 | 1 | External | $\overline{\text{INT0}}$ |

TM0.3 control function:
0: without Auto-Reload function 1: Auto-Reload function

**10. Base Timer**

The MCU has a base timer that is shared with the warm-up timer and the clock source is OSC (Low frequency oscillation: Crystal 32.768KHz or RC 262KHz). After MCU is reset, it counts at every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow. This causes the interrupt of base timer interrupt request flag to 1.Therefore, base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal output.

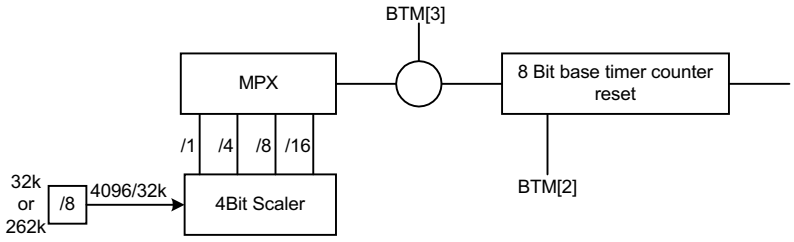
The timer accepts 4096Hz or 32KHz clock, and base timer generates an accurate timing interrupt. This base time prescaler can be reset by a program for accurate timing.

This clock-input source is sleeted by BTM register.

| Address | Bit3 | Bit2 | Bit1 | Bit0 | Function |
|---|---|---|---|---|---|
| **$03** | BTM.3 | BTM.2 | BTM.1 | BTM.0 | Base timer mode register |

BTM.3 = 0: Disable the base timer BTM.3 = 1: Enable the base timer
BTM.2 = 0: Non reset the base timer BTM.2 = 1: reset the base timer

| BTM.1 | BTM.0 | Prescaler Ratio | Clock source |
|---|---|---|---|
| 0 | 0 | /1 | 4096Hz or 32KHz |
| 0 | 1 | /4 | 4096Hz or 32KHz |
| 1 | 0 | /8 | 4096Hz or 32KHz |
| 1 | 1 | /16 | 4096Hz or 32KHz |



**11. LCD Driver**

The LCD driver contains a controller, a voltage generator, 4common signal pins and 34segment driver pins. There is 1/4 duty and 1/3 bias driving mode programmable. **System register $15 should be set '1".**

The LCD SEG1~30 can also be used as output port, it is selected by the bit 2 of the system register $16. When SEG1~30 is to be output port, you write data to bit 0 of the same addresses (350H-36DH). LCD RAM could be used as data memory if you need. When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the same value before executing the "STOP" instruction.

(a)LCD Control Register

| Add. | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| **$15** | LPS1 | LPS0 | LCDOFF | **Should be set "1"** |

LCDOFF: LCD on/off switch.
0: LCD on. 1: LCD off.

LPS1, LPS0: LCD clock frequency control
0,0: LCDCLK = OSC/64
0,1: LCDCLK = OSC/512
1,0: LCDCLK = System clock/512
1,1: LCDCLK = System clock/4096

*System clock= Instruction cycle time
Frame frequency=LCDCLK/16

| CLK Frequency | LPS1, LPS0 | | | |
|---|---|---|---|---|
| | 0,0 | 0,1 | 1,0 | 1,1 |
| OSC=32kHz (#), OSCX=455kHz | 32Hz | 4Hz | 1Hz | 1/8Hz |
| OSC=32kHz, OSCX=455kHz (#) | 32Hz | 4Hz | 14Hz | 1.7Hz |
| OSC=32kHz (#), OSCX=1.8MHz | 32Hz | 4Hz | 1Hz | 1/8Hz |
| OSC=32kHz, OSCX=1.8MHz (#) | 32Hz | 4Hz | 55Hz | 6.9Hz |
| OSC=32kHz(#), OSCX=2MHz | 32Hz | 4Hz | 1Hz | 1/8Hz |
| OSC=32kHz, OSCX=2MHz (#) | 32Hz | 4Hz | 61Hz | 7.6Hz |
| OSC=262kHz (#), OSCX=455kHz | 256Hz | 32Hz | 8Hz | 1Hz |
| OSC=262kHz, OSCX=455kHz (#) | 256Hz | 32Hz | 14Hz | 1.7Hz |
| OSC=262kHz (#), OSCX=1.8MHz | 256Hz | 32Hz | 8Hz | 1Hz |
| OSC=262kHz , OSCX=1.8MHz (#) | 256Hz | 32Hz | 55Hz | 6.9Hz |
| OSC=262kHz (#), OSCX=2MHz | 256Hz | 32Hz | 8Hz | 1Hz |
| OSC=262kHz , OSCX=2MHz (#) | 256Hz | 32Hz | 61Hz | 7.6Hz |

The clk before (#) is sleeted as CPU system clk.
Frame frequency=LCDCLK/16 (32Hz)
When LCD is set SCAN OUT, COMx are pulled high. It is easy to implement the keyboard scan.
When CPU is in STOP mode, the COMx and SEGx are pulled low. It can easily be waken up by keyboard scan (Port interrupt).
When CPU is in HALT mode, the COMx and SEGx are normal. It can easily be waken up by base timer、timer0 or port interrupt.

(b)LCD power

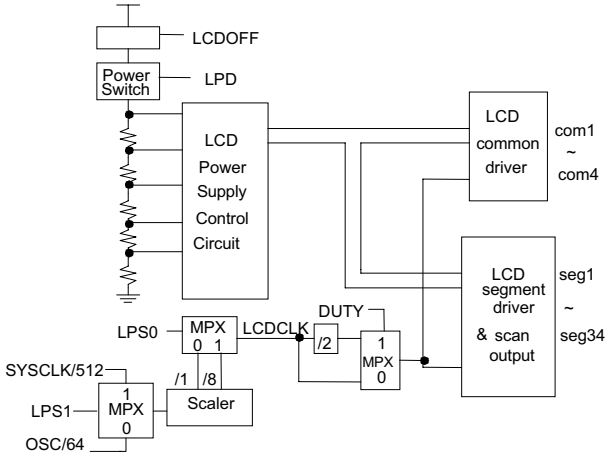



**Figure 6 LCD block diagram for reference only**

Build-in special LCD power control for LCD power modulation.

| Add. | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|
| **$16** | LPD | O/S | - | - |

O/S: Set LCD segment/common to be LCD segment output or output ports
0: LCD segment output 1: output ports.
When LPD is set to 1, the LCD voltage power would be degraded about 0.5V, depending on the VDD level. It is designed to reduce extra LCD contrast control output pins. Then the LCD can be fitted automatically for different voltage levels by the software.

(c) Configuration of LCD RAM

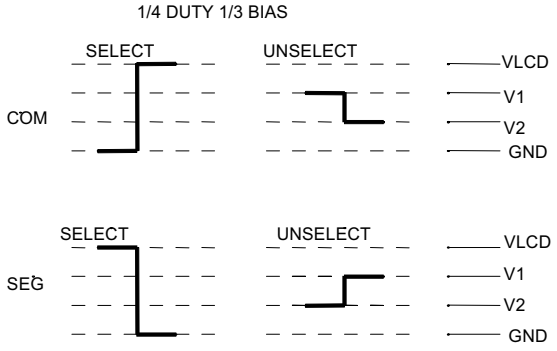
LCD 1/4 duty, 1/3 bias (COM1~4,SEG1~34)

| Address | Bit3 | Bit2 | Bit1 | Bit0 | Address | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| | **COM4** | **COM3** | **COM2** | **COM1** | | **COM4** | COM3 | **COM2** | **COM1** |
| 300H | SEG1 | SEG1 | SEG1 | SEG1 | 311H | SEG18 | SEG18 | SEG18 | SEG18 |
| 301H | SEG2 | SEG2 | SEG2 | SEG2 | 312H | SEG19 | SEG19 | SEG19 | SEG19 |
| 302H | SEG3 | SEG3 | SEG3 | SEG3 | 313H | SEG20 | SEG20 | SEG20 | SEG20 |
| 303H | SEG4 | SEG4 | SEG4 | SEG4 | 314H | SEG21 | SEG21 | SEG21 | SEG21 |
| 304H | SEG5 | SEG5 | SEG5 | SEG5 | 315H | SEG22 | SEG22 | SEG22 | SEG22 |
| 305H | SEG6 | SEG6 | SEG6 | SEG6 | 316H | SEG23 | SEG23 | SEG23 | SEG23 |
| 306H | SEG7 | SEG7 | SEG7 | SEG7 | 317H | SEG24 | SEG24 | SEG24 | SEG24 |
| 307H | SEG8 | SEG8 | SEG8 | SEG8 | 318H | SEG25 | SEG25 | SEG25 | SEG25 |
| 308H | SEG9 | SEG9 | SEG9 | SEG9 | 319H | SEG26 | SEG26 | SEG26 | SEG26 |
| 309H | SEG10 | SEG10 | SEG10 | SEG10 | 31AH | SEG27 | SEG27 | SEG27 | SEG27 |
| 30AH | SEG11 | SEG11 | SEG11 | SEG11 | 31BH | SEG28 | SEG28 | SEG28 | SEG28 |
| 30BH | SEG12 | SEG12 | SEG12 | SEG12 | 31CH | SEG29 | SEG29 | SEG29 | SEG29 |
| 30CH | SEG13 | SEG13 | SEG13 | SEG13 | 31DH | SEG30 | SEG30 | SEG30 | SEG30 |
| 30DH | SEG14 | SEG14 | SEG14 | SEG14 | 31EH | SEG31 | SEG31 | SEG31 | SEG31 |
| 30EH | SEG15 | SEG15 | SEG15 | SEG15 | 31FH | SEG32 | SEG32 | SEG32 | SEG32 |
| 30FH | SEG16 | SEG16 | SEG16 | SEG16 | 320H | SEG33 | SEG33 | SEG33 | SEG33 |
| 310H | SEG17 | SEG17 | SEG17 | SEG17 | 321H | SEG34 | SEG34 | SEG34 | SEG34 |

SEG1-30 is used as scan output port.

| Address | Bit0 | Address | Bit0 | Address | Bit0 | Address | Bit0 |
|---|---|---|---|---|---|---|---|
| 350H | SEG1 | 358H | SEG9 | 360H | SEG17 | 368H | SEG25 |
| 351H | SEG2 | 359H | SEG10 | 361H | SEG18 | 369H | SEG26 |
| 352H | SEG3 | 35AH | SEG11 | 362H | SEG19 | 36AH | SEG27 |
| 353H | SEG4 | 35BH | SEG12 | 363H | SEG20 | 36BH | SEG28 |
| 354H | SEG5 | 35CH | SEG13 | 364H | SEG21 | 36CH | SEG29 |
| 355H | SEG6 | 35DH | SEG14 | 365H | SEG22 | 36DH | SEG30 |
| 356H | SEG7 | 35EH | SEG15 | 366H | SEG23 | | |
| 357H | SEG8 | 35FH | SEG16 | 367H | SEG24 | | |

(d)LCD waveform



**12. Interrupt**

4 interrupt sources are available on SH66P13A:

- External interrupt ( $\overline{INT0}$ )
- Timer0 interrupt
- Base timer interrupt
- Port's falling edge detection interrupt( $\overline{INT1}$ )

**The Configuration of System Register $00:**

| Address | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function |
|---|---|---|---|---|---|
| $00 | IEX | IET0 | IEBT | IEP | 1: Enable/0: Disable |

(a) External Interrupt ( $\overline{INT0}$ )

External interrupt is shared with the PA.0, falling edge active. When the bit 3 of the register $0 (IEX) is set to 1, the external interrupt is enabled, writing a "0" to PA.0 will generate an external interrupt.

(b) Timer 0 interrupt, Base Timer Interrupt, Port Interrupt ( $\overline{INT1}$ )

If IEx = 1 then all valid interrupt requests will cause interrupt. The overflow of timer 0 will create the interrupt of timer 0.The overflow of the Base timer will create the interrupt of the Base timer. The falling edge of every port in PORTB will create $\overline{INT1}$ interrupt (The condition is that the other port must be input/output high level).

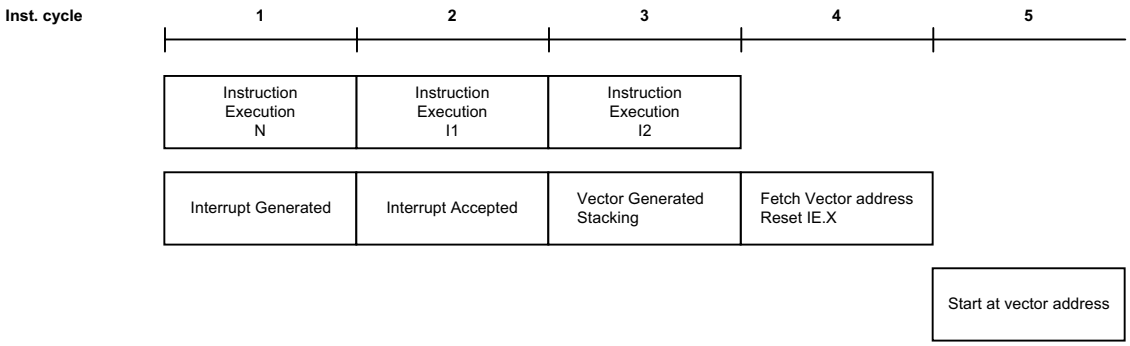
(c) The Enable Flags and Request Flags

Both the Enable flags and Request flags are mapped on $00 and $01 of the system register. They can be read or written by the software.

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

(d) Interrupt Servicing Sequence Diagram:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

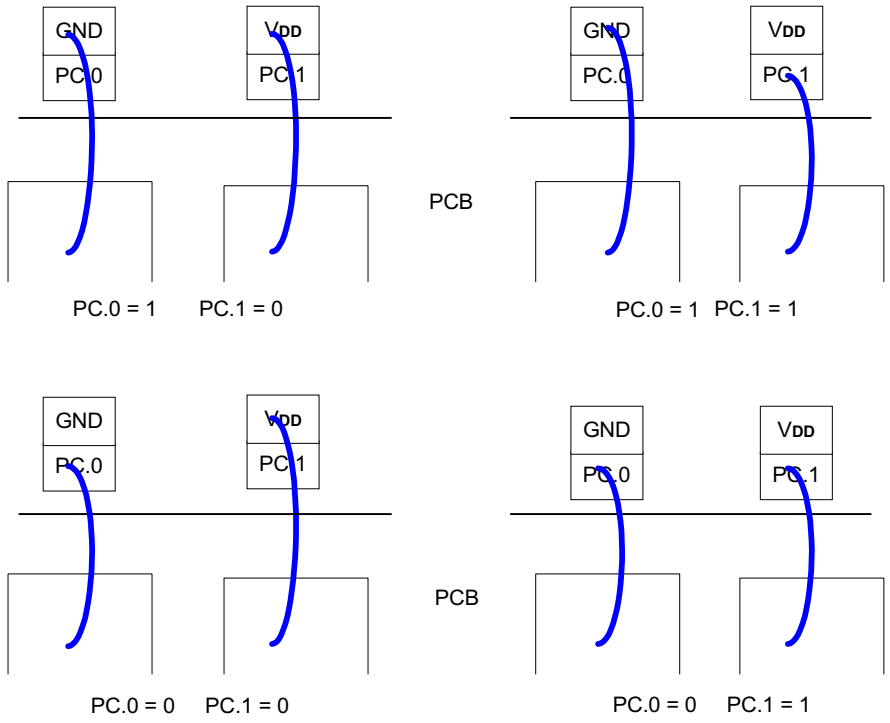


## 13. Options

Bonding Options

System register $0A is reserved for the user .It is opened for system developer to select these 2 bonding options, selecting subprogram that is programmed by the user.

| $0A.1 (PC.1) | $0A.0 (PC.0) | |
|---|---|---|
| 0 | 0 | goto subroutine 1 |
| 0 | 1 | goto subroutine 2 (Default) |
| 1 | 0 | goto subroutine 3 |
| 1 | 1 | goto subroutine 4 |




**SH66P14A Bonding Option**

(b) Code Option

Oscillator (OSC) type:
0 = Set as 32.768KHz crystal (Default)
as 262KHz RC

## 14. HALT and STOP Mode

After the execution of HALT instruction, SH66P13A will enter halt mode.
In halt mode, CPU will stop operating. But peripheral circuit (Timer & Base timer) will keep operating.
After the execution of STOP instruction, SH66P13A will enter stop mode.
In stop mode, the whole chip (including oscillator) will stop operating.
In HALT mode, SH66P13A can be waked up if any interrupt occurs.
In STOP mode, SH66P13A can be waked up if port interrupt occurs.

## 15. Warm-up Counter

In RC mode, the warm-up counter prescaler is divided by $2^7$ (128).
In Crystal mode, the warm-up counter prescaler is divided by $2^{15}$ (32768).

## Instruction Set

All instructions are one cycle and one word instruction. The characteristic is memory-oriented operation.
Arithmetic and Logical Instruction

**Accumulator Type**

| Mnemonic | Instruction Code | Function | Flag Change |
|---|---|---|---|
| ADC X (, B) | 00000 0bbb xxx xxxx | AC ← Mx + AC + CY | CY |
| ADCM X (, B) | 00000 1bbb xxx xxxx | AC, Mx ← Mx + AC + CY | CY |
| ADD X (, B) | 00001 0bbb xxx xxxx | AC ← Mx + AC | CY |
| ADDM X (, B) | 00001 1bbb xxx xxxx | AC, Mx ← Mx + AC | CY |
| SBC X (, B) | 00010 0bbb xxx xxxx | AC ← Mx + -AC + CY | CY |
| SBCM X (, B) | 00010 1bbb xxx xxxx | AC, Mx ← Mx + -AC + CY | CY |
| SUB X (, B) | 00011 0bbb xxx xxxx | AC ← Mx + -AC + 1 | CY |
| SUBM X (, B) | 00011 1bbb xxx xxxx | AC, Mx ← Mx + -AC + 1 | CY |
| EOR X (, B) | 00100 0bbb xxx xxxx | AC ← Mx ⊕ AC | |
| EORM X (, B) | 00100 1bbb xxx xxxx | AC, Mx ← Mx ⊕ AC | |
| OR X (, B) | 00101 0bbb xxx xxxx | AC ← Mx \| AC | |
| ORM X (, B) | 00101 1bbb xxx xxxx | AC, Mx ← Mx \| AC | |
| AND X (, B) | 00110 0bbb xxx xxxx | AC ← Mx & AC | |
| ANDM X (, B) | 00110 1bbb xxx xxxx | AC, Mx ← Mx & AC | |
| SHR | 11110 0000 000 0000 | 0 → AC [3]; AC [0] → CY;<br>AC shift right one bit | CY |

**Immediate Type**

| Mnemonic | Instruction Code | Function | Flag Change |
|---|---|---|---|
| ADI X, I | 01000 iiii xxx xxxx | AC ← Mx + I | CY |
| ADIM X, I | 01001 iiii xxx xxxx | AC, Mx ← Mx + I | CY |
| SBI X, I | 01010 iiii xxx xxxx | AC ← Mx + -I + 1 | CY |
| SBIM X, I | 01011 iiii xxx xxxx | AC, Mx ← Mx + -I + 1 | CY |
| EORIM X, I | 01100 iiii xxx xxxx | AC, Mx ← Mx ⊕ I | |
| ORIM X, I | 01101 iiii xxx xxxx | AC, Mx ← Mx v I | |
| ANDIM X, I | 01110 iiii xxx xxxx | AC, Mx ← Mx ^ I | |

**Decimal Adjust**

| Mnemonic | Instruction Code | Function | Flag Change |
|---|---|---|---|
| DAA X | 11001 0110 xxx xxxx | AC, Mx ← Decimal adjust for add. | CY |
| DAS X | 11001 1010 xxx xxxx | AC, Mx ← Decimal adjust for sub. | CY |

**Transfer Instruction**

| Mnemonic | Instruction Code | Function | Flag Change |
|---|---|---|---|
| LDA X (, B) | 00111 0bbb xxx xxxx | AC ← Mx | |
| STA X (, B) | 00111 1bbb xxx xxxx | Mx ← AC | |
| LDI X, I | 01111 iiii xxx xxxx | AC, Mx ← I | |

**Control Instruction**

| Mnemonic | Instruction Code | Function | Flag Change |
|---|---|---|---|
| BAZ X | 10010 xxxx xxx xxxx | PC ← X if AC = 0 | |
| BNZ X | 10000 xxxx xxx xxxx | PC ← X if AC ≠ 0 | |
| BC X | 10011 xxxx xxx xxxx | PC ← X if CY = 1 | |
| BNC X | 10001 xxxx xxx xxxx | PC ← X if CY ≠ 1 | |
| BA0 X | 10100 xxxx xxx xxxx | PC ← X if AC (0) = 1 | |
| BA1 X | 10101 xxxx xxx xxxx | PC ← X if AC (1) = 1 | |
| BA2 X | 10110 xxxx xxx xxxx | PC ← X if AC (2) = 1 | |
| BA3 X | 10111 xxxx xxx xxxx | PC ← X if AC (3) = 1 | |
| CALL X | 11000 xxxx xxx xxxx | ST ← CY; PC + 1<br>PC ← X (Not include P) | |
| RTNW H; L | 11010 000h hhh llll | PC ← ST; TBR ← hhhh;<br>AC ← llll | |
| RTNI | 11010 1000 000 0000 | CY; PC ← ST | CY |
| HALT | 11011 0000 000 0000 | | |
| STOP | 11011 1000 000 0000 | | |
| JMP X | 1110p xxxx xxx xxxx | PC ← X (Include p) | |
| TJMP | 11110 1111 111 1111 | PC ← (PC11-PC8) (TBR) (AC) | |
| NOP | 11111 1111 111 1111 | No Operation | |

**Where**

| | | | |
|---|---|---|---|
| PC | Program counter | I | Immediate data |
| AC | Accumulator | ⊕ | Logical exclusive OR |
| -AC | Complement of accumulator | \| | Logical OR |
| CY | Carry flag | & | Logical AND |
| Mx | Data memory | bbb | RAM bank |
| P | ROM page | | |
| ST | Stack | TBR | Table Branch Register |

### Absolute Maximum Rating*

DC Supply Voltage . . . . . .-0.3V to +7.0V

Input Voltage . . . . . -0.3V to $V_{DD}$ + 0.3V

Operating Ambient Temperature . . . . . -10℃ to +60℃

Storage Temperature . . . . . .-55℃ to +125℃

### *Comments

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics**

($V_{DD}$ = 3.0V, GND = 0V, $T_A$ = 25°C, $F_{OSC}$ = 32.768KHz, $F_{OSCX}$ is not used, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | 2.5 | 3 | 5.5 | V | |
| Operating Current | $I_{OP}$ | - | 10 | 20 | μA | All output pins unload execute NOP instruction exclude LCD bias current, LPD off |
| LCD voltage divider resistor | $R_{LCD}$ | - | 275 | - | KΩ | |
| Standby Current | $I_{SB1}$ | - | 2 | 4 | μA | All output pins unload (HALT mode) exclude LCD bias current, LPD off |
| Standby Current | $I_{SB2}$ | - | - | 1 | μA | All output pins unload (STOP mode), LCD off, LPD off |
| Input High Voltage | $V_{IH}$ | 0.7 X $V_{DD}$<br>0.85 X $V_{DD}$ | - | $V_{DD}$ + 0.3<br>$V_{DD}$ + 0.3 | V | PORTA, PORTB<br>$\overline{INT0}$ , $\overline{RESET}$ |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.3 X $V_{DD}$<br>0.15 X $V_{DD}$ | V | PORTA, PORTB<br>$\overline{INT0}$ , $\overline{RESET}$ |
| Drive-high resistance | $R_{OH}$ | - | 300 | - | KΩ | PORTA, PORTB ($I_{OH}$ = -10μA, $V_{OH}$ = 0) |
| Output high voltage | $V_{OH1}$ | 0.7 X $V_{DD}$ | - | - | V | PORTA.0, PORTA.3, PORTB ($I_{OH}$ = -2mA) |
| Output low voltage | $V_{OL1}$ | - | - | 0.8 | V | PORTA.0, PORTA.3, PORTB ($I_{OL}$ = 2mA) |
| Output high voltage | $V_{OH2}$ | 0.7 X $V_{DD}$ | - | - | V | PORTA.1, PORTA.2 or PSG output, $I_{OH}$ = -5mA |
| Output low voltage | $V_{OL2}$ | - | - | 0.8 | V | PORTA.1, PORTA.2 or PSG output, $I_{OL}$ = 5mA |
| Output high voltage | $V_{OH3}$ | 2.8 | - | - | V | SEGx, C = 50P, rise time < 1000ns |
| Output low voltage | $V_{OL3}$ | - | - | 0.2 | V | SEGx |
| Output high voltage | $V_{OH4}$ | $V_{DD}$ - 0.6 | - | - | V | SEG1 - 30to be output port, $I_{OH}$ = -1mA |
| Output low voltage | $V_{OL4}$ | - | - | 0.8 | V | SEG1 - 30to be output port, $I_{OL}$ = 1mA |
| Output high voltage | $V_{OH5}$ | $V_{DD}$ - 1.0 | - | - | V | COMx, $I_{OH}$ = -1mA |
| Output low voltage | $V_{OL5}$ | - | - | 0.8 | V | COMx, $I_{OL}$ = 1mA |
| LCD lighting | $I_{LCD}$ | - | 8 | 10 | μA | $V_{DD}$ = 3V, exclude CPU core operation current |

Operation frequency vs. $I_{SB1}$
$I_{SB1X}$ = (Frequency/32.768KHz) X $I_{SB1}$ X 0.8, ($V_{DD}$ = 3.0V)
Operation frequency vs. $I_{OP}$
$I_{OPX}$ = (Frequency/32.768KHz) X $I_{OP}$ X 0.8, ($V_{DD}$ = 3.0V)
HLM vs. $I_{OP}$, $I_{SB1}$ and $I_{SB2}$
If HLM = 1, $I_{OPX}$ = $I_{OP}$ X 2, $I_{SB2X}$ = $I_{SB2}$ X 2

**LPD Circuitry**

(GND = 0V, $T_A$ = 25°C, $F_{OSC}$ = 32.768KHz, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| LPD-detected Voltage | $V_{LPD}$ | - | 2.0 | - | V | |

**AC Characteristics**

($V_{DD}$ = 3.0V, GND = 0V, $T_A$ = 25°C, $F_{OSC}$ = 32.768KHz, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Oscillation Start Time | $t_{STT}$ | - | 2 | 5 | s | |
| Frequency Stability | \|ΔF\|/F | - | - | 1 | PPM | [F(3.0)-F(2.5)]/F(3.0), crystal oscillator |

**AC Characteristics**

($V_{DD}$ = 3.0V, GND = 0V, $T_A$ = 25°C, $F_{OSC}$ = 262KHz, $F_{OSCX}$ stop, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Oscillation Start Time | $t_{STT}$ | - | - | 100 | μs | |
| Frequency Stability | \|ΔF\|/F | - | - | 10 | % | [F(3.0)-F(2.5)]/F(3.0), Bias resistance accuracy within 1% |

**AC Characteristics**

($V_{DD}$ = 4.5V, GND = 0V, $T_A$ = 25°C, $F_{OSC}$ = 262KHz, $F_{OSCX}$ stop, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Frequency Stability | \|ΔF\|/F | - | - | 10 | % | [F(4.5)-F(3.6)]/F(4.5), Bias resistance accuracy within 1% |

**Typical RC Oscillator Resistor vs. Frequency: (for reference only)**

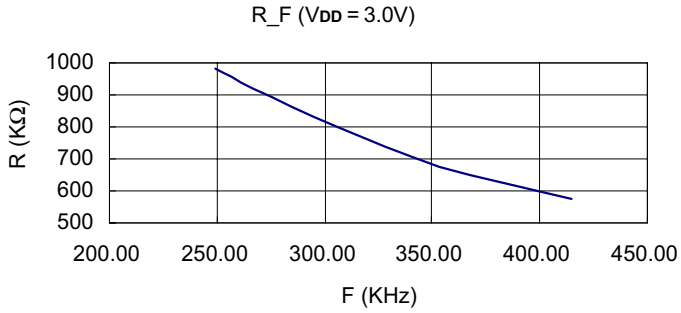



**Figure 7. Resistor vs. $F_{OSC}$**

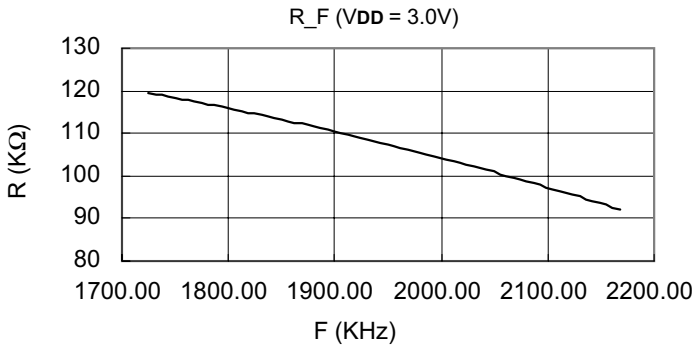
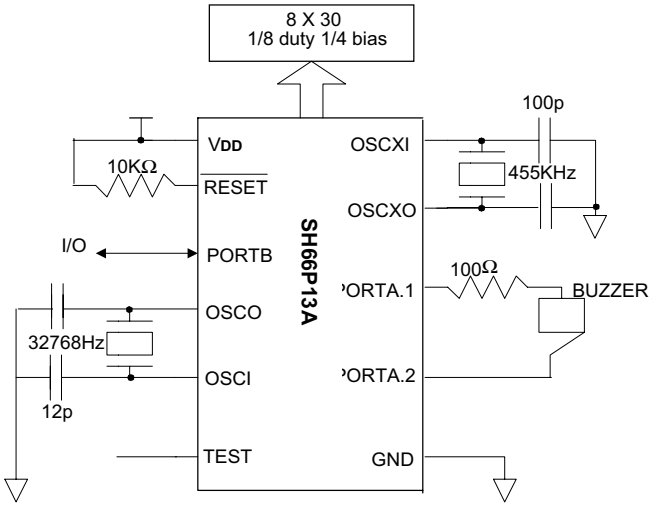



**Figure 8. Resistor vs. $F_{OSCX}$**

## Application Circuit (for reference only)

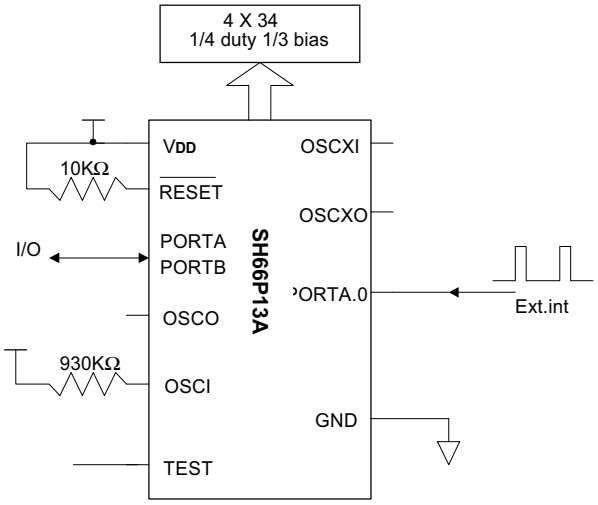
**AP1:**

OSC: Crystal oscillator 32.768KHz (code option)
OSCX: Ceramic oscillator 455KHz
PORTB: I/O
PORTA.1, PORTA.2: ALARM output
LCD: Internal LCD 1/8 duty, 1/4 bias



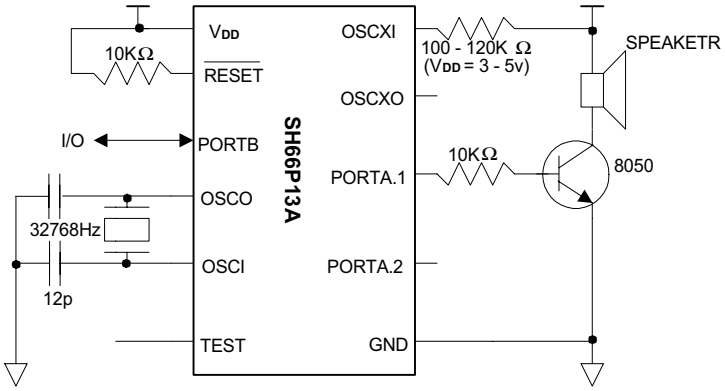

**AP2:**

OSC: RC oscillator 262KHz (mask option)
LCD: Internal LCD 1/4 duty, 1/3 bias
PORTA, PORTB: I/O
PORTA.0: External interrupt



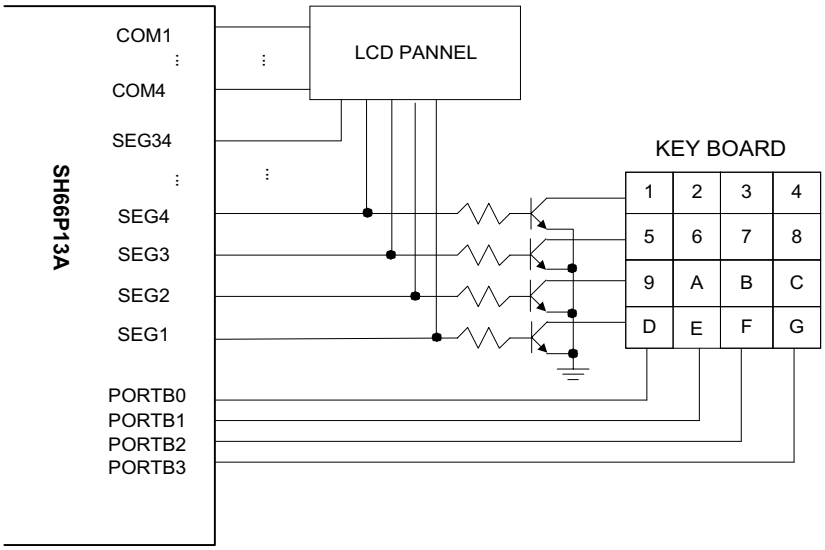
**AP3:**

OSC: Crystal oscillator 32.768KHz (mask option)
OSCX: RC oscillator 1.8MHz
PORTB: I/O
PORTA.1: PSG output
PORTA.2: $\overline{PSG}$ output



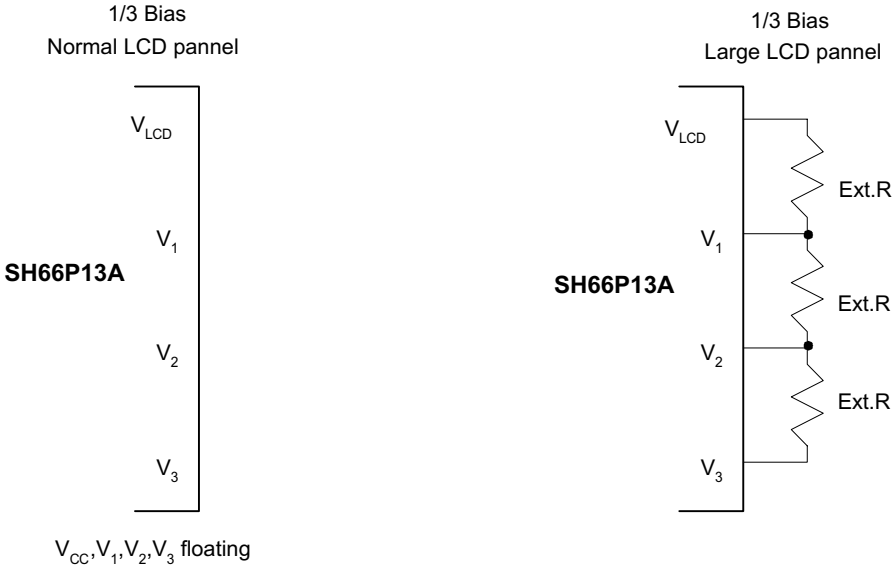

**AP4:**

Internal LCD bias.1/4 DUTY 1/4 bias
SEG1 - SEG4 as SCAN output port



**AP5:**

Large LCD panel: External LCD bias



### Music Table1

Following is the music scale reference table for channel 1(or channel 2) under OSCX = 1.8MHz. Up to 6 octave is possible. Music scale data for 1.8M OSCX and SEL0 = SEL1 = 1

| Note | Ideal freq. | N | OCT1 /OCT2 | LSFR (C1.6~C1.0) (C2.14~C2.8) | Real freq. | Error% | Note | Ideal freq. | N | OCT1/ OCT2 | LSFR (C1.6~C1.0) (C2.14~C2.8) | Real freq. | Error% |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **B1** | 61.73 | 114 | 1 | 42 | 61.68 | -0.08 | **B4** | 493.88 | 114 | 0 | 42 | 493.42 | -0.09 |
| **C2** | 65.10 | 108 | 1 | 23 | 65.10 | 0.01 | **C5** | 523.25 | 108 | 0 | 23 | 520.83 | -0.46 |
| **#C2** | 69.29 | 101 | 1 | 64 | 69.62 | 0.47 | **#C5** | 554.35 | 101 | 0 | 64 | 556.93 | 0.47 |
| **D2** | 73.42 | 96 | 1 | 0B | 73.24 | -0.24 | **D5** | 587.33 | 96 | 0 | 0B | 585.94 | -0.24 |
| **#D2** | 77.78 | 90 | 1 | 4E | 78.13 | 0.44 | **#D5** | 622.24 | 90 | 0 | 4E | 625.00 | 0.44 |
| **E2** | 82.41 | 85 | 1 | 54 | 82.72 | 0.38 | **E5** | 659.26 | 85 | 0 | 54 | 661.77 | 0.38 |
| **F2** | 87.31 | 81 | 1 | 4F | 86.81 | -0.58 | **F5** | 698.46 | 81 | 0 | 4F | 694.44 | -0.58 |
| **#F2** | 92.50 | 76 | 1 | 74 | 92.52 | 0.02 | **#F5** | 739.97 | 76 | 0 | 74 | 740.13 | 0.02 |
| **G2** | 98.00 | 72 | 1 | 43 | 97.66 | -0.35 | **G5** | 783.99 | 72 | 0 | 43 | 781.25 | -0.35 |
| **#G2** | 103.82 | 68 | 1 | 38 | 103.40 | -0.40 | **#G5** | 830.59 | 68 | 0 | 38 | 827.21 | -0.41 |
| **A2** | 110.00 | 64 | 1 | 9 | 109.86 | -0.13 | **A5** | 880.00 | 64 | 0 | 9 | 878.91 | -0.12 |
| **#A2** | 116.54 | 60 | 1 | 13 | 117.19 | 0.56 | **#A5** | 932.31 | 60 | 0 | 13 | 937.50 | 0.56 |
| **B2** | 123.47 | 57 | 1 | 1B | 123.36 | -0.09 | **B5** | 987.77 | 57 | 0 | 1B | 986.84 | -0.09 |
| **C3** | 130.81 | 54 | 1 | 5A | 130.21 | -0.46 | **C6** | 1046.48 | 54 | 0 | 5A | 1041.67 | -0.46 |
| **#C3** | 138.59 | 51 | 1 | 56 | 137.87 | -0.52 | **#C6** | 1108.71 | 51 | 0 | 56 | 1102.94 | -0.52 |
| **D3** | 146.83 | 48 | 1 | 37 | 146.48 | -0.24 | **D6** | 1174.63 | 48 | 0 | 37 | 1171.88 | -0.24 |
| **#D3** | 155.56 | 45 | 1 | 3D | 156.25 | 0.44 | **#D6** | 1244.48 | 45 | 0 | 3D | 1250.00 | 0.44 |
| **E3** | 164.81 | 43 | 1 | 76 | 163.52 | -0.79 | **E6** | 1318.48 | 43 | 0 | 76 | 1308.14 | -0.78 |
| **F3** | 174.61 | 40 | 1 | 31 | 175.78 | 0.67 | **F6** | 1396.88 | 40 | 0 | 31 | 1406.25 | 0.67 |
| **#F3** | 184.99 | 38 | 1 | 46 | 185.03 | 0.02 | **#F6** | 1479.95 | 38 | 0 | 46 | 1480.26 | 0.02 |
| **G3** | 196.00 | 36 | 1 | 1A | 195.31 | -0.35 | **G6** | 1567.95 | 36 | 0 | 1A | 1562.50 | -0.35 |
| **#G3** | 207.65 | 34 | 1 | 69 | 206.80 | -0.41 | **#G6** | 1661.18 | 34 | 0 | 69 | 1654.41 | -0.41 |
| **A3** | 220.00 | 32 | 1 | 25 | 219.73 | -0.12 | **A6** | 1759.96 | 32 | 0 | 25 | 1757.81 | -0.12 |
| **#A3** | 233.08 | 30 | 1 | 17 | 234.38 | 0.56 | **#A6** | 1864.62 | 30 | 0 | 17 | 1875.00 | 0.56 |
| **B3** | 246.94 | 28 | 1 | 5D | 251.12 | 1.69 | **B6** | 1975.49 | 28 | 0 | 5D | 2008.93 | 1.69 |
| **C4** | 261.63 | 27 | 1 | 3B | 260.42 | -0.46 | **C7** | 2092.96 | 27 | 0 | 3B | 2083.33 | -0.46 |
| **#C4** | 277.18 | 25 | 1 | 6E | 281.25 | 1.47 | **#C7** | 2217.41 | 25 | 0 | 6E | 2250.00 | 1.47 |
| **D4** | 293.66 | 24 | 1 | 5C | 292.97 | -0.24 | **D7** | 2349.27 | 24 | 0 | 5C | 2343.75 | -0.24 |
| **#D4** | 311.12 | 23 | 1 | 39 | 305.71 | -1.74 | **#D7** | 2488.96 | 23 | 0 | 39 | 2445.65 | -1.74 |
| **E4** | 329.63 | 21 | 1 | 66 | 334.82 | 1.58 | **E7** | 2636.96 | 21 | 0 | 66 | 2678.57 | 1.58 |
| **F4** | 349.23 | 20 | 1 | 4C | 351.56 | 0.67 | **F7** | 2793.77 | 20 | 0 | 4C | 2812.50 | 0.67 |
| **#F4** | 369.99 | 19 | 1 | 19 | 370.07 | 0.02 | **#F7** | 2959.89 | 19 | 0 | 19 | 2960.53 | 0.02 |
| **G4** | 392.00 | 18 | 1 | 32 | 390.63 | -0.35 | **G7** | 3135.90 | 18 | 0 | 32 | 3125.00 | -0.35 |
| **#G4** | 415.30 | 17 | 1 | 65 | 413.60 | -0.41 | **#G7** | 3322.37 | 17 | 0 | 65 | 3308.82 | -0.41 |
| **A4** | 440.00 | 16 | 1 | 4A | 439.45 | -0.12 | **A7** | 3519.93 | 16 | 0 | 4A | 3515.63 | -0.12 |
| **#A4** | 466.15 | 15 | 1 | 15 | 468.75 | 0.56 | **#A7** | 3729.23 | 15 | 0 | 15 | 3750.00 | 0.56 |
| **B4** | 493.88 | 14 | 1 | 2A | 502.23 | 1.69 | **B7** | 3950.98 | 14 | 0 | 2A | 4017.86 | 1.69 |

### Music Table2

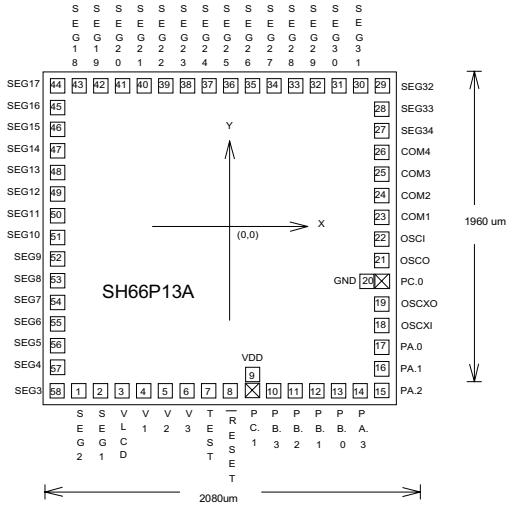
Following is the music scale reference table for channel 1(or channel 2) under OSC = 32.768KHz. Up to 4-octave is possible.
Music scale data for 32K OSC and SEL0 = SEL1 = 0

| Note | Ideal freq. | N | OCT1 /OCT2 | LSFR (C1.6~C1.0) (C2.14~C2.8) | Real freq. | Error% | Note | Ideal freq. | N | OCT1 /OCT2 | LSFR (C1.6~C1.0) (C2.14~C2.8) | Real freq. | Error% |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A1** | 55.00 | 37 | 1 | 0D | 55.35 | 0.64 | **C4** | 261.63 | 63 | 0 | 12 | 260.06 | -0.60 |
| **#A1** | 58.27 | 35 | 1 | 34 | 58.51 | 0.42 | **#C4** | 277.18 | 59 | 0 | 26 | 277.70 | 0.19 |
| **B1** | 61.73 | 33 | 1 | 52 | 62.06 | 0.54 | **D4** | 293.66 | 56 | 0 | 36 | 292.57 | -0.37 |
| **C2** | 65.41 | 31 | 1 | 4B | 66.07 | 1.00 | **#D4** | 311.12 | 53 | 0 | 35 | 309.13 | -0.64 |
| **#C2** | 69.29 | 30 | 1 | 17 | 68.27 | -1.48 | **E4** | 329.63 | 50 | 0 | 2D | 327.68 | -0.59 |
| **D2** | 73.42 | 28 | 1 | 5D | 73.14 | -0.38 | **F4** | 349.23 | 47 | 0 | 6F | 348.60 | -0.18 |
| **#D2** | 77.78 | 26 | 1 | 77 | 78.77 | 1.27 | **#F4** | 369.99 | 44 | 0 | 7B | 372.36 | 0.64 |
| **E2** | 82.41 | 25 | 1 | 6E | 81.92 | -0.60 | **G4** | 392.00 | 42 | 0 | 6C | 390.10 | -0.49 |
| **F2** | 87.31 | 23 | 1 | 39 | 89.04 | 1.99 | **#G4** | 415.30 | 39 | 0 | 63 | 420.10 | 1.16 |
| **#F2** | 92.50 | 22 | 1 | 73 | 93.09 | 0.64 | **A4** | 440.00 | 37 | 0 | 0D | 442.81 | 0.64 |
| **G2** | 98.00 | 21 | 1 | 66 | 97.52 | -0.49 | **#A4** | 466.15 | 35 | 0 | 34 | 468.11 | 0.42 |
| **#G2** | 103.82 | 20 | 1 | 4C | 102.40 | -1.37 | **B4** | 493.88 | 33 | 0 | 52 | 496.49 | 0.53 |
| **A2** | 110.00 | 19 | 1 | 19 | 107.79 | -2.01 | **C5** | 523.25 | 31 | 0 | 4B | 528.52 | 1.01 |
| **#A2** | 116.54 | 18 | 1 | 32 | 113.78 | -2.37 | **#C5** | 554.35 | 30 | 0 | 17 | 546.13 | -1.48 |
| **B2** | 123.47 | 17 | 1 | 65 | 120.47 | -2.43 | **D5** | 587.33 | 28 | 0 | 5D | 585.14 | -0.37 |
| **C3** | 130.81 | 16 | 1 | 4 | 128.00 | -2.15 | **#D5** | 622.24 | 26 | 0 | 77 | 630.15 | 1.27 |
| **#C3** | 138.59 | 15 | 1 | 0C | 136.53 | -1.48 | **E5** | 659.26 | 25 | 0 | 6E | 655.36 | -0.59 |
| **D3** | 146.83 | 112 | 0 | 0A | 146.29 | -0.37 | **F5** | 698.46 | 23 | 0 | 39 | 712.35 | 1.99 |
| **#D3** | 155.56 | 105 | 0 | 1E | 156.04 | 0.31 | **#F5** | 739.97 | 22 | 0 | 73 | 744.73 | 0.64 |
| **E3** | 164.81 | 99 | 0 | 11 | 165.50 | 0.42 | **G5** | 783.99 | 21 | 0 | 66 | 780.19 | -0.49 |
| **F3** | 174.61 | 94 | 0 | 2C | 174.30 | -0.18 | **#G5** | 830.59 | 20 | 0 | 4C | 819.20 | -1.37 |
| **#F3** | 184.99 | 89 | 0 | 1D | 184.09 | -0.49 | **A5** | 880.00 | 19 | 0 | 19 | 862.32 | -2.01 |
| **G3** | 196.00 | 84 | 0 | 29 | 195.05 | -0.49 | **#A5** | 932.31 | 18 | 0 | 32 | 910.22 | -2.37 |
| **#G3** | 207.65 | 79 | 0 | 3E | 207.39 | -0.12 | **B5** | 987.77 | 17 | 0 | 65 | 963.77 | -2.43 |
| **A3** | 220.00 | 74 | 0 | 50 | 221.41 | 0.64 | **C6** | 1046.48 | 16 | 0 | 4A | 1024.00 | -2.15 |
| **#A3** | 233.08 | 70 | 0 | 0E | 234.06 | 0.42 | **#C6** | 1108.71 | 15 | 0 | 15 | 1092.27 | -1.48 |
| **B3** | 246.94 | 66 | 0 | 62 | 248.24 | 0.53 | **D6** | 1174.63 | 14 | 0 | 2A | 1170.29 | -0.37 |

**Ordering Informations**

| Part No. | Packages |
|---|---|
| SH66P13AH | CHIP FORM |
| SH66P13AF | QFP 100 |

## Bonding Diagram

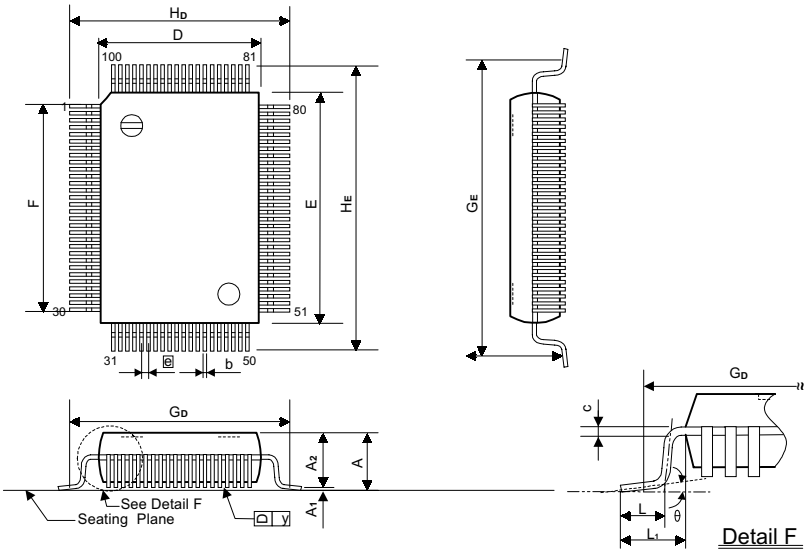



Substrate connect to GND

| Pad No. | Designation | X(μm) | Y(μm) | Pad No. | Designation | X(μm) | Y(μm) |
|---|---|---|---|---|---|---|---|
| 1 | SEG2 | -784 | -854 | 29 | SEG[32] | 904 | 854 |
| 2 | SEG1 | -664 | -854 | 30 | SEG[31] | 784 | 854 |
| 3 | $V_{LCD}$ | -544 | -854 | 31 | SEG[30] | 660 | 854 |
| 4 | V1 | -424 | -854 | 32 | SEG[29] | 540 | 854 |
| 5 | V2 | -304 | -854 | 33 | SEG[28] | 420 | 854 |
| 6 | V3 | -184 | -854 | 34 | SEG[27] | 300 | 854 |
| 7 | TEST | -64 | -854 | 35 | SEG[26] | 180 | 854 |
| 8 | $\overline{RESET}$ | 56 | -854 | 36 | SEG[25] | 60 | 854 |
| 9 | $V_{DD}$ | 176 | -758 | 37 | SEG[24] | -60 | 854 |
| bonding option | PC1 | 176 | -854 | 38 | SEG[23] | -180 | 854 |
| 10 | PB3 | 304 | -854 | 39 | SEG[22] | -300 | 854 |
| 11 | PB2 | 424 | -854 | 40 | SEG[21] | -420 | 854 |
| 12 | PB1 | 544 | -854 | 41 | SEG[20] | -540 | 854 |
| 13 | PB0 | 664 | -854 | 42 | SEG[19] | -660 | 854 |
| 14 | PA3 | 784 | -854 | 43 | SEG[18] | -784 | 854 |
| 15 | PA2 | 904 | -854 | 44 | SEG[17] | -904 | 854 |
| 16 | PA1 | 916 | -724 | 45 | SEG[16] | -916 | 724 |
| 17 | PA0 | 916 | -604 | 46 | SEG[15] | -916 | 600 |
| 18 | OSCXI | 916 | -484 | 47 | SEG[14] | -916 | 480 |
| 19 | OSCXO | 916 | -364 | 48 | SEG[13] | -916 | 360 |
| 20 | GND | 820 | -236 | 49 | SEG[12] | -916 | 240 |
| bonding option | PC0 | 916 | -236 | 50 | SEG[11] | -916 | 120 |
| 21 | OSCO | 916 | -116 | 51 | SEG[10] | -916 | 0 |
| 22 | OSCI | 916 | 4 | 52 | SEG[9] | -916 | -120 |
| 23 | COM1 | 916 | 124 | 53 | SEG[8] | -916 | -240 |
| 24 | COM2 | 916 | 244 | 54 | SEG[7] | -916 | -360 |
| 25 | COM3 | 916 | 364 | 55 | SEG[6] | -916 | -480 |
| 26 | COM4 | 916 | 484 | 56 | SEG[5] | -916 | -600 |
| 27 | SEG[34] | 916 | 604 | 57 | SEG[4] | -916 | -724 |
| 28 | SEG[33] | 916 | 724 | 58 | SEG[3] | -904 | -854 |

## Package Informations

QFP 100L Outline Dimensions unit: inch/mm




| Symbol | Dimensions in inch | Dimensions in mm |
|---|---|---|
| A | 0.130 Max. | 3.30 Max. |
| A**1** | 0.004 Min. | 0.10 Min. |
| A**2** | 0.112 ± 0.005 | 2.85 ± 0.13 |
| b | 0.012 +0.004<br>-0.002 | 0.31 +0.10<br>-0.05 |
| c | 0.006 +0.004<br>-0.002 | 0.15 +0.10<br>-0.05 |
| D | 0.551 ± 0.005 | 14.00 ± 0.13 |
| E | 0.787 ± 0.005 | 20.00 ± 0.13 |
| e | 0.026 ± 0.006 | 0.65 ± 0.15 |
| F | 0.742 NOM. | 18.85 NOM. |
| GD | 0.693 NOM. | 17.60 NOM. |
| GE | 0.929 NOM. | 23.60 NOM. |
| HD | 0.740 ± 0.012 | 18.80 ± 0.31 |
| HE | 0.976 ± 0.012 | 24.79 ± 0.31 |
| L | 0.047 ± 0.008 | 1.19 ± 0.20 |
| L1 | 0.095 ± 0.008 | 2.41 ± 0.20 |
| y | 0.006 Max. | 0.15 Max. |
| θ | 0° ~ 12° | 0° ~ 12° |

**Notes:**

1. Dimensions D&E do not include resin fins.
2. Dimensions GD & GE are for PC Board surfaces mount pad pitch (Design reference only).

**Data Sheet Version History**

| Version | Content | Date |
|---|---|---|
| 1.0 | Original | Nov.2003 |