SINO WEALTH

SH67K91

20K 4-bit Micro-controller with LCD Driver, 4/8 channels Chord

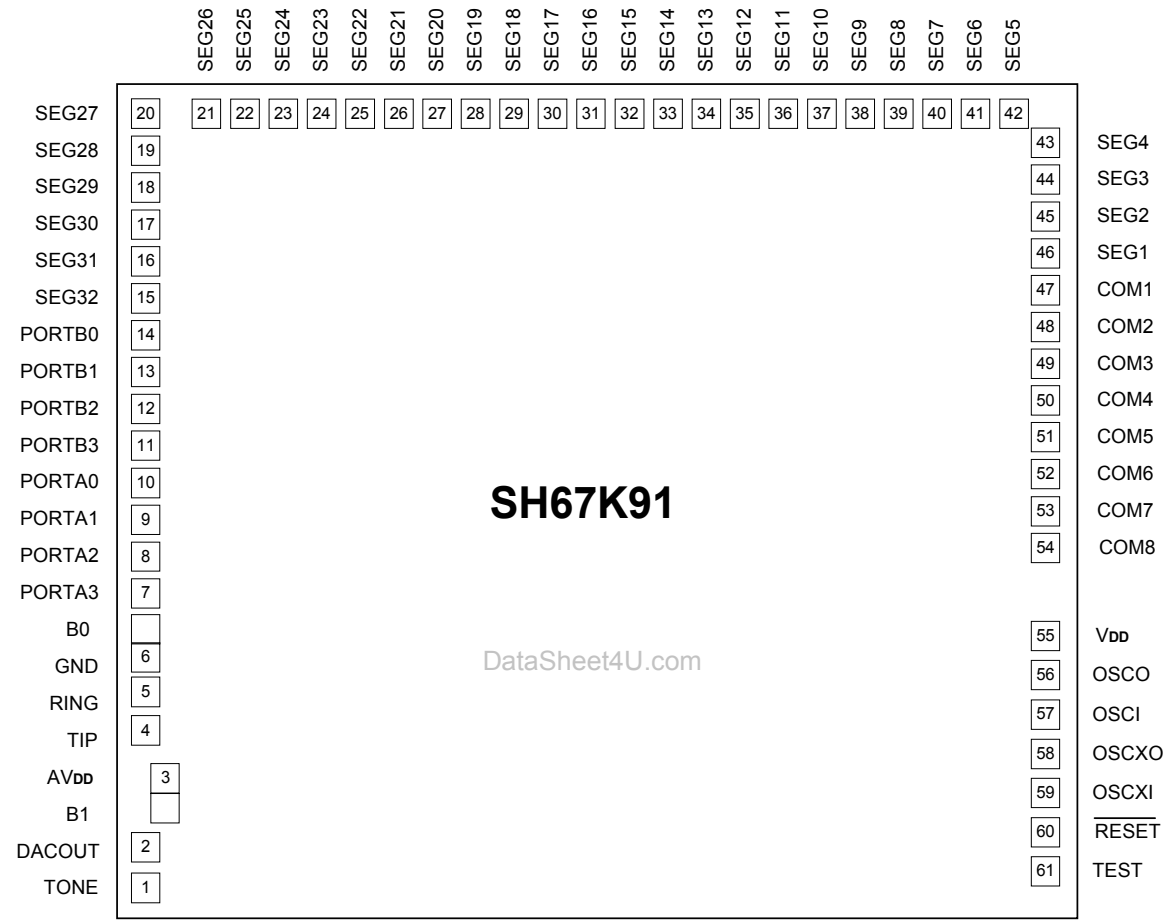
Feature

- SH6610C-Based Single-Chip 4-bit Micro-controller
- ROM: 20K X 16 bits
- RAM: 1437 X 4 bits
  - 48 bytes System Control Register
  - 1325 bytes Data Memory
  - 64 bytes LCD RAM
- Operation Voltage: 2.4V - 5.5V
- 16 CMOS Bi-directional I/O pads (8 shared with Segment)
- 4-Level Stacks (include interrupts)
- One 8-bit Auto Re-load Timer/Counter
- 8-bit Base Timer
- Powerful Interrupt Sources
  - External Interrupt (falling edge)
  - Timer0 Interrupt
  - Base Timer Interrupt
  - External Interrupts: PORTB and PORTC
- LCD Driver
  - 32 Seg X 4 Com (1/4 duty, 1/3 or 1/4 Bias)
  - 32 Seg X 5 Com (1/5 duty, 1/3 or 1/4 Bias)
  - 32 Seg X 6 Com (1/6 duty, 1/3 or 1/4 Bias)
  - 32 Seg X 8 Com (1/8 duty, 1/3 or 1/4 Bias)
- 12 Segments Used as Scan Output
- 4/8 Channels Chords
- 9 bits DAC
- Oscillator (Code Option)
  OSC
  - Crystal Oscillator 32.768kHz
  - RC Oscillator: 262kHz
  OSCX
  - Ceramic Resonator 455kHz - 4MHz
  - RC Oscillator 4MHz
- Instruction Cycle Time
  - 122.07μs for 32.768 kHz Crystal
  - 15.27μs for 262 kHz RC
  - 1μs for 4 MHz RC
- Two Low Power Operation Mode: HALT and STOP
- Warm-up Timer for Power-On Reset (POR)
- Available In CHIP FORM

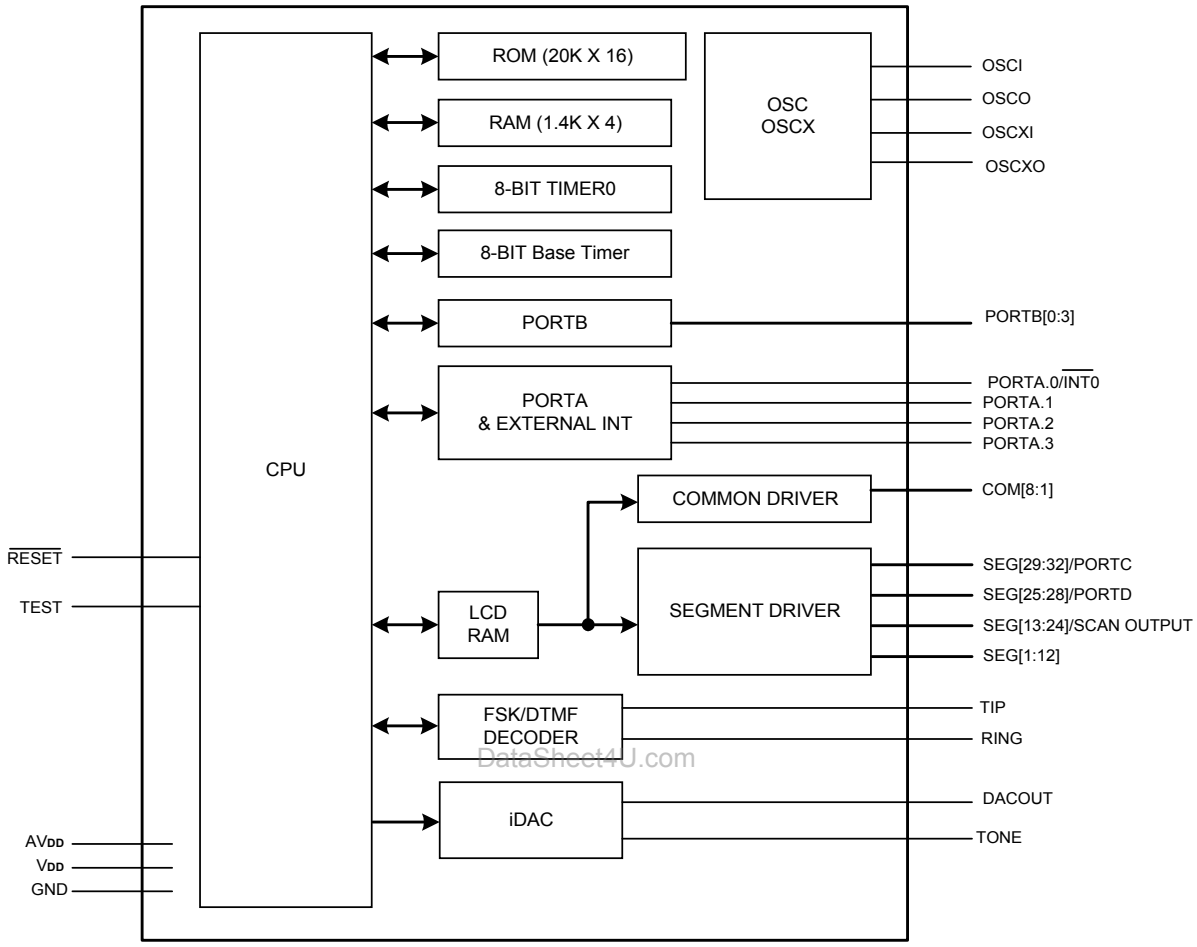
General Description

SH67K91 is a single-chip 4-bit micro-controller. This device integrates a SH6610C CPU core, RAM, ROM, Timer, LCD driver, I/O port, 4/8 channels chord and DAC. This chip contains a built-in dual-oscillator to enhance the total chip performance. This device is suitable for simple CID cord phone.

Pad Configuration



Block Diagram



Pad Description (Total 61 Pads)

Pad No.	Designation	I/O	Description
55	V_{DD}	P	Power supply
3	AV_{DD}	P	Power supply
6	GND	P	Ground pad
61	TEST	I	Test pad (Internal pull-low). No connection for user
60	$\overline{RESET}$	I	Reset input (No internal pull-high)
58	OSCXO	O	High Speed Oscillator output pad
59	OSCXI	I	High Speed Oscillator input pad
56	OSCO	O	Low Speed Oscillator output pad
57	OSCI	I	Low Speed Oscillator input pad
7 - 10	PORTA3 - PORTA0	I/O	Bit programmable I/O, PA0 shared with $\overline{INT0}$
11 - 14	PORTB3 - PORTB0	I/O	Bit programmable I/O, Vector interrupt ($\overline{INT1}$)
15 - 18	SEG32 - SEG29 /PORTC3 - PORTC0	O/ I/O	Segment signal output for LCD display Share with PORTC
19 - 22	SEG28 - SEG25 /PORTD3 - PORTD0	O/ I/O	Segment signal output for LCD display Share with PORTD
23 - 34	SEG24 - SEG13	O	Segment signal output for LCD display Share with scan output
35 - 46	SEG12 - SEG1	O	Segment signal output for LCD display
54 - 47	COM8 - COM1	O	Common signal output for LCD display
4	TIP	I	Connected with TIP side & Ring side for twisted pair
5	RING	I	
2	DACOUT	O	DAC output
1	TONE	O	Tone output

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can only include 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustments for addition/subtraction (DAA, DAS)

Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or a CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be executed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum levels allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of the stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O: $000 - $02F
Data memory: $030 - $2FF, $340 - $3FF, $430 - $5CF
(total 1325 X 4 bits)
Reserved: $5D0- $5FF
LCD RAM space: $300 - $33F

RAM Mapping

$000 - $02F	System Register
$400 - $42F	
$030 - $2FF	Data Memory
$300 - $33F	LCD Display memory
$340 - $3FF	Data Memory
$430 - $5CF	
$5D0-$5FF	Reserved

Note: $400 - $42F and $000 - $02F refer to the same System Register.

RAM bank table: (RAMBNK: System Register RAMBNK0)

RAMBNK0 = 0	Bank 0 **B = 000**	Bank 1 **B = 001**	Bank 2 **B = 010**	Bank 3 **B = 011**	Bank 4 **B = 100**	Bank 5 **B = 101**	Bank 6 **B = 110**	Bank 7 **B = 111**
	$000 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3FF
RAMBNK0 = 1	Bank 8 **B = 000**	Bank 9 **B = 001**	Bank 10 **B = 010**	Bank 11 **B = 011**				
	$430 - $47F	$480 - $4FF	$500 - $57F	$580 - $5FF				

2.2 Configuration of System Register

The Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags
$02	TM0.3	TM0.2	TM0.1	TM0.0	R/W	Timer0 mode register
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	W	Timer0 load low nibble
	TC0L.3	TC0L.2	TC0L.1	TC0L.0	R	Timer0 counter low nibble
$05	TL0H.3	TL0H.2	TL0H.1	TL0H.0	W	Timer0 load high nibble
	TC0H.3	TC0H.2	TC0H.1	TC0H.0	R	Timer0 counter high nibble
$06	BTC.7	BTC.6	BTC.5	BTC.4	R	High nibble of Base Timer counter
$07	BTC.3	BTC.2	BTC.1	BTC.0	R	Low nibble of Base Timer counter
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PPULL	HLM	OXM	OXON	R/W	Bit0: Turn on OSCX oscillator Bit1: CPU clocks select (1: OSC X /0: OSC) Bit2: Heavy load mode Bit3: Port pull-high control for Port excluding PA0
$0D	RAMBNK	LCM2	LCM1	LCM0	R/W	Bit3: RAM Bank control bit Bit2 - 0: LCD contrast adjustment register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table branch register
$0F	INX.3	INX.2	INX1	INX.0	R/W	Index register (INX)
$10	DPL3	DPL2	DPL1	DPL0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	LCDON	O/S2	O/S1	O/S0	R/W	Bit1 - 0: segment/PORTC - D sharing control bits Bit2: Segment/scan output control bit for segment13 - 24 Bit3: LCD on/off control bit
$14	COM_MD1	COM_MD0	BIAS	LCD _FREQ	R/W	Bit0: Lcd frame frequency selection bit Bit1: Lcd Bias selection bit Bit3 - 2: duty selection bit
$15	PACR.3	PACR.2	PACR.1	PACR.0	R/W	Set PORTA to be input/output port
$16	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	Set PORTB to be input/output port
$17	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	Set PORTC to be input/output port
$18	IRQ_PA0	IRQ _FSKIN	B1	B0	R/W R/W R R	Bit3: PA0 interrupt request flag Bit2: FSKIN interrupt request flag Bit1 - 0: Bonding Option

The Configuration of System Register (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$19	TM0.4	PDCR	-	-	R/W	Bit3: the clock source selection bit of timer 0 Bit2: Set PORTD to be input/output port
$1A	DAC _S3	DAC _S2	DAC _S1	DAC _S0	R/W	DAC function control bit
$1B	CH_M	CH_S2	CH_S1	CH_S0	R/W	Bit2 - 0: Channel number of Melody selection bits Bit3: chord mode selection bit
$1C	-	TONE10 DG10 -	TONE 9 DG9 -	TONE 8 DG8 DA8	R/W	Prescaler register for Tone generator High nibble of DAC data register
$1D	TONE7 DG7 DA7	TONE6 DG6 DA6	TONE5 DG5 DA5	TONE4 DG4 DA4	R/W	Counter register for Tone generator Middle nibble of DAC data register
$1E	TONE3 DG3 DA3	TONE2 DG2 DA2	TONE1 DG1 DA1	TONE0 DG0 DA0	R/W	Counter register for Tone generator Low nibble of DAC data register
$1F	ROMBNK3	ROMBNK2	ROMBNK1	ROMBNK0	R/W	Bit 3 - 0: Rom Bank Register
$20	-	VOL 6	VOL 5	VOL 4	R/W	Volume register of Melody
$21	VOL 3	VOL 2	VOL 1	VOL 0	R/W	
$22	Reserved					
$23	-	-	AMP_ON	-	R/W	Bit1: Amplifier power switch
$24	RDT.3	RDT.2	RDT.1	RDT.0	W R	Read Data Table address Read Data register
$25	RDT.7	RDT.6	RDT.5	RDT.4		
$26	RDT.11	RDT.10	RDT.9	RDT.8		
$27	RDT.15	RDT.14	RDT.13	RDT.12		
$28	SEG24	SEG23	SEG22	SEG21	R/W	Scanning output Port Control register
$29	SEG20	SEG19	SEG18	SEG17	R/W	
$2A	SEG16	SEG15	SEG14	SEG13	R/W	
$2B	Reserved					
$2C	Reserved					
$2D	Reserved					
$2E	PA0_PEN	PL/PH	INT0_PA0	DACOUT _S	R/W	Bit3: Pull-high/low resistor control bit of PA0 0: Pull-high/low resistor disable 1: Pull-high/low resistor enable Bit2: Pull-low or pull-high resistor selection control bit of PA0 0: Pull-high resistor enable, Pull-low resistor disable 1: Pull-high resistor disable, Pull-low resistor enable Bit1: Interrupt mode of PA0 (one source of INT0) 0: falling edge interrupt of PA0 1: Rising edge interrupt of PA0 Bit0: DAC output pad selection 0: DAC output from TONE pad 1: DAC output from DACOUT pad
$2F	-	-	-	-	-	Reserved

3. ROM

The ROM can address 20480 words X 16 bits of program area from $0000 to $4FFF.

3.1 Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to $\overline{INT0}$ or FSKIN service routine
$002	JMP*	Jump to Timer0 service routine
$003	JMP*	Jump to Base timer service routine
$004	JMP*	Jump to $\overline{INT1}$ service routine

*JMP instruction can be replaced by any instruction.

3.2 ROM Data Read Table (RDT)

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$25	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$26	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$27	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 16-bit write-only PC address load register (RDT.15 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first then low nibble). Then after one instruction, the right data will be put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

3.3 Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of the ROM space (BANK0). The upper 2K of the CPU address space maps to one of the nineteen banks (BNK.3 - 0 = $00 - $08) of the upper 18K of the ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space							
	BNK = $00	**BNK = $01**	**BNK = $02**	**BNK = $03**	**BNK = $04**	**BNK = $05**	**BNK = $06**	**BNK = $07**
$000 - $7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
$800 - $FFF	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)	2000 - 27FF (BANK 4)	2800 - 2FFF (BANK 5)	3000 - 37FF (BANK 6)	3800 - 3FFF (BANK 7)	4000 - 47FF (BANK 8)

CPU Address	ROM Space	
	BNK = $08	
$000 - $7FF	0000 - 07FF (BANK 0)	
$800 - $FFF	4800 - 4FFF (BANK 9)	

4. Initial State

4.1. System Register State

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset
$00	IEX	IET0	IEBT	IEP	0000
$01	IRQX	IRQT0	IRQBT	IRQP	0000
$02	TM0.3	TM0.2	TM0.1	TM0.0	0000
$03	BTM.3	BTM.2	BTM.1	BTM.0	0000
$04	T0L.3	T0L.2	T0L.1	T0L.0	0000
	TC0L.3	TC0L.2	TC0L.1	TC0L.0	0000
$05	TL0H.3	TL0H.2	TL0H.1	TL0H.0	0000
	TC0H.3	TC0H.2	TC0H.1	TC0H.0	0000
$06	BTC.7	BTC.6	BTC.5	BTC.4	0000
$07	BTC.3	BTC.2	BTC.1	BTC.0	0000
$08	PA.3	PA.2	PA.1	PA.0	xxxx
$09	PB.3	PB.2	PB.1	PB.0	xxxx
$0A	PC.3	PC.2	PC.1	PC.0	xxxx
$0B	PD.3	PD.2	PD.1	PD.0	xxxx
$0C	PPULL	HLM	OXM	OXON	0000
$0D	RAMBNK	LCM2	LCM1	LCM0	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx
$0F	INX.3	INX.2	INX1	INX.0	xxxx
$10	DPL3	DPL2	DPL1	DPL0	xxxx
$11	-	DPM.2	DPM.1	DPM.0	xxxx
$12	-	DPH.2	DPH.1	DPH.0	xxxx
$13	LCDON	O/S2	O/S1	O/S0	0011
$14	COM_MD1	COM_MD0	BIAS	LCD_FREQ	0000
$15	PACR.3	PACR.2	PACR.1	PACR.0	0000
$16	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000
$17	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000
$18	IRQ_PA0	IRQ_FSKIN	B1	B0	0001
$19	TM0.4	PDCR	-	-	0000
$1A	DAC_S3	DAC_S2	DAC_S1	DAC_S0	0000
$1B	CH_M	CH_S2	CH_S1	CH_S0	0000
$1C	-	TONE10 DG10 -	TONE 9 DG9 -	TONE 8 DG8 DA8	0000
$1D	TONE7 DG7 DA7	TONE6 DG6 DA6	TONE5 DG5 DA5	TONE4 DG4 DA4	0000

System Register State (Continued)

Address	Bit3	Bit2	Bit1	Bit0	Power-on Reset/Pin Reset
$1E	TONE3 DG3 DA3	TONE2 DG2 DA2	TONE1 DG1 DA1	TONE0 DG0 DA0	0000
$1F	ROMBNK3	ROMBNK2	ROMBNK1	ROMBNK0	0000
$20	-	VOL 6	VOL 5	VOL 4	0000
$21	VOL 3	VOL 2	VOL 1	VOL 0	0000
$23	-	-	AMP_ON	-	0000
$24	RDT.3	RDT.2	RDT.1	RDT.0	0000
$25	RDT.7	RDT.6	RDT.5	RDT.4	0000
$26	RDT.11	RDT.10	RDT.9	RDT.8	0000
$27	RDT.15	RDT.14	RDT.13	RDT.12	0000
$28	SEG24	SEG23	SEG22	SEG21	0000
$29	SEG20	SEG19	SEG18	SEG17	0000
$2A	SEG16	SEG15	SEG14	SEG13	0000
$2E	PA0_PEN	PL/PH	INT0_PA0	DACOUT_S	0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4

5.1 Instruction Cycle Time:

(1) 4/32.768kHz (≈122.12μs) for 32.768kHz oscillator.
(2) 4/262kHz(≈ 15.27μs) for 262kHz oscillator.
(3) 4/455kHz (≈ 8.79μs) for 455kHz oscillator.
(4) 4/4MHz (= 1μs) for 4MHz oscillator.

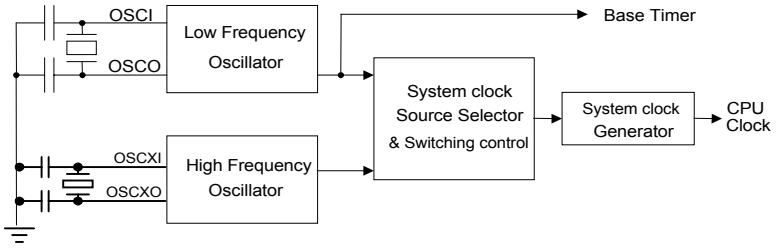
5.2 Circuit Configuration

SH67K91 has two on-chip oscillation circuits OSC and OSCX.

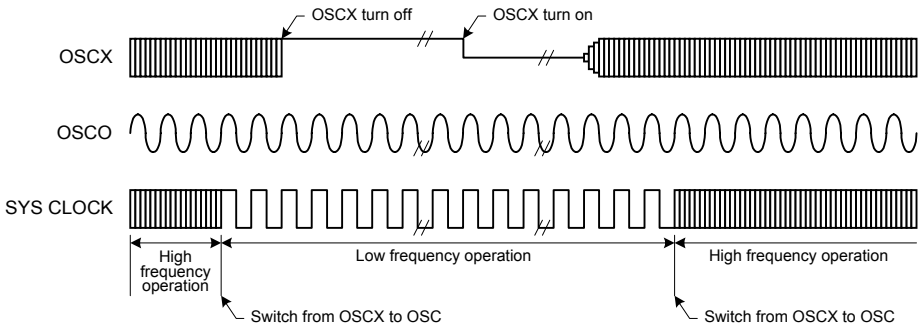
OSC is a low frequency oscillator (32.768kHz crystal) or RC (Typ. 262kHz) determined by the code option. OSCX also has two types: ceramic (455kHz - 4MHz) or RC (4MHz) determined by code option. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At the start of reset initialization, the OSC starts oscillation and OSCX is turned off. Immediatly after reset initialization, the OSC clock is automatically selected as the system clock input source.

Oscillator Block Diagram



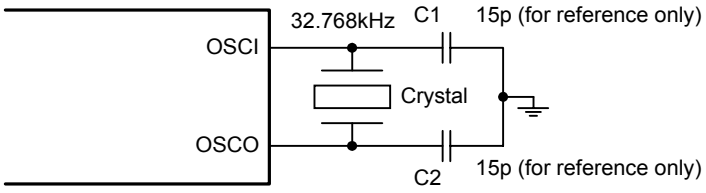
Timing of System Clock Switching



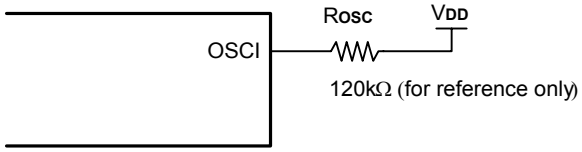
5.3. OSC Oscillation

The OSC generates the basic clock pulses that provide the CPU and peripherals (Timer0, BaseTimer, LCD) with an operating clock.

(1) OSC Crystal oscillator type



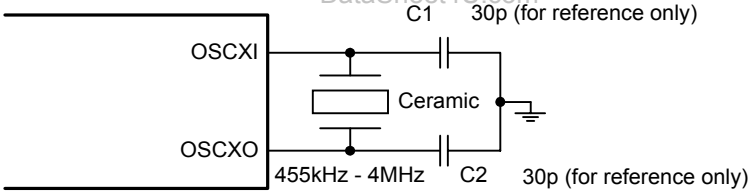
(2) OSC RC oscillator type



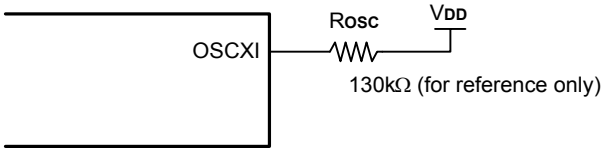
5.4. OSCX Oscillator

OSCX has two clock oscillators. The code options select the Ceramic or RC as the CPU's clock.
If the OSCX is not used, it must be masked into Ceramic resonator and the OSCXI must be connected to GND.

(1) OSCX Ceramic oscillator type



(2) OSCX RC oscillator type



5.5 Control of Oscillator

The oscillator control register configuration is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0C	PPULL	HLM	OXM	OXON	R/W	Bit0: Turn on OSCX oscillator Bit1: CPU clocks select (1:OSCX /0:OSC)

OXON: OSCX oscillation on/off.
0: Turn off OSCX oscillator 1: Turn on OSCX oscillator

OXM: switching system clock.
0: select OSC as system clock 1: select OSCX as system clock

5.6. Programming Notes

It takes at least 5 ms for the OSCX oscillation circuit to turn on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, the user must wait a minimum of 5ms since the OSCX oscillation is running. However, the start time varies with respect to oscillator characteristics and the condition of use. Thus the wait time depends on the application. When switching from OSCX to OSC, OSCX is turned off with one instruction. The OSCX turn off control will be delayed for one instruction cycle automatically to prevent CPU operation error.

6. I/O PORT

The MCU provides 16 bi-directional I/O pads. The PORT data is put in register $08 - $0B. The PORT control register ($15 - $17, $19) controls the PORT as input or output. Each I/O port for PA3 - 1,PB, PC, PD has an internal pull-high resistor, which is controlled by PULLEN of $0C and the data of the port, when the PORT is used as input.

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data
$15	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$16	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$17	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$19	TM04	PDCR	-	-	R/W	PORTD input/output control

Each bit of the PORTA, PORTB and PORTC has its own direction-control bit, and the PORTD has one control bit only for all bits.

PA (/B/C) CR.n, (n = 0, 1, 2, 3)

0: Set I/O as an input direction. (Power on initial)

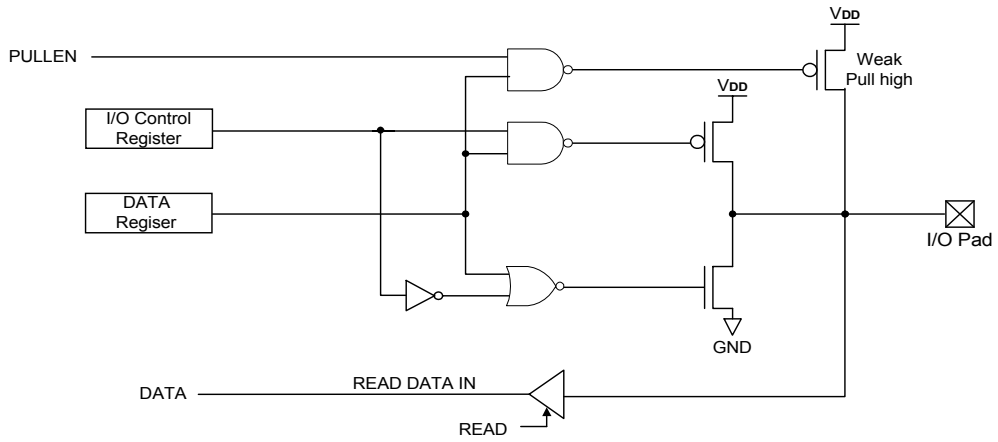
1: Set I/O as an output direction.

PDCR

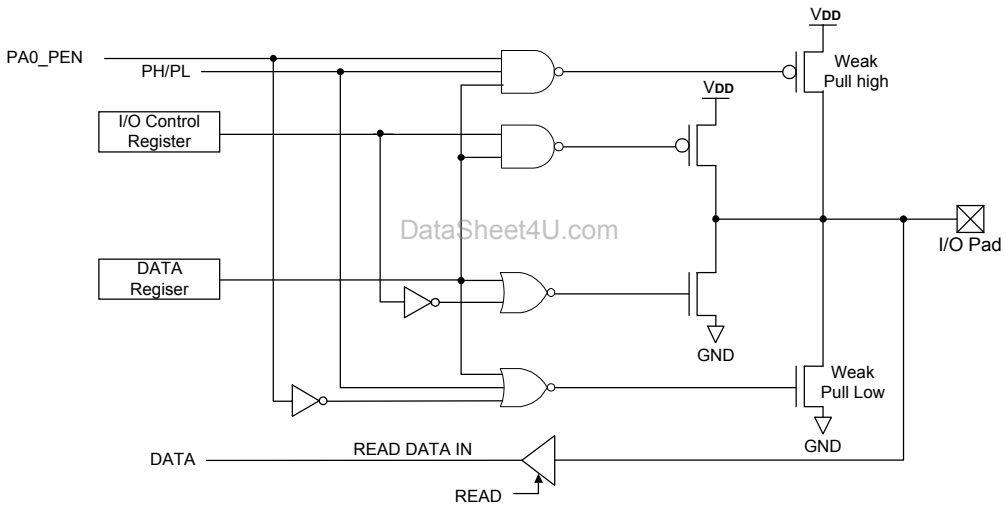
0: Set PD3 - 0 as an input direction. (Power on initial)

1: Set PD3 - 0 as an output direction.

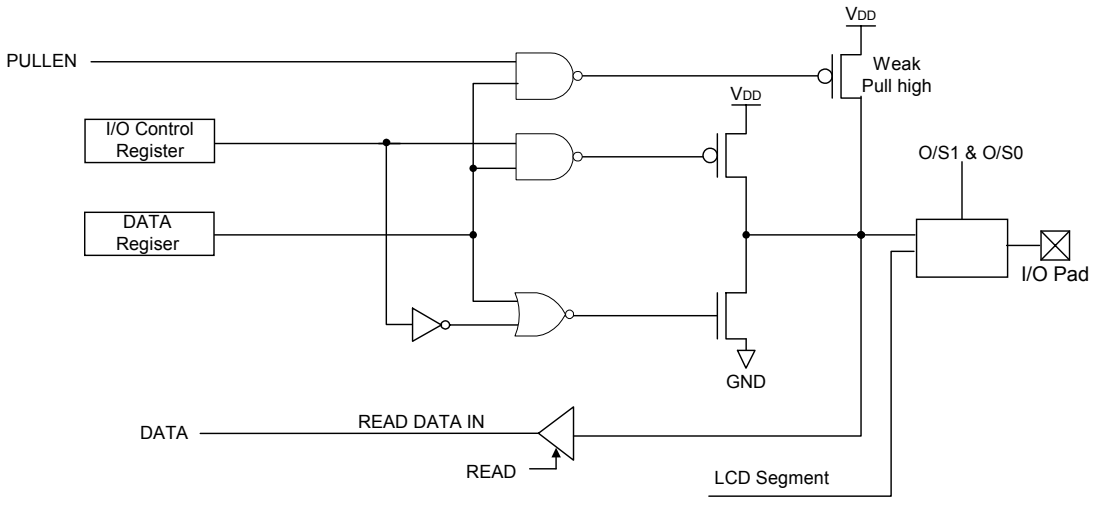
Equivalent Circuit for PB3 - 0,PA3 - 1



Equivalent Circuit for PA0



Equivalent Circuit for PC3 - 0,PD3 - 0



6.1 System Register (PMOD)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0C	PPULL	HLM	OXM	OXON	R/W	Bit2: Heavy load mode Bit3: Port pull-high control
$2E	PA0_PEN	PL/PH	INT0_PA0	DACOUT_S	R/W	Bit3: Pull high/low resistor control bit of PA0 0: Pull high/low resistor disable 1: Pull high/low resistor enable Bit2: Pull-low resistor or pull-high resistor selection control bit of PA0 0: Pull-high resistor enable, Pull-low resistor disable 1: Pull-high resistor disable, Pull-low resistor enable

HLM: Enable heavy load mode
0: Disable
1: Enable

PPULL: Pull-high resistor control bit of PA3 - 1,PB, PC, PD
0: Disable pull-high resistor
1: Enable pull-high resistor

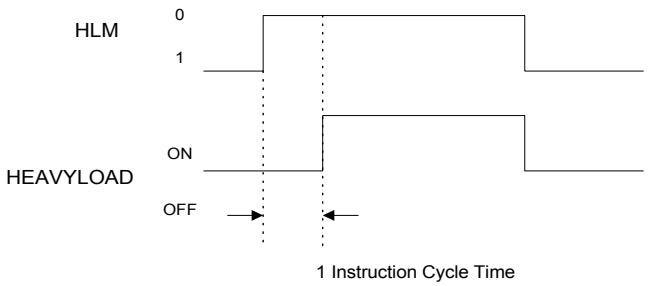
PA0_PEN: Pull high/low resistor control bit of PA0
0: Pull high/low resistor disable
1: Pull high/low resistor enable

PL/PH: Pull-low resistor or pull- high resistor selection control bit of PA0
0: Pull- high resistor enable, Pull-low resistor disable
1: Pull- high resistor disable, Pull-low resistor enable

6.2 Heavy Load Mode (HLM)

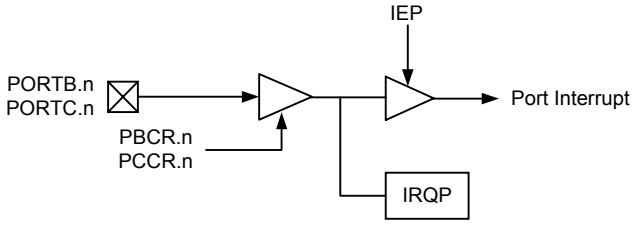
The MCU has a heavy load protection circuit for when the battery load becomes heavy, such as, when an external buzzer sounds or an external speaker is turned on. In this mode, the crystal oscillator circuit is backed-up for high gain. When this mode is set up, more power would be provided to an oscillator circuit. Unless it is necessary, avoid setting this mode with the software since the mode enterance would delay for one instruction. Please activate heavy load driving only after setting HLM for at least one instruction wait cycle through the software. The following shows the programming setting.

HLM: 0 = Heavy load protection mode is released
1 = Heavy load protection mode is set.



6.3. Port Interrupt

The PORTB and PORTC are used as port interrupt sources.
The following is the port interrupt function block-diagram.



Note: n = 0, 1, 2, 3

Port Interrupt (PBC INT) PROGRAMMING NOTES

If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.

1. Set the port as input port, fill port data register with 1 and avoid port floating.
2. Pull-high the port (Use external pull high resistance or set PULLEN to 1).

And further falling edge transition would not be able to make interrupt request until all of the pins are returned to V_{DD} in PBC INT application.

When PORTC is shared to segment, user can only generate interrupt on PORTB.

6.4. External Interrupt ($\overline{INT0}$)

PA0 and FSKIN are shared by external interrupts (active low).

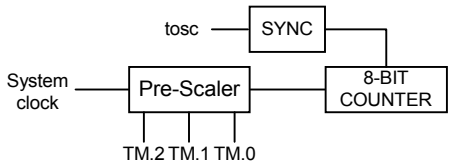
7. Timer0

SH67K91 has one 8-bit timer.

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. TIMER0 Configurations and Operation

The Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has both low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, followed by the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high-order digit is written, or counter counts overflow from $FF to $00.

Timer Load Register: The register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

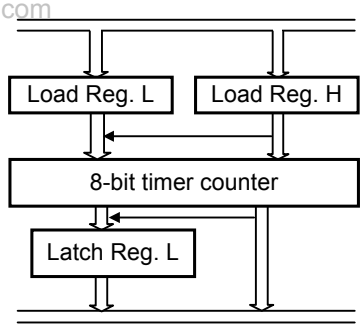
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.2. Timer0 Mode Register

The timer can be programmed in several different prescalers by setting Timer Mode register (TM0).

The 8-bit counter prescaler overflows output pulses. The Timer Mode register (TM0) is 3-bit register used for the timer control as shown in Table 1. The mode register selects the input pulse sources into the timer. The clock source of timer0 is selected by the TM0.4 control bit.

Table 1. Timer0 Mode register

TM0.3	TM0.2	TM0.1	TM0.0	Prescaler	Clock Source		Auto Reload
					TM0.4=1($19.3)	TM0.4=0($19.3)	
0	0	0	0	/2048	OSC/4	System clock	No
0	0	0	1	/512	OSC/4	System clock	No
0	0	1	0	/128	OSC/4	System clock	No
0	0	1	1	/32	OSC/4	System clock	No
0	1	0	0	/8	OSC/4	System clock	No
0	1	0	1	/4	OSC/4	System clock	No
0	1	1	0	/2	OSC/4	System clock	No
0	1	1	1	/1	OSC/4	System clock	No
1	0	0	0	/2048	OSC/4	System clock	Yes
1	0	0	1	/512	OSC/4	System clock	Yes
1	0	1	0	/128	OSC/4	System clock	Yes
1	0	1	1	/32	OSC/4	System clock	Yes
1	1	0	0	/8	OSC/4	System clock	Yes
1	1	0	1	/4	OSC/4	System clock	Yes
1	1	1	0	/2	OSC/4	System clock	Yes
1	1	1	1	/1	OSC/4	System clock	Yes

TM0.3 control function:

0: without Auto-Reload function for timer0 1: Auto-Reload function for timer0

TM0.4 control function:

0: clock source of timer0 is system clock 1: clock source of timer0 is OSC/4 clock

8. Base Timer

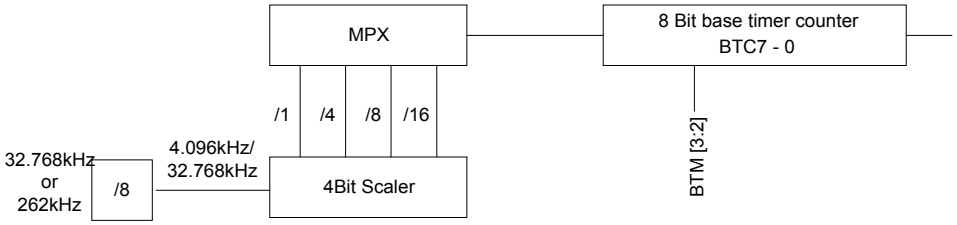
The MCU has a base timer that is shared with the warm-up timer and the clock source is OSC (Low frequency oscillation: Crystal 32.768kHz or RC 262kHz). After MCU is reset, it counts at every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow. This causes the interrupt of base timer interrupt request flag to 1.Therefore, the base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal output.

The timer accepts 4096Hz or 32.768kHz clock, and base timer generates an accurate timing interrupt.

This clock-input source is selected by BTM register.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
	1	0	X	X		Enable the base timer
	Other states		X	X		Disable the base timer, clear base timer counters and keep them as $00
$06	BTC.7	BTC.6	BTC.5	BTC.4	R	The counter register of base timer
$07	BTC.3	BTC.2	BTC.1	BTC.0		

BTM.1	BTM.0	Prescaler Ratio	Clock Source
0	0	/1	4.096kHz or 32.768kHz
0	1	/4	4.096kHz or 32.768kHz
1	0	/8	4.096kHz or 32.768kHz
1	1	/16	4.096kHz or 32.768kHz



9. LCD Driver

The LCD driver contains a controller, a voltage generator, 8/4 common driver pads and 32 segment driver pads. There are 8 different driving programmable modes: 1/8 duty and 1/3 bias, 1/8 duty and 1/4 bias, 1/6 duty and 1/3 bias, 1/6 duty and 1/4 bias, 1/5 duty and 1/3 bias, 1/5 duty and 1/4 bias, 1/4 duty and 1/3 bias, 1/4 duty and 1/4 bias. The driving mode is controlled by the system register $14 and the power on initialization status is 1/8 duty, and 1/4 bias. The controller consists of display data RAM and a duty generator.

The LCD SEG13 - 24 can also be used as output port, which is selected by the bit 2 of the system register $13. When SEG13 - 24 are selected to be output port, one should write data to RAM addresses ($28 - $2A). The LCD SEG25 - 32 can also be used as I/O port (PORTC and PORTD), which is selected by bit 1,0 of the system register $13. LCD RAM could be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM would still retain the value.

When LCD is off, both common and segment outputs are low.

9.1. LCD Control Register

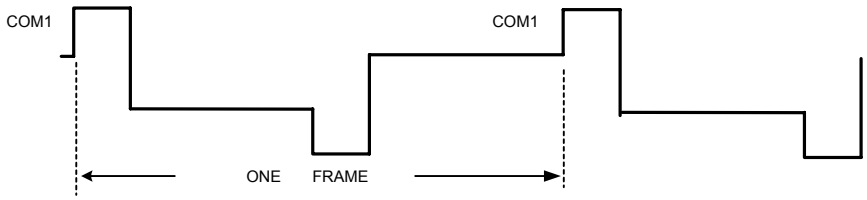
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	RAMBNK	LCM2	LCM1	LCM0	R/W	Bit2 - 0: LCD contrast adjustment register
$13	LCDON	O/S2	O/S1	O/S0	R/W	Bit1 - 0: segment/PORTC - D sharing control bits Bit2: Segment/scan output control bit for segment13 - 24 Bit3: LCD on/off control bit
$14	COM_M1	COM_MD0	BIAS	LCD_FREQ	R/W	Bit0: Lcd frame frequency selection bit Bit1: Lcd Bias selection bit Bit3 - 2: duty selection bit
$28	SEG24	SEG23	SEG22	SEG21	R/W	Data Register of LCD SEG24 - 21 when SEG24 - 21 shared as output port.
$29	SEG20	SEG19	SEG18	SEG17	R/W	Data Register of LCD SEG20 - 17 when SEG20 - 17 shared as output port.
$2A	SEG16	SEG15	SEG14	SEG13	R/W	Data Register of LCD SEG16 - 13 when SEG16 - 13 shared as output port.

LCD ON/OFF control and LCD shared control register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	LCDON	O/S2	O/S1	O/S0	R/W	LCD ON/OFF control and LCD shared control
	0	X	X	X		LCD OFF
	1	X	X	X		LCD ON
	X	0	X	X		Segment13 - 24 set as segment signal of LCD
	X	1	X	X		Segment13 - 24 set as output port
	X	X	0	0		Segment25 - 32 shared as LCD Segment output
	X	X	0	1		Segment29 - 32 shared as PORTC3-PORTC0 Segment28 - 25 shared as LCD Segment output
	X	X	1	X		Segment29 - 32 shared as PORTC3-PORTC0 Segment28 - 25 shared as PORTD3-PORTD0

LCD Duty and Bias setting register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	COM_MD1	COM_MD0	BIAS	LCD_FREQ	R/W	
	0	0	X	X		LCD driver = 1/8 duty
	0	1	X	X		LCD driver = 1/6 duty, COM8 - 7 output unselected level
	1	0	X	X		LCD driver = 1/5 duty, COM8 - 6 output unselected level
	1	1	X	X		LCD driver = 1/4 duty, COM8 - 5 output unselected level
	X	X	0	X		LCD driver = 1/4 bias
	X	X	1	X		LCD driver = 1/3 bias
	X	X	X	0		LCD frame frequency = 64Hz
	X	X	X	1		LCD frame frequency = 32Hz



When the CPU is in the STOP mode, the COMx and SEGx are pulled low. It can easily be woken up by a keyboard scan (Port interrupt). When the CPU is in the HALT mode, the COMx and SEGx are normal. It can easily be woken up by base timer、timer0 or port interrupt.

9.2. Configuration of LCD RAM

Segment1 - 32, 1/8 duty

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$330	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$331	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$332	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$333	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$334	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$335	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$336	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$337	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$338	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$339	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$33A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$33B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$33C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$33D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$33E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$33F	SEG32	SEG32	SEG32	SEG32

Segment1 - 32, 1/6 duty

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$330	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$331	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$332	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$333	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$334	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$335	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$336	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$337	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$338	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$339	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$33A	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$33B	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$33C	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$33D	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$33E	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$33F	SEG32	SEG32

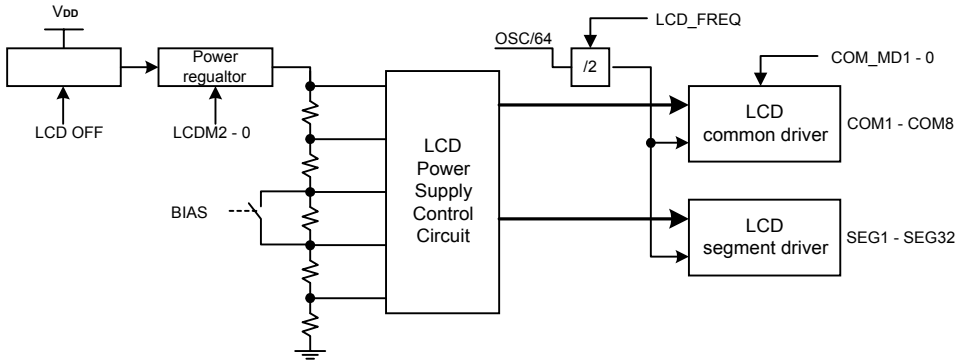
Segment1 - 32, 1/5 duty

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit0
	COM4	COM3	COM2	COM1		COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$330	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$331	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$332	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$333	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$334	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$335	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$336	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$337	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$338	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$339	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$33A	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$33B	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$33C	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$33D	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$33E	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$33F	SEG32

Segment1 - 32, 1/4 duty

Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32

9.3 LCD Power



The contrast control register can adjust the contrast of LCD.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	RAMBNK	LCM2	LCM1	LCM0	R/W	Bit2 - 0: LCD contrast adjustment register

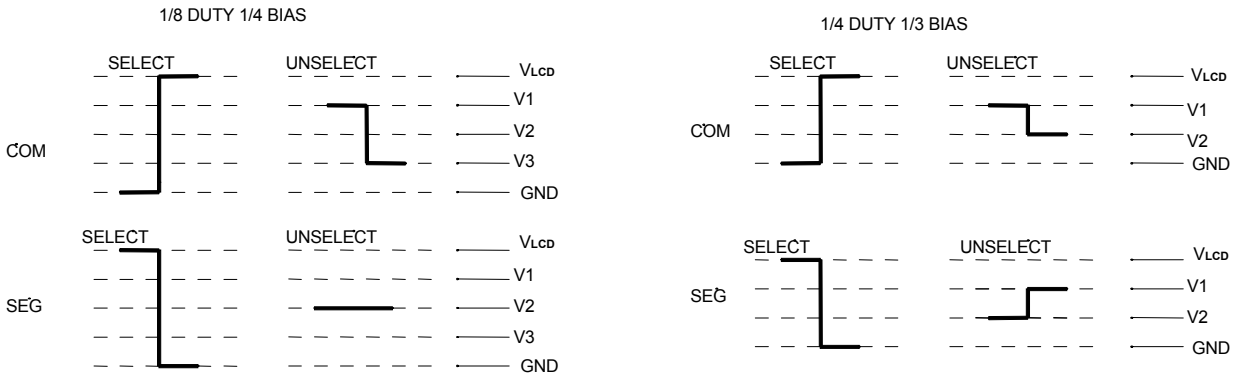
LCDM2	LCDM1	LCDM0	V_{LCD}/V_{DD}	
			Mainchip	EV
0	0	0	0.70	0.60
0	0	1	0.76	0.65
0	1	0	0.82	0.70
0	1	1	0.88	0.90
1	0	0	0.94	0.95
1	0	1	1.00	1.00
1	1	0	1.00	1.00
1	1	1	1.00	1.00

Note:

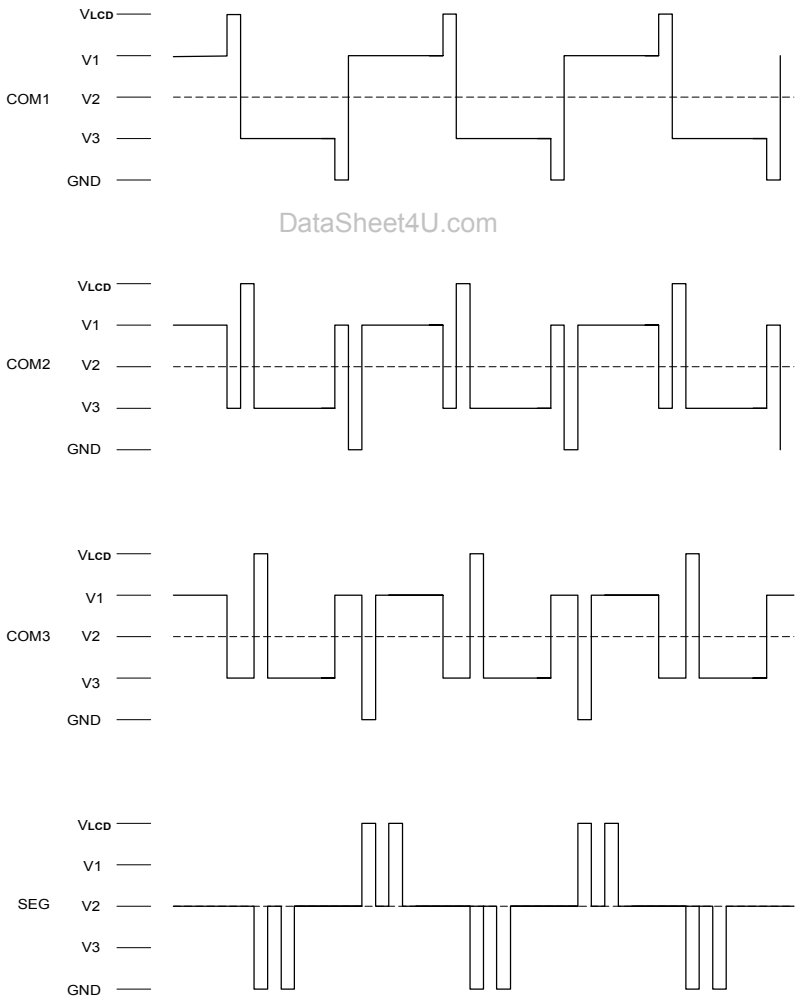
There is some difference for LCD contrast level setting between mainchip and EV chip.

For mainchip, the V_{LCD} level setting is linear from 0.7V_{DD} to V_{DD} and the step is 0.06V_{DD}, and for EV chip, the V_{LCD} level setting is non-linear from 0.6V_{DD} to V_{DD}.

9.4 LCD Waveform



Example: 1/8 duty, 1/4 bias



10. Interrupt

Four interrupt sources are available on SH67K91:

- External interrupt ($\overline{\text{INT0}}$)
- Timer0 interrupt
- Base Timer interrupt
- Port's falling edge detection interrupt ($\overline{\text{INT1}}$)

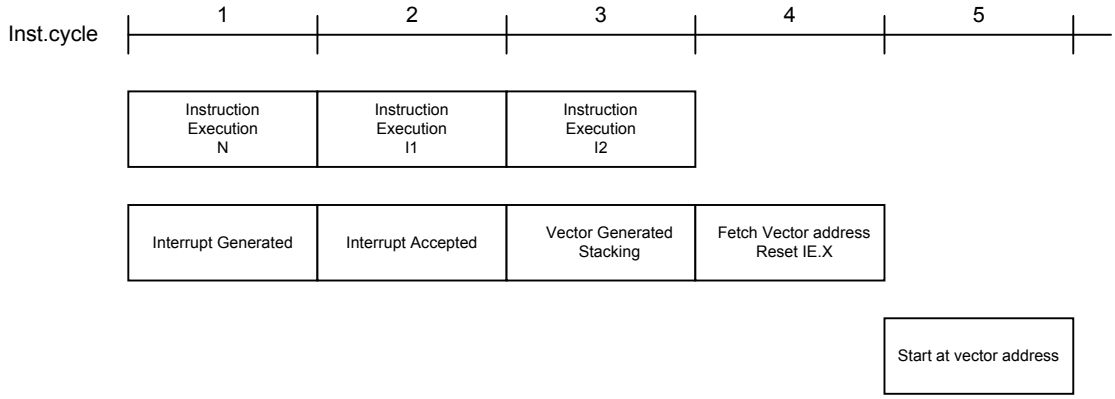
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to “0” at initialization by the chip reset.

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Reamrks
$00	IEX	IET0	IEBT	IEP	R/W	1: Enable/0: Disable
$01	IRQEX	IRQT0	IRQBT	IRQP	R/W	1: Request/0: No request
$18	IRQ_PA0	IRQ_FSKIN	B1	B0	R/W	IRQ_PA0: 1: PA0 interrupt Request 0: No request IRQ_FSKIN: 1: FSKIN interrupt Request 0: No request

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

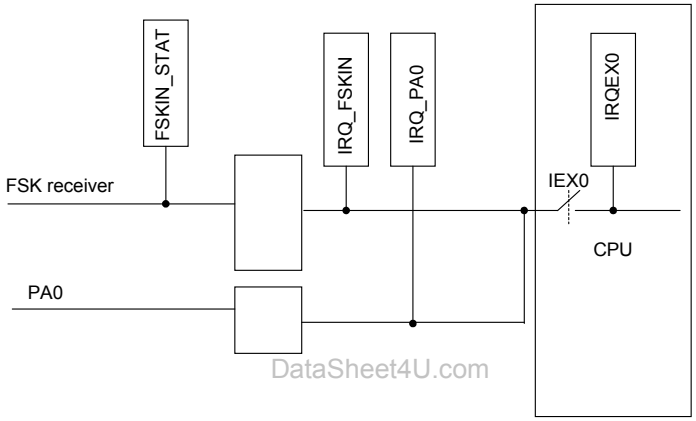
During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt ($\overline{INT0}$)

Interrupt 0 is shared with the PORTA0, the FSK receiver, falling edge active. When the bit 3 of the register $0 (IEX) is set to 1, the interrupt0 is enabled. Writing a "0" to PA0 will generate an external interrupt.

When the an interrupt0 occurred, one must read the IRQPA0, IRQ_FSKIN first to judge the interrupt source is from PA0, the FSK receiver.

IEX:	Interrupt0 on/off switch.	
	0: disable.	1: Enable
IRQEX:	Interrupt0 interrupt request	
	0: No request	1: Request
IRQ_PA0:	PA0 interrupt request	
	0: No request	1: Request
IRQ_FSKIN:	FSK receiver interrupt request	
	0: No request	1: Request



Note:

While external interrupt is enabled, writing a "1" (or “0”) to the external interrupt I/O port will generate an external interrupt.

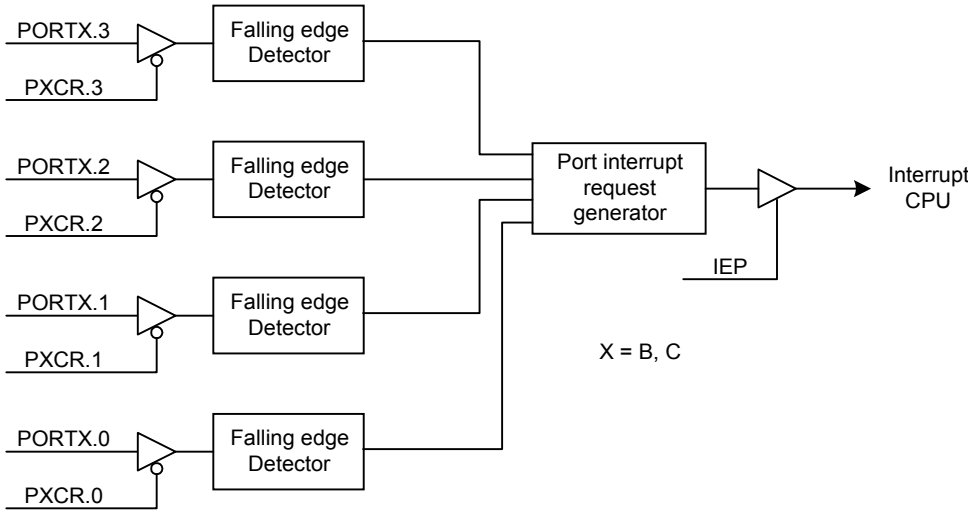
Timer Interrupt

The input clocks of Timer0 and Base Timer are based on system clock. The timers overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQBT1 = 1), If the interrupt enable flag is enabled (IET0 or IEBT1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from the HALT mode.

Port Falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

Any one of the I/O input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from the HALT or the STOP mode.



Port Interrupt Block Diagram

11. 4/8 Channels Chords/ 9bit DAC

Melody Prescaler /DTMF Generator/DAC data register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1A	DAC_S3	DAC_S2	DAC_S1	DAC_S0	R/W	DAC function control register
$1B	CH_M	CH_S2	CH_S1	CH_S0	R/W	Chord mode control bit, and Channel control register
$1C	-	TONE10 DG10 -	TONE 9 DG9 -	TONE 8 DG8 DA8	R/W	Tone prescaler DTMF Generator Presacler DAC data register
$1D	TONE7 DG7 DA7	TONE6 DG6 DA6	TONE5 DG5 DA5	TONE4 DG4 DA4		
$1E	TONE3 DG3 DA3	TONE2 DG2 DA2	TONE1 DG1 DA1	TONE0 DG0 DA0		
$20	-	VOL 6	VOL 5	VOL 4	R/W	Volume register
$21	VOL 3	VOL 2	VOL 1	VOL 0		
$2E	PA0_PEN	PL/PH	INT0_PA0	DACOUT_S	R/W	DAC output pad selection

CH_M: the chord type select bit
0: 4 or less 4 channels chords
1: 8 or more 4 channel schords

CH_S2 - 0: the index bits of eight channel for setting the prescaler and volume register.

TONE10 - 8/DG10 - 8/DA8: the High nibble of Prescaler register of Tone generator or high nibble of DAC data

TONE7 - 4/DG7 - 4/DA7 - 4: the Middle nibble of Prescaler register of Tone generator or middle nibble of DAC data

TONE3 - 0/DG3 - 0/DA3 - 0 the Low nibble of Prescaler register of Tone generator or low nibble of DAC data
While writing DAC data or prescaler data, please writing the Low nibble first, then middle nibble and the high nibble at last.

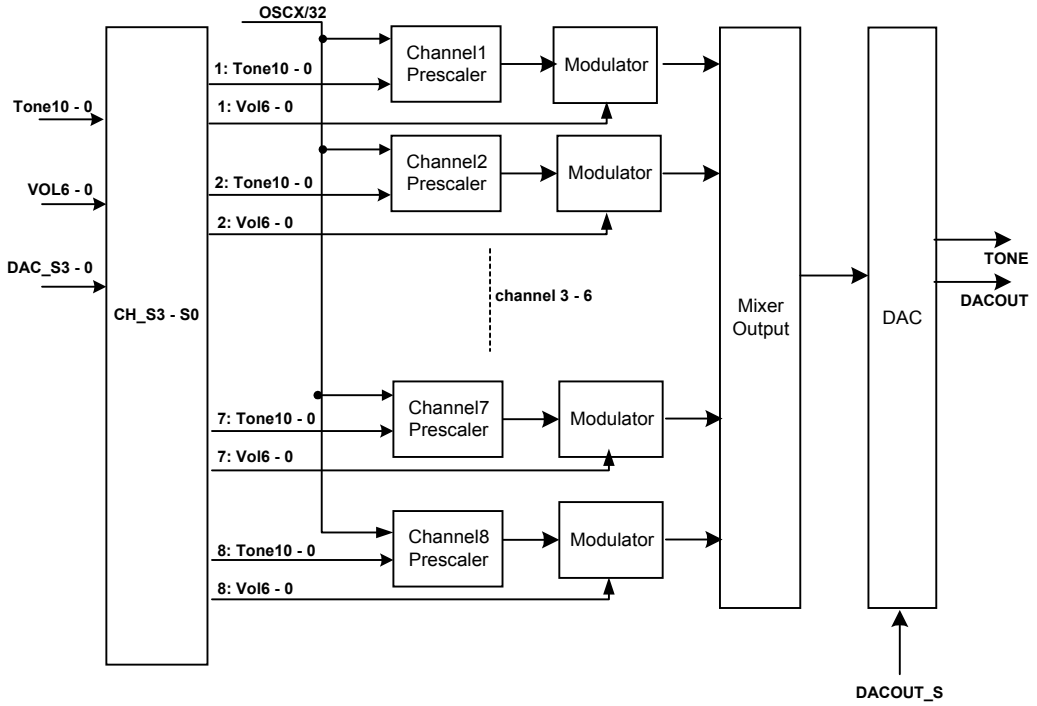
VOL6 - 0: the volume register Tone generator
While writing Volume data, please write the Low nibble first, then the high nibble.

DAC_S3 - 0: the operation mode setting of DAC

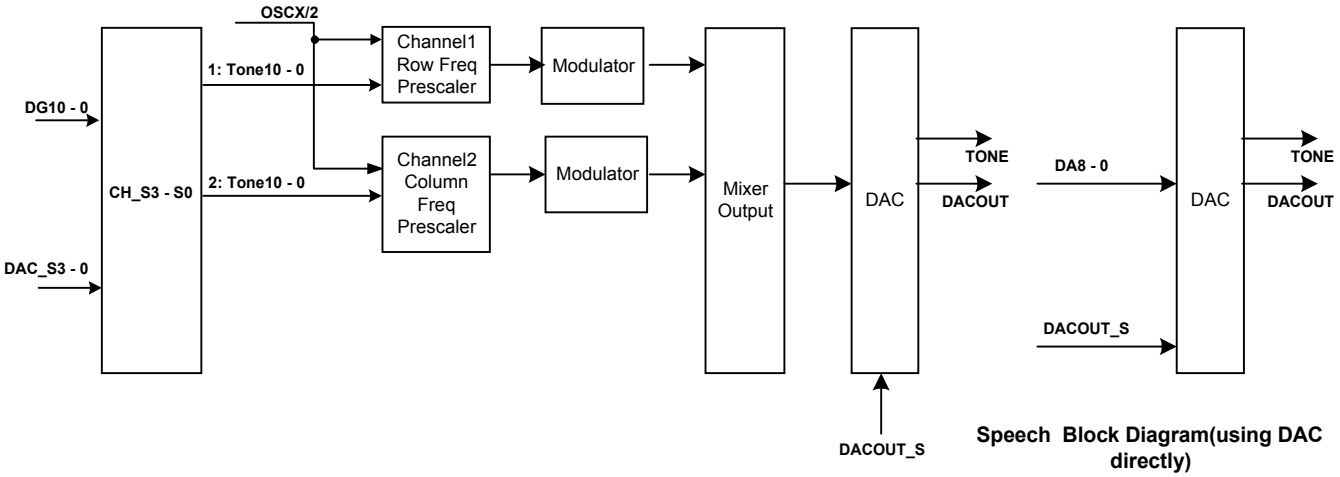
DACOUT_S: the DAC output pad selection control bit
0: DAC output from TONE Pad
1: DAC output from DACOUT Pad

DAC_S3	DAC_S2	DAC_S1	DAC_S0	Melody (DAC data is from the Melody)	DTMF Generaotr	DAC (DAC data is from the DA8 - 0)
0	0	0	0	All Disable	Disable	Disable
0	0	0	1	All Disable	Disable	Enable
0	0	1	0	All Disable	Enable	Disable
0	0	1	1	Reserved		
0	1	x	x			
1	0	0	0	Channel 1 enable	Disable	Disable
1	0	0	1	Channel 1 - 2 enable	Disable	Disable
1	0	1	0	Channel 1 - 3 enable	Disable	Disable
1	0	1	1	Channel 1 - 4 enable	Disable	Disable
1	1	0	0	Channel 1 - 5 enable	Disable	Disable
1	1	0	1	Channel 1 - 6 enable	Disable	Disable
1	1	1	0	Channel 1 - 7 enable	Disable	Disable
1	1	1	1	Channel 1 - 8 enable	Disable	Disable

When DAC_S3 - 0 = 0000, the power of meoldy modulator block and DAC block is off.



Melody Block Diagram



DTMF Generator Block Diagram

Speech Block Diagram(using DAC directly)

12. STOP/HALT Mode

After the execution of the HALT instruction, SH67K91 will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Timer, Base timer, …etc.) will keep the same status.

After the execution of the STOP instruction, SH67K91 will enter the STOP mode. The whole chip (including oscillator) will STOP operating.

In the HALT mode, SH67K91 can be waked up if any interrupt occurs.

In the STOP mode, SH67K91 can be waked up if port interrupt occurs.

When CPU is awaked from the HALT/STOP by any initial source, it will execute the relevant initial serve subroutine at first. Then the next instruction is executed.

STOP/HALT mode	Oscillator	CPU core	Wake up
STOP	OSC Stop OSCX Stop	Hold	$\overline{RST}$, $\overline{INT0}$, $\overline{INT1}$
HALT	OSC live OSCX live	Hold	$\overline{RST}$, $\overline{INT0}$, $\overline{INT1}$, T0INT, BTINT

13. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

13.1. Power-on Reset

Warm-up time interval:

(1) In RC oscillator mode, the warm-up counter prescaler divide ratio is $/2^7$ (128).

(2) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $/2^{12}$ (4096).

13.2. Wake-up from the STOP Mode

Warm-up time interval:

(1) In RC oscillator mode, the warm-up counter prescaler divide ratio is $/2^{12}$ (4096).

(2) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $/2^{12}$ (4096).

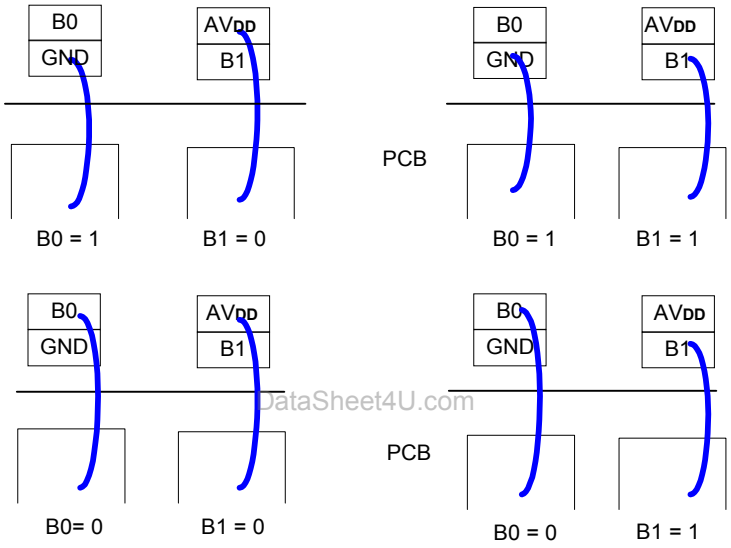
The clock source of warm-up timer is system clock.

System clock is unchange When system return from STOP mode.

14. Bonding Option

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$18	IRQ_PA0	IRQ_FSKIN	B1	B0	R	B1, B0: Bonding option
			0	1	R	Default bonding option
			0	0	R	B0 bond to GND
			1	1	R	B1 bond to AVDD
			1	0	R	B0 bond to GND & B1 bond to AVDD



Up to 4 different bonding options are possible for user's needs. The chip's program has 4 different program flows that varies depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

15. Code Option

C: OSC clock source

0: 32.768kHz crystal

1: 262kHz RC

L: OSCX clock source

0: 455kHz - 4MHz ceramic

1: 4MHz RC

16. Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

16.1. Arithmetic and Logical Instruction

16.1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC [3], AC [0] -> CY; AC shift right one bit	CY

16.1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

16.1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub	CY

16.2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

16.3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC +1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- ll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

17. Chord Table

Following is the chord scale reference table for all channel under OSCX = 4MHz. (Up to 6 octaves are possible)

Note	Ideal freq.	N	Tone Prescaler	Real freq.	Error%	Note	Ideal freq.	N	Tone Prescaler	Real freq.	Error%
B1	61.73	2024	7E8	61.73	0.00	**B4**	493.88	252	FC	494.07	-0.04
C2	65.10	1919	77F	65.10	-0.01	**C5**	523.25	238	EE	523.01	0.05
#C2	69.29	1803	70B	69.29	0.00	**#C5**	554.35	224	E0	555.56	-0.22
D2	73.42	1702	6A6	73.40	0.03	**D5**	587.33	212	D4	586.85	0.08
#D2	77.78	1606	646	77.78	-0.01	**#D5**	622.24	200	C8	621.89	0.06
E2	82.41	1516	5EC	82.40	0.01	**E5**	659.26	189	BD	657.89	0.21
F2	87.31	1431	597	87.29	0.02	**F5**	698.46	178	B2	698.32	0.02
#F2	92.50	1350	546	92.52	-0.03	**#F5**	739.97	168	A8	739.64	0.04
G2	98.00	1275	4FB	97.96	0.04	**G5**	783.99	158	9E	786.16	-0.28
#G2	103.82	1203	4B3	103.82	0.00	**#G5**	830.59	149	95	833.33	-0.33
A2	110.00	1135	46F	110.04	-0.03	**A5**	880.00	141	8D	880.28	-0.03
#A2	116.54	1072	430	116.50	0.04	**#A5**	932.31	133	85	932.84	-0.06
B2	123.47	1011	3F3	123.52	-0.04	**B5**	987.77	126	7E	984.25	0.36
C3	130.81	955	3BB	130.75	0.04	**C6**	1046.48	118	76	1050.42	-0.38
#C3	138.59	901	385	138.58	0.01	**#C6**	1108.71	112	70	1106.19	0.23
D3	146.83	850	352	146.89	-0.04	**D6**	1174.63	105	69	1179.25	-0.39
#D3	155.56	803	323	155.47	0.06	**#D6**	1244.48	99	63	1250.00	-0.44
E3	164.81	757	2F5	164.91	-0.06	**E6**	1318.48	94	5E	1315.79	0.20
F3	174.61	715	2CB	174.58	0.02	**F6**	1396.88	88	58	1404.49	-0.55
#F3	184.99	675	2A3	184.91	0.04	**#F6**	1479.95	83	53	1488.10	-0.55
G3	196.00	637	27D	195.92	0.04	**G6**	1567.95	79	4F	1562.50	0.35
#G3	207.65	601	259	207.64	0.00	**#G6**	1661.18	74	4A	1666.67	-0.33
A3	220.00	567	237	220.07	-0.03	**A6**	1759.96	70	46	1760.56	-0.03
#A3	233.08	535	217	233.21	-0.06	**#A6**	1864.62	66	42	1865.67	-0.06
B3	246.94	505	1F9	247.04	-0.04	**B6**	1975.49	62	3E	1984.13	-0.44
C4	261.63	477	1DD	261.51	0.05	**C7**	2092.96	59	3B	2083.33	0.46
#C4	277.18	450	1C2	277.16	0.01	**#C7**	2217.41	55	37	2232.14	-0.66
D4	293.66	425	1A9	293.43	0.08	**D7**	2349.27	52	34	2358.49	-0.39
#D4	311.12	401	191	310.95	0.06	**#D7**	2488.96	49	31	2500.00	-0.44
E4	329.63	378	17A	329.82	-0.06	**E7**	2636.96	46	2E	2659.57	-0.86
F4	349.23	357	165	349.16	0.02	**F7**	2793.77	44	2C	2777.78	0.57
#F4	369.99	337	151	369.82	0.05	**#F7**	2959.89	41	29	2976.19	-0.55
G4	392.00	318	13E	391.85	0.04	**G7**	3135.90	39	27	3125.00	0.35
#G4	415.30	300	12C	415.28	0.00	**#G7**	3322.37	37	25	3289.47	0.99
A4	440.00	283	11B	440.14	-0.03	**A7**	3519.93	35	23	3472.22	1.36
#A4	466.15	267	10B	466.42	-0.06	**#A7**	3729.23	33	21	3676.47	1.41
B4	493.88	252	FC	494.07	-0.04	**B7**	3950.98	31	1F	3906.25	1.13

DTMF Generator Tone Register: (under OSCX = 4MHz.)

	Channel 2 Prescaler	$033	$02E	$029	$025
Channel 1 Prescaler	COL ROW	1209Hz	1336Hz	1477Hz	1633Hz
$059	697Hz	1	2	3	A
$050	770Hz	4	5	6	B
$048	852Hz	7	8	9	C
$041	941Hz	#	0	*	D

Electrical Characteristics

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -10℃ to +60℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, fosc = 32.768kHz, foscx is not used, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.4	3.0	5.5	V	
Operating Current	I_{OP}	-	10	20	μA	All output pads unload execute NOP instruction excluding LCD bias current and FSK recevier
Standby Current	I_{SB1}	-	2	4	μA	All output pads unload (HALT mode) excluding LCD bias current and FSK recevier
Standby Current	I_{SB2}	-	-	1	μA	All output pads unload (STOP mode), LCD off and excluding FSK recevier
Input High Voltage	V_{IH}	0.7 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	-0.3	-	0.3 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Input High Voltage	V_{IH}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$ (Schmitt trigger input)
Input Low Voltage	V_{IL}	-0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$ (Schmitt trigger input)
Pull -high Resistance	R_{OH}	-	200	-	kΩ	PORTA - D (I_{OH} = 10μA)
Output High Voltage	V_{OH1}	0.7 X V_{DD}	-	-	V	PORTA - D (I_{OH} = 2mA)
Output Low Voltage	V_{OL1}	-	-	0.8	V	PORTA - D (I_{OL} = -2mA)
Output High Voltage	V_{OH2}	V_{DD} - 0.6	-	-	V	SEG13 - 24 to be output port, I_{OH} = 1mA
Output Low Voltage	V_{OL2}	-	-	0.8	V	SEG13 - 24 to be output port, I_{OL} = -1mA
LCD Voltage Divider Resistor	R_{LCD}	-	235	-	kΩ	
LCD Driving on resistor	R_{ON}	-	5	-	kΩ	LCD COM1 - 8, LCD SEG1 - 32, the voltage variation of V1, V2, V3, V4 is less than 0.2V.

HLM vs. I_{OP}, I_{SB1} and I_{SB2}
If HLM = 1, I_{OPX} = I_{OP} X 2, I_{SB2X} = I_{SB2} X 2.

DC Electrical Characteristics (Continued)

(V_{DD} = 5.0V, GND = 0V, T_A = 25℃, f_{OSC} = 32.768kHz, f_{OSCX} is not used, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.4	5.0	5.5	V	
Operating Current	I_{OP}	-	20	40	μA	All output pads unload execute NOP instruction excluding LCD bias current and FSK recevier
Standby Current	I_{SB1}	-	5	10	μA	All output pads unload (HALT mode) excluding LCD bias current and FSK recevier
Standby Current	I_{SB2}	-	-	1	μA	All output pads unload (STOP mode), LCD off and excluding FSK recevier
Input High Voltage	V_{IH}	0.7 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	-0.3	-	0.3 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Input High Voltage	V_{IH}	0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$ (Schmitt trigger input)
Input Low Voltage	V_{IL}	-0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$ (Schmitt trigger input)
Pull-high Resistance	R_{OH}	-	200	-	kΩ	PORTA - D (I_{OH} = 10μA)
Output High Voltage	V_{OH1}	0.7 X V_{DD}	-	-	V	PORTA - D (I_{OH} = 3mA)
Output Low Voltage	V_{OL1}	-	-	0.8	V	PORTA - D (I_{OL} = -3mA)
Output High Voltage	V_{OH2}	V_{DD} - 0.6	-	-	V	SEG13 - 24 to be output port, I_{OH} = 1mA
Output Low Voltage	V_{OL2}	-	-	0.8	V	SEG13 - 24 to be output port, I_{OL} = -1mA
LCD Voltage Divider Resistor	R_{LCD}	-	235	-	kΩ	
LCD Driving on resistor	R_{ON}	-	5	-	kΩ	LCD COM1 - 8, LCD SEG1 - 32, the voltage variation of V1, V2, V3, V4 is less than 0.2V.

HLM vs. I_{OP}, I_{SB1} and I_{SB2}
If HLM = 1, I_{OPX} = I_{OP} X 2, I_{SB2X} = I_{SB2} X 2.

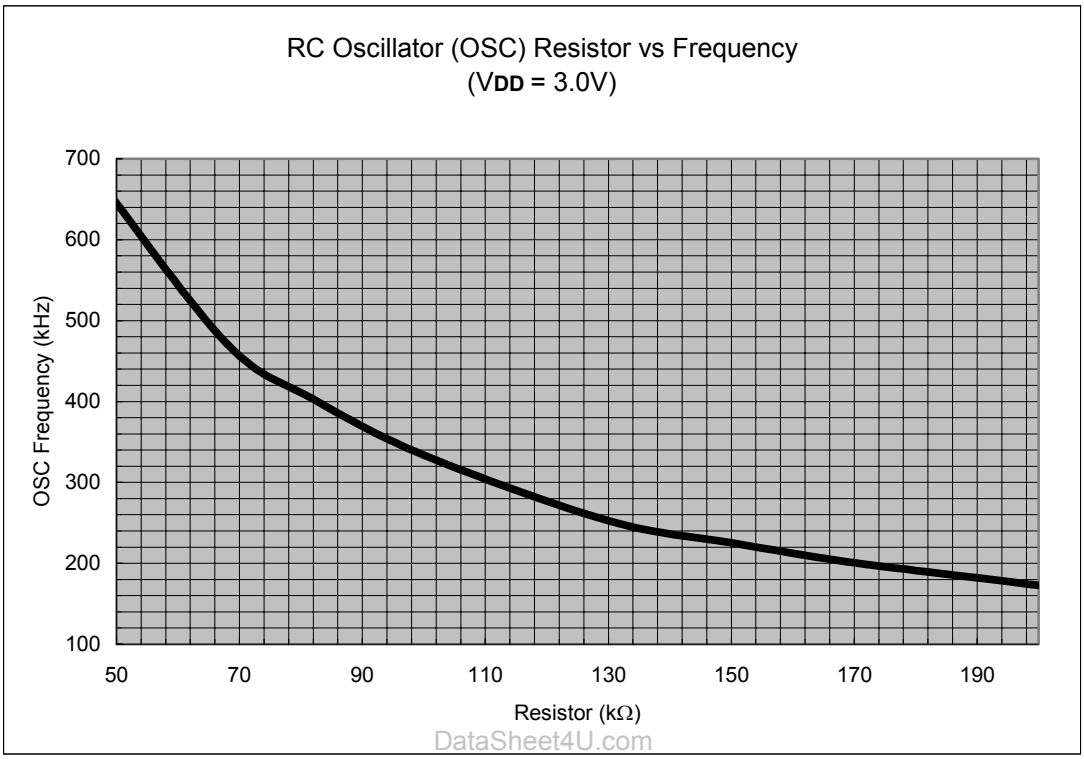
AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, f_{OSC} = 32.768kHz, unless otherwise specified)

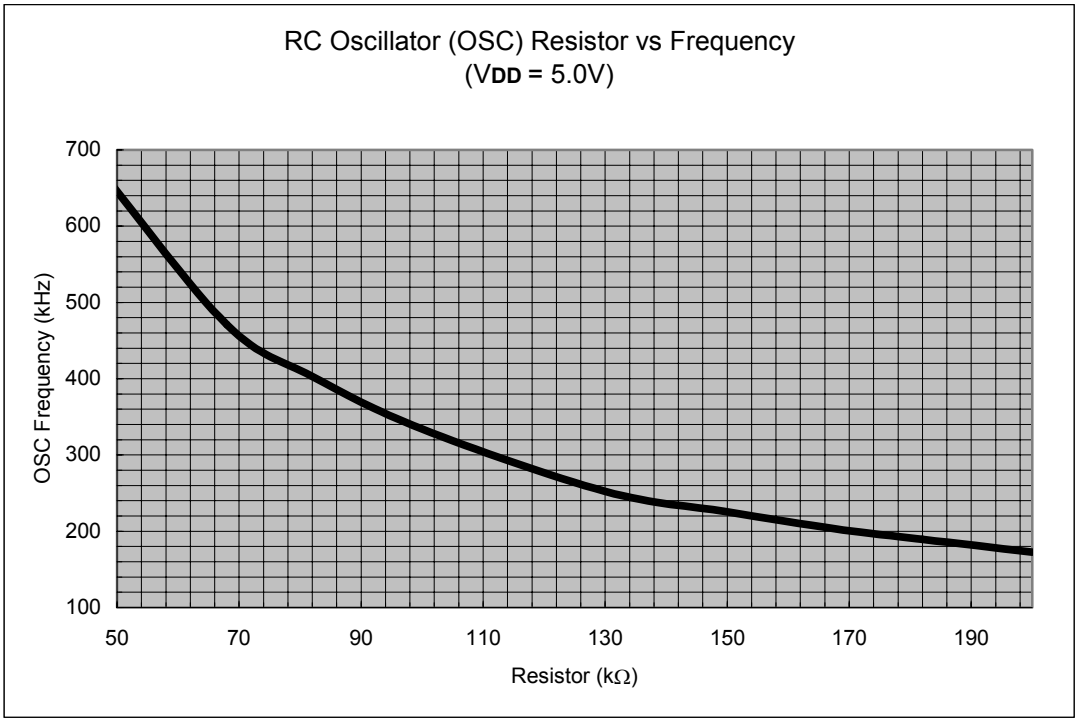
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	1	2	s	32.768kHz Crystal Oscillator
Frequency Stability	|Δf|/f	-	-	1	PPM	[f (3.0) - f (2.5)] /f (3.0), 32.768kHz Crystal Oscillator

AC Characteristics (V_{DD} = 5.0V, GND = 0V, T_A = 25℃, f_{OSC} = 32.768kHz, unless otherwise specified)

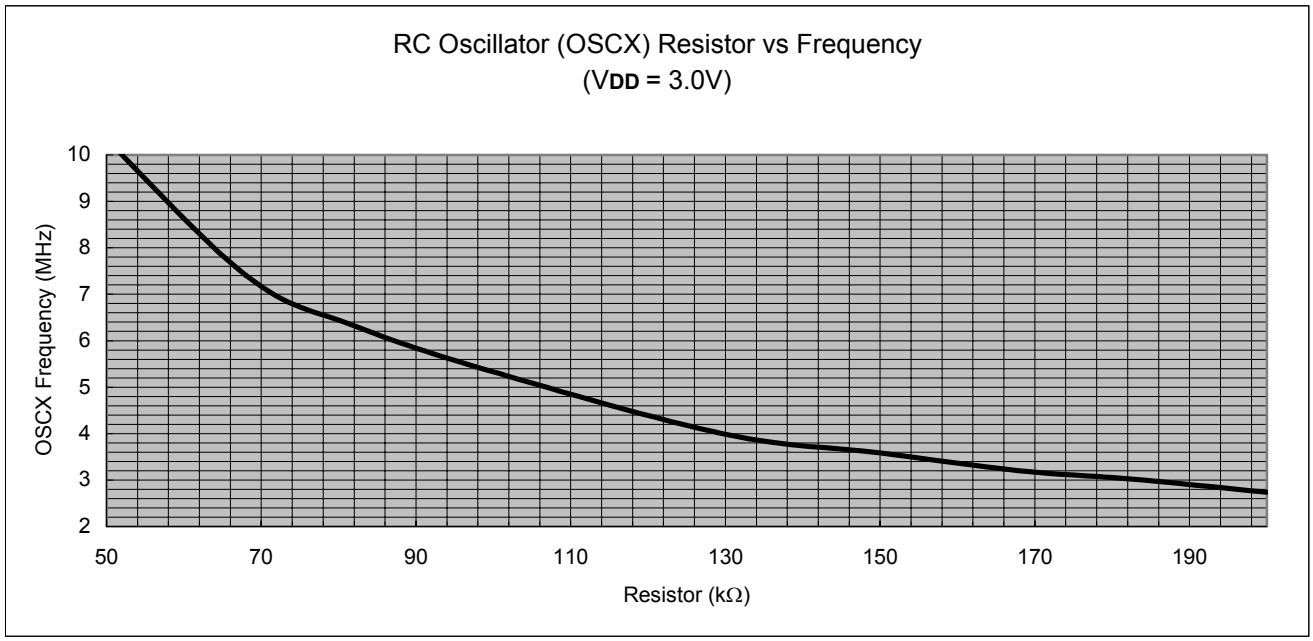
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	1	2	s	32.768kHz Crystal Oscillator
Frequency Stability	|Δf|/f	-	-	1	PPM	[f (5.0) - f (4.5)] /f (5.0), 32.768kHz Crystal Oscillator

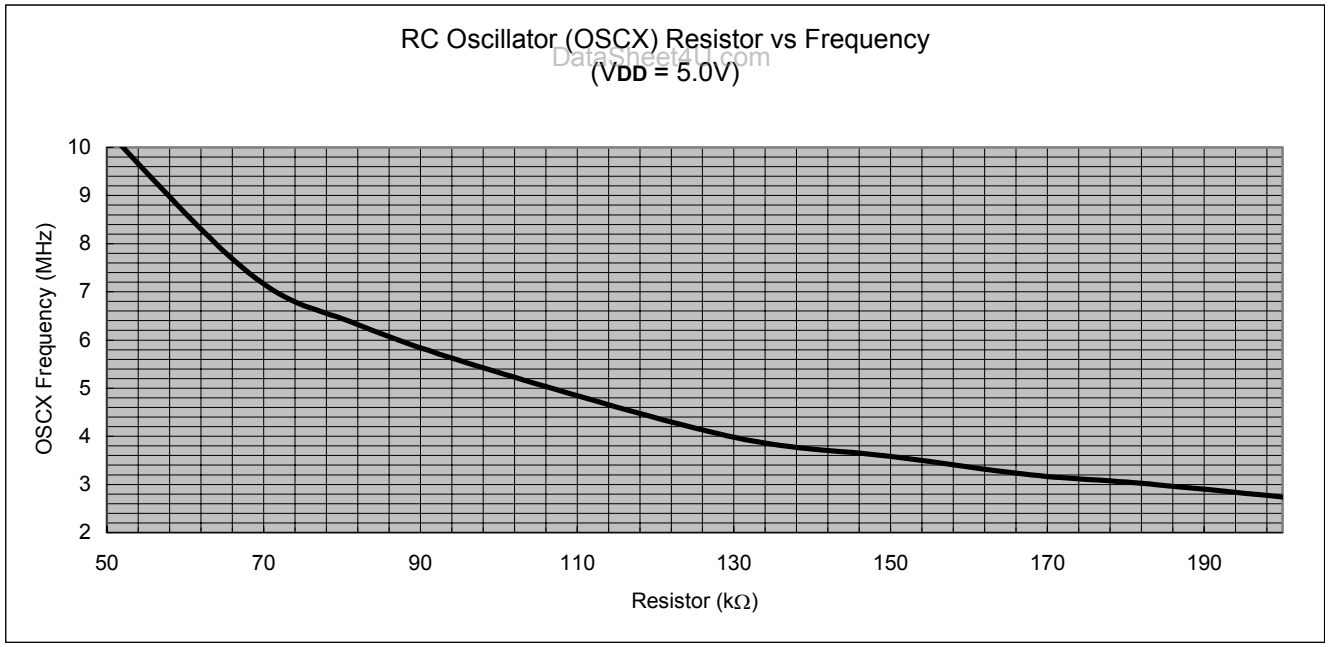
RC Oscillator Characteristics Graphs (for reference only)



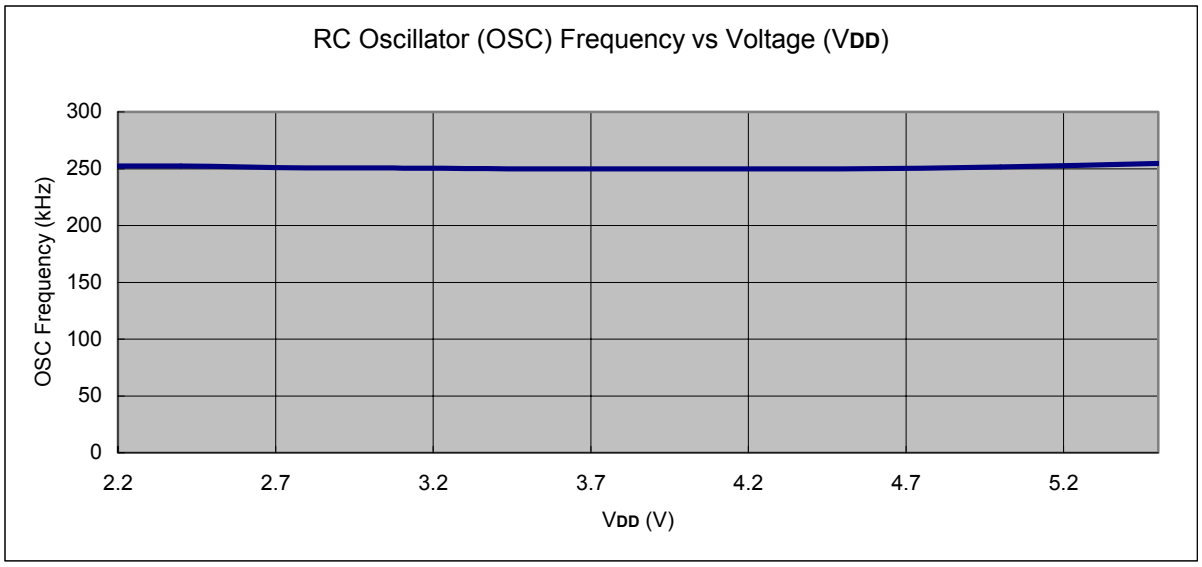


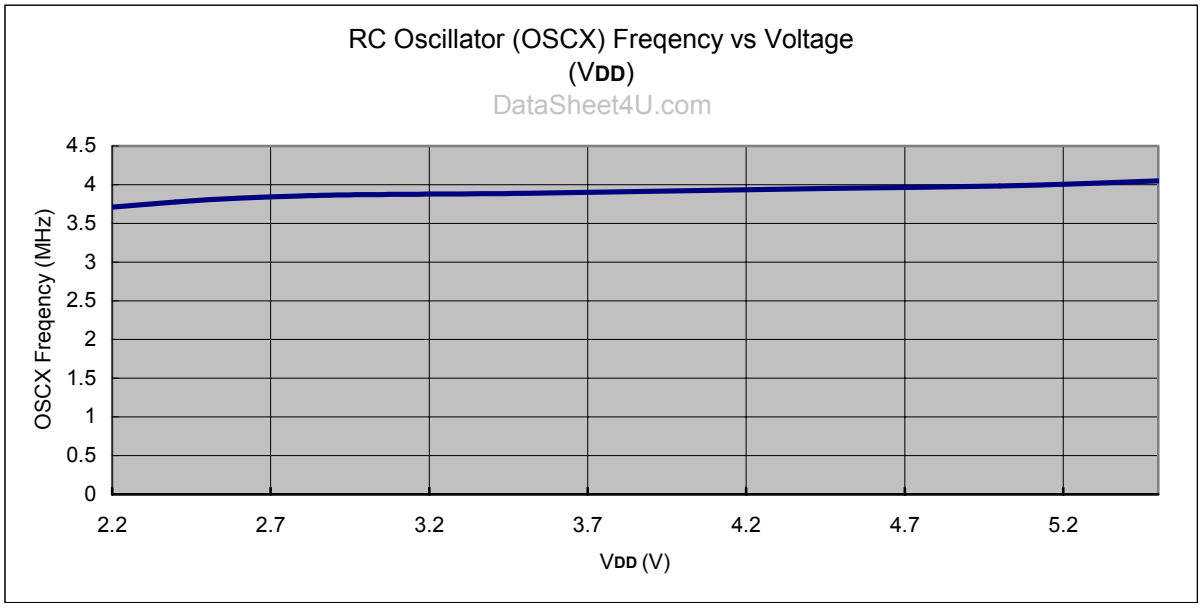
RC Oscillator Characteristics Graphs (Continued)



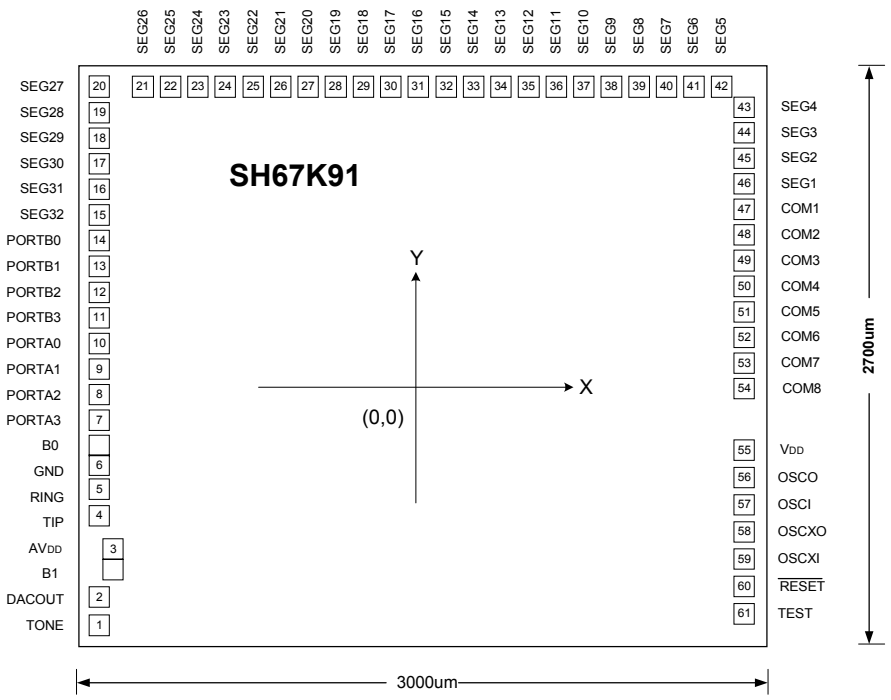


RC Oscillator Characteristics Graphs (Continued)





Bonding Diagram



Pad Location

unit:μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	TONE	-1365	-1208	20	SEG27	-1365	1207.5
2	DACOUT	-1365	-1078	21	SEG26	-1187	1207.5
Bonding Option	B1	-1299	-946.5	22	SEG25	-1057	1207.5
3	AVDD	-1299	-850	23	SEG24	-927	1207.5
4	TIP	-1365	-711.5	24	SEG23	-807	1207.5
5	RING	-1365	-596.5	25	SEG22	-697	1207.5
6	GND	-1365	-486.5	26	SEG21	-587	1207.5
Bonding Option	B0	-1365	-389.5	27	SEG20	-477	1207.5
7	PORTA3	-1365	-282.5	28	SEG19	-367	1207.5
8	PORTA2	-1365	-172.5	29	SEG18	-257	1207.5
9	PORTA1	-1365	-62.5	30	SEG17	-147	1207.5
10	PORTA0	-1365	47.5	31	SEG16	-37	1207.5
11	PORTB3	-1365	157.5	32	SEG15	73	1207.5
12	PORTB2	-1365	267.5	33	SEG14	183	1207.5
13	PORTB1	-1365	377.5	34	SEG13	293	1207.5
14	PORTB0	-1365	487.5	35	SEG12	403	1207.5
15	SEG32	-1365	597.5	36	SEG11	513	1207.5
16	SEG31	-1365	707.5	37	SEG10	623	1207.5
17	SEG30	-1365	827.5	38	SEG9	733	1207.5
18	SEG29	-1365	947.5	39	SEG8	843	1207.5
19	SEG28	-1365	1077.5	40	SEG7	963	1207.5

Pad Location (Continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
41	SEG6	1093	1207.5	52	COM6	1365	66
42	SEG5	1223	1207.5	53	COM7	1365	-44
43	SEG4	1365	1116	54	COM8	1365	-154
44	SEG3	1365	986	55	V_{DD}	1365	-374
45	SEG2	1365	856	56	OSCO	1365	-484
46	SEG1	1365	736	57	OSCI	1365	-594
47	COM1	1365	616	58	OSCXO	1365	-714
48	COM2	1365	506	59	OSCXI	1365	-834
49	COM3	1365	396	60	$\overline{RESET}$	1365	-964
50	COM4	1365	286	61	TEST	1365	-1094
51	COM5	1365	176				

Ordering Information

Part No.	Package	Packing
SH67K91-yyxxx/061HR	CHIP	TRAY

Note:

(1) "-yyxxx": "yy" means 2 bits option and "xxx" means 3 bits code seriary number. If the product is OTP type and in blank order, those bits should be none.

(2) The data after mark "/" in Part No. block is the package and packing information for ordering.

(3) Any other package or packing request, please refer to following table.

Package		Packing	
D	DIP	**R**	Normal package size and in tray packing
F	QFP	**U**	Normal package size and in tube packing
H	CHIP	**A**	Normal package size and in tape & reel packing
J	CER-DIP	**D**	Larger package size and in tray packing
K	SKINNY	**L**	Larger package size and in tube packing
L	PLCC	**B**	Larger package size and in tape & reel packing
M	SOP	**T**	Smaller package size and in tray packing
N	OTHER	**S**	Smaller package size and in tube packing
Q	GOOD DIE ON WAFER	**N**	Smaller package size and in tape & reel packing
S	SOJ		
T	TO92		
V	VSOP/TSOP		
W	WAFER		
X	TSSOP		

Data Sheet Revision History

The following table shows the revision history for this document

Revision No.	History	Date
1.0	Original	Nov. 2004