SH67L17

24K 4-bit Micro-controller with LCD Driver

Features

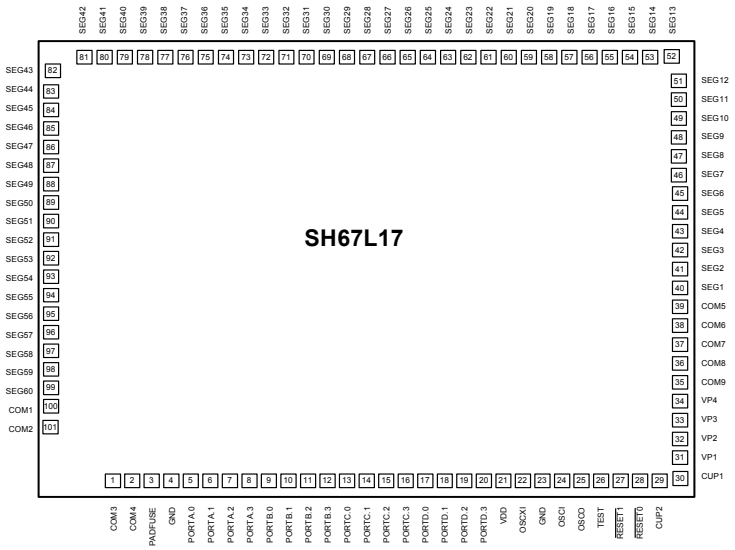
- SH6610D-based single-chip 4-bit micro-controller with LCD driver
- ROM: 24K X 16bits
- RAM: 4136 X 4 bits
  - 43 System Control Register
  - 4093 Data memory
  - 180 LCD RAM
- Operation Voltage: 1.2V - 1.7V (Typical 1.5V)
- 16 CMOS Bi-directional I/O Pins
- 8-Level Stack (Including Interrupts)
- One 8-bit Base Timer
- Warm-Up Timer
- Powerful Interrupt Sources:
  - External interrupt ($\overline{INT}$ share with PORTA.0)
  - Base timers interrupt
  - PORTB & PORTC interrupts (Falling edge)
- 2 Clock Sources
  OSC: (Code Option selects the type of OSC)
  - Crystal Oscillator: 32.768kHz
  - RC Oscillator: 131kHz

  OSCX:
  - RC oscillator: 500kHz (Roscx)
- Instruction Cycle Time (4/fosc)
- Two Low Power Operation Modes: HALT And STOP
- Special HALT/STOP mode
- Reset
  - Built-in Watchdog Timer (WDT) (Code Option)
  - Built-in Power-on Reset (POR)
  - $\overline{RESET\ 0}$ & $\overline{RESET\ 1}$
- LCD Driver:
  - 60SEG X 9COM (1/9 Duty, 1/4 Bias)
- Built-in Pull-high Resistor For PORTA - PORTD
- Built-in Voltage Fourfold Charge Pump Circuit
- 8 X 8 BCD hardware multiplier
- 16/8 BCD hardware divider
- RAM common space in every RAM bank
- Low power consumption
- Available in CHIP FORM

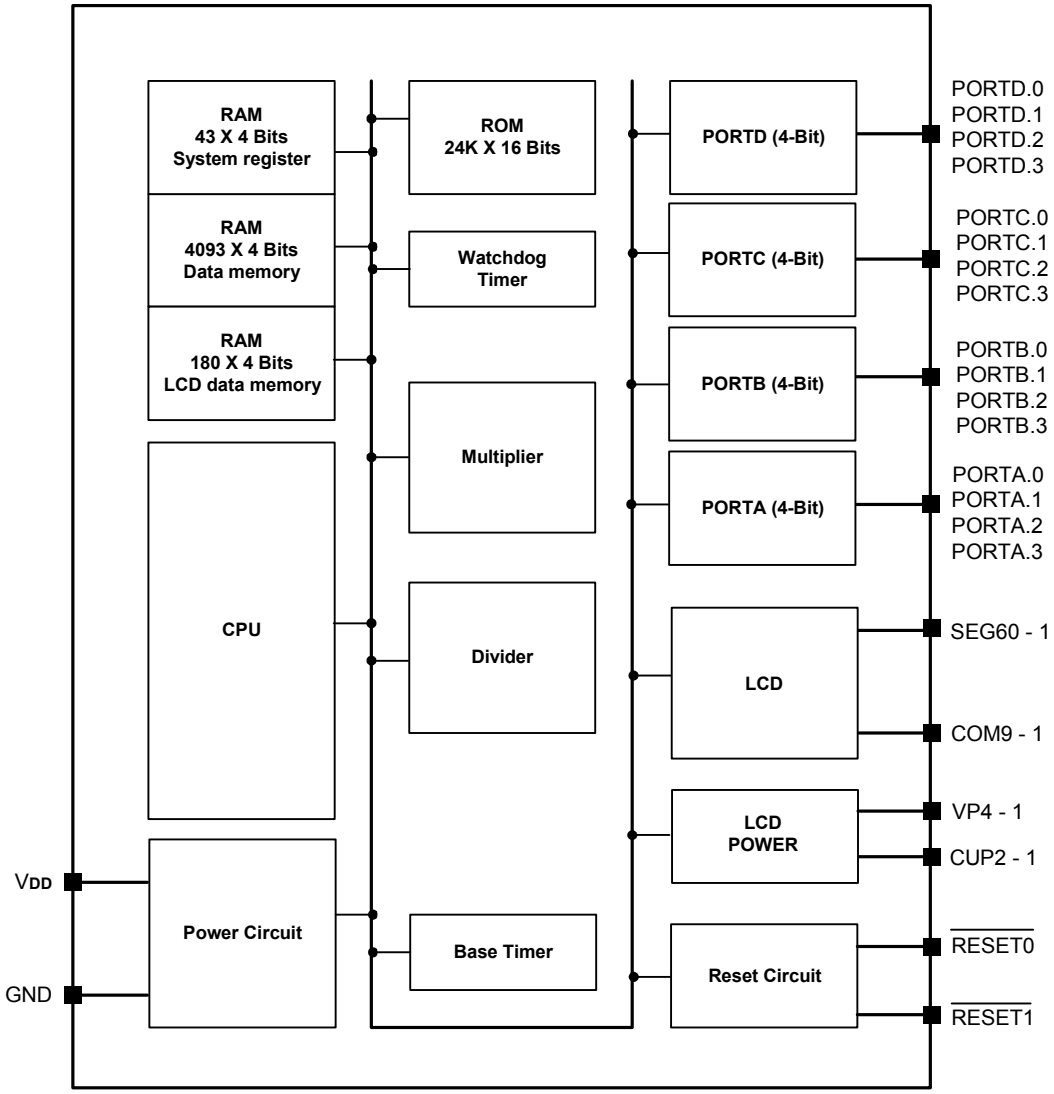
General Description

SH67L17 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, RAM, ROM, Base Timer, a hardware multiplier, a hardware divider, LCD driver, I/O ports, and voltage pump circuit. The SH67L17 is suitable for scientific calculator application.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Pad Name	I/O	Description
40 - 99	SEG1 - SEG60	O	Segment signal output for LCD display
100, 101, 1 - 2, 39 - 35	COM1 - COM9	O	Common signal output for LCD display
34 - 31	VP4 - VP1	P	Power supply pin for LCD driver
29 - 30	CUP2 - CUP1	P	Connection for voltage treble capacitor
26	TEST	I	Test pin internally pull-low (No connection for user)
3	PADFUSE	I	External pull-low
27	$\overline{\text{RESET1}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
28	$\overline{\text{RESET0}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
21	V_{DD}	P	Power supply pin
23	GND	P	Ground pin
4	GND	P	Ground pin
24	OSCI	I	OSC input pin, connected to a crystal or external resistor
25	OSCO	O	OSC output pin. No output in RC mode
22	OSCXI	I	OSCX input pin. Connected to a external resistor
5 - 8	PORTA.3 - 0	I/O	Bit programmable I/O, PORTA.0 could be external interrupt input ($\overline{\text{INT}}$)
9 - 12	PORTB.3 - 0	I/O	Bit programmable I/O Vector interrupt (Active falling edge)
13 - 16	PORTC.3 - 0	I/O	Bit programmable I/O Vector interrupt (Active falling edge)
17 - 20	PORTD.3 - 0	I/O	Bit programmable I/O

Which, I: input; O: output; P: Power; Z: High impedance

Functional Description

1. CPU

The CPU contains the following functional blocks:

Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code Bit7-Bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H-3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9 - Bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $01F, $3C0 - $3CA
Data memory: $020 - $2FF, $3CB - $3FF, $460 - $7FF, $860 - $BFF, $C60 - $FFF & $1060 - $1267
LCD RAM space: $300 - $33B, $330 - $37B, $380 - $3BB
RAM Bank space: $020 - $3FF (share address)
RAM common area space: $000 - $05F

RAM bank table: (RAMB: System Register $13 Bit2, 1, 0)

Bank0 RAMB = 000 B = 0	Bank1 RAMB = 000 B = 1	Bank2 RAMB = 000 B = 2	Bank3 RAMB = 000 B = 3	Bank4 RAMB = 000 B = 4	Bank5 RAMB = 000 B = 5	Bank 6 RAMB = 000 B = 6	Bank7 RAMB = 000 B = 7
$060 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3FF
Bank8 RAMB = 001 B = 0	Bank9 RAMB = 001 B = 1	Bank10 RAMB = 001 B = 2	Bank11 RAMB = 001 B = 3	Bank12 RAMB = 001 B = 4	Bank13 RAMB = 001 B = 5	Bank14 RAMB = 001 B = 6	Bank15 RAMB = 001 B = 7
$460 - $47F	$480 - $4FF	$500 - $57F	$580 - $5FF	$600 - $67F	$680 - $6FF	$700 - $77F	$780 - $7FF
Bank16 RAMB = 010 B = 0	Bank17 RAMB = 010 B = 1	Bank18 RAMB = 010 B = 2	Bank19 RAMB = 010 B = 3	Bank20 RAMB = 010 B = 4	Bank21 RAMB = 010 B = 5	Bank22 RAMB = 010 B = 6	Bank23 RAMB = 010 B = 7
$860 - $87F	$880 - $8FF	$900 - $97F	$980 - $9FF	$A00 - $A7F	$A80 - $AFF	$B00 - $B7F	$B80 - $BFF
Bank24 RAMB = 011 B = 0	Bank25 RAMB = 011 B = 1	Bank26 RAMB = 011 B = 2	Bank17 RAMB = 011 B = 3	Bank28 RAMB = 011 B = 4	Bank29 RAMB = 011 B = 5	Bank30 RAMB = 011 B = 6	Bank31 RAMB = 011 B = 7
$C60 - $C7F	$C80 - $CFF	$D00 - $D7F	$D80 - $DFF	$E00 - $E7F	$E80 - $EFF	$F00 - $F7F	$F80 - $FFF
Bank32 RAMB = 100 B = 0	Bank33 RAMB = 100 B = 1	Bank34 RAMB = 100 B = 2	Bank35 RAMB = 100 B = 3	Bank36 RAMB = 100 B = 4			
$1060 - $107F	$1080 - $10FF	$1100 - $117F	$1180 - $11FF	$1200 - $1267			

Where, B: RAM bank bit use in instructions

2.2. Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	-	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	-	IRQBT	IRQP	R/W	Interrupt request flags register
$02	-	-	GO/DONE	M/D	R/W	Bit0: Multiplier/Divider mode control register Bit1: Multiplier/Divider status flag register
$03	RST	BTM.2	BTM.1	BTM.0	R/W R	Bit2-0: Base timer mode register Bit3: $\overline{\text{RESET 0}}$ / $\overline{\text{RESET 1}}$ causes system reset control register
$04	MLTL.3	MLTL.2	MLTL.1	MLTL.0	R/W	Multiplicator low nibble/Dividend low nibble register
$05	MLTH.3	MLTH.2	MLTH.1	MLTH.0	R/W	Multiplicator high nibble/Dividend middle0 nibble register
$06	MLDL.3	MLDL.2	MLDL.1	MLDL.0	R/W	Multiplicand low nibble/Dividend middle1 nibble register
$07	MLDH.3	MLDH.2	MLDH.1	MLDH.0	R/W	Multiplicand high nibble/Dividend high nibble register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	DIVL.3	DIVL.2	DIVL.1	DIVL.0	R/W	Divisor low nibble register
$0D	DIVH.3	DIVH.2	DIVH.1	DIVH.0	R/W	Divisor high nibble register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register

Configuration of System Register (continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	-	RAMB.2	RAMB.1	RAMB.0	R/W	Bit2-0: RAM Bank register
$14	PULLEN	LCD ON	PUMP ON	-	R/W	Bit1: LCD Pump ON/OFF control register Bit2: LCD display ON/OFF control register Bit3: Port pull-high control register
$15	QLN.3	QLN.2	QLN.1	QLN.0	R/W	Quotient low nibble register
$16	QMZ.3	QMZ.2	QMZ.1	QMZ.0	R/W	Quotient middle0 nibble register
$17	QMO.3	QMO.2	QMO.1	QMO.0	R/W	Quotient middle1 nibble register
$18	QHN.3	QHN.2	QHN.1	QHN.0	R/W	Quotient high nibble register
$19	PLN.3	PLN.2	PLN.1	PLN.0	R/W	Product low nibble/Residue low nibble register
$1A	PMZ.3	PMZ.2	PMZ.1	PMZ.0	R/W	Product middle0 nibble/Residue high nibble register
$1B	PMO.3	PMO.2	PMO.1	PMO.0	R/W	Product middle1 nibble register
$1C	PHN.3	PHN.2	PHN.1	PHN.0	R/W	Product high nibble register
$1D	SPDUP	-	OXM	OXON	R/W	Bit0: OSCX oscillation on/off control register Bit1: system clock select register Bit3: Speed up the 32.768kHz Crystal Oscillator in the CPU turn-on status control register
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
$1F	BNK.3	BNK.2	BNK.1	BNK.0	R/W	ROM Bank register
$3C0	RELL.3	RELL.2	RELL.1	RELL.0	R/W	Special STOP mode OSC control Low nibble register
$3C1	RELM.3	RELM.2	RELM.1	RELM.0	R/W	Special STOP mode OSC control Middle nibble register
$3C2	RELH.3	RELH.2	RELH.1	RELH.0	R/W	Special STOP mode OSC control High nibble register
$3C3	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$3C4	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$3C5	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$3C6	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$3C7	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$3C8	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$3C9	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$3CA	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

3. ROM

The ROM can address 24576 X 16 bits of program area from $0000 to $5FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to External interrupt service routine
$002	JMP*	Reserved
$003	JMP*	Jump to Base Timer interrupt service routine
$004	JMP*	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

3.2. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU address space maps to one of the eleven banks (BNK.3 - 0 = $00 - $0F) of the upper 22K of ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space							
	BNK = $00	BNK = $01	BNK = $02	BNK = $03	BNK = $04	BNK = $05	BNK = $06	BNK = $07
Lower 2K Address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
Upper 2K Address	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)	2000 - 27FF (BANK 4)	2800 - 2FFF (BANK 5)	3000 - 37FF (BANK 6)	3800 - 3FFF (BANK 7)	4000 - 47FF (BANK 8)

CPU Address	ROM Space							
	BNK = $08	BNK = $09	BNK = $0A	-	-	-	-	-
Lower 2K Address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	-	-	-	-	-
Upper 2K Address	4800 - 4FFF (BANK 9)	5000 - 57FF (BANK 10)	5800 - 5FFF (BANK 11)	-	-	-	-	-

4 Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on reset	Reset0 Pin Reset	Reset1 Pin Reset	WDT Reset
$00	IEX	-	IEBT	IEP	0-00	0-00	0-00	0-00
$01	IRQX	-	IRQBT	IRQP	0-00	0-00	0-00	0-00
$02	-	-	GO/DONE	M/D	0-00	0-00	0-00	0-00
$03	RST	BTM.2	BTM.1	BTM.0	0000	0000	1000	uuuu
$04	MLTL.3	MLTL.2	MLTL.1	MLTL.0	0000	0000	0000	0000
$05	MLTH.3	MLTH.2	MLTH.1	MLTH.0	0000	0000	0000	0000
$06	MLDL.3	MLDL.2	MLDL.1	MLDL.0	0000	0000	0000	0000
$07	MLDH.3	MLDH.2	MLDH.1	MLDH.0	0000	0000	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000	0000	0000
$0C	DIVL3	DIVL2	DIVL1	DIVL0	0000	0000	0000	0000
$0D	DIVH3	DIVH2	DIVH1	DIVH0	0000	0000	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu	uuuu	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu	uuuu	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu	uuuu	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu	-uuu	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu	-uuu	-uuu
$13	-	RAMB2	RAMB1	RAMB0	-000	-000	-000	-000
$14	PULLEN	LCD ON	PUMP ON	-	000-	000-	000-	000-
$15	QLN.3	QLN.2	QLN.1	QLN.0	0000	0000	0000	0000
$16	QMZ.3	QMZ.2	QMZ.1	QMZ.0	0000	0000	0000	0000
$17	QMO.3	QMO.2	QMO.1	QMO.0	0000	0000	0000	0000
$18	QHN.3	QHN.2	QHN.1	QHN.0	0000	0000	0000	0000
$19	PLN.3	PLN.2	PLN.1	PLN.0	0000	0000	0000	0000
$1A	PMZ.3	PMZ.2	PMZ.1	PMZ.0	0000	0000	0000	0000
$1B	PMO.3	PMO.2	PMO.1	PMO.0	0000	0000	0000	0000
$1C	PHN.3	PHN.2	PHN.1	PHN.0	0000	0000	0000	0000
$1D	SPDUP	-	OXM	OXON	1-00	1-00	1-00	u-00
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	0000	0000	1000
$1F	BNK.3	BNK.2	BNK.1	BNK.0	0000	0000	0000	0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

System Register State (continued):

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on reset	Reset0 Pin Reset	Reset1 Pin Reset	WDT Reset
$3C0	RELL.3	RELL.2	RELL.1	RELL.0	0000	0000	0000	0000
$3C1	RELM.3	RELM.2	RELM.1	RELM.0	0000	0000	0000	0000
$3C2	RELH.3	RELH.2	RELH.1	RELH.0	0000	0000	0000	0000
$3C3	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000	0000	0000
$3C4	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000	0000	0000
$3C5	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000	0000	0000
$3C6	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000	0000	0000
$3C7	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	xxxx	xxxx	xxxx
$3C8	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	xxxx	xxxx	xxxx
$3C9	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	xxxx	xxxx	xxxx
$3CA	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	xxxx	xxxx	xxxx

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock = fosc/4

5.1. Instruction Cycle Time:

(1) 4/32.768kHz (≈ 122.07μs) for 32.768kHz oscillator.
(2) 4/131kHz (≈ 30.53μs) for 131kHz RC oscillator.
(3) 4/500kHz (= 8μs) for 500kHz RC oscillator.

5.2. Circuit Configuration

SH67L17 has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ. 32.768kHz) or RC (Typ. 131kHz) determined by the code option. This is designed for low frequency operation. OSCX has one type: RC (500kHz). It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC clock is automatically selected as the system clock input source.

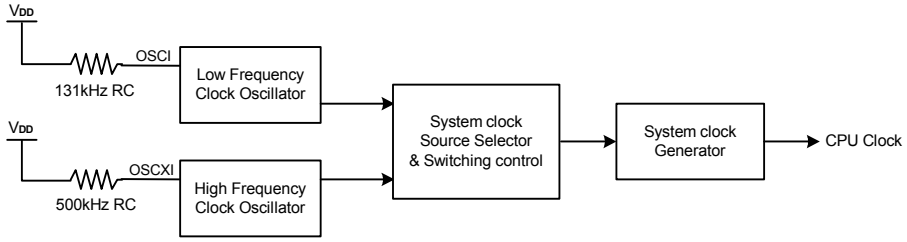


Figure 1. Oscillator Block Diagram

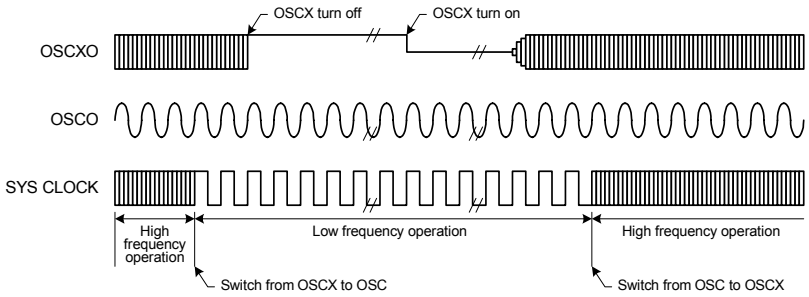
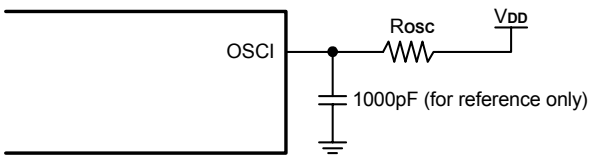


Figure 2. Timing of System Clock Switching

5.3. OSC Oscillator

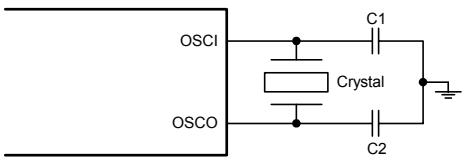
The OSC generates the basic clock pulses that provide the CPU and peripherals (Base timer, LCD) with an operating clock.

(1) OSC RC oscillator



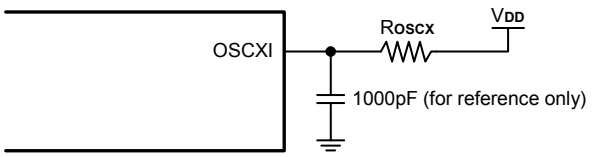
External Rosc RC

(2) OSC Crystal oscillator



5.4. OSCX Oscillator

OSCX RC oscillator



External Roscx RC

5.5. Control of Oscillator

The oscillator control register configuration is shown as follows.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1D	SPDUP	-	OXM	OXON	R/W	Bit0: OSCX oscillation on/off control register Bit1: system clock select register Bit3: Speed up the 32.768kHz Crystal Oscillator in the CPU turn-on status control register
	X	-	X	0		Turn off OSCX oscillation
	X	-	X	1		Turn on OSCX oscillation
	X	-	0	X		Select OSC as system clock
	X	-	1	X		Select OSCX as system clock
	0	-	X	X		Turn off the Speed-up function
	1	-	X	X		Turn on the Speed-up function

It is recommended to turn off the" Speed up the 32.768kHz Crystal Oscillator in the CPU turn-on status" function when 32.768kHz Crystal is stable.

When OXON is clear to "0", OXM will be clear to "0" by hardware.

Programming Notes:

It takes at least 5ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When the CPU system clock switching from OSC to OSCX, the user has to wait at least 5ms till the OSCX oscillation is activated. In addition, the start time varies a lot with respect to oscillator characteristics and operational conditions. Therefore the waiting time depends on applications. When switching from OSCX to OSC, and turning off OSCX in one instruction, the OSCX turns off control would be delayed for one instruction cycle automatically to prevent CPU operation error.

5.6. Capacitor Selection for Oscillator

*- The specified ceramic resonator has internal built-in load capacity

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS
			φ 3x8 - 32.768KHz	Vectron International

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures

6. I/O Port

The MCU provides 16 bi-directional I/O ports. The PORT data is put in register $08 - $0B. The PORT control register $3C3 - $3C6 controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PULLEN of $14 and the data of the port, when the PORT is used as input.

Port I/O mapping address is shown as follows:

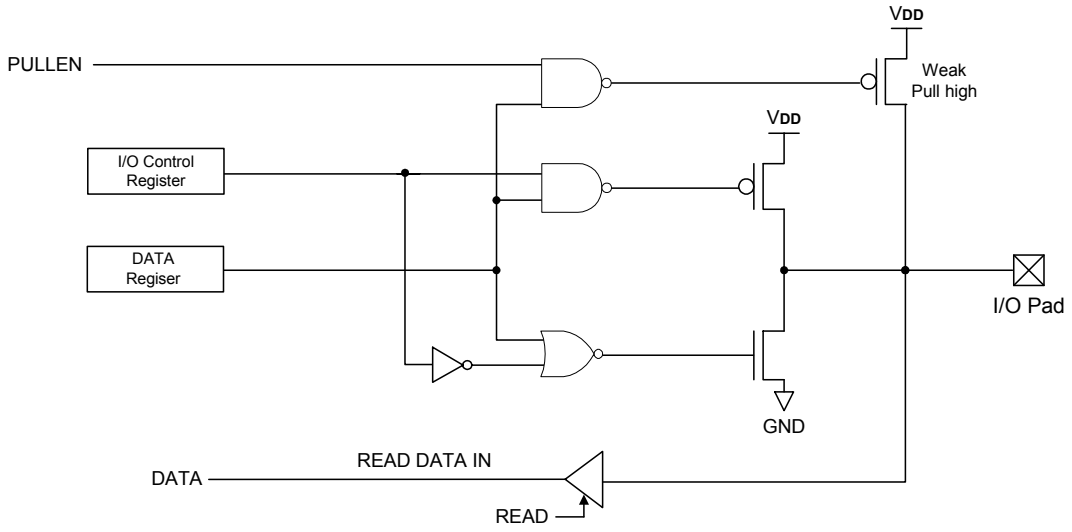
Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$3C3	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$3C4	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$3C5	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$3C6	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register

PA (/B/C/D) CR.n, (n = 0, 1, 2, 3)

0: Set I/O as an input direction. (Power on initial)

1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin.



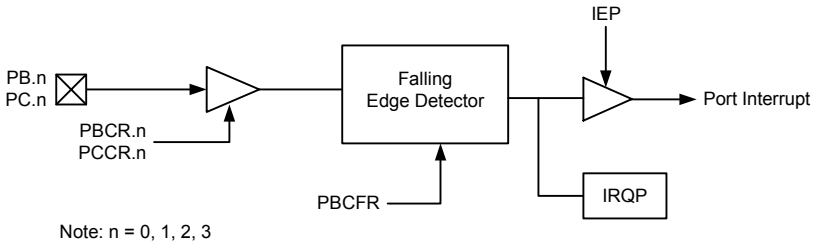
System Register $14

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$14	PULLEN				R/W	Bit3: Port Pull-high control register
	0	X	X	X	R/W	Port Pull-high resistor disable
	1	X	X	X	R/W	Port Pull-high resistor enable

To turn on the pull-high resistor, user must set PULLEN to “1”, and write “1” to the port data register when the port is input.

PORTB, PORTC Interrupt

The PORTB and PORTC are used as the port interrupt sources. Following is the port interrupt function block-diagram.



Port Interrupt (PORTB & PORTC interrupts) PROGRAMMING NOTES:

If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.

1. Set the port as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the port (Use external pull-high resistance or set PULLEN to “1” and write “1” to the port data register).

And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD} in PBC INT application.

7. Base Timer

The base timer generates the different frequency interrupt for real time clock based on the value of BTM.

Base Timer Mode Registers:

BTM.2	BTM.1	BTM.0	R/W	Interrupt Period	Clock Source
0	0	0	R/W	8s	131kHz RC or 32.768kHz Crystal
0	0	1	R/W	4s	131kHz RC or 32.768kHz Crystal
0	1	0	R/W	1s	131kHz RC or 32.768kHz Crystal
0	1	1	R/W	0.5s	131kHz RC or 32.768kHz Crystal
1	0	0	R/W	0.125s	131kHz RC or 32.768kHz Crystal
1	0	1	R/W	62.5ms	131kHz RC or 32.768kHz Crystal
1	1	0	R/W	31.3ms	131kHz RC or 32.768kHz Crystal
1	1	1	R/W	7.8ms	131kHz RC or 32.768kHz Crystal

8. Interrupt

Three interrupt sources are available on SH67L17:

- External interrupt ($\overline{INT}$ share with PORTA.0)
- Base timers interrupt
- PORTB & PORTC interrupts (Falling edge)

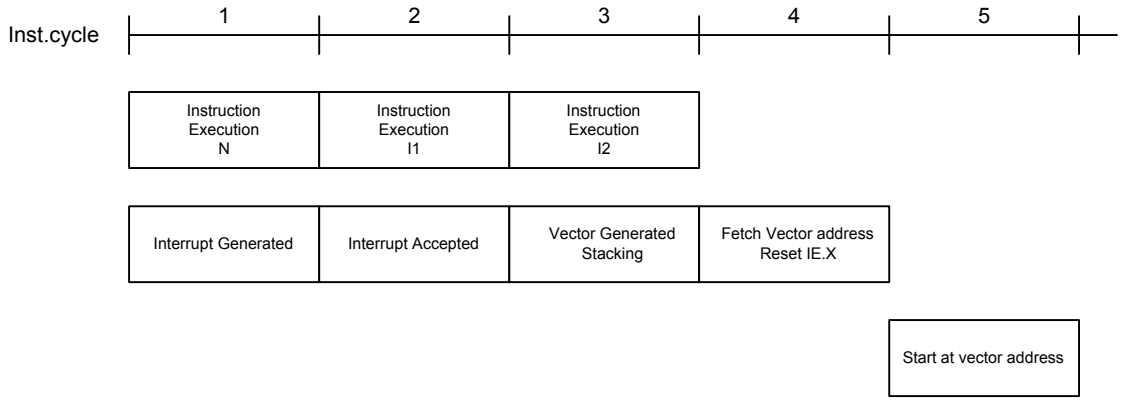
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	-	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	-	IRQBT	IRQP	R/W	Interrupt request flags register

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are cleared to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt

When Bit3 of system register $00 (IEX) is set to “1”, the external interrupt will be enabled, and a falling edge signal on the external interrupt I/O port will generate an external interrupt. External Interrupt can be used to wake the CPU from HALT or STOP mode.

Base Timer Interrupt

The Base timer is based on OSC clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQBT = 1), If the interrupt enable flag is enabled IEBT = 1, a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.
Any one of the I/O input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

9. LCD Driver

The LCD driver contains a controller, a voltage generator, 9 common driver pads and 60 segment driver pads. There is one driving programmable mode: 1/9 duty, 1/4 bias. The controller consists of display data RAM and a duty generator.

The LCD frame frequency is about 45Hz because of the LCD driver clock fetched from the OSC oscillator. (Crystal 32.768kHz or RC 131kHz/4) f_{LCD} = fosc/(360 X 2)

The LCD data RAM is a dual port RAM that transfers data to segment pads automatically without a program control. The LCD RAM can be used as data memory if needed.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When the LCD is off, both the COM and the SEG output low.

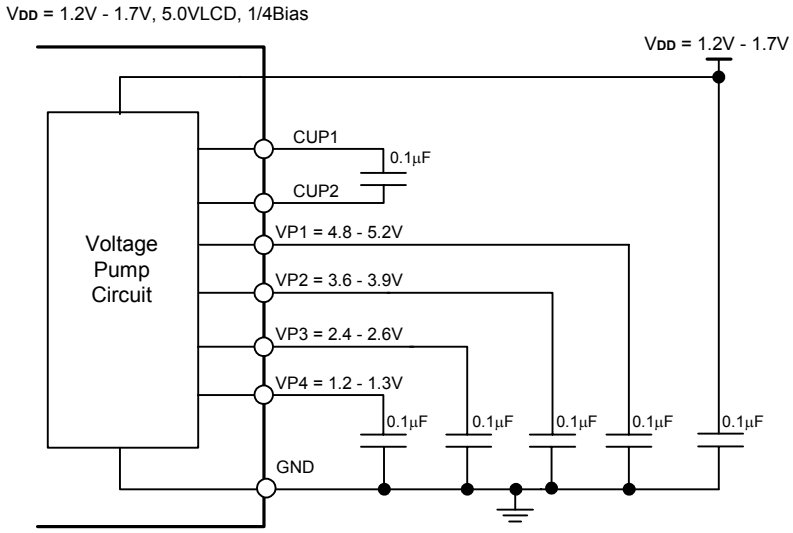
Configuration of LCD RAM Area: (Segments 1 - 60, 1/9duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$340	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$341	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$342	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$343	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$344	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$345	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$346	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$347	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$348	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$349	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$34A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$34B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$34C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$34D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$34E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$34F	SEG16	SEG16	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$350	SEG17	SEG17	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$351	SEG18	SEG18	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$352	SEG19	SEG19	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$353	SEG20	SEG20	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$354	SEG21	SEG21	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$355	SEG22	SEG22	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$356	SEG23	SEG23	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$357	SEG24	SEG24	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$358	SEG25	SEG25	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$359	SEG26	SEG26	SEG26	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$35A	SEG27	SEG27	SEG27	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$35B	SEG28	SEG28	SEG28	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$35C	SEG29	SEG29	SEG29	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$35D	SEG30	SEG30	SEG30	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$35E	SEG31	SEG31	SEG31	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$35F	SEG32	SEG32	SEG32	SEG32
$320	SEG33	SEG33	SEG33	SEG33	$360	SEG33	SEG33	SEG33	SEG33
$321	SEG34	SEG34	SEG34	SEG34	$361	SEG34	SEG34	SEG34	SEG34
$322	SEG35	SEG35	SEG35	SEG35	$362	SEG35	SEG35	SEG35	SEG35
$323	SEG36	SEG36	SEG36	SEG36	$363	SEG36	SEG36	SEG36	SEG36
$324	SEG37	SEG37	SEG37	SEG37	$364	SEG37	SEG37	SEG37	SEG37
$325	SEG38	SEG38	SEG38	SEG38	$365	SEG38	SEG38	SEG38	SEG38
$326	SEG39	SEG39	SEG39	SEG39	$366	SEG39	SEG39	SEG39	SEG39
$327	SEG40	SEG40	SEG40	SEG40	$367	SEG40	SEG40	SEG40	SEG40
$328	SEG41	SEG41	SEG41	SEG41	$368	SEG41	SEG41	SEG41	SEG41
$329	SEG42	SEG42	SEG42	SEG42	$369	SEG42	SEG42	SEG42	SEG42
$32A	SEG43	SEG43	SEG43	SEG43	$36A	SEG43	SEG43	SEG43	SEG43

Configuration of LCD RAM Area (Segments 1 - 60, 1/9duty): (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$32B	SEG44	SEG44	SEG44	SEG44	$36B	SEG44	SEG44	SEG44	SEG44
$32C	SEG45	SEG45	SEG45	SEG45	$36C	SEG45	SEG45	SEG45	SEG45
$32D	SEG46	SEG46	SEG46	SEG46	$36D	SEG46	SEG46	SEG46	SEG46
$32E	SEG47	SEG47	SEG47	SEG47	$36E	SEG47	SEG47	SEG47	SEG47
$32F	SEG48	SEG48	SEG48	SEG48	$36F	SEG48	SEG48	SEG48	SEG48
$330	SEG49	SEG49	SEG49	SEG49	$370	SEG49	SEG49	SEG49	SEG49
$331	SEG50	SEG50	SEG50	SEG50	$371	SEG50	SEG50	SEG50	SEG50
$332	SEG51	SEG51	SEG51	SEG51	$372	SEG51	SEG51	SEG51	SEG51
$333	SEG52	SEG52	SEG52	SEG52	$373	SEG52	SEG52	SEG52	SEG52
$334	SEG53	SEG53	SEG53	SEG53	$374	SEG53	SEG53	SEG53	SEG53
$335	SEG54	SEG54	SEG54	SEG54	$375	SEG54	SEG54	SEG54	SEG54
$336	SEG55	SEG55	SEG55	SEG55	$376	SEG55	SEG55	SEG55	SEG55
$337	SEG56	SEG56	SEG56	SEG56	$377	SEG56	SEG56	SEG56	SEG56
$338	SEG57	SEG57	SEG57	SEG57	$378	SEG57	SEG57	SEG57	SEG57
$339	SEG58	SEG58	SEG58	SEG58	$379	SEG58	SEG58	SEG58	SEG58
$33A	SEG59	SEG59	SEG59	SEG59	$37A	SEG59	SEG59	SEG59	SEG59
$33B	SEG60	SEG60	SEG60	SEG60	$37B	SEG60	SEG60	SEG60	SEG60
Address	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Address**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	-	**-**	**-**	**COM9**		**-**	**-**	**-**	**COM9**
$380	-	-	-	SEG1	$39E	-	-	-	SEG31
$381	-	-	-	SEG2	$39F	-	-	-	SEG32
$382	-	-	-	SEG3	$3A0	-	-	-	SEG33
$383	-	-	-	SEG4	$3A1	-	-	-	SEG34
$384	-	-	-	SEG5	$3A2	-	-	-	SEG35
$385	-	-	-	SEG6	$3A3	-	-	-	SEG36
$386	-	-	-	SEG7	$3A4	-	-	-	SEG37
$387	-	-	-	SEG8	$3A5	-	-	-	SEG38
$388	-	-	-	SEG9	$3A6	-	-	-	SEG39
$389	-	-	-	SEG10	$3A7	-	-	-	SEG40
$38A	-	-	-	SEG11	$3A8	-	-	-	SEG41
$38B	-	-	-	SEG12	$3A9	-	-	-	SEG42
$38C	-	-	-	SEG13	$3AA	-	-	-	SEG43
$38D	-	-	-	SEG14	$3AB	-	-	-	SEG44
$38E	-	-	-	SEG15	$3AC	-	-	-	SEG45
$38F	-	-	-	SEG16	$3AD	-	-	-	SEG46
$390	-	-	-	SEG17	$3AE	-	-	-	SEG47
$391	-	-	-	SEG18	$3AF	-	-	-	SEG48
$392	-	-	-	SEG19	$3B0	-	-	-	SEG49
$393	-	-	-	SEG20	$3B1	-	-	-	SEG50
$394	-	-	-	SEG21	$3B2	-	-	-	SEG51
$395	-	-	-	SEG22	$3B3	-	-	-	SEG52
$396	-	-	-	SEG23	$3B4	-	-	-	SEG53
$397	-	-	-	SEG24	$3B5	-	-	-	SEG54
$398	-	-	-	SEG25	$3B6	-	-	-	SEG55
$399	-	-	-	SEG26	$3B7	-	-	-	SEG56
$39A	-	-	-	SEG27	$3B8	-	-	-	SEG57
$39B	-	-	-	SEG28	$3B9	-	-	-	SEG58
$39C	-	-	-	SEG29	$3BA	-	-	-	SEG59
$39D	-	-	-	SEG30	$3BB	-	-	-	SEG60

Connection Diagram



System Register $14:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	PULLEN	LCD ON	PUMP ON	-	R/W	Bit1: LCD Pump ON/OFF control register Bit2: LCD display ON/OFF control register
	X	0	X	-		LCD display OFF
	X	1	X	-		LCD display ON
	X	X	0	-		LCD pump off
	X	X	1	-		LCD pump on

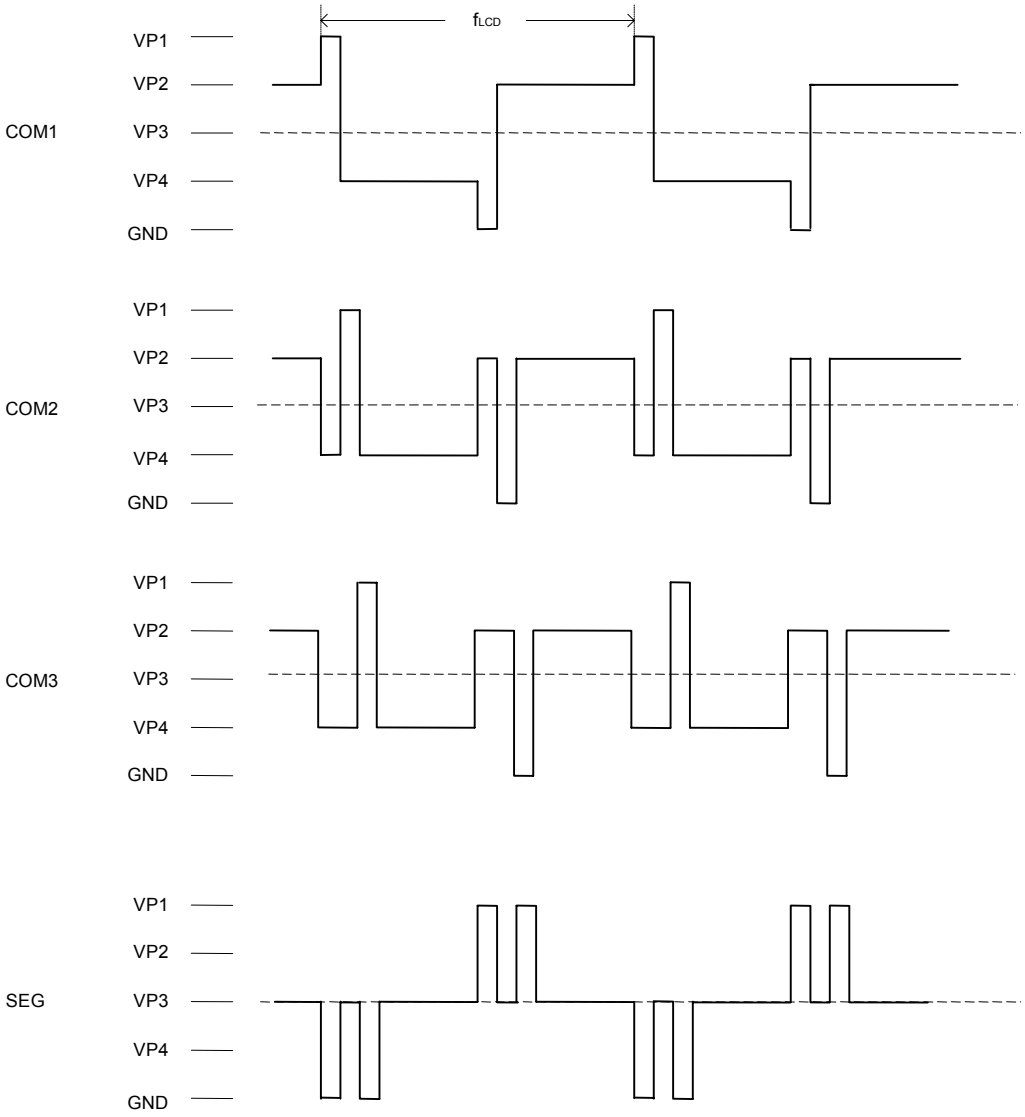
Programming Notes:

When PUMP OFF and LCD ON, both the COM and the SEG output GND.

To turn on the PUMP circuit the Bit2 (LCD ON) of $14 should be clear to “0” at first.

LCD Waveform

The output waveform of 1/9 duty and 1/4 bias is shown as follows.



10. ROM Data Read Table (RDT)

Read ROM Data Table (RDT)

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C7	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$3C8	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$3C9	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$3CA	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 15-bit write-only PC address load register (RDT.14 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first then low nibble), then after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

11. HALT or STOP

After the execution of HALT instruction, SH67L17 will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Base timer, LCD) will keep status.

After the execution of STOP instruction, SH67L17 will enter the STOP mode. The whole chip (including oscillator) will STOP operating.

In the HALT mode, SH67L17 can be waked up if any interrupt occurs.

In the STOP mode, SH67L17 can be waked up if port interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to halt/stop is executed.

Notes: If the **"Special HALT/STOP mode"** is enabled by the code option, the system has a special HALT/STOP mode.

System Register $3C0 - $3C2

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C0	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control Low nibble register
$3C1	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control Middle nibble register
$3C2	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control High nibble register

To turn off the OSC in the special STOP mode, the registers of $3C0, $3C1 and $3C2 must be satisfied to the condition as follow:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C0	1	0	1	0	R/W	Special setting for OSC control in the STOP mode
$3C1	0	1	0	1	R/W	Special setting for OSC control in the STOP mode
$3C2	1	1	0	0	R/W	Special setting for OSC control in the STOP mode

This special STOP mode could improve the reliability of the MCU.

Programming Notes:

If the system needs to enter the special STOP mode, the PORTA.0 should be set in input status with the pull-high resistor enabled by the software programming. At the same time, the external interrupt (/INT0) should be enabled (Bit3 of system register $00 is set to "1") by program. Otherwise, the system cannot enter the special STOP mode correctly. When the system wakes up from the special stop mode, $3C0, $3C1and $3C2 will be cleared to "0" automatically.

If the system needs to enter the special HALT mode, the Base timer interrupt (BT) should be enabled (Bit1 of system register $00 is set to "1") by software. Otherwise, the system cannot enter the special HALT mode correctly.

12. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

12.1. Power-on Reset and Pin Reset:

(1) In RC oscillator mode, f**osc** = 131kHz, the warm-up counter prescaler divide ratio is $1/2^7$ (128).
(2) In Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

12.2. Wake up from stop mode, WDT Reset, LVR Reset:

(1) In RC oscillator mode, f**osc** = 131kHz, the warm-up counter prescaler divide ratio is $1/2^7$ (128).
(2) In Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

13. Watchdog Timer (WDT)

The watchdog timer is a down-count counter, and its clock source is fetched from the system clock and will not run in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E Bit2-0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E Bit3) will be automatically set to "1" by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
	X	0	0	0	R/W	Watchdog timer overflow period is 8s
	X	0	0	1	R/W	Watchdog timer overflow period is 4s
	X	0	1	0	R/W	Watchdog timer overflow period is 1s
	X	0	1	1	R/W	Watchdog timer overflow period is 0.5s
	X	1	0	0	R/W	Watchdog timer overflow period is 0.125s
	X	1	0	1	R/W	Watchdog timer overflow period is 62.5ms
	X	1	1	0	R/W	Watchdog timer overflow period is 31.2ms
	X	1	1	1	R/W	Watchdog timer overflow period is 7.8ms
	0	X	X	X	R	No watchdog timer overflow resets
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer overflow period is valid for V_{DD} = 1.5V.

14. Hardware Multiplier

The MCU has an 8 X 8 BCD hardware multiplier. By making the multiply a hardware operation, it completes in 6 instructions cycle. This is an unsigned multiplier that gives a 16-bit result. The multiplicand/multiplicator should be written into the multiplicand/multiplicator register by software and the result is stored into the product register.

System Register $04 - $07

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$04	MLTL3	MLTL2	MLTL1	MLTL0	R/W	Multiplicator low nibble/Dividend low nibble register
$05	MLTH3	MLTH2	MLTH1	MLTH0	R/W	Multiplicator high nibble/Dividend middle0 nibble register
$06	MLDL3	MLDL2	MLDL1	MLDL0	R/W	Multiplicand low nibble/Dividend middle1 nibble register
$07	MLDH3	MLDH2	MLDH1	MLDH0	R/W	Multiplicand high nibble/Dividend high nibble register

System Register $19 - $1C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$19	PLN3	PLN2	PLN1	PLN0	R/W	Product low nibble/Residue low nibble register
$1A	PMZ3	PMZ2	PMZ1	PMZ0	R/W	Product middle0 nibble/Residue high nibble register
$1B	PMO3	PMO2	PMO1	PMO0	R/W	Product middle1 nibble register
$1C	PHN3	PHN2	PHN1	PHN0	R/W	Product high nibble register

System Register $02 is the hardware multiplier/divider control register.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	-	-	GO/DONE	M/D	R/W	Bit0: Multiplier/ Divider mode select register Bit1: Multiplier/Divider status flag register
	-	-	X	0		Select divider
	-	-	X	1		Select multiplier
	-	-	0	X		Multiplier/divider calculate has completed
	-	-	1	X		Multiplier/divider is during calculating.

The multiplicator register low (/high) nibble is $04 (/$05) and the multiplicand register low (/high) nibble is $06 (/$07). The product register low (/middle0/middle1/high) nibble is $19 (/$1A/$1B/$1C).

Set Multiplier/Divider status flag register to "1" to start calculating, then after 6 instructions it is clear to "0" by hardware when calculate has completed.

15. Hardware Divider

The MCU has a 16/8 BCD hardware divider. By making the division a hardware operation, it completes in 8 instructions cycle. This is an unsigned divider that gives a 16-bit quotient and an 8-bit residue. The dividend/divisor should be written into the dividend/divisor register by software and the result is stored into the quotient/residue register.

System Register $04 - $07, $0C, $0D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$04	MLTL3	MLTL2	MLTL1	MLTL0	R/W	Multiplicator low nibble/Dividend low nibble register
$05	MLTH3	MLTH2	MLTH1	MLTH0	R/W	Multiplicator high nibble/Dividend middle0 nibble register
$06	MLDL3	MLDL2	MLDL1	MLDL0	R/W	Multiplicand low nibble/Dividend middle1 nibble register
$07	MLDH3	MLDH2	MLDH1	MLDH0	R/W	Multiplicand high nibble/Dividend high nibble register
$0C	DIVL3	DIVL2	DIVL1	DIVL0	R/W	Divisor low nibble register
$0D	DIVH3	DIVH2	DIVH1	DIVH0	R/W	Divisor high nibble register

System Register $15 - 1A

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	QLN.3	QLN.2	QLN.1	QLN.0	R/W	Quotient low nibble register
$16	QMZ.3	QMZ.2	QMZ.1	QMZ.0	R/W	Quotient middle0 nibble register
$17	QMO.3	QMO.2	QMO.1	QMO.0	R/W	Quotient middle1 nibble register
$18	QHN.3	QHN.2	QHN.1	QHN.0	R/W	Quotient high nibble register
$19	PLN3	PLN2	PLN1	PLN0	R/W	Product low nibble/Residue low nibble register
$1A	PMZ3	PMZ2	PMZ1	PMZ0	R/W	Product middle0 nibble/Residue high nibble register

The dividend register low (/middle0/middle1/high) nibble is $04 (/$05/$06/$07), the divisor register low (/high) nibble is $0C (/$0D), the quotient register low (/middle0/middle1/high) nibble is $15 (/$16/$17/$18) and the residue low (/high) nibble is $19 (/$1A).

System Register $02 is the hardware multiplier/divider control register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	-	-	GO/DONE	M/D	R/W	Bit0: Multiplier/ Divider mode select register Bit1: Multiplier/Divider status flag register
	-	-	X	0		Select divider
	-	-	X	1		Select multiplier
	-	-	0	X		Multiplier/divider calculate has completed
	-	-	1	X		Multiplier/divider is during calculating.

Set Multiplier/Divider status flag register to “1” to start calculating, then after 8 instructions it is clear to “0” by hardware when calculate has completed.

Notes:

If write irregular data (such as 0A-0F) to $04/$05/$06/$07/$0C/$0D and start calculating, then when calculate is completed the result register ($04/$05/$06/$07/$0C/$0D) will be set to”0F”. Or if write 00 to both divisor Low and High Nibble, when calculate is completed the result will be set to “0F” also.

16. Pin Reset

The MCU integrates two Reset Pins: Reset0 and Reset1. Both Reset0 and Reset1 can be set as the level triggering or the edge triggering by Code Option.

When Level triggering is selected by Code Option and system is in the level triggering Reset, during the reset period, the LCD PUMP will be turn off.

The Bit3 of $03 will be clear to “0” after Pin Reset0 Reset, and it will be set to “1” after Pin Reset1 Reset.

17.Code Option:

(a) Special HALT/STOP:

OP_SP:
0 = Disable
1 = Enable

(b) Watch Dog Timer:

OP_WDT:
0 = Disable
1 = Enable

(c) Reset Triggering Mode:

OP_RESET:
0 = Level triggering
1 = Edge triggering

(d) OSC Type:

OP_OSC:
0 = 131kHz RC
1 = 32.768kHz Crystal

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11 - PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . .0°C to +70°C

Storage Temperature . . . . . .-55°C to +125°C

***Comments**

Stresses exceed those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.2 - 1.7V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	30kHz ≤ f_{OSC} ≤ 500kHz
Operating Current	I_{OP}	-	10	15	μA	f_{OSC} = 131kHz RC All output pins unloaded, execute NOP instruction, (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	4	6	μA	f_{OSC} = 32.768kHz Crystal All output pins unloaded, execute NOP instruction, (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	30	50	μA	f_{OSCX} = 500kHz, (OSCX as system clock) All output pins unloaded, Execute NOP instruction, (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
Standby Current	I_{SB}	-	3	5	μA	f_{OSC} = 131kHz RC All output pins unloaded (HALT mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	2	3	μA	f_{OSC} = 32.768kHz Crystal All output pins unloaded (HALT mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	10	15	μA	f_{OSCX} = 500kHz, All output pins unloaded (HALT mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
		-	-	1	μA	All output pins unloaded (STOP mode), (excluding LCD bias current, WDT off.) (V_{DD} = 1.5V)
Reset Current	I_{RST}	-	-	20	μA	Chip current when $\overline{\text{RESET}}$ 0 is available, (V_{DD} = 1.5V)
LCD Lighting	I_{LCD}	-	-	10	μA	No panel loaded. LCD pump frequency = 16K, (V_{DD} = 1.5V)
Input High Voltage	V_{IH}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
		0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{\text{INT}}$, $\overline{\text{RESET}}$, TEST (schmitt trigger input)
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD
		GND - 0.3	-	0.15 X V_{DD}	V	$\overline{\text{INT}}$, $\overline{\text{RESET}}$, TEST (schmitt trigger input)
Output High Voltage	V_{OH1}	0.8 X V_{DD}	-	-	V	PORTA, B, C, D (I_{OH} = - 0.3mA) (V_{DD} = 1.5V)
Output Low Voltage	V_{OL1}	-	-	0.2 X V_{DD}	V	PORTA, B, C, D (I_{OL} = 0.3mA) (V_{DD} = 1.5V)
LCD ON Driving Resistor	R_{ON}	-	5	8	kΩ	SEG1 - 60, COM1 - 9
Pull-high Resistor	R_P	-	150	-	kΩ	PORT Pull-high resistor (V_{OH} = 0, I_{OH} = -10μA) (V_{DD} = 1.5V)
$\overline{\text{RESET}}$ Pull-high Resistor	R_{P1}	-	200	-	kΩ	$\overline{\text{RESET0}}$ & $\overline{\text{RESET1}}$ Pin input "1" (level trigger) (V_{DD} = 1.5V)
		-	1000	-	kΩ	$\overline{\text{RESET0}}$ & $\overline{\text{RESET1}}$ Pin input "0" (level trigger) (V_{DD} = 1.5V)
		-	200	-	kΩ	$\overline{\text{RESET0}}$ & $\overline{\text{RESET1}}$ (Edge trigger) (V_{DD} = 1.5V)

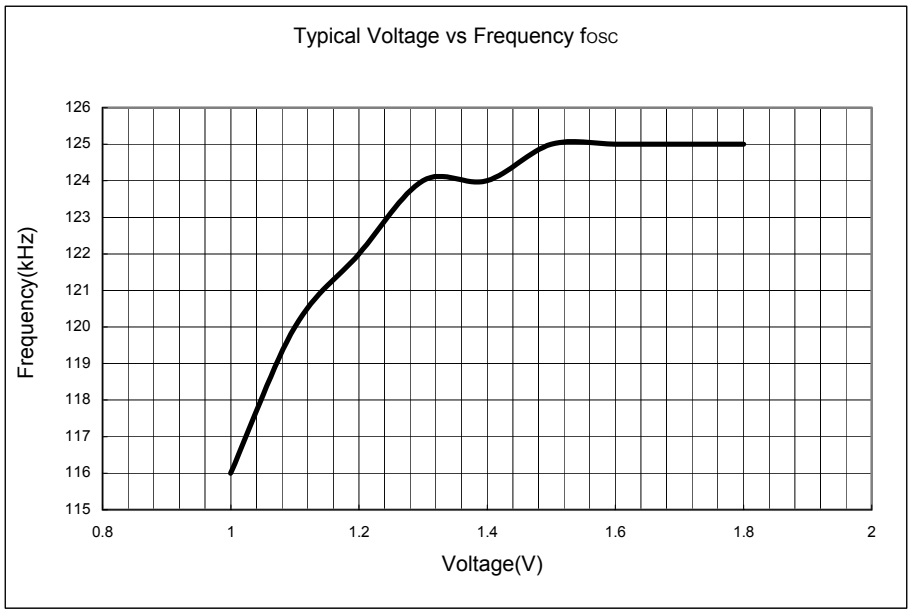
AC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Frequency Variation	Δf/f	-	-	±20	%	Include chip to chip variations f_{OSC} = 131kHz, T_A = -10°C to +70°C
		-	-	±20	%	Include chip to chip variations f_{OSCX} = 500kHz, T_A = -10°C to +70°C

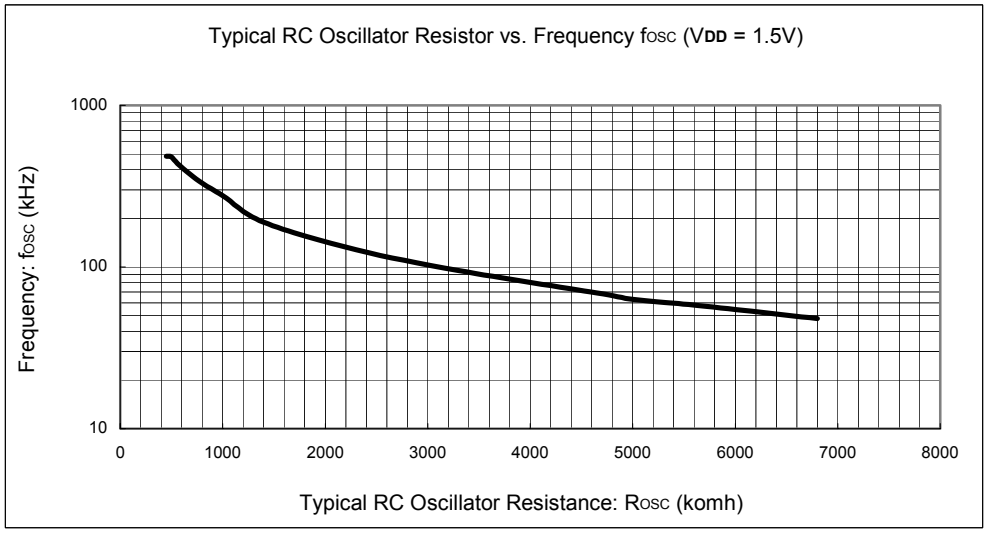
RC Oscillator Characteristics Graphs

RC oscillator Characteristics Graphs (for reference only)

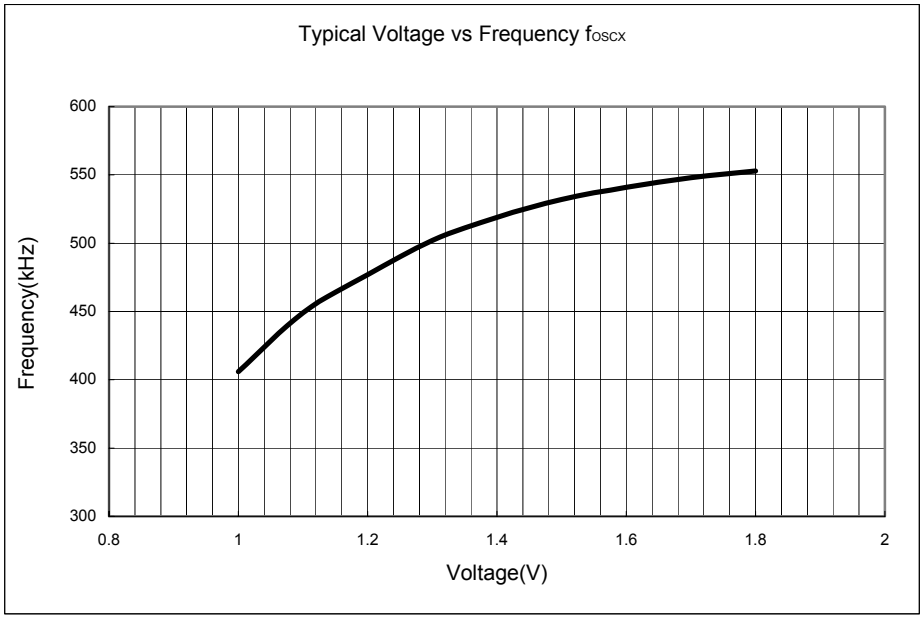
(a) Typical Voltage vs Frequency **fosc**



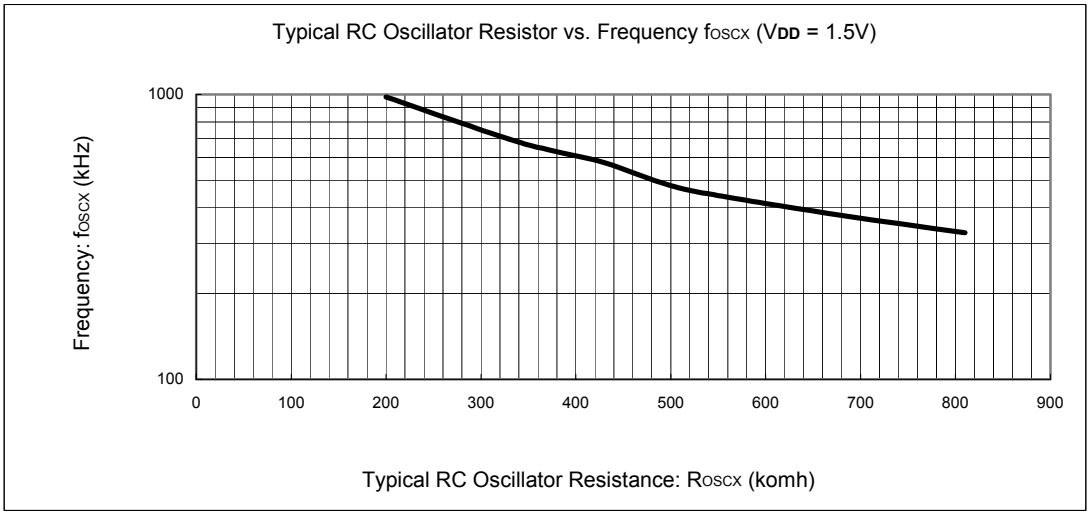
(b) Typical RC Oscillator Resistor vs. Frequency **fosc** (V_{DD} = 1.5V)



(c) Typical Voltage vs Frequency f**oscx**



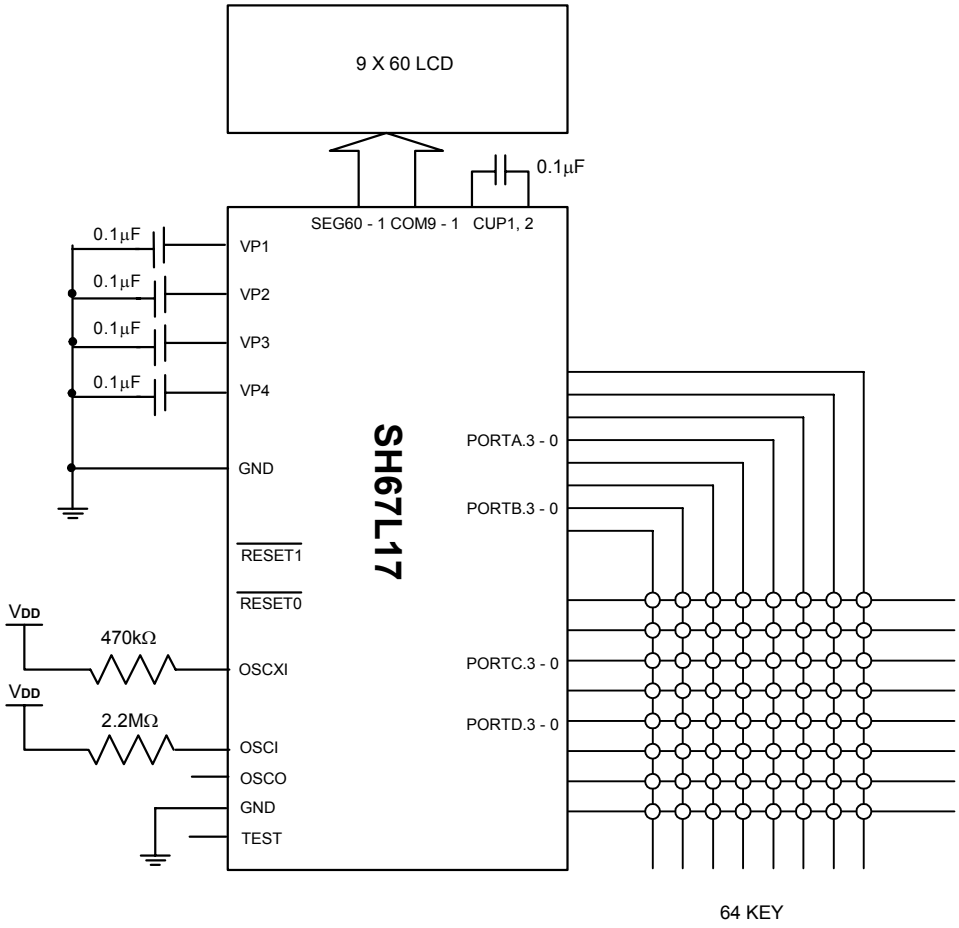
(d) Typical RC Oscillator Resistor vs. Frequency f**oscx** (V**DD** = 1.5V)



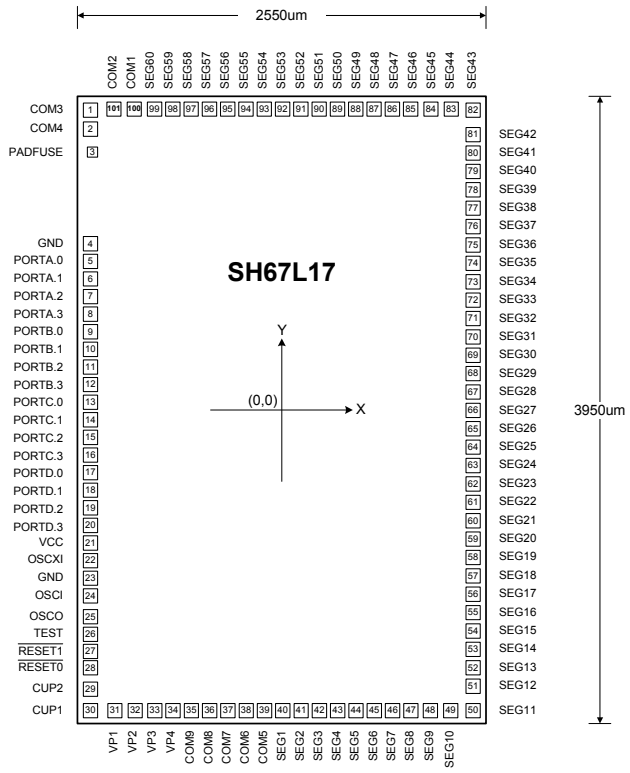
Application Circuits (for reference only)

Note: SH67L17 chip substrate connects to system ground.

AP1: (1) Operating Voltage: 1.5V
(2) Oscillator: RC: 131kHz OSCX RC: 500kHz
(3) LCD: 5.0V, 1/9 duty, 1/4 bias
(4) PORTA - D: I/O.



Bonding Diagram



*** Substratum connects to ground.**

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	COM3	-1154	1846	21	VCC	-1154	-810
2	COM4	-1154	1726	22	OSCXI	-1154	-920
3	PADFUSE	-1141.9	1563	23	GND	-1154	-1030
4	GND	-1154	1060	24	OSCI	-1154	-1140
5	PORTA.0	-1154	950	25	OSCO	-1154	-1260
6	PORTA.1	-1154	840	26	TEST	-1154	-1370
7	PORTA.2	-1154	730	27	$\overline{\text{RESET1}}$	-1154	-1480
8	PORTA.3	-1154	620	28	$\overline{\text{RESET0}}$	-1154	-1595
9	PORTB.0	-1154	510	29	CUP2	-1154	-1715
10	PORTB.1	-1154	400	30	CUP1	-1154	-1846
11	PORTB.2	-1154	290	31	VP1	-1012	-1846
12	PORTB.3	-1154	180	32	VP2	-887	-1846
13	PORTC.0	-1154	70	33	VP3	-767	-1846
14	PORTC.1	-1154	-40	34	VP4	-657	-1846
15	PORTC.2	-1154	-150	35	COM9	-547	-1846
16	PORTC.3	-1154	-260	36	COM8	-437	-1846
17	PORTD.0	-1154	-370	37	COM7	-327	-1846
18	PORTD.1	-1154	-480	38	COM6	-217	-1846
19	PORTD.2	-1154	-590	39	COM5	-107	-1846
20	PORTD.3	-1154	-700	40	SEG1	3	-1846

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
41	SEG2	113	-1846	72	SEG33	1154	660
42	SEG3	223	-1846	73	SEG34	1154	770
43	SEG4	333	-1846	74	SEG35	1154	880
44	SEG5	443	-1846	75	SEG36	1154	995
45	SEG6	553	-1846	76	SEG37	1154	1110
46	SEG7	663	-1846	77	SEG38	1154	1225
47	SEG8	773	-1846	78	SEG39	1154	1340
48	SEG9	894	-1846	79	SEG40	1154	1455
49	SEG10	1019	-1846	80	SEG41	1154	1575
50	SEG11	1154	-1840	81	SEG42	1154	1695
51	SEG12	1154	-1695	82	SEG43	1154	1840
52	SEG13	1154	-1575	83	SEG44	1009	1846
53	SEG14	1154	-1455	84	SEG45	884	1846
54	SEG15	1154	-1340	85	SEG46	764	1846
55	SEG16	1154	-1225	86	SEG47	654	1846
56	SEG17	1154	-1110	87	SEG48	544	1846
57	SEG18	1154	-995	88	SEG49	434	1846
58	SEG19	1154	-880	89	SEG50	324	1846
59	SEG20	1154	-770	90	SEG51	214	1846
60	SEG21	1154	-660	91	SEG52	104	1846
61	SEG22	1154	-550	92	SEG53	-6	1846
62	SEG23	1154	-440	93	SEG54	-116	1846
63	SEG24	1154	-330	94	SEG55	-226	1846
64	SEG25	1154	-220	95	SEG56	-336	1846
65	SEG26	1154	-110	96	SEG57	-446	1846
66	SEG27	1154	0	97	SEG58	-556	1846
67	SEG28	1154	110	98	SEG59	-666	1846
68	SEG29	1154	220	99	SEG60	-776	1846
69	SEG30	1154	330	100	COM1	-904	1846
70	SEG31	1154	440	101	COM2	-1029	1846
71	SEG32	1154	550				

Ordering Information

Part No.	Package
SH67L17H	Chip Form

Data Sheet Revision History

Version	Content	Date
2.0	Update the LCD waveform frame frequency	Aug. 2010
1.0	Original	Aug. 2006