SH67L18

8K 4-bit Low Power Micro-controller with LCD Driver

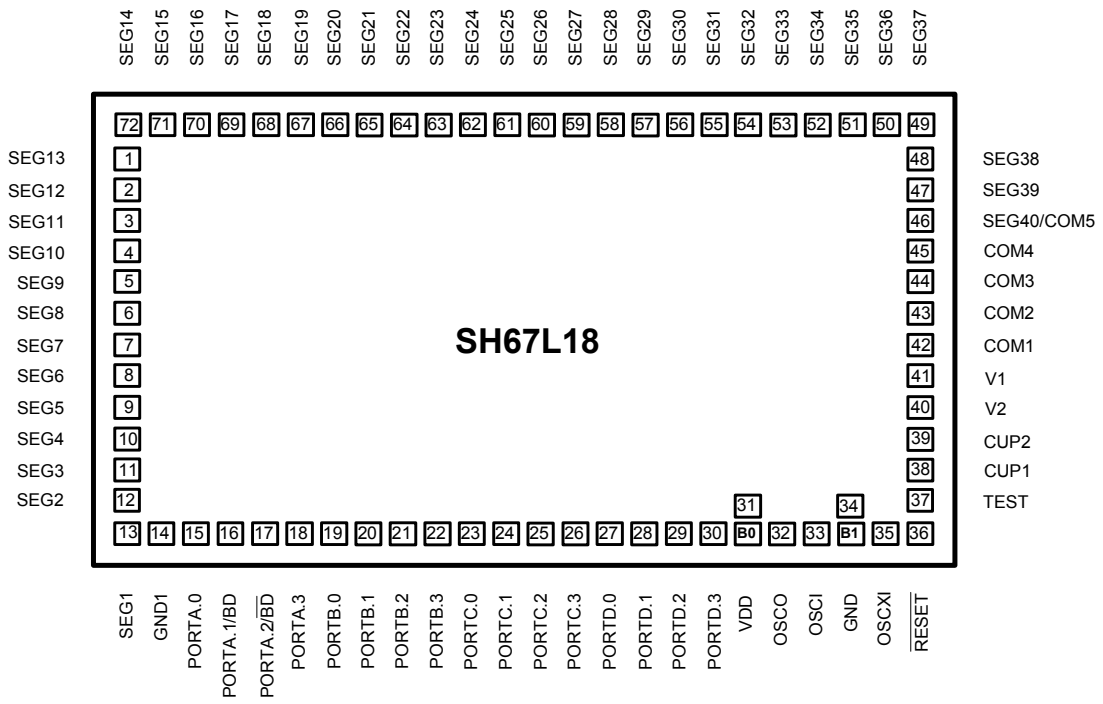
Features

- SH6610D-based single-chip 4-bit micro-controller with LCD driver
- ROM: 8K X 16 bits
- RAM: 768 X 4 bits
  - 32 System Control Register
  - 736 Data memory
  - 195 bits LCD RAM
- Operation Voltage:
  fOSCX = 300kHz, V_{DD} = 1.2V - 1.7V (Typical 1.5V)
  fOSCX = 800kHz, V_{DD} = 1.3V - 1.7V
- 16 CMOS Bi-directional I/O pads (including 4 input only pads)
- 8-Level Stack (Including Interrupts)
- Powerful Interrupt Sources:
  - External interrupt (Low active)
  - Base Timer interrupt
  - PORTB, PORTC & PORTD interrupts (Low active)
- Oscillator (Code Option):
  OSCX:
  - RC oscillator: 300kHz
  - RC oscillator: 800kHz
- Base timer clock source (Code Option):
  OSC:
  - Crystal Oscillator: 32.768kHz
  - RC oscillator: 32kHz
- Instruction Cycle Time (4/**fosc**)
- Two Low Power Operation Modes: HALT And STOP
- Reset
  - Built-in Watchdog Timer (WDT) (Code Option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR) (Code Option)
- LCD Driver:
  40SEG X 4COM (1/4 Duty, 1/3 Bias)
  39SEG X 5COM (1/5 Duty, 1/3 Bias)
- Built-in Voltage Tripler Charge Pump Circuit
- Built-in Alarm Generator
- Single solar supply application (Code Option)
- Low power consumption
- Read Rom Data Table function (RDT)
- Bonding option for multi-code software
- Available in CHIP FORM

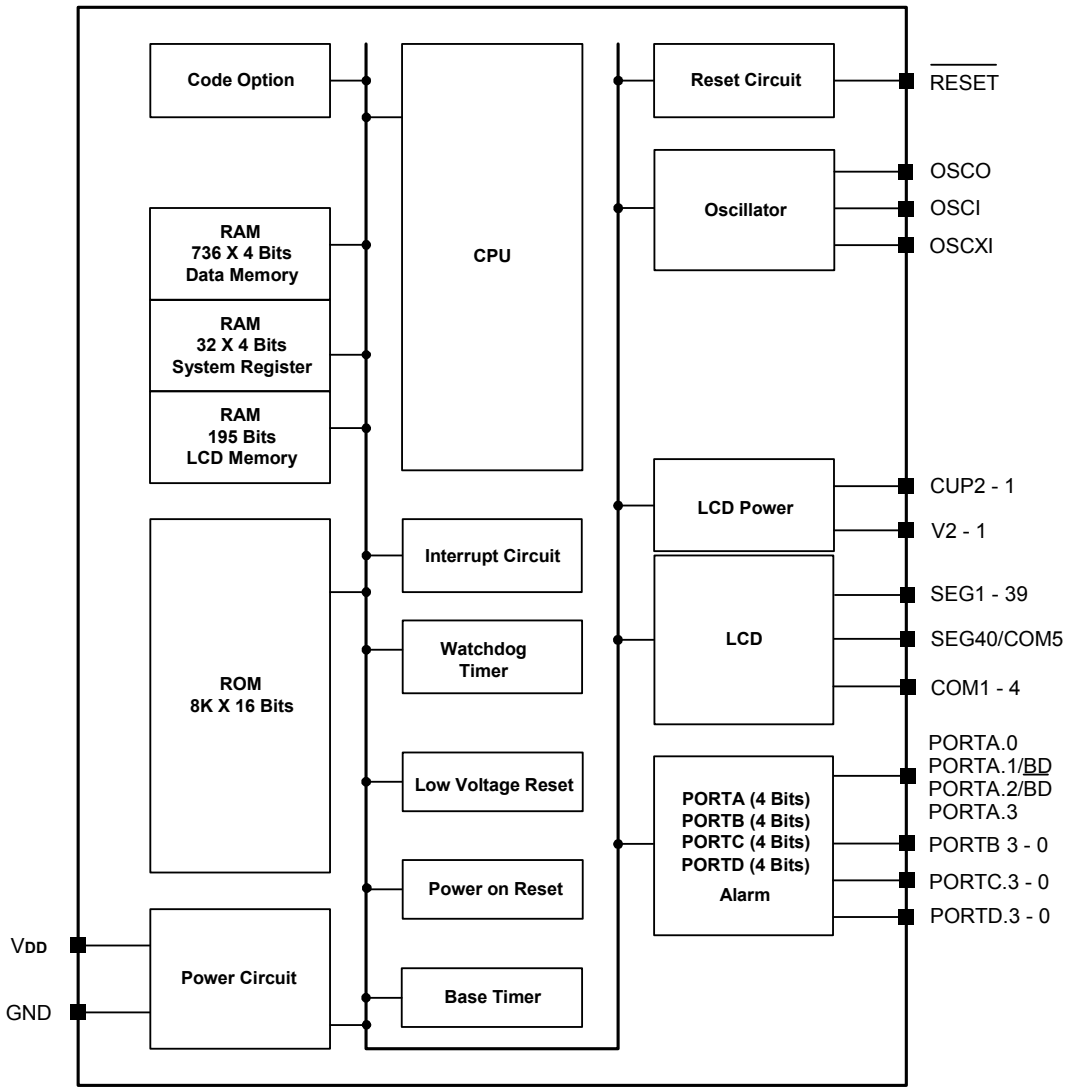
General Description

SH67L18 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core; RAM, ROM, Base Timer, Alarm generator, LCD driver, I/O ports, and voltage tripler charge pump circuit. The SH67L18 is suitable for fraction calculator application.

Pad Configuration



Block Diagram



Pad Description

No. of Pad	Pad Name	I/O	Description
1 - 13 47 - 72	SEG13 - SEG1 SEG39 - SEG14	O	Segment signal output for LCD display
46	SEG40/COM5	O	Segment/Common signal output for LCD display
42 - 45	COM1 - COM4	O	Common signal output for LCD display
40 - 41	V2 - V1	P	Power supply pin for LCD driver
38 - 39	CUP1 - CUP2	P	Connection for voltage treble capacitor
37	TEST	I	Test pin internally pull-low (No connection for user)
36	$\overline{\text{RESET}}$	I	Pin reset input (level or edge triggering selected by code option, Low active or falling edge active, internal pull-high and Schmitt trigger input)
31	V_{DD}	P	Power supply pin
34	GND	P	Ground pin
14	GND1	P	Ground pin
	B0	I	Bonding option (internally pull-low)
	B1	I	Bonding option (internally pull-high)
33	OSCI	I	OSC input pin, connected to a crystal or external resistor
32	OSCO	O	OSC output pin. No output in RC mode
35	OSCXI	I	OSCX input pin, connected to an external resistor
18 - 15	PORTA.3-0	I/O	Bit programmable I/O, External interrupt (PORTA.0) (Active low level) PORTA.1 (BD) and PORTA.2 ($\overline{\text{BD}}$) can be Alarm output
22 - 19	PORTB.3-0	I/O	Bit programmable I/O, Vector interrupt (Active low level)
26 - 23	PORTC.3-0	I/O	Bit programmable I/O, Vector interrupt (Active low level)
30 - 27	PORTD.3-0	I	Input port. Vector Interrupt (Active low level)

Which, I: input; O: output; P: Power;

Functional Description

1. CPU

The CPU contains the following functional blocks:
Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:
Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).
The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4 Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code Bit7-Bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H--3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9 - Bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $01F
Data memory: $020 - $2FF, $328 - $32F, $358 - $35F
LCD RAM space: $300 - $327, $330 - $357

RAM bank table:

Bank0 B = 0	Bank1 B = 1	Bank2 B = 2	Bank3 B = 3	Bank4 B = 4	Bank5 B = 5	Bank 6 B = 6
$020 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F

Where, B: RAM bank bit use in instructions.

2.2. Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	-	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	-	IRQBT	IRQP	R/W	Interrupt request flags register
$02	PUMP ON	-	-	-	R/W	Bit3: LCD pump ON/OFF control register
$03	-	BTM.2	BTM.1	BTM.0	R/W	Bit2-0: Base timer mode register
$04	OSCON	HVL	-	-	R/W	Bit2:OSC heavy load mode control register Bit3:OSC ON/OFF control register
$05	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSC control Low nibble register
$06	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSC control Middle nibble register
$07	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSC control High nibble register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R	PORTD data register
$0C	-	ALMON	-	ALMF	R/W	Bit0: Alarm carrier frequency control register. Bit2: Alarm enable control register
$0D	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	PULLEN	LCDON	B1	B0	R/W R	Bit1-0: Bonding option register Bit2: LCD display ON/OFF control register Bit3: Port Pull-High Control register
$14	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$15	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$16	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$17	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	-	-	-	-	-	Reserved
$1C	LVRF	-	-	-	R	Low Voltage Reset Flag register
$1D	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable register
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
$1F	-	-	BNK1	BNK0	R/W	Bit1-0: ROM Bank register

3. ROM

The ROM can address 8K X 16 bits of program area from $0000 to $1FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to External interrupt service routine
$002	JMP*	Reserved
$003	JMP*	Jump to Base Timer interrupt service routine
$004	JMP*	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

3.3. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM spaces. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU addressing space maps to one of the three banks (BANK 1, 2, 3) of the upper 6K of ROM. (According to the Bank Register $1F)

The bank switch mapping is as follows:

CPU Address	ROM Space, $1FH = 0	ROM Space, $1FH = 1	ROM Space, $1FH = 2
Lower 2K address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
Upper 2K address	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset	Reset Pin Reset	WDT Reset	LVR Reset
$00	IEX	-	IEBT	IEP	0-00	0-00	0-00	0-00
$01	IRQX	-	IRQBT	IRQP	0-00	0-00	0-00	0-00
$02	PUMP ON	-	-	-	0---	u---	0---	0---
$03	-	BTM.2	BTM.1	BTM.0	-000	-000	-000	-000
$04	OSCON	HVL	-	-	00--	u0--	00--	00--
$05	RELL3	RELL2	RELL1	RELL0	0000	0000	0000	0000
$06	RELM3	RELM2	RELM1	RELM0	0000	0000	0000	0000
$07	RELH3	RELH2	RELH1	RELH0	0000	0000	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000	0000	0000
$0C	-	ALMON	-	ALMF	-0-0	-0-0	-0-0	-0-0
$0D	AEC3	AEC2	AEC1	AEC0	0000	0000	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu	uuuu	xxxx
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu	uuuu	xxxx
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu	uuuu	xxxx
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu	-uuu	-xxx
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu	-uuu	-xxx
$13	PULLEN	LCDON	B1	B0	00uu	00uu	00uu	00uu
$14	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	xxxx	0000	xxxx
$15	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	xxxx	0000	xxxx
$16	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	xxxx	0000	xxxx
$17	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	xxxx	0000	xxxx
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000	0000	0000
$1B	-	-	-	-	----	----	----	----
$1C	LVRF	-	-	-	0---	0---	u---	1---
$1D	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	0000	0000	0000	0000
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	0000	1000	0000
$1F	-	-	BNK1	BNK0	--00	--00	--00	--00

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

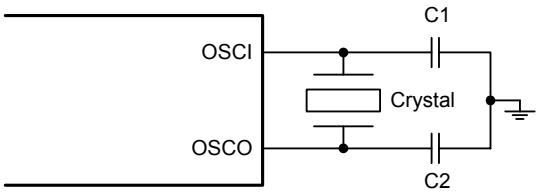
SH67L18 has two on-chip oscillation circuits OSC and OSCX.
The OSCX oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = f**oscx**/4
The OSC oscillator generates the clock pulses that provide the Base timer and the LCD driver. The OSC oscillator can be controlled ON/OFF by the OSCON bit setting in the OSC control register.

5.1. Instruction Cycle Time

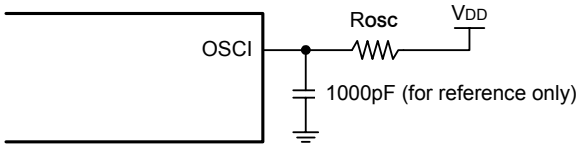
(1) 4/300kHz (≈ 13.33μs) for 300kHz oscillator.
(2) 4/800kHz (= 5μs) for 800kHz oscillator.

5.2. OSC Oscillator Type

(1) Crystal oscillator: 32.768kHz



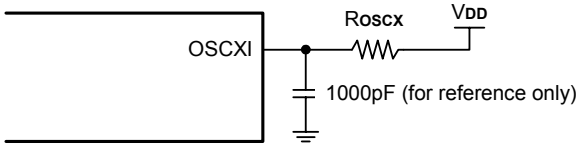
(2) RC oscillator: 32kHz



External R**osc** RC

5.3.OSCX Oscillator

RC oscillator: 300kHz - 800kHz



External R**oscx** RC

5.4. Capacitor Selection for Oscillator

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V**DD** and the temperature range for the application.

Before selecting crystal, the user should consult the crystal manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Port

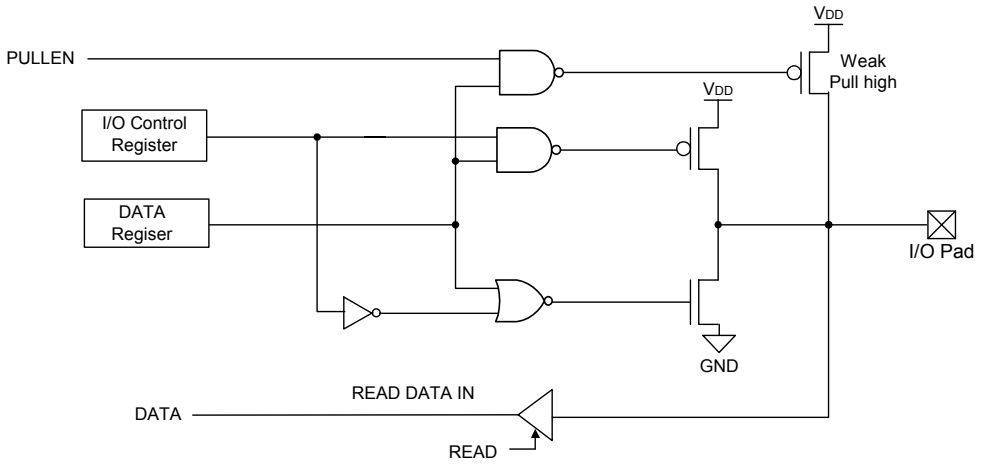
The MCU provides 12 bi-directional I/O ports and 4 input ports. The PORT data is put in register $08 - $0B. The PORT control register $18 - $1A controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PULLEN of $13 and the data of the port, when the PORT is used as input. PORTA.3 - 0 PORTB.3 - 0 and PORTC.3 - 0 are bi-directional I/O ports as well as PORTD.3 - 0 input only.

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R	PORTD data register
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	-	-	-	-	-	Reserved

PA (/B/C) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin.



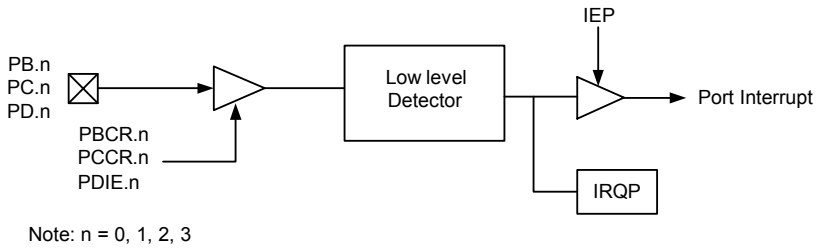
System Register $13

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PULLEN	LCDON	B1	B0	R/W R	Bit3: Port Pull-High Control register
	0	X	X	X	R/W	Port Pull-high resistor disable (Power on initial)
	1	X	X	X	R/W	Port Pull-high resistor enable

To turn on the pull-high resistor, user must set PULLEN to “1”, and write “1” to the port data register (including PORTD) when the port is input.

PORTB, PORTC and PORTD Interrupt

The PORTB, PORTC and PORTD are used as the port interrupt sources. Following is the port interrupt function block-diagram.



Note: n = 0, 1, 2, 3

Port Interrupt (PORTB, PORTC & PORTD interrupts) PROGRAMMING NOTES:

If user wants to generate an interrupt when a low level emerges on the port, the following must be executed.

1. Set the port as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the port (Use external pull-high resistance or set PULLEN to “1” and write “1” to the port data register).

In order to correctly return from the port interrupt-processing subroutine, the low level applying on the port must be released before the relative IRQ flag clearing and IE resetting. Otherwise, it is possible to reenter the active interrupt.

Since PORTD.3-0 can be used as input ports only, there are another interrupts enable control registers for each I/O in PORTD.

System Register $1D: Port Interrupt Enable Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1D	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable control register

PDIEN.n, (n = 0, 1, 2, 3)
0: Disable port interrupt. (Power on initial)
1: Enable port interrupt.

External Interrupt (PORTA.0):

If user wants to generate an external interrupt when a low level emerges on PORTA.0, the following must be executed.

1. Set PORTA.0 as input port, fill port data register with “1” and avoid port floating.
2. Pull-high PORTA.0 (Use external pull-high resistance or set PULLEN to “1”).

In order to correctly return from the external (PORTA.0) interrupt-processing subroutine, the low level applying on the PORTA.0 must be released before the relative IRQ flag clearing and IE resetting. Otherwise, it is possible to reenter the active interrupt.

7. Base Timer

The Base timer generates the different frequency interrupt for real time clock based on the value of BTM. The heavy load register, HVL, is used to switch 32.768kHz Crystal oscillator into heavy load mode that makes the oscillation easier in the startup period but more current is needed.

After the Base timer is enabled, it counts every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow. This causes the interrupt of the Base timer interrupt request flag to 1. Therefore, the Base timer can function as an interval timer periodically.

Base Timer Mode Registers (BTM):

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$03	-	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register (BTM)

BTM.2	BTM.1	BTM.0	R/W	Interrupt Period	Clock Source
0	0	0	R/W	Stop (Power on initial)	32kHz RC or 32.768kHz Crystal
0	0	1	R/W	1Hz	32kHz RC or 32.768kHz Crystal
0	1	0	R/W	2Hz	32kHz RC or 32.768kHz Crystal
0	1	1	R/W	4Hz	32kHz RC or 32.768kHz Crystal
1	0	0	R/W	8Hz	32kHz RC or 32.768kHz Crystal
1	0	1	R/W	16Hz	32kHz RC or 32.768kHz Crystal
1	1	0	R/W	32Hz	32kHz RC or 32.768kHz Crystal
1	1	1	R/W	64Hz	32kHz RC or 32.768kHz Crystal

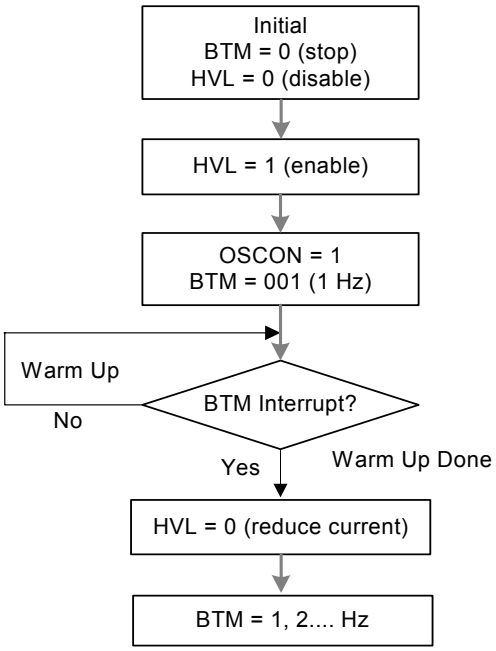
System Register $04: OSC control registers

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$04	OSCON	HVL	-	-	R/W	Bit2: OSC heavy load mode control register Bit3: OSC ON/OFF control register
	X	0	-	-	R/W	Disable heavy load mode for 32.768kHz crystal OSC (Power on initial)
	X	1	-	-	R/W	Enable heavy load mode for 32.768kHz crystal OSC
	0	X	-	-	R/W	Turn off OSC oscillator (Power on initial)
	1	X	-	-	R/W	Turn on OSC oscillator

Programming Notes:

1. Since the Base timer clock source is fetched from the OSC oscillator, turn on the OSC oscillator before the Base timer will operate.
2. The initial value of the BTM register is 00H.It means that the Base Timer can be controlled ON/OFF by the BTM register's software writing.
3. Since the Base timer clock comes from the OSC oscillator, the Base timer can operate even in the STOP mode if the OSCON bit value of the OSC control register ($04) is 1 and the BTM register's value is non-zero.
4. Please enable the OSC (Crystal or RC) oscillator before turning the PUMP/LCD on, since the LCD driver's clock source is fetched from the OSC oscillator, similar as the Base timer.

The Example of using the Base Timer:



8. Alarm Output

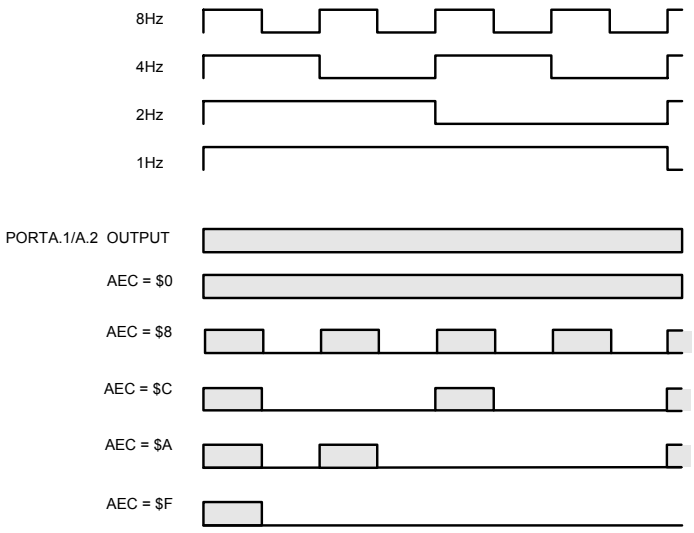
System Register $0C: Alarm control register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0C	-	ALMON	-	ALMF	R/W	Bit0: Alarm carrier frequency control register Bit2: Alarm enable control register
	-	0	-	X	R/W	Alarm OFF (Power on initial)
	-	1	-	X	R/W	Alarm ON, PORTA.1 (BD) and PORTA.2 ($\overline{BD}$) shared with buzzer output
		X		0	R/W	Alarm carrier frequency is 4kHz (Power on initial)
		X		1	R/W	Alarm carrier frequency is 2kHz

System Register $0D: Envelope setting register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
	0	0	0	0	R/W	DC envelope (Power on initial)
	X	X	X	1	R/W	1Hz envelope AND other envelope choice logically
	X	X	1	X	R/W	2Hz envelope AND other envelope choice logically
	X	1	X	X	R/W	4Hz envelope AND other envelope choice logically
	1	X	X	X	R/W	8Hz envelope AND other envelope choice logically

The programming Alarm waveform is shown as below:



Alarm Output Waveform

To activate the Alarm function, first switch the ALMON to the Alarm output mode. After setting ALMON equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time. The Alarm will output GND in the STOP mode.

Notes:

The Alarm function block's clock is fetched from the OSC (32.768kHz Crystal Oscillator or 32kHz RC Oscillator selected by the code option). It is necessary to enable the OSC (Crystal or RC) oscillator before using the Alarm function.

9. Interrupt

Three interrupt sources are available on SH67L18:
- External interrupt (INT0 share with PORTA.0)
- Base Timer interrupt
- PORTB, PORTC & PORTD interrupts (Low active)

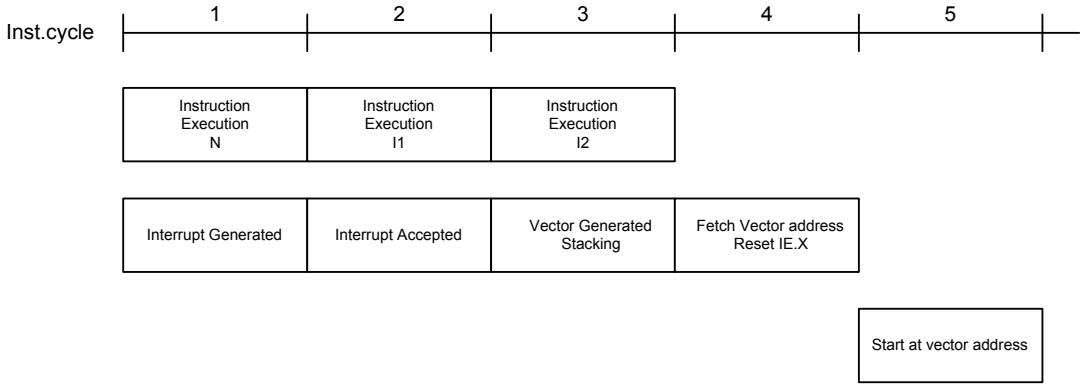
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	-	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQX	-	IRQBT	IRQP	R/W	Interrupt request flags register

When IEx is set to “1” and the interrupt request is generated (IRQx is “1”), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are cleared to “0” automatically, so when IRQx is “1” and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt

When Bit3 of system register $00 (IEX) is set to “1”, the external interrupt will be enabled, and a low level applying on the external interrupt I/O port will generate an external interrupt. External Interrupt can be used to wake the CPU from HALT or STOP mode.

Base Timer Interrupt

The Base timer is based on OSC clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQBT = 1), If the interrupt enable flag is enabled IEBT = 1, a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT or STOP mode.

Port Low active Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

Any one of the I/O input port applying with a low level would generate an interrupt request (IRQP = 1). In order to avoid multi-responses, it is strongly recommended that the relative input port cannot be connected with a low level all the time. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

10. LCD Driver

The LCD driver contains a controller, a voltage generator, 5 common driver pads, and 40 segment driver pads. There are two different driving programmable modes: 1/4 duty and 1/3 bias, 1/5 duty and 1/3 bias. The controller consists of display data RAM and a duty generator.

The LCD data RAM is a dual port RAM that transfers data to segment pads automatically without a program control. The LCD RAM can be used as data memory if needed.

Since the LCD driver clock comes from the OSC oscillator, the LCD can display on even in the STOP mode if the OSCON bit value of the OSC control register ($04) is 1.

When the LCD pump is turned off, the data of LCD RAM keeps the value.

When the LCD is **display** off, both the COM and the SEG output low.

Memory from $300 to $35F(full nibble) are mapping to LCD display area that can be used as general data RAM when the LCD display is turned off (LCD ON = 0).

Configuration of LCD RAM Area: (SEG 1 - 40, 1/4duty)

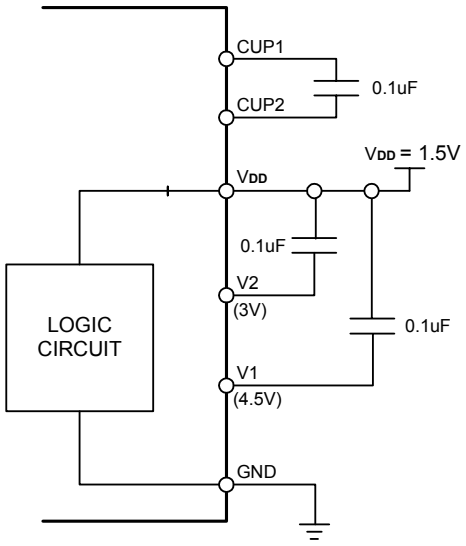
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$314	SEG21	SEG21	SEG21	SEG21
$301	SEG2	SEG2	SEG2	SEG2	$315	SEG22	SEG22	SEG22	SEG22
$302	SEG3	SEG3	SEG3	SEG3	$316	SEG23	SEG23	SEG23	SEG23
$303	SEG4	SEG4	SEG4	SEG4	$317	SEG24	SEG24	SEG24	SEG24
$304	SEG5	SEG5	SEG5	SEG5	$318	SEG25	SEG25	SEG25	SEG25
$305	SEG6	SEG6	SEG6	SEG6	$319	SEG26	SEG26	SEG26	SEG26
$306	SEG7	SEG7	SEG7	SEG7	$31A	SEG27	SEG27	SEG27	SEG27
$307	SEG8	SEG8	SEG8	SEG8	$31B	SEG28	SEG28	SEG28	SEG28
$308	SEG9	SEG9	SEG9	SEG9	$31C	SEG29	SEG29	SEG29	SEG29
$309	SEG10	SEG10	SEG10	SEG10	$31D	SEG30	SEG30	SEG30	SEG30
$30A	SEG11	SEG11	SEG11	SEG11	$31E	SEG31	SEG31	SEG31	SEG31
$30B	SEG12	SEG12	SEG12	SEG12	$31F	SEG32	SEG32	SEG32	SEG32
$30C	SEG13	SEG13	SEG13	SEG13	$320	SEG33	SEG33	SEG33	SEG33
$30D	SEG14	SEG14	SEG14	SEG14	$321	SEG34	SEG34	SEG34	SEG34
$30E	SEG15	SEG15	SEG15	SEG15	$322	SEG35	SEG35	SEG35	SEG35
$30F	SEG16	SEG16	SEG16	SEG16	$323	SEG36	SEG36	SEG36	SEG36
$310	SEG17	SEG17	SEG17	SEG17	$324	SEG37	SEG37	SEG37	SEG37
$311	SEG18	SEG18	SEG18	SEG18	$325	SEG38	SEG38	SEG38	SEG38
$312	SEG19	SEG19	SEG19	SEG19	$326	SEG39	SEG39	SEG39	SEG39
$313	SEG20	SEG20	SEG20	SEG20	$327	SEG40	SEG40	SEG40	SEG40

Configuration of LCD RAM Area: (SEG 1 - 39, 1/5duty)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		-	-	-	COM5
$300	SEG1	SEG1	SEG1	SEG1	$330	-	-	-	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$331	-	-	-	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$332	-	-	-	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$333	-	-	-	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$334	-	-	-	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$335	-	-	-	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$336	-	-	-	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$337	-	-	-	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$338	-	-	-	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$339	-	-	-	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$33A	-	-	-	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$33B	-	-	-	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$33C	-	-	-	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$33D	-	-	-	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$33E	-	-	-	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$33F	-	-	-	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$340	-	-	-	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$341	-	-	-	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$342	-	-	-	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$343	-	-	-	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$344	-	-	-	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$345	-	-	-	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$346	-	-	-	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$347	-	-	-	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$348	-	-	-	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$349	-	-	-	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$34A	-	-	-	SEG27
$31B	SEG28	SEG28	SEG28	SEG28	$34B	-	-	-	SEG28
$31C	SEG29	SEG29	SEG29	SEG29	$34C	-	-	-	SEG29
$31D	SEG30	SEG30	SEG30	SEG30	$34D	-	-	-	SEG30
$31E	SEG31	SEG31	SEG31	SEG31	$34E	-	-	-	SEG31
$31F	SEG32	SEG32	SEG32	SEG32	$34F	-	-	-	SEG32
$320	SEG33	SEG33	SEG33	SEG33	$350	-	-	-	SEG33
$321	SEG34	SEG34	SEG34	SEG34	$351	-	-	-	SEG34
$322	SEG35	SEG35	SEG35	SEG35	$352	-	-	-	SEG35
$323	SEG36	SEG36	SEG36	SEG36	$353	-	-	-	SEG36
$324	SEG37	SEG37	SEG37	SEG37	$354	-	-	-	SEG37
$325	SEG38	SEG38	SEG38	SEG38	$355	-	-	-	SEG38
$326	SEG39	SEG39	SEG39	SEG39	$356	-	-	-	SEG39

Connection Diagram

V_{DD} = 1.5V, 4.5V LCD,1/5 duty, 1/3 bias and 1/4 duty, 1/3bias



System Register $02:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	PUMP ON	-	-	-	R/W	Bit3: LCD pump ON/OFF control register
	0	-	-	-	R/W	LCD pump OFF (Power on initial)
	1	-	-	-	R/W	LCD pump ON

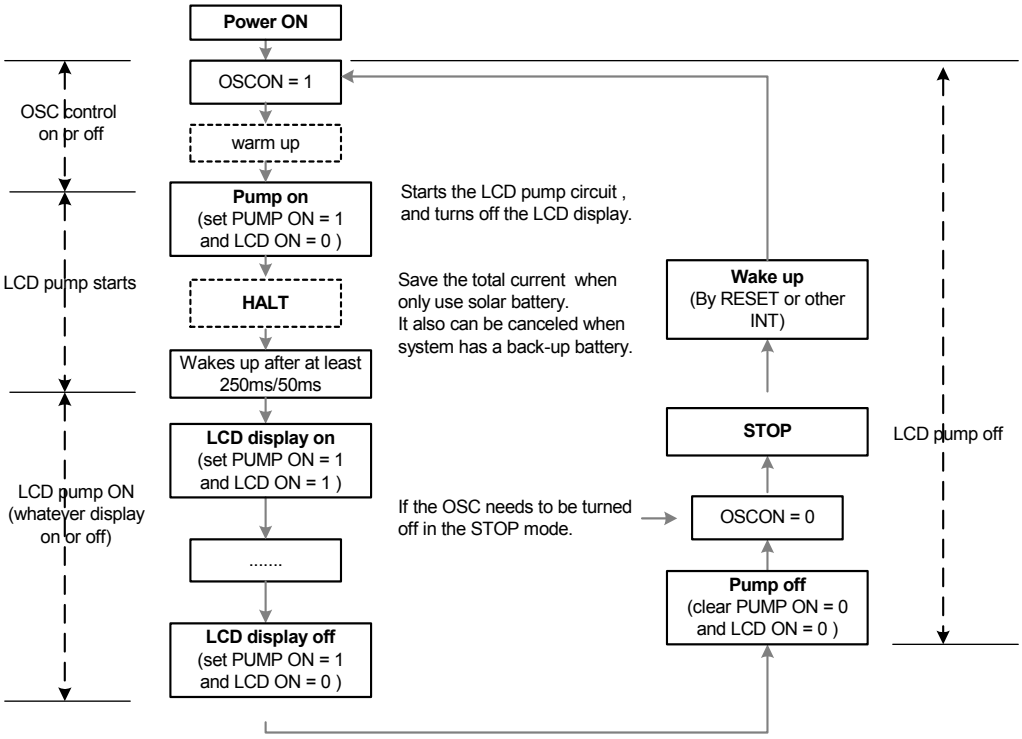
System Register $13:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PULLEN	LCDON	B1	B0	R/W R	Bit2: LCD display ON/OFF control register
	X	0	X	X	R/W	LCD display OFF (Power on initial)
	X	1	X	X	R/W	LCD display ON

Programming Notes:

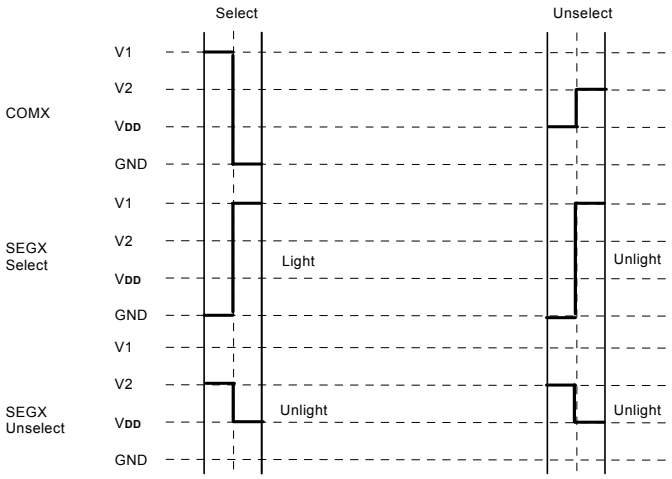
1. The pump circuit frequency is 4KHz regardless of the OSC oscillator type.
2. The LCD frame frequency is 42.67Hz/41.67Hz (1/4duty) or 40.96Hz/40.00Hz (1/5duty) because of the LCD driver clock fetched from the OSC oscillator. (32.768KHz Crystal or 32KHz RC) $f_{LCD} = f_{OSC}/(384 \times 2)$, (1/4duty) or $f_{LCD} = f_{OSC}/(400 \times 2)$), (1/5duty)
3. Please enable the OSC (Crystal or RC) oscillator before turning the LCD pump & display on, since the LCD driver's clock source is fetched from the OSC oscillator.
4. As the LCD pump circuits need more currents while starting up, please confirm the LCD pump & display is OFF (LCD ON = 0, PUMP ON = 0) before turning on the OSC oscillator
5. Do not turn the LCD pump & display on during the OSC oscillator warm-up period. Otherwise, the pump & display circuits may not work properly and successfully since the OSC oscillator is not stable enough.
6. Both the COMMON and the SEGMENT output the ground level if the PUMP ON bit is cleared to "0" even when the LCD ON bit is set to 1.
7. It is recommended that the proper setting flow for turning on the LCD pump & display should be followed as below:
   A. Clear the LCD ON bit and the PUMP ON bit to 0. Then turn on the OSC oscillator. (Set OSCON bit to 1.)
   B. Insert a sufficient delay time (64ms for 32.768kHz crystal and 4ms for 32kHz RC) to satisfy the OSC warm up period.
   C. Set the PUMP ON bit to 1 to turn on the LCD pump circuit. Then force the system to enter the HALT mode to reduce the current consumption. If the system is in a single solar supply application, 250ms delay period is necessary. If the system is in the backup battery using, the delay time is at least 50 ms.
   D. Set the LCD ON bit to 1 to turn on the LCD display after the LCD RAM has been initialized.

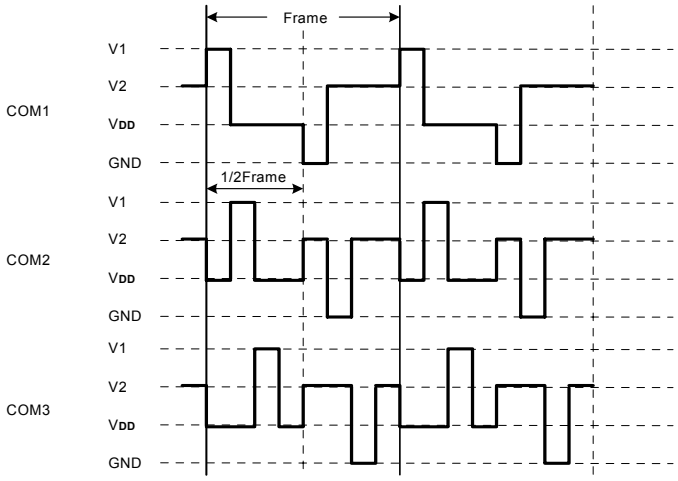
Example:



LCD Waveform

1/5duty, 1/4 duty, 1/3 bias LCD waveform (V_{DD} = 1.5V, V1 = 4.5V, V2 = 3V)





11. Read ROM Data Table (RDT)

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$15	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$16	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$17	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 13 bit write-only PC address load register (RDT.12 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should fill 0 to higher 3 bit (Bit 13 - 15) first, then write the ROM table address to RDT register (high nibble first then low nibble), after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

12. HALT and STOP Mode

After the execution of HALT instruction, SH67L18 will enter the HALT mode. In the HALT mode, the CPU will stop operating. But peripheral circuit (Base Timer, LCD driver…) will keep status.

After the execution of STOP instruction, SH67L18 will enter the STOP mode. The whole chip (including oscillator) will stop operating. But the peripheral circuits such as the OSC oscillator, the LCD driver and the Base Timer can keep status if these function blocks have been enabled before entering the STOP mode.

In the HALT mode, SH67L18 can be waked up if any interrupt occurs.

In the STOP mode, SH67L18 can be waked up if Port Interrupt (including the External Interrupt) occurs. SH67L18 can also be waked up by the Base Timer interrupt if the OSC oscillator and the Base Timer have been enabled before entering the STOP mode.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

Special HALT and STOP Mode

If the “Single Solar Supply Application” is enabled by the code option, the system has a special HALT/STOP mode.

System Register $05 - $07

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$05	RELL3	RELL2	RELL1	RELL0	R/W	Special STOP mode OSCX control Low nibble register
$06	RELM3	RELM2	RELM1	RELM0	R/W	Special STOP mode OSCX control Middle nibble register
$07	RELH3	RELH2	RELH1	RELH0	R/W	Special STOP mode OSCX control High nibble register

To turn off the OSCX in the special STOP mode, the registers of $05, $06 and $07 must be satisfied to the condition as follow:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$05	1	0	1	0	R/W	Special setting for OSCX control in the STOP mode
$06	0	1	0	1	R/W	Special setting for OSCX control in the STOP mode
$07	1	1	0	0	R/W	Special setting for OSCX control in the STOP mode

This special STOP mode could improve the reliability of the MCU.

Programming Notes:

If the system needs to enter the special STOP mode, the PORTA.0 should be set in input status with the pull-high resistor enabled by the software programming. At the same time, the external interrupt ($\overline{\text{INT0}}$) should be enabled (Bit3 of system register $00 is set to “1”) by means of the program setting. Otherwise, the system cannot enter the special STOP mode correctly. When the system wakes up from the special stop mode, $05, $06 and $07 will be cleared to “0” automatically.

If the system needs to enter the special HALT mode, the Base timer interrupt (BT) should be enabled (Bit1 of system register $00 is set to “1”) by software. At the same time, the Base timer should be enabled (Bit2-0 of system register $03 is none-zero) by means of the program setting. Otherwise, the system cannot enter the special HALT mode correctly.

13. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

13.1. Power-on Reset for OSCX

Warm-up time interval:

In 300kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192). (27.3ms)

In 800kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192). (10.2ms)

13.2. Register Control on for OSC

In 32kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{6}$ (64). (2.0ms)

In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024). (31.3ms)

13.3. Pin Reset for OSCX

Warm-up time interval:

In 300kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{9}$ (512). (1.7ms)

In 800kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{9}$ (512). (0.6ms)

13.4. Wake up from STOP Mode

Warm-up time interval:

In 300kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{9}$ (512). (1.7ms)

In 800kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{9}$ (512). (0.6ms)

14. Watchdog Timer (WDT)

The watchdog timer is a down-count counter, and its clock source is OSCX (300kHz RC or 800kHz RC), it will not run if OSCX is turn off. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E Bit2-0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
	X	0	0	0	R/W	WDT overflow period is about 1s. (300kHz or 800kHz) (Power on initial)
	X	0	0	1	R/W	WDT overflow period is about 0.5s. (300kHz or 800kHz)
	X	0	1	0	R/W	WDT overflow period is about 0.125s. (300kHz or 800kHz)
	X	0	1	1	R/W	WDT overflow period is about 62.5ms. (300kHz or 800kHz)
	X	1	X	0	R/W	WDT overflow period is about 31.25ms. (300kHz or 800kHz)
	X	1	X	1	R/W	WDT overflow period is about 15.625ms. (300kHz or 800kHz)
	0	X	X	X	R	No watchdog timer overflow resets
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer overflow period is valid for V_{DD} = 1.5V.

15. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device.
The LVR function is selected by the code option.
The LVR circuit has the following functions when LVR function is enabled:
- Generates a system reset when $V_{DD} \leq V_{LVR}$
- Cancels the system reset when $V_{DD} > V_{LVR}$

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	LVRF	-	-	-	R	Bit3: Low voltage reset flag register
	0	-	-	-	R	No LVR reset (Power on initial)
	1	-	-	-	R	LVR reset has issued

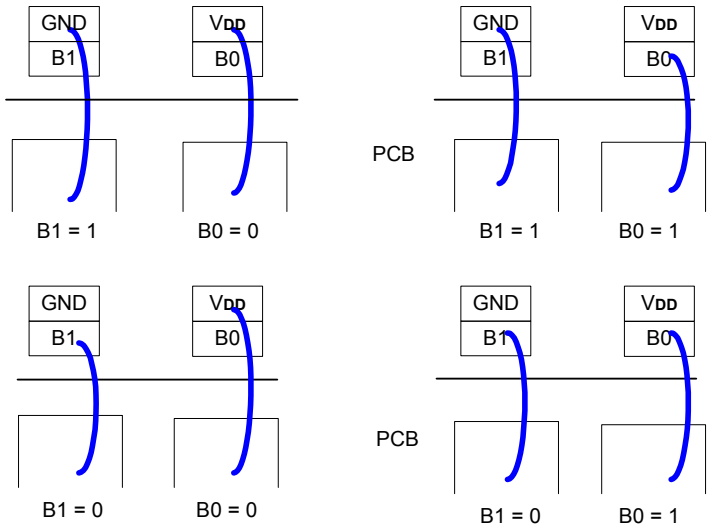
LVR flag will always keep '1' when the LVR happens, LVRF will be cleared to '0' by reading the system register $1C.

Note:
If the Low Voltage Reset function is disabled by the code option, the LVRF bit will be cleared to "0", regardless the system reset result.

16. Bonding Option

System Register $13:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PULLEN	LCDON	B1	B0	R/W R	Bit1-0: Bonding option register
	X	X	1	0	R	Default bonding option
	X	X	0	0	R	B1 bond to GND
	X	X	1	1	R	B0 bond to V_{DD}
	X	X	0	1	R	B1 bond to GND & B0 bond to V_{DD}



Up to 4 different bonding options are possible for user's needs. The chip's program has 4 different program flows that vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

Programming Notes:

To correctly fetch the contents of bonding options in variety applications, it is necessary to insert a dummy read instruction before the genuine reading from the system register $13.

17. Code Option

Addresses: $2000

Body data: 0111 1010 0001 1000 (7A18)

Addresses: $2001

Data: XOWR DLSC 0000 0000

(a) X (OSCX clock source):

0 = "**fosc**x = 300kHz RC" (Default)

1 = "**fosc**x = 800kHz RC"

(b) O (OSC clock source):

0 = "fosc = 32kHz RC" (Default)

1 = "fosc = 32.768kHz Crystal"

(c) W (WDT selection):

0 = Disable WDT (Default)

1 = Enable WDT

(d) R (Reset triggering type selection):

0 = RESET level triggering (low active) (Default)

1 = RESET edge triggering (falling edge)

(e) D (LCD duty selection):

0 = 1/4 duty (Default)

1 = 1/5 duty

(f) L (Low Voltage Reset selection):

0 = Disable LVR (Default)

1 = Enable LVR

(g) S (Single solar supply application selection):

0 = single solar supply application disable (Default)

1 = single solar supply application enable

(h) C (OSCX RC curve selection):

0 = RC frequency will change as V_{DD} alters (Default)

1 = RC frequency will not change as V_{DD} alters

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -10°C to +70°C

Storage Temperature . . . . . .-55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	130kHz ≤ fosc ≤ 500kHz
		1.3	1.5	1.7	V	500kHz ≤ fosc ≤ 800kHz
Operating Current	I_{OP}	-	15	20	μA	foscx = 300kHz, (OSCX as system clock) All output pins unloaded, Execute NOP instruction. (Excluding OSC, Base timer, LCD and Alarm current) V_{DD} = 1.5V
		-	40	50	μA	foscx = 800kHz, (OSCX as system clock) All output pins unloaded, Execute NOP instruction. (Excluding OSC, Base timer, LCD and Alarm current) V_{DD} = 1.5V
Standby Current	I_{SB}	-	8	12	μA	foscx = 300kHz, All output pins unloaded (HALT mode) (Excluding OSC, Base timer, LCD and Alarm current) V_{DD} = 1.5V
		-	22	28	μA	foscx = 800kHz, All output pins unloaded (HALT mode) (Excluding OSC, Base timer, LCD and Alarm current) V_{DD} = 1.5V
		-	1	2	μA	foscx = 300kHz or 800kHz, OSC = 32.768kHz Crystal oscillator or 32kHz RC All output pins unloaded (STOP mode), OSC on (not heavy load mode), Base timer off, LCD off and Alarm off V_{DD} = 1.5V (Excluding bonding option current)
		-	-	1	μA	All output pins unloaded (STOP mode), OSC off, Base timer off, LCD off and Alarm off, V_{DD} = 1.5V (Excluding bonding option current)
Reset Current	I_{RST}	-	-	3	μA	Chip current when RESET is available, V_{DD} = 1.5V (Excluding OSC, LCD and bonding option current)
LCD Lighting	I_{LCD}	-	-	1	μA	No panel loaded. LCD pump frequency = 4k

DC Electrical Characteristics (GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input High Voltage	V_{IH}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD V_{DD} = 1.5V
		0.85 X V_{DD}	-	V_{DD} + 0.3	V	INT, RESET, TEST (Schmitt trigger input) V_{DD} = 1.5V
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, PORTB, PORTC, PORTD V_{DD} = 1.5V
		GND - 0.3	-	0.15 X V_{DD}	V	INT, RESET, TEST (Schmitt trigger input) V_{DD} = 1.5V
Output High Voltage	V_{OH}	0.8 X V_{DD}	-	-	V	PORTA, B, C, D (I_{OH} = -0.3mA) V_{DD} = 1.5V
		V_{P1} - 0.2	-	-	V	SEGX, I_{OH} = -3μA
		V_{P1} - 0.2	-	-	V	COMX, I_{OH} = -8μA
Output Low Voltage	V_{OL}	-	-	0.2 X V_{DD}	V	PORTA, B, C, D (I_{OL} = 0.3mA) V_{DD} = 1.5V
		-	-	0.2	V	SEGX, I_{OL} = 3μA
		-	-	0.2	V	COMX, I_{OL} = 8μA
Pull-high Resistor	R_P	-	150	-	kΩ	PORT Pull-high resistor (V_{OH} = 0, I_{OH} = -10μA) V_{DD} = 1.5V
RESET Pull-high Resistor	R_{P1}	-	200	-	kΩ	Pull high resistor for RESET pin input “1”
		-	1000	-	kΩ	Pull high resistor for RESET pin input “0”
LVR Voltage	V_{LVR}	-	0.8	1.1	V	LVR function is enabled
LVR Operating current	I_{LVR}	-	1	2	μA	LVR function is enabled, V_{DD} = 1.5V

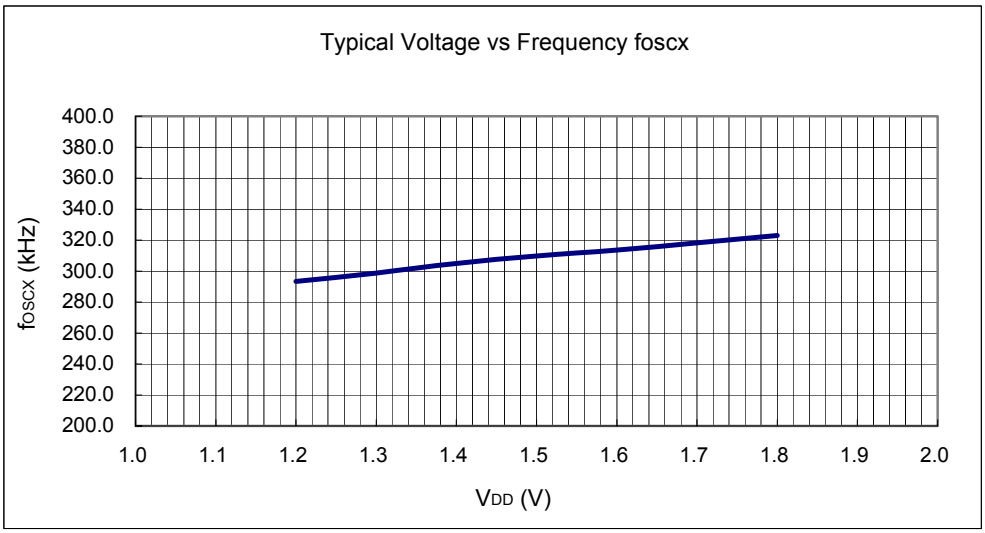
AC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Frequency Variation	ΔF/F	-20	-	+20	%	Include chip-to-chip variations f_{OSCX} = 300kHz, when the condition is “OSCX RC frequency will not change as V_{DD} alters”. T_A = -10°C to +70°C
		-40	-	+20	%	Include chip-to-chip variations f_{OSCX} = 300kHz, when the condition is “OSCX RC frequency will change as V_{DD} alters”. T_A = -10°C to +70°C
		-20	-	+20	%	Include chip to chip variations f_{OSCX} = 800kHz, T_A = -10°C to +70°C

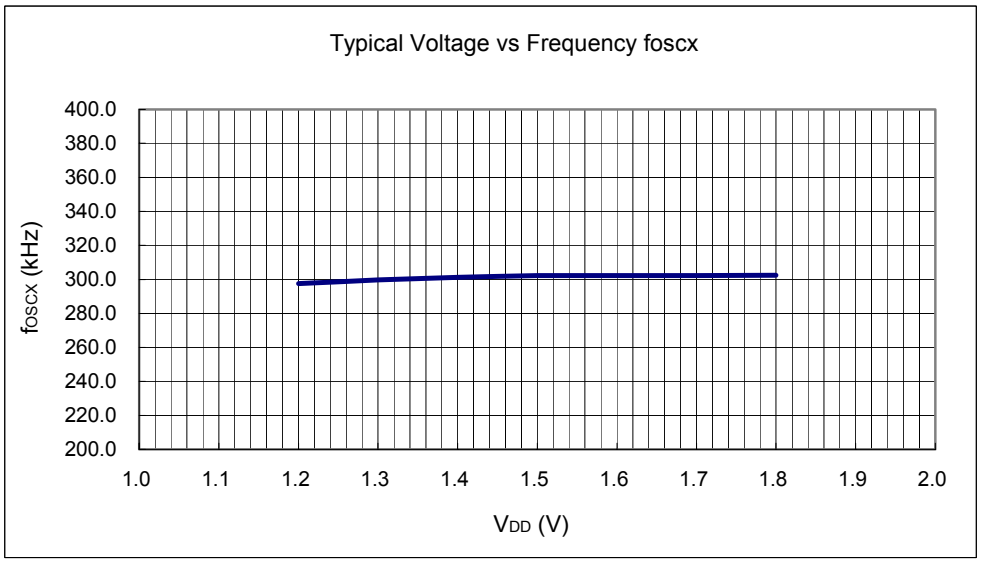
RC Oscillator Characteristics Graphs

RC oscillator Characteristics Graphs (for reference only)

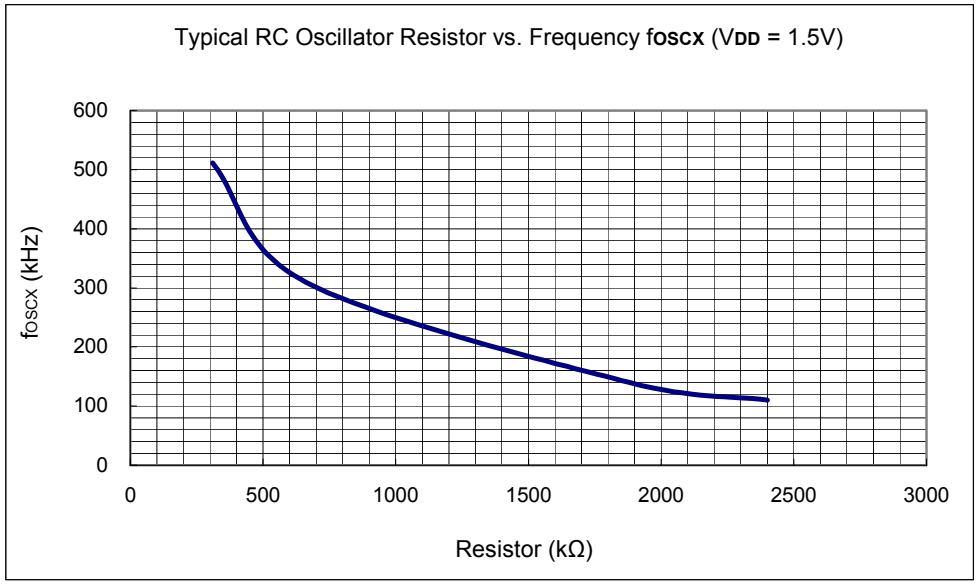
(a) Typical Voltage vs Frequency foscx (300kHz RC) (RC frequency will change as V_{DD} alters) (R_{OSCX} = 660kΩ)



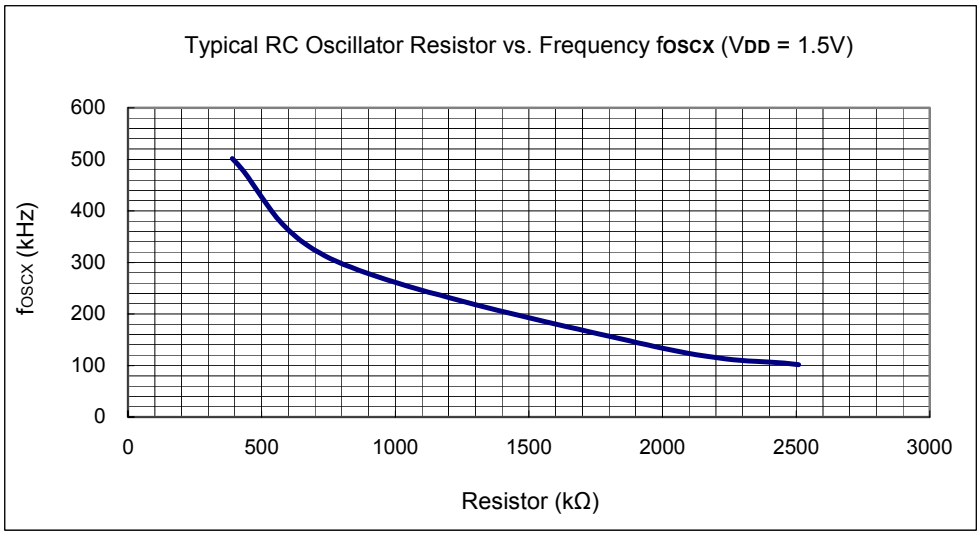
(b) Typical Voltage vs Frequency foscx (300kHz RC) (RC frequency will not change as V_{DD} alters) (R_{OSCX} = 780kΩ)



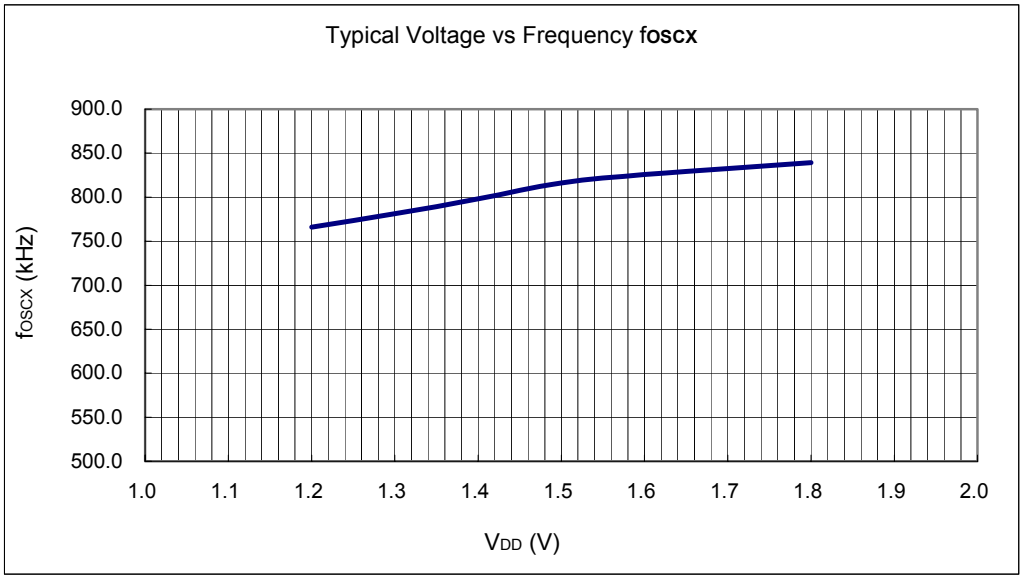
(c) Typical RC Oscillator Resistor vs. Frequency foscx (300kHz RC) (V_{DD} = 1.5V) (RC frequency will change as V_{DD} alters)



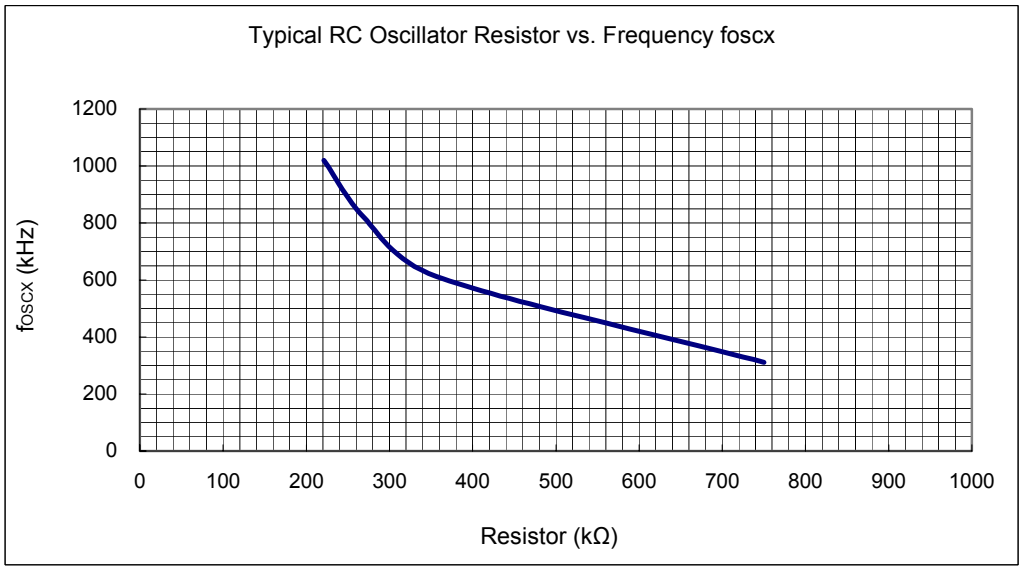
(d) Typical RC Oscillator Resistor vs. Frequency foscx (300kHz RC) (V_{DD} = 1.5V) (RC frequency will not change as V_{DD} alters)



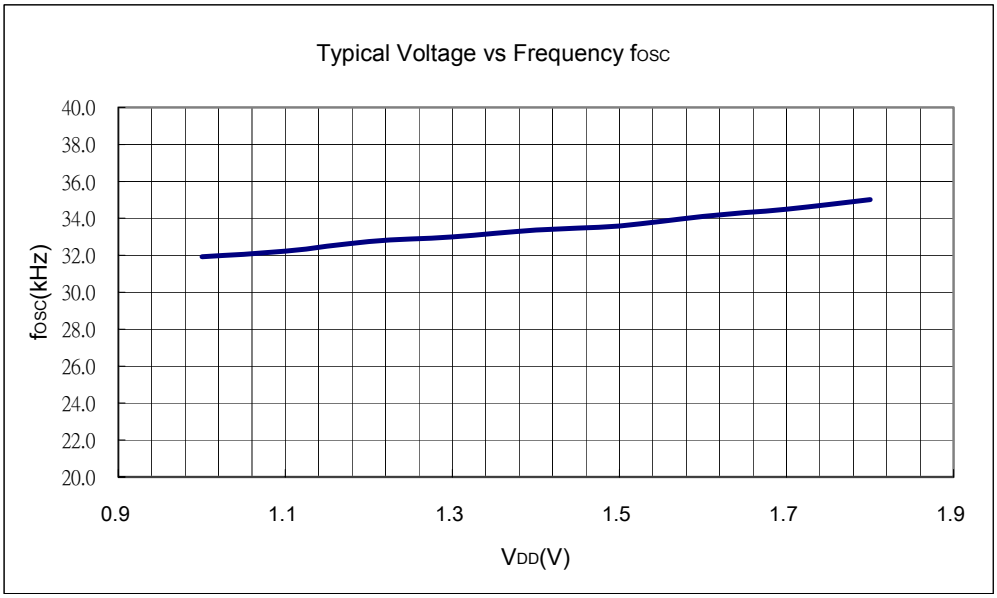
(e) Typical Voltage vs Frequency foscx (800kHz RC) (Roscx = 270kΩ)



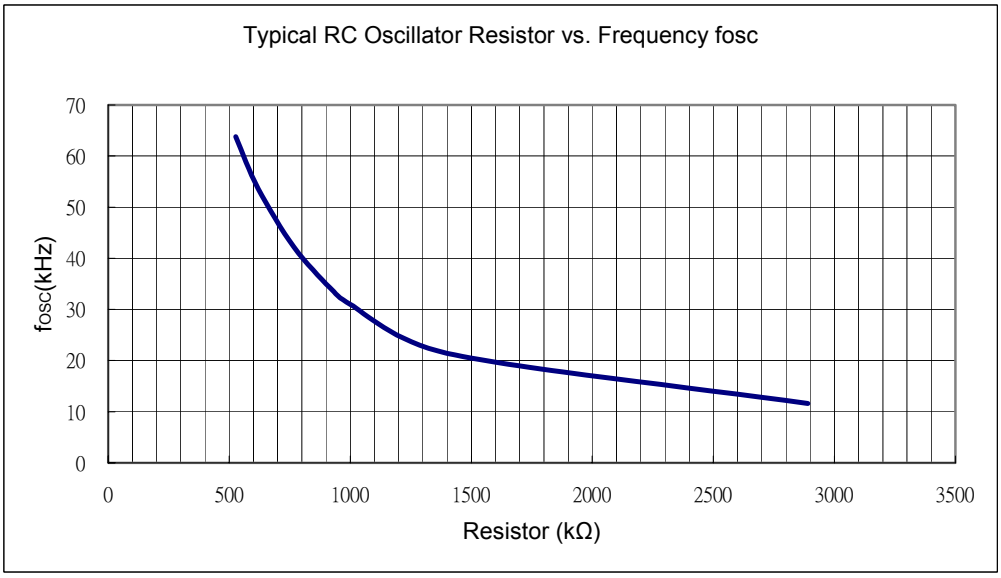
(f) Typical RC Oscillator Resistor vs. Frequency foscx (800kHz RC) (VDD = 1.5V)



(g) Typical Voltage vs Frequency fosc (32kHz RC) (Rosc = 890kΩ)

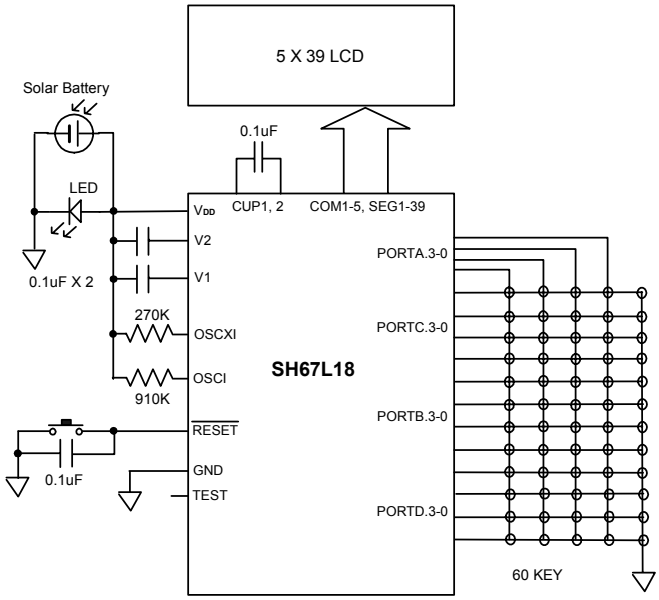


(h) Typical RC Oscillator Resistor vs. Frequency fosc (32kHz RC) (VDD = 1.5V)

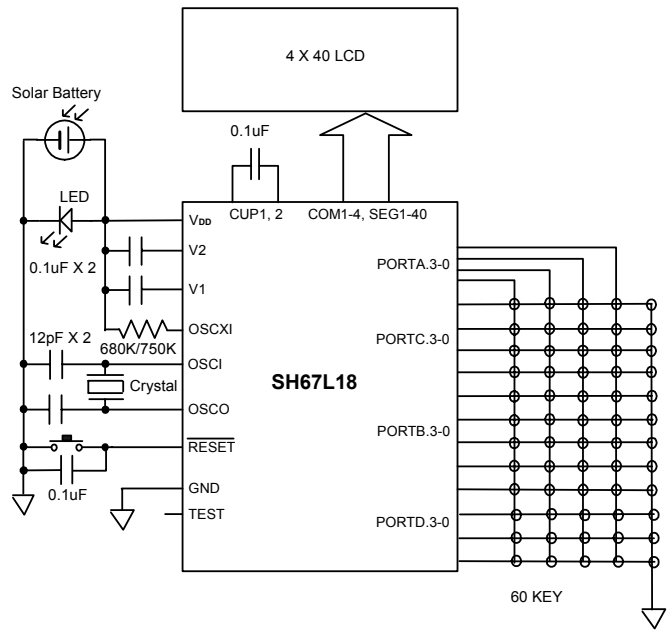


Application Circuits (for reference only)

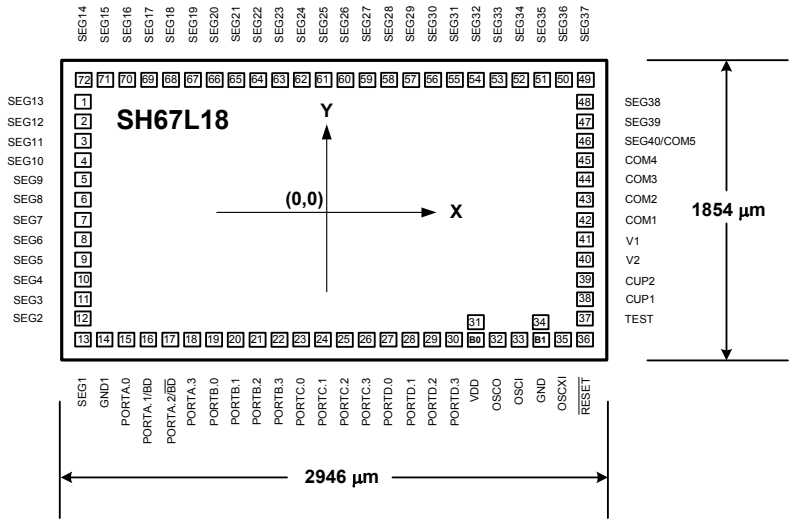
AP1: (1) Operating Voltage: 1.5V
(2) Oscillator: OSC RC: 32kHz, OSCX RC: 800kHz
(3) LCD: 4.5V, 1/5 duty, 1/3 bias
(4) PORTA - D: I/O



AP2: (1) Operating Voltage: 1.5V
(2) Oscillator: OSC 32.768KHz Crystal, OSCX RC: 300kHz
(3) LCD: 4.5V, 1/4 duty, 1/3 bias
(4) PORTA - D: I/O



Bonding Diagram



*** Substratum connects to ground.**

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG13	-1340.00	645.00	21	PORTB.0	-400.00	-795.00
2	SEG12	-1340.00	515.00	22	PORTB.1	-290.00	-795.00
3	SEG11	-1340.00	395.00	23	PORTC.0	-180.00	-795.00
4	SEG10	-1340.00	275.00	24	PORTC.1	-70.00	-795.00
5	SEG9	-1340.00	165.00	25	PORTC.2	40.00	-795.00
6	SEG8	-1340.00	55.00	26	PORTC.3	150.00	-795.00
7	SEG7	-1340.00	-55.00	27	PORTD.0	260.00	-795.00
8	SEG6	-1340.00	-165.00	28	PORTD.1	370.00	-795.00
9	SEG5	-1340.00	-275.00	29	PORTD.2	480.00	-795.00
10	SEG4	-1340.00	-395.00	30	PORTD.3	590.00	-795.00
11	SEG3	-1340.00	-515.00	-	B0	725.00	-798.00
12	SEG2	-1340.00	-645.00	31	V_{DD}	725.00	-701.00
13	SEG1	-1340.00	-775.00	32	OSCO	850.00	-795.00
14	GND	-1200.00	-795.00	33	OSCI	960.00	-795.00
15	PORTA.0	-1060.00	-795.00	-	B1	1085.00	-798.00
16	PORTA.1	-950.00	-795.00	34	GND	1085.00	-701.00
17	PORTA.2	-840.00	-795.00	35	OSCXI	1220.00	-795.00
18	PORTA.3	-730.00	-795.00	36	$\overline{\text{RESET}}$	1340.00	-775.00
19	PORTB.0	-620.00	-795.00	37	TEST	1340.00	-645.00
20	PORTB.1	-510.00	-795.00	38	CUP1	1340.00	-515.00

Pad Location (continued) unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
39	CUP2	1340.00	-395.00	56	SEG30	495.00	795.00
40	V2	1340.00	-275.00	57	SEG29	385.00	795.00
41	V1	1340.00	-165.00	58	SEG28	275.00	795.00
42	COM1	1340.00	-55.00	59	SEG27	165.00	795.00
43	COM2	1340.00	55.00	60	SEG26	55.00	795.00
44	COM3	1340.00	165.00	61	SEG25	-55.00	795.00
45	COM4	1340.00	275.00	62	SEG24	-165.00	795.00
46	SEG40	1340.00	395.00	63	SEG23	-275.00	795.00
47	SEG39	1340.00	515.00	64	SEG22	-385.00	795.00
48	SEG38	1340.00	645.00	65	SEG21	-495.00	795.00
49	SEG37	1340.00	795.00	66	SEG20	-605.00	795.00
50	SEG36	1200.00	795.00	67	SEG19	-715.00	795.00
51	SEG35	1065.00	795.00	68	SEG18	-825.00	795.00
52	SEG34	945.00	795.00	69	SEG17	-945.00	795.00
53	SEG33	825.00	795.00	70	SEG16	-1065.00	795.00
54	SEG32	715.00	795.00	71	SEG15	-1200.00	795.00
55	SEG31	605.00	795.00	72	SEG14	-1340.00	795.00

Ordering Information

Part No.	Package
SH67L18H	Chip form

Data Sheet Revision History

Version	Content	Date
2.0	Revised the external resistor value of RC oscillators in the application circuit.	Aug. 2007
1.0	Original	Apr. 2007