



SH67P53/K53

OTP/Mask 4-Bit micro-controller with LCD Driver

Features

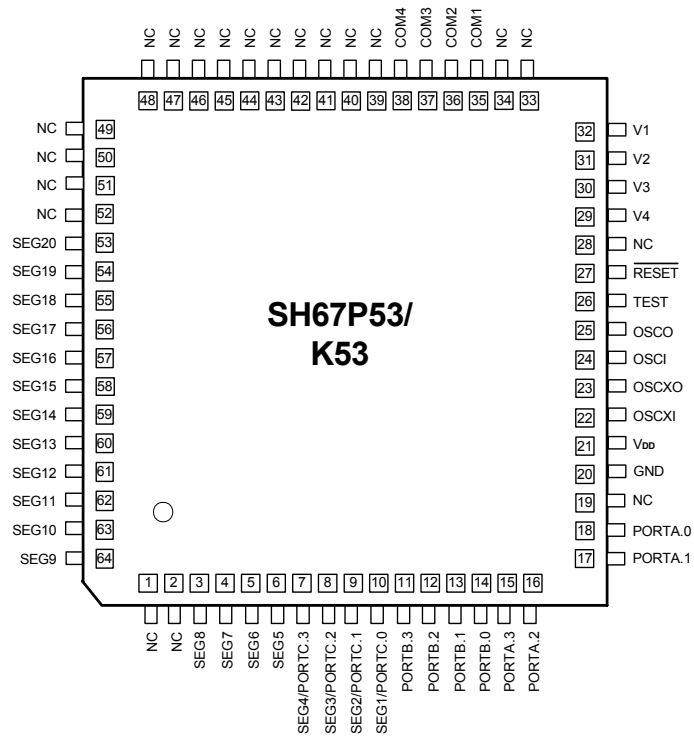
- SH6610D-Based Single-Chip 4-Bit Micro-controller with LCD Driver
- OTP ROM: 4K X 16 bits (SH67P53)
- MASK ROM: 4K X 16 bits (SH67K53)
- RAM: 196 X 4bits
 - 32 System Control Register
 - 144 Data RAM
 - 20 LCD RAM
- Operation Voltage:
 - System oscillator = 30kHz - 4MHz, $V_{DD} = 2.4V - 6.0V$
 - System oscillator = 30kHz - 8MHz, $V_{DD} = 4.5V - 6.0V$
- 12 CMOS Bi-directional I/O Pins
- Built-in Pull-high/Pull-low Resistor for PORTA-PORTC
- 8-Level Stack (Including interrupts)
- One 8-Bit Auto Re-loaded Timer/Counter
- Warm-Up Timer
- Powerful Interrupt Sources:
 - External Interrupt: (Rising/Falling edge)
 - Timer0 Interrupt
 - Base Timer Interrupt
 - External Interrupt: PORTB & PORTC (Rising/Falling Edge)
- LCD Driver:
 - 20 SEG X 4 COM (1/4 duty 1/3 bias)
- LCD can be used as Scan Output
- LCD shared as LED Matrix
- Built-in Watchdog Timer
- Two-Level low voltage reset (LVR) (Code Option)
- Oscillator
 - OSC: (Code Option)
 - Crystal Oscillator: 32.768kHz
 - RC Oscillator: 262kHz
OSCX: (system register)
 - Ceramic Resonator/Crystal Oscillator: 400kHz - 8MHz
 - RC oscillator: 2MHz - 8MHz
- Instruction cycle time (4/fosc)
- Built-in Read ROM Data Table (RDT)
- Two low power operation modes: HALT and STOP
- OTP type & Code protection (SH67P53)
- MASK type (SH67K53)
- 64-pin LQFP and CHIP FORM Package

General Description

SH67P53/67K53 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, RAM, ROM, timer, LCD driver, I/O ports, watchdog timer, low voltage reset, LED Matrix driver. The SH67P53/67K53 is suitable for home appliance application.

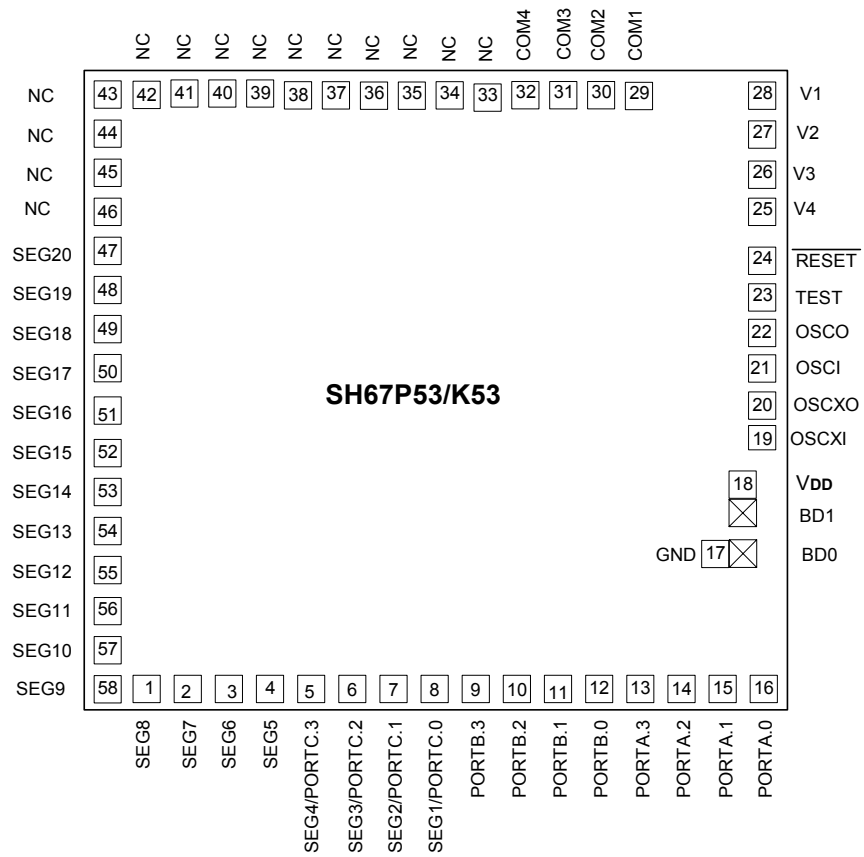


PIN Configuration



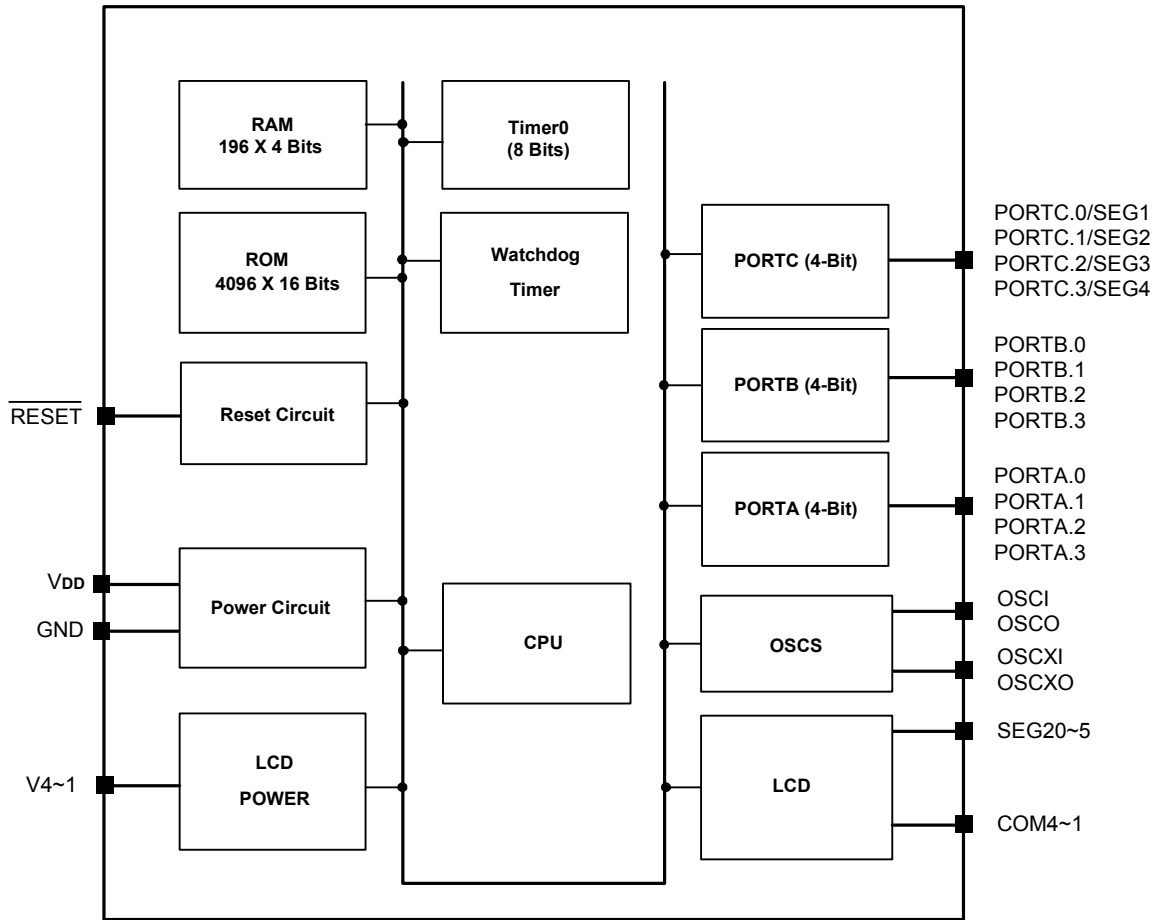


Pad Configuration





Block Diagram





Pin Description

Pad NO	Pin NO	Pin Name	I/O	Description
5-8	7-10	PORTC.3~0	I/O	Bit programmable I/O, shared with SEG4 – 1 Vector Interrupt (Active rising or falling edge by system register setup)
9-12	11-14	PORTB.3~0	I/O	Bit programmable I/O Vector Interrupt (Active rising or falling edge by system register setup)
13-16	15-18	PORTA.3~0	I/O	Bit programmable I/O
17	20	GND	P	Ground pin
-	-	BD0	I	Bonding option 0
18	21	VDD	P	Power supply pin
-	-	BD1	I	Bonding option 1
19	22	OSCXI	I	OSC input pin, connected to a crystal, ceramic or external resistor
20	23	OSCXO	O	Oscillator X output
21	24	OSCI	I	Oscillator input
22	25	OSCO	O	Oscillator output
23	26	TEST	I	Test pin must be connected to GND
24	27	RESET	I	Reset input (active low, Schmitt trigger input)
25-28	29-32	V4~1	I	Connected with external LCD divided resistor
32-29	38-35	COM4~1	O	Common signal output for LCD display
47-58	53-64	SEG20~9	O	Segment signal output for LCD display, Shared with scan output
1-4	3-6	SEG8~5	O	Segment signal output for LCD display
-	-	NC	-	No connect for user

Which, I: input; O: output; P: Power; Z: High impedance

OTP Programming Pin Description* (OTP program mode)

Pad NO	Pin NO	Pin Name	I/O	Shared by	Description
18	21	VDD	P	VDD	Programming Power supply (+5.5V)
24	27	VPP	P	RESET	Programming high voltage Power supply (+11.0V)
17	20	GND	P	GND	Ground pin
21	24	SCK	I	OSCI	Programming Clock input pin
16	18	SDA	I/O	PORTA.0	Programming Data pin

*: OTP program mode is only available for SH67P53.



Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0). The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K. The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or

2. ROM

The ROM can address 4096 X 16 bits of program area from \$000 to \$FFF.

2.1. Vector Address Area (\$000 to \$004)

The program is sequentially executed. There is an area address \$000 through \$004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
\$000	JMP*	Jump to RESET service routine
\$001	JMP*	Jump to External interrupt service routine
\$002	JMP*	Jump to Timer0 service routine
\$003	JMP*	Jump to Base Timer service routine
\$004	JMP*	Jump to PORT interrupt service routine

*JMP instruction can be replaced by any instruction.

data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2³) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range is 000H-3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.



3. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

3.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: \$000 - \$01F

Data memory: \$020 - \$0AF

LCD RAM space: \$300 - \$313

Segment scan output RAM: \$358 - \$363

3.2. Configuration of System Register:

System Register \$000-\$01F RAM Map:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
\$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
\$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register
\$02	T0M.3	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register Bit3: Timer0 Auto-Reload enable/disable control register
\$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
\$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter low nibble register
\$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter high nibble register
\$06	-	-	-	-	-	Reserved
\$07	-	LCDON	RLCD1	RLCD0	R/W	Bit1-0: LCD divider resistors control register Bit2: LCD on/off control register
\$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
\$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
\$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
\$0B	-	-	-	-	-	Reserved
\$0C	-	-	BD 1	BD 0	R -	Bit1-0: Bonding option register Bit2&3 must be set to "0" by User's program and always kept low
\$0D	LVD	O/S2	O/S1	O/S0	R/W	Bit0: PORTC as LCD SEG 4~1 control register Bit1 must be set to "1" by User's program and always kept high Bit2: LCD SEG9-20 as output control register Bit3: LCD Voltage degrade register
\$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
\$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
\$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
\$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
\$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
\$13	PULLEN	PH/PL	PBCFR	EINFR	R/W	Bit0: External interrupt (PORTA.0) rising/falling edge control register Bit1: PORTB, PORTC interrupt rising/falling edge control register Bit2: Port pull-high/low set register Bit3: Port pull-high/low enable control register
\$14	OXS	-	OXM	OXON	R/W	Bit0: OSCX oscillator on/off control register Bit1: CPU clock select control register Bit3: OSCX type select control register



The Configuration of System Register (continue)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
\$15	LPS1	LPS0	-	-	R/W	Bit1-0: must be set to “1” by User’s program and always kept high Bit3-2: LCD frequency control register
\$16	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
\$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
\$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
\$19	-	-	-	-	-	Reserved
\$1A	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
\$1B	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
\$1C	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
\$1D	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register
\$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
\$1F	-	-	-	-	-	Reserved



4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset/Pin Reset /Low Voltage Reset	WDT Reset
\$00	IEX	IET0	IEBT	IEP	0000	0000
\$01	IRQX	IRQT0	IRQBT	IRQP	0000	0000
\$02	T0M.3	T0M.2	T0M.1	T0M.0	0000	uuuu
\$03	BTM.3	BTM.2	BTM.1	BTM.0	0000	uuuu
\$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
\$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
\$06	-	-	-	-	-	-
\$07	-	LCDON	RLCD1	RLCD0	-000	-uuu
\$08	PA.3	PA.2	PA.1	PA.0	0000	0000
\$09	PB.3	PB.2	PB.1	PB.0	0000	0000
\$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
\$0B	-	-	-	-	0000	0000
\$0C	-	-	BD 1	BD 0	00xx	uuxx
\$0D	LVD	O/S2	O/S1	O/S0	0000	uuuu
\$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
\$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
\$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
\$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
\$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
\$13	PULLEN	PH/PL	PBCFR	EINFR	0100	0uuu
\$14	OXS	-	OXM	OXON	0-00	u-0u
\$15	LPS1	LPS0	-	-	0000	uuuu
\$16	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
\$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
\$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
\$19	-	-	-	-	0000	0000
\$1A	RDT.3	RDT.2	RDT.1	RDT.0	0000	uuuu
\$1B	RDT.7	RDT.6	RDT.5	RDT.4	0000	uuuu
\$1C	RDT.11	RDT.10	RDT.9	RDT.8	0000	uuuu
\$1D	RDT.15	RDT.14	RDT.13	RDT.12	0000	uuuu
\$1E	WDF	WDT.2	WDT.1	WDT.0	0000	1000
\$1F	-	-	-	-	-	-

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States:

Others	After any Reset
Program Counter (PC)	\$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined



5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4

5.1 Instruction cycle time:

- (1) 4/32.768kHz (≈122μs) for 32.768kHz oscillator.
- (2) 4/455kHz (≈ 8.79μs) for 455kHz oscillator.
- (3) 4/4MHz (= 1μs) for 4MHz oscillator.
- (4) 4/8MHz (= 0.5μs) for 8MHz oscillator.

5.2 Circuit Configuration

SH67P53/67K53 has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ. 32.768kHz) or RC (Typ.262kHz) determined by the Code Option. This is designed for low frequency operation. OSCX also has two types: ceramic/crystal (Typ.455kHz) or RC (2MHz to 8MHz) to be determined by the software option. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC clock is automatically selected as the system clock input source.

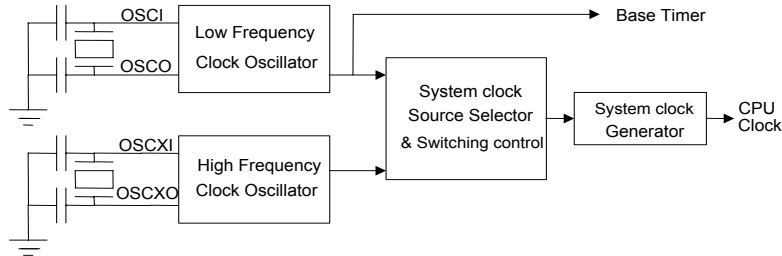


Figure 1. Oscillator Block Diagram

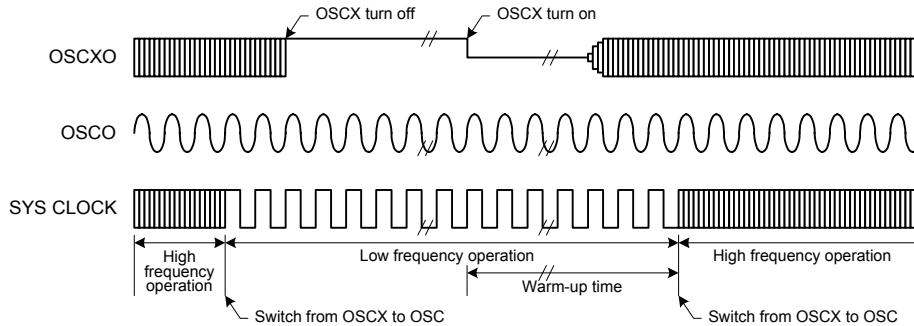


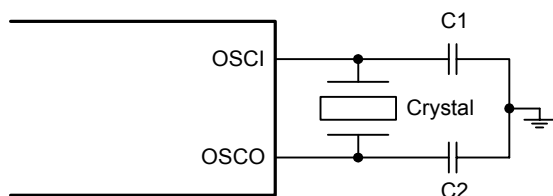
Figure 2. Timing of system Clock Switching



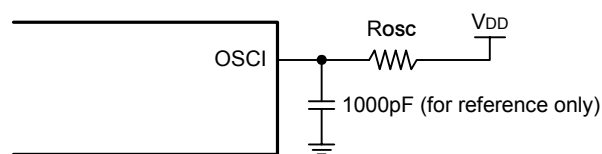
5.3 OSC Oscillator

The OSC generates the basic clock pulses that provide the CPU and peripherals (Base Timer, LCD) with an operating clock.

(1) OSC Crystal oscillator



(2) OSC RC oscillator



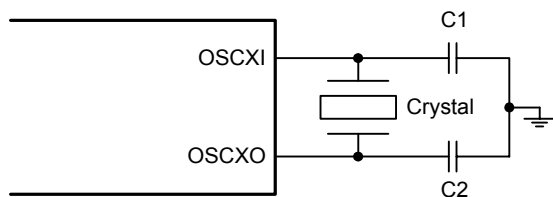
External RC

5.4. OSCX Oscillator

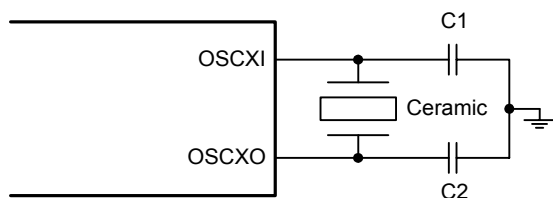
OSCX has two clock oscillators. The software options select the Ceramic/Crystal or RC as the CPU's sub clock.

If the OSCX is not used, it must be masked to be Ceramic resonator and the OSCXI must be connected to GND.

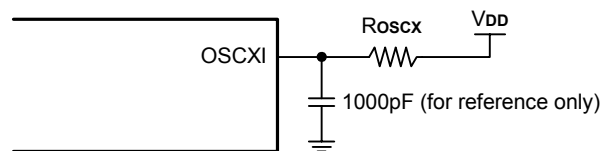
(1) OSCX Crystal oscillator



(2) OSCX Ceramic resonator



(3) OSCX RC oscillator



External RC

**5.5. Control of Oscillator**

The oscillator control register configuration is shown as follow.

Address	Bit3	Bit2	Bit1	Bit0
\$14	OXS	-	OXM	OXON

OXON: OSCX oscillation on/off.

0: Turn-off OSCX oscillation

1: Turn-on OSCX oscillation

OXM: switching system oscillator.

0: select OSC as system oscillator

1: select OSCX as system oscillator

OXS: OSCX oscillator type selection

0: OSCX set as Ceramic Resonator/Crystal Oscillator

1: OSCX set as RC oscillator

5.6. Programming Notes

It takes at least 5 ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When the CPU system clock switching from OSC to OSCX, the user has to wait at least 5ms till the OSCX oscillation is activated. In addition, the start time varies with respect to oscillator characteristics and the conditions. Therefore the waiting time depends on the applications. When switching from OSCX to OSC, and turning off OSCX in one instruction, the OSCX turns off control would be delayed for one instruction. If switching from OSCX to OSC and turning off OSCX in one instruction, the OSCX turn off control will be delayed for one instruction cycle automatically to prevent CPU operation error.

5.7 Capacitor selection for oscillator

Ceramic Resonators			Crystal Oscillator		
Frequency	C1	C2	Frequency	C1	C2
455kHz	47 - 100pF	47 - 100pF	32.768kHz	5 - 12.5pF	5 - 12.5pF
4MHz	20 - 30pF	20 - 30pF	4MHz	8 - 15pF	8 - 15pF

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit <http://www.sinowealth.com> for more recommended manufactures



6. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

6.1. Functions of the LVR Circuit

The LVR function is selected by Code Option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates an internal reset signal when $V_{DD} \leq V_{LVR}$
- Cancels the internal reset signal when $V_{DD} > V_{LVR}$

Here, V_{LVR} which is LVR detect voltage has two level select by Code Option:

7. I/O Ports

The MCU provides 12 bi-directional I/O pins. The PORT data is put in register \$08 - \$0A. The PORT control register (\$16 - \$18) controls the PORT as input or output. Each I/O port has an internal pull-high/pull-low resistor, which is controlled by PULLEN, PH/PL of \$13 and data of the port, when the PORT is used as input.

Port I/O mapping address is shown as follows:

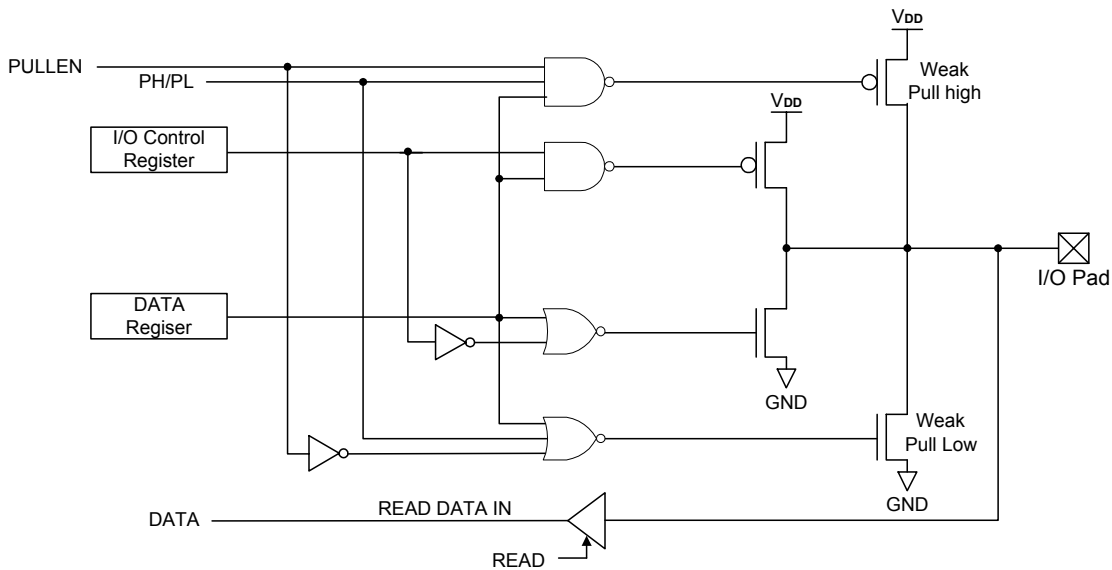
Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
\$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
\$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
\$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
\$16	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
\$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
\$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register

PA (/B/C)CR.n, (n = 0, 1, 2, 3)

0: Set I/O as an input direction. (Power on initial)

1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin





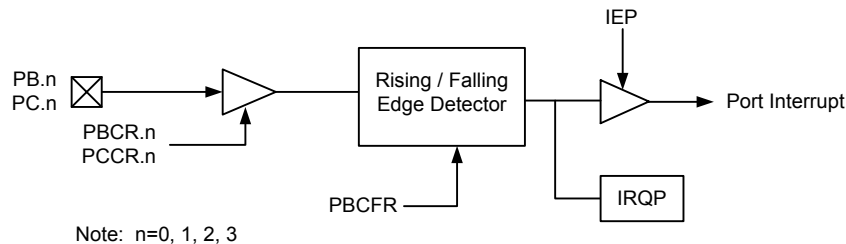
System Register \$13

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
\$13	PULLEN	PH/PL	PBCFR	EINFR	R/W	Bit0: External interrupt (PORTA.0) rising/falling edge set Bit1: PORTB, PORTC interrupt rising/failing edge set Bit2: Port pull-high/low set Bit3: Port pull-high/low enable control
	1	X	X	X	R/W	Port Pull-high/Pull-low enable
	0	X	X	X	R/W	Port Pull-high/Pull-low disable
	X	1	X	X	R/W	Port Pull-high resistor ON
	X	0	X	X	R/W	Port Pull-low resistor ON
	X	X	1	X	R/W	PBC Rising Edge interrupt
	X	X	0	X	R/W	PBC Falling Edge interrupt
	X	X	X	1	R/W	External Rising Edge interrupt
	X	X	X	0	R/W	External Falling Edge interrupt

To turn on the pull high resistor, user must set PULLEN to 1, set PH/PL to 1, and write 1 to the port data register.
To turn on the pull low resistor, user must set PULLEN to 1, set PH/PL to 0, and write 0 to the port data register.

PORTB, PORTC Interrupt

The PORTB and PORTC are used as the port interrupt sources. Following is the port interrupt function block-diagram.



Note: n=0, 1, 2, 3

Port interrupt (PBC INT) PROGRAMMING NOTES:

- If user wants to generate an interrupt when a rising edge from GND to V_{DD} emerges in the port, the following must be executed.
 1. Set the port as input port, fill port data register with “0” and avoid port floating.
 2. Pull-low the port (Use external pull-low resistance or set PULLEN to “1” and set PH/PL to “0”).
 3. Set Rising Edge register. (Set PBCFR to “1” in PBC INT application.)
 And further rising edge transition would not be able to make interrupt request until all of the pins return to GND in PBC INT application.

- If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.
 1. Set the port as input port, fill port data register with “1” and avoid port floating.
 2. Pull-high the port (Use external pull-high resistance or set PULLEN to “1” and set PH/PL to “1”).
 3. Set Falling Edge register. (Set PBCFR to “0” in PBC INT application.)
 And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD} in PBC INT application.

When PORTC is used as segment, user can generate interrupt only on PORTB.

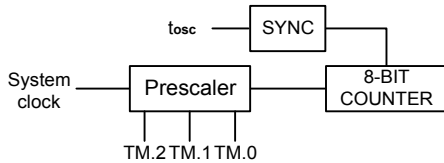


8. Timer0

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from \$FF to \$00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

8.1 Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TLOL, TLOH) and an 8-bit read-only timer counter (TCOL, TCOH). Each of them has low-order digits and high-order digits. Writing data into the timer load register (TLOL, TLOH) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded

with the contents of the load register when the high order digit is written or counter counts overflow from \$FF to \$00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

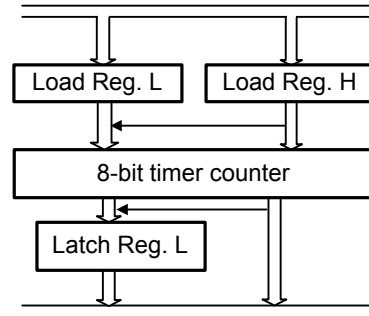
Please follow these steps:

Write Operation:

- Low nibble first
- High nibble to update the counter

Read Operation:

- High nibble first
- Low nibble followed.



8.2. Timer0 Mode Register

The timer can be programmed in several different prescalers by setting Timer Mode register (TOM).

The clock source pre-scale by the 8-level counter first, then generate the output plus to timer counter. The Timer Mode registers (TOM) are 3-bit registers used for the timer control as shown in Table 1.

Table 1 Timer0 Mode Register (\$02)

TOM.2	TOM.1	TOM.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^9$	System clock
0	1	0	$/2^7$	System clock
0	1	1	$/2^5$	System clock
1	0	0	$/2^3$	System clock
1	0	1	$/2^2$	System clock
1	1	0	$/2^1$	System clock
1	1	1	$/2^0$	PORTA.0 (Falling Edge)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
\$02	TOM.3	TOM.2	TOM.1	TOM.0	R/W	Bit2-0: Timer0 Mode register Bit3: Timer0 Auto-Reload enable/disable control register
	1	X	X	X	R/W	Timer0 Auto-Reload enable
	0	X	X	X	R/W	Timer0 Auto-Reload disable



9. Base Timer

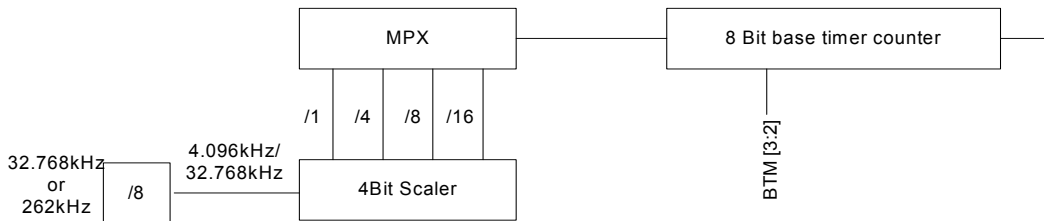
The MCU has a base timer which's clock source is OSC (Low frequency oscillation: Crystal 32.768kHz or RC 262kHz). After MCU is reset, it counts at every clock-input signal. When it counts to \$FF, right after next clock input, counter counts to \$00 and generates an overflow. This causes the interrupt of base timer interrupt request flag to 1. Therefore, the base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal output.

The timer accepts 4.096kHz or 32.768kHz clock, and base timer generates an accurate timing interrupt.

This clock-input source is selected by BTM register.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
\$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
	1	0	X	X	R/W	Enable the base timer
	Other states		X	X	R/W	Disable the base timer, clear base timer counters and keep them as \$00

BTM.1	BTM.0	Prescaler Ratio	Clock Source
0	0	/1	4.096kHz or 32.768kHz
0	1	/4	4.096kHz or 32.768kHz
1	0	/8	4.096kHz or 32.768kHz
1	1	/16	4.096kHz or 32.768kHz



**10. Watchdog Timer (WDT)**

Watchdog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that the WDT will always run even in the STOP mode (if it is enabled). The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits (\$1E bit2 - bit0) are used to select different overflow frequency. The watchdog timer overflow flag (\$1E bit3) will be automatically set to "1" by hardware when the watchdog timer overflows. By reading or writing the system register \$1E, the watchdog timer should re-count before the overflow happens.

System Register \$1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2 - 0: Watchdog timer control Bit3: Watchdog timer overflow flag
	X	0	0	0	R/W	Watchdog timer-out period = 4096ms
	X	0	0	1	R/W	Watchdog timer-out period = 1024ms
	X	0	1	0	R/W	Watchdog timer-out period = 256ms
	X	0	1	1	R/W	Watchdog timer-out period = 128ms
	X	1	0	0	R/W	Watchdog timer-out period = 64ms
	X	1	0	1	R/W	Watchdog timer-out period = 16ms
	X	1	1	0	R/W	Watchdog timer-out period = 4ms
	X	1	1	1	R/W	Watchdog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer overflow period is valid for $V_{DD} = 5V$.



11. LCD Driver

The LCD driver contains a controller, a voltage generator, 4 common driver pins and 20 segment driver pins. There is only one driving programmable mode: 1/4 duty & 1/3bias.

The controller consists of display data RAM and a duty generator.

The LCD SEG9 ~ 20 can also be used as output port which is selected by the bit 2 of the system register \$0D. When SEG9 ~ 20 are used as output ports, one should write data to bit 0 of the same addresses (\$358 - \$363). The LCD SEG 1 - 4 can also be used as I/O port (PORTC), which is selected by bit 0,1 of the system register \$0D. The LCD SEG/COM can also be shared to LED application. LCD RAM could be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When LCD off, both common and segment output low.

11.1. LCD Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$07	-	LCDON	RLCD1	RLCD0	R/W	Bit2: LCD display ON control register
	-	0	X	X		LCD OFF
	-	1	X	X		LCD ON

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$0D	LVD	O/S2	O/S1	O/S0	R/W	Bit1, 0: PORTC or LCD segment control register Bit2: Output ports or LCD segment control register
	X	X	1	0		PORTC as I/O ports.
	X	X	1	1		PORTC as LCD SEG 1 ~ 4
	X	0	X	X		SEG9-SEG20 as LCD segment
	X	1	X	X		SEG9-SEG20 as scan output ports

O/S1, O/S0: Set PORTC as LCD segment or I/O PORT, After each reset it must be set to "1,0" or "1,1", otherwise the current will be abnormal.

When LVD is set to 1 and the divider resistors is 270kΩ, the LCD voltage power will be degraded to about 90% of VDD. It is designed to reduce extra LCD contrast control output pins. Then the LCD can be fitted automatically for different voltage levels by the software.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$15	LPS1	LPS0	-	-	R/W	Bit3,2: LCD frame frequency control register

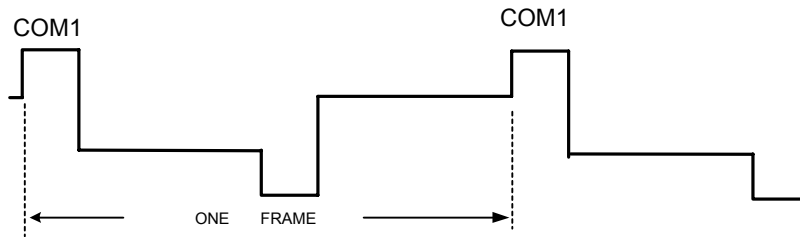
NOTE: Bti0&1 must be set to "1" by User's program and always kept high.



LPS1, LPS0: LCD frame frequency control. LCD clock is divided from OSC, so LCD frame frequency will change in proportion to the variation of OSC frequency in spite of OSC type.

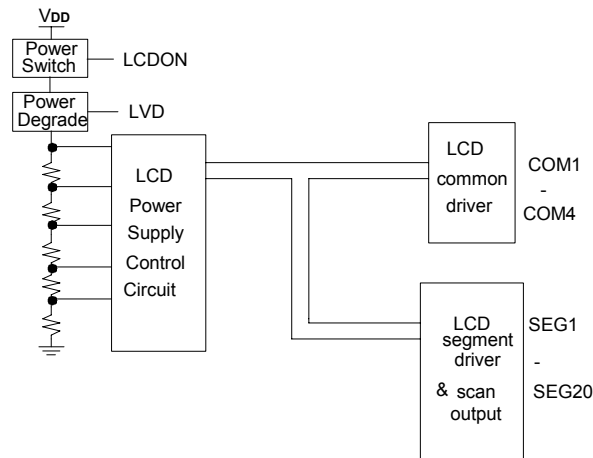
FRAME Frequency (OSC = 32.768kHz)	LPS1, LPS0			
	0, 0	0, 1	1, 0	1, 1
IN 1/4 DUTY MODE	32Hz	16Hz	8Hz	4Hz

FRAME Frequency (OSC = 262kHz)	LPS1, LPS0			
	0, 0	0, 1	1, 0	1, 1
IN 1/4 DUTY MODE	256Hz	128Hz	64Hz	32Hz



LCD output frame

11.2. LCD Power



Built in special LCD power control for LCD power modulation.

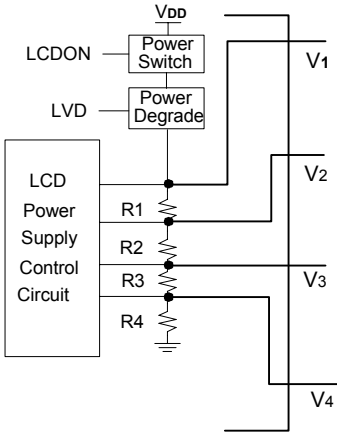


Select Different Divider Resistance

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$07	-	LCDON	RLCD1	RLCD0	R/W	Bit1, 0: LCD bias resistor control register Bit2: LCD on/off control register
	-	X	0	0		R1 = R2 = R3 = R4 = 270k(Default)
	-	X	0	1		R1 = R2 = R3 = R4 = 90k
	-	X	1	0		R1 = R2 = R3 = R4 = 30k
	-	X	1	1		R1 = R2 = R3 = R4 = 10k

When large LCD panel is used, user can set the value of \$07 to increase the bias current for better LCD performance. But it will cost more power, when smaller divider resistances are used.

When the CPU is in STOP mode, the common and segment is pulled low. It can easily be woken up by a keyboard scan (Port interrupt).





11.3. Configuration of LCD RAM Area

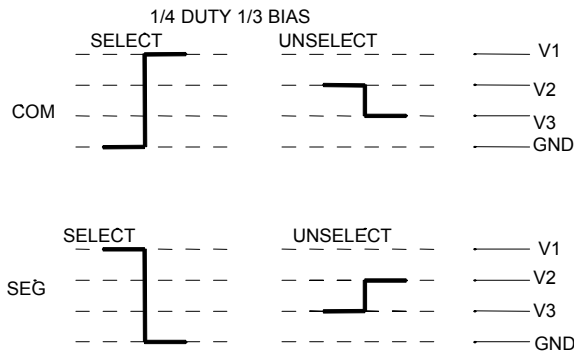
LCD 1/4 Duty, 1/3 Bias (COM1 - 4, SEG1 - 20)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
\$300	SEG1	SEG1	SEG1	SEG1	\$30A	SEG11	SEG11	SEG11	SEG11
\$301	SEG2	SEG2	SEG2	SEG2	\$30B	SEG12	SEG12	SEG12	SEG12
\$302	SEG3	SEG3	SEG3	SEG3	\$30C	SEG13	SEG13	SEG13	SEG13
\$303	SEG4	SEG4	SEG4	SEG4	\$30D	SEG14	SEG14	SEG14	SEG14
\$304	SEG5	SEG5	SEG5	SEG5	\$30E	SEG15	SEG15	SEG15	SEG15
\$305	SEG6	SEG6	SEG6	SEG6	\$30F	SEG16	SEG16	SEG16	SEG16
\$306	SEG7	SEG7	SEG7	SEG7	\$310	SEG17	SEG17	SEG17	SEG17
\$307	SEG8	SEG8	SEG8	SEG8	\$311	SEG18	SEG18	SEG18	SEG18
\$308	SEG9	SEG9	SEG9	SEG9	\$312	SEG19	SEG19	SEG19	SEG19
\$309	SEG10	SEG10	SEG10	SEG10	\$313	SEG20	SEG20	SEG20	SEG20

SEG9 - 20 is used as scan output port

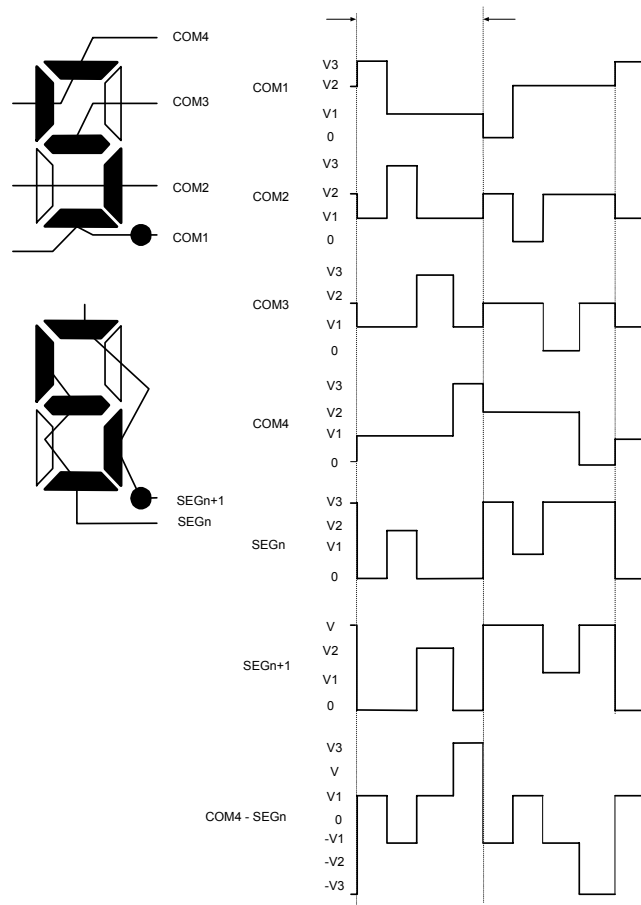
Address	Bit0	Address	Bit0
\$358	SEG9	\$35E	SEG15
\$359	SEG10	\$35F	SEG16
\$35A	SEG11	\$360	SEG17
\$35B	SEG12	\$361	SEG18
\$35C	SEG13	\$362	SEG19
\$35D	SEG14	\$363	SEG20

11.4. LCD Waveform





Example 1/4 Duty 1/3 Bias



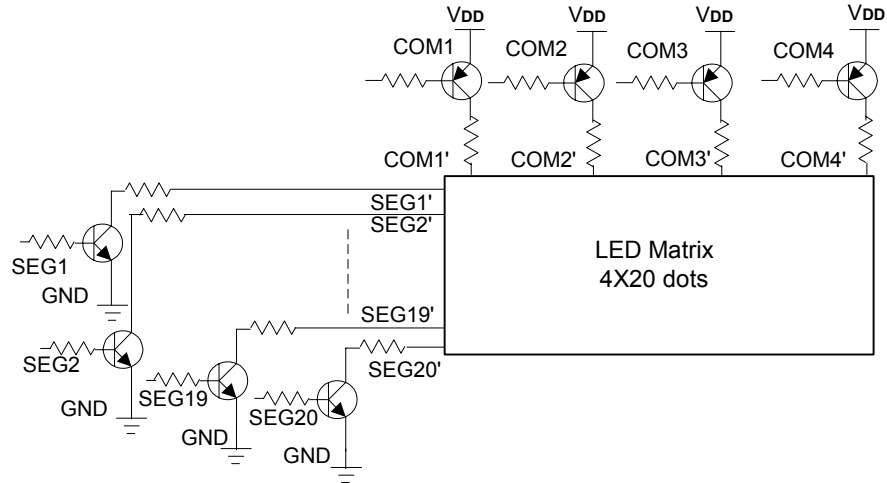


11.5. Shared to LED Application

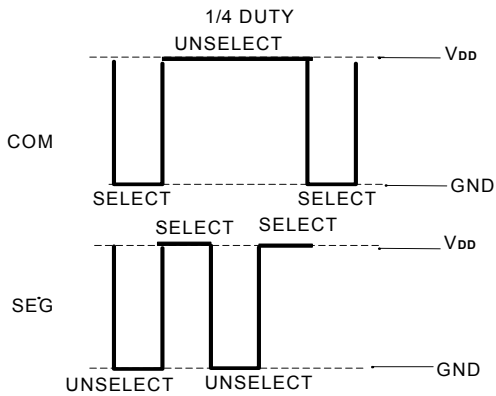
User can use common & segment in the application of LED matrix by Code Option and configuration of LED RAM is the same as LCD RAM.

Notes:

The common & segment cannot driver the LED matrix directly for the cause of weak driving ability. So in the LED Matrix application the driving circuit will be used such as following. Example 1/4 Duty LED Matrix Application Circuit.

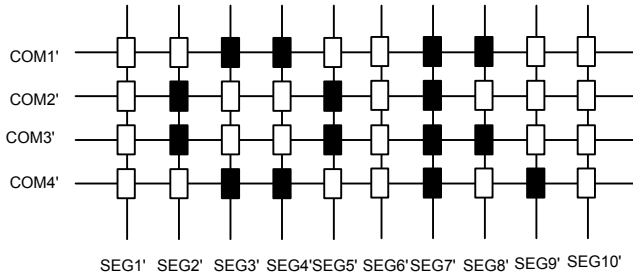
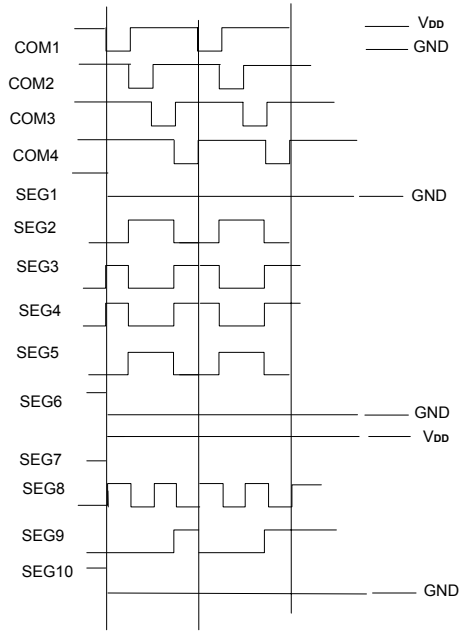


11.6. LED Waveform





Example 1/4 Duty 4X10 Dots



COMx' & SEGx'refer to the driving-amplified output of COMx & SEGx.

12. ROM DATA Read Table (RDT)

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$1A	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
\$1B	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
\$1C	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
\$1D	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 12-bit write-only PC address load register (RDT.11 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should fill 0 to higher 4 bit (bit 12 - 15) first, then write the ROM table address to RDT register (high nibble first then low nibble), after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).



13. Interrupt

Four interrupt sources are available on SH67P53/67K53:

- External interrupt (INT0)
- Timer0 interrupt
- Base timer interrupt
- PORTB - C interrupt (Falling edge)

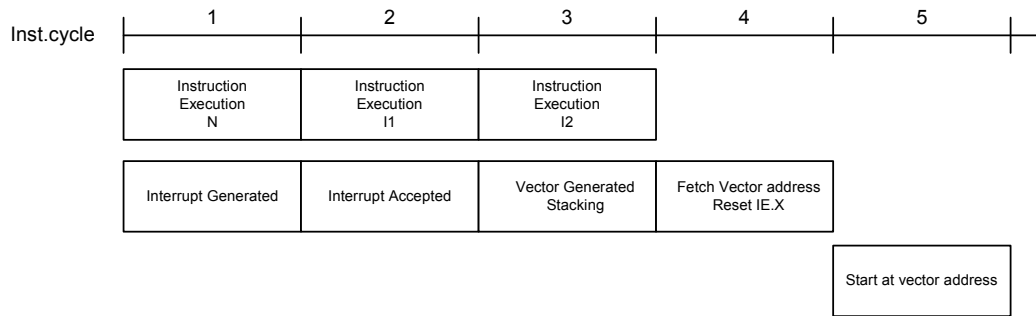
13.1. Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on \$00 and \$01 of the system register. They can be accessed or tested by the program. Those flags are cleared to "0" at initialization by the chip reset.

System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$00	IEX	IET0	IEBT	IEP	R/W	Interrupt enable flags register
\$01	IRQX	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register

When IEx is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to "0" automatically, so when IRQx is 1 and IEx is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

13.2. External Interrupt

When bit3 of system register \$00 (IEX) is set to "1", the external interrupt will be enabled, and a rising (or falling) edge signal on the external interrupt I/O port will generate an external interrupt.

13.3. Timer0 Interrupt

The input clock of Timer0 is based on system clock. The timer overflow from \$FF to \$00 will generate an internal interrupt request (IRQT0 = 1), If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

13.4. Base Timer Interrupt

The input clock of Base Timer is based on OSC clock. The timer overflow from \$FF to \$00 will generate an internal interrupt request (IRQBT = 1), If the interrupt enable flag is enabled (IEBT = 1), a timer interrupt service routine will start. Base Timer interrupt can also be used to wake the CPU from HALT mode.

13.5. Port Falling/Rising Edge Interrupt

Only the digital input port can generate an external interrupt. The analog input cannot generate an interrupt request. When PBCFR.n set to "0", any one of the I/O input pin transitions from VDD to GND would generate an interrupt request. And further falling edge transition would not be able to make interrupt request until all of the pins return to VDD. When PBCFR.n set to "1", any one of the I/O input pin transitions from GND to VDD would generate an interrupt request. And further rising edge transition would not be able to make interrupt request until all of the pins return to GND.



14. HALT and STOP Mode

After the execution of HALT instruction, SH67P53/67K53 will enter HALT mode. In the HALT mode, CPU will stop operating. But peripheral circuit (Timer0, Base Timer, and Watchdog Timer) will keep status.

After the execution of STOP instruction, SH67P53/67K53 will enter STOP mode. The whole chip (including oscillator) will stop operating exclude watchdog timer, if it is enabled.

In HALT mode, SH67P53/67K53 can be waked up if any interrupt occurs.

In STOP mode, SH67P53/67K53 can be waked up if port interrupt occurs or Watchdog timer overflow (when WDT is enabled).

When CPU is waked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to halt/stop is executed.

15. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

A. Power-on Reset, Pin Reset, Wake up from stop mode and LVR Reset:

(1) In RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^7$ (128).

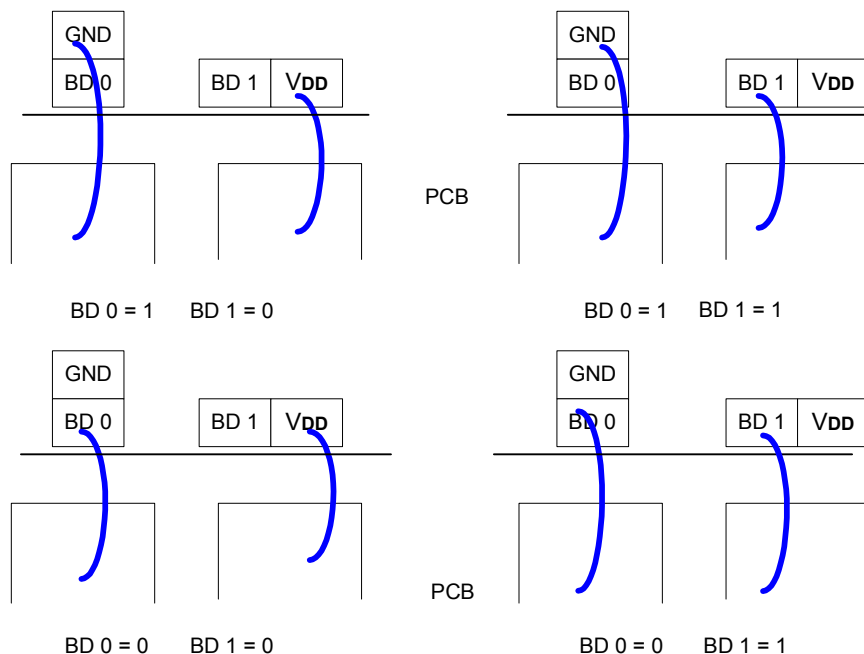
(2) In Ceramic Resonator/Crystal oscillator mode, the warm-up counter prescaler is divided ratio is $1/2^{12}$ (4096).



16. Bonding Option

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
\$0C	-	-	BD 1	BD 0	R	Bit1-0: Bonding option register
	X	X	0	1		Default bonding option
	X	X	1	1		BD1 bond to VDD
	X	X	0	0		BD0 bond to GND
	X	X	1	0		BD0 bond to GND and BD1 bond to VDD



Up to 4 different bonding options are possible for user's needs. The chip's program has 4 different program flows that varies depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.



17. Code Option

- (a) Oscillate type:
 - 0 = 32.768kHz Crystal oscillator
 - 1 = 262kHz RC oscillator
- (b) OSCX range select:
 - 0 = 400kHz - 2MHz
 - 1 = 2MHz-8MHz
- (c) Watchdog timer:
 - 0 = Enable
 - 1 = Disable
- (d) LVR Reset
 - 0 = Disable
 - 1 = Enable
- (e) LVR level
 - 0 = Level1: 4.0V
 - 1 = Level2: 2.5V
- (f) LCD/LED matrix
 - 0 = LCD application
 - 1 = LED matrix application

**Instruction Set**

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction**1.1. Accumulator Type**

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	$AC \leftarrow Mx + AC + CY$	CY
ADCM X (, B)	00000 1bbb xxx xxxx	$AC, Mx \leftarrow Mx + AC + CY$	CY
ADD X (, B)	00001 0bbb xxx xxxx	$AC \leftarrow Mx + AC$	CY
ADDM X (, B)	00001 1bbb xxx xxxx	$AC, Mx \leftarrow Mx + AC$	CY
SBC X (, B)	00010 0bbb xxx xxxx	$AC \leftarrow Mx + -AC + CY$	CY
SBCM X (, B)	00010 1bbb xxx xxxx	$AC, Mx \leftarrow Mx + -AC + CY$	CY
SUB X (, B)	00011 0bbb xxx xxxx	$AC \leftarrow Mx + -AC + 1$	CY
SUBM X (, B)	00011 1bbb xxx xxxx	$AC, Mx \leftarrow Mx + -AC + 1$	CY
EOR X (, B)	00100 0bbb xxx xxxx	$AC \leftarrow Mx \oplus AC$	
EORM X (, B)	00100 1bbb xxx xxxx	$AC, Mx \leftarrow Mx \oplus AC$	
OR X (, B)	00101 0bbb xxx xxxx	$AC \leftarrow Mx AC$	
ORM X (, B)	00101 1bbb xxx xxxx	$AC, Mx \leftarrow Mx AC$	
AND X (, B)	00110 0bbb xxx xxxx	$AC \leftarrow Mx \& AC$	
ANDM X (, B)	00110 1bbb xxx xxxx	$AC, Mx \leftarrow Mx \& AC$	
SHR	11110 0000 000 0000	$0 \rightarrow AC[3], AC[0] \rightarrow CY;$ AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	$AC \leftarrow Mx + I$	CY
ADIM X, I	01001 iiii xxx xxxx	$AC, Mx \leftarrow Mx + I$	CY
SBI X, I	01010 iiii xxx xxxx	$AC \leftarrow Mx + -I + 1$	CY
SBIM X, I	01011 iiii xxx xxxx	$AC, Mx \leftarrow Mx + -I + 1$	CY
EORIM X, I	01100 iiii xxx xxxx	$AC, Mx \leftarrow Mx \oplus I$	
ORIM X, I	01101 iiii xxx xxxx	$AC, Mx \leftarrow Mx I$	
ANDIM X, I	01110 iiii xxx xxxx	$AC, Mx \leftarrow Mx \& I$	

1.3. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	$AC, Mx \leftarrow$ Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	$AC, Mx \leftarrow$ Decimal adjust for sub	CY



2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← llll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator		Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register



Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage -0.3V to +7.0V
 Input Voltage -0.3V to V_{DD} + 0.3V
 Operating Ambient Temperature -40°C to +85°C
 Storage Temperature -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = 3.0V ,GND = 0V, T_A = 25°C, f_{osc} = 32.768kHz, f_{oscx} is not used, LCD voltage divider resistor = 270kΩ, 1/4 LCD bias, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V _{DD}	2.4	3	6	V	
Operating Current	I _{OP1}	-	12	22	μA	All output pins unload execute NOP instruction, LCD off, WDT off
Operating Current	I _{OP2}	-	0.3	0.5	mA	All output pins unloaded, OSCX as system oscillator, f _{oscx} = 4MHz (Execute NOP instruction)
Standby Current	I _{SB1}	-	4	6	μA	All output pins unload (HALT mode), WDT off, LVR off, LCD off
Standby Current	I _{SB1H}	-	200	300	μA	All output pins unload, (HALT mode) OSCX as system oscillator, f _{oscx} = 4MHz WDT off
Standby Current	I _{SB2}	-	-	1	μA	All output pins unload (STOP mode), LCD off, WDT off
Input High Voltage	V _{IH}	0.7 X V _{DD}	-	V _{DD} + 0.3	V	PORTA - PORTC
Input High Voltage	V _{IH1}	0.8 X V _{DD}	-	V _{DD} + 0.3	V	$\overline{\text{RESET}}$ (Schmitt trigger input)
Input Low Voltage	V _{IL}	-0.3	-	0.3 X V _{DD}	V	PORTA - PORTC
Input Low Voltage	V _{IL1}	-0.3	-	0.2 X V _{DD}	V	$\overline{\text{RESET}}$ (Schmitt trigger input)
Output High Voltage	V _{OH1}	0.7 X V _{DD}	-	-	V	PORTA.0, PORTA.3, PORTB - C (I _{OH} = -2mA)
Output Low Voltage	V _{OL1}	-	-	0.2 X V _{DD}	V	PORTA.0, PORTA.3, PORTB - C (I _{OL} = 2mA)
Output High Voltage	V _{OH2}	0.7 X V _{DD}	-	-	V	PORTA.1 - 2 or Alarm output, I _{OH} = -5mA
Output Low Voltage	V _{OL2}	-	-	0.2 X V _{DD}	V	PORTA.1 - 2 or Alarm output, I _{OL} = 5mA
Output High Voltage	V _{OH3}	V _{DD} - 0.6	-	-	V	SEGx to be output port or LED SEGx I _{OH} = -1mA
Output Low Voltage	V _{OL3}	-	-	0.6	V	SEGx to be output port or LED SEGx, I _{OL} = 1mA
Output High Voltage	V _{OH4}	V _{DD} - 0.6	-	-	V	LED COMx, I _{OH} = -100μA
Output Low Voltage	V _{OL4}	-	-	GND + 0.6	V	LED COMx, I _{OL} = 2.5mA
LCD Driving on resistor	R _{ON}	-	5	-	kΩ	LCD COMx, LCD SEGx, the voltage variation of V1, V2, V3, V4 is less than 0.2V
Pull-high Resistor	R _{PH}	-	200	-	kΩ	PORTA - C
Pull-low Resistor	R _{PL}	-	200	-	kΩ	PORTA - C
WDT Current	I _{WDT}	-	-	10	μA	
LCD Lighting	I _{LCD}	-	8	10	μA	
LCD voltage divider resistor	R _{LCD}	-	270 90 30 10	-	kΩ	RLCD1, RLCD0 = 0, 0 RLCD1, RLCD0 = 0, 1 RLCD1, RLCD0 = 1, 0 RLCD1, RLCD0 = 1, 1



DC Electrical Characteristics

(VDD = 5.0V, GND = 0V, TA = 25°C, fosc = 32.768kHz, foscx is not used, LCD voltage divider resistor = 270kΩ, 1/4 LCD bias, unless otherwise specified)

Parameter	Symbol	Min.	Typ	Max.	Unit	Conditions
Operating Voltage	VDD	2.4	5	6	V	
Operating Current	IOP1	-	22	42	μA	All output pins unload execute NOP instruction, LCD off, WDT off
Operating Current	IOP2	-	1.5	2	mA	All output pins unloaded, OSCX as system oscillator, foscx = 8MHz (Execute NOP instruction)
Standby Current	ISB1	-	7	12	μA	All output pins unload (HALT mode), WDT off, LVR off
Standby Current	ISB1H	-	600	800	μA	All output pins unload, (HALT mode), OSCX as system oscillator, foscx = 8MHz WDT off
Standby Current	ISB2	-	-	1	μA	All output pins unload (STOP mode), LCD off, WDT off
Input High Voltage	VIH	0.7 X VDD	-	VDD + 0.3	V	PORTA - PORTC
Input High Voltage	VIH1	0.8 X VDD	-	VDD + 0.3	V	RESET (Schmitt trigger input)
Input Low Voltage	VIL	-0.3	-	0.3 X VDD	V	PORTA - PORTC
Input Low Voltage	VIL1	-0.3	-	0.2 X VDD	V	RESET (Schmitt trigger input)
Pull-high Resistor	RPH	-	150	-	kΩ	PORTA - C
Pull-low Resistor	RPL	-	150	-	kΩ	PORTA - C
WDT Current	IWDT	-	-	20	μA	
LCD Lighting	ILCD	-	12	15	μA	



SH67P53/K53

AC Characteristics ($V_{DD} = 3.0V$, $GND = 0V$, $T_A = 25^\circ C$, $f_{osc} = 32.768kHz$ crystal, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	1	2	s	
Instruction Time	T_{cy}		122.07		μs	

AC Characteristics ($GND = 0V$, $T_A = 25^\circ C$, $f_{osc} = 262kHz$ RC, f_{oscx} stop, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Variation	$ \Delta f /f$	-	-	20	%	Include supply voltage and chip-to-chip variation

AC Characteristics ($GND = 0V$, $T_A = 25^\circ C$, $f_{oscx} = 8MHz$ RC, unless otherwise specified)

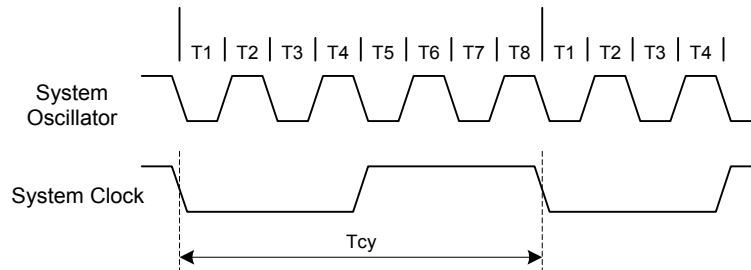
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Variation	$ \Delta f /f$	-	-	20	%	Include supply voltage and chip-to-chip variation

Low Voltage Reset Electrical Characteristics ($V_{DD} = 2.4 - 6V$, $GND = 0V$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage 1	V_{LVR1}	2.4	2.5	2.6	V	LVR Enable
LVR Voltage 2	V_{LVR2}	3.8	4.0	4.2	V	LVR Enable

Timing Waveform

System Clock Timing Waveform

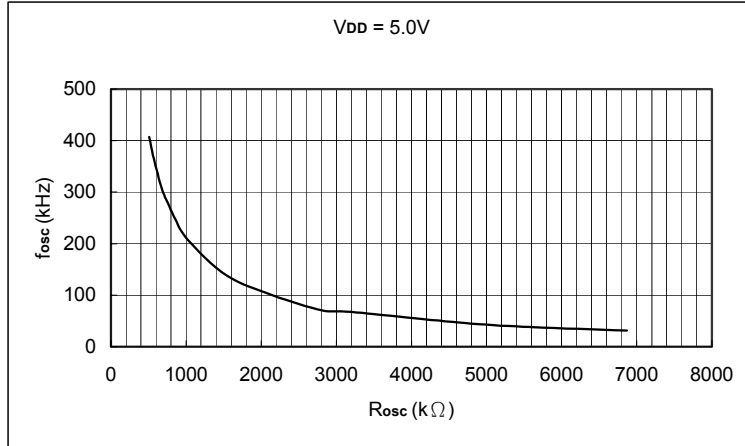




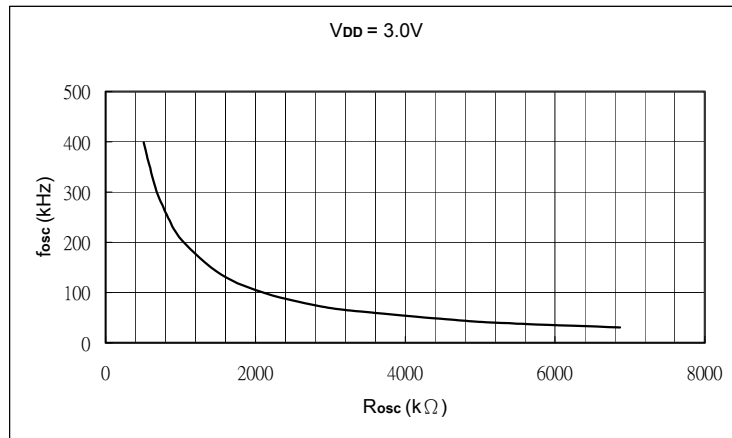
RC Oscillator Characteristics Graphs (for reference only)

Typical RC Oscillator Resistor vs. Frequency:

(1) fosc vs. Rosc



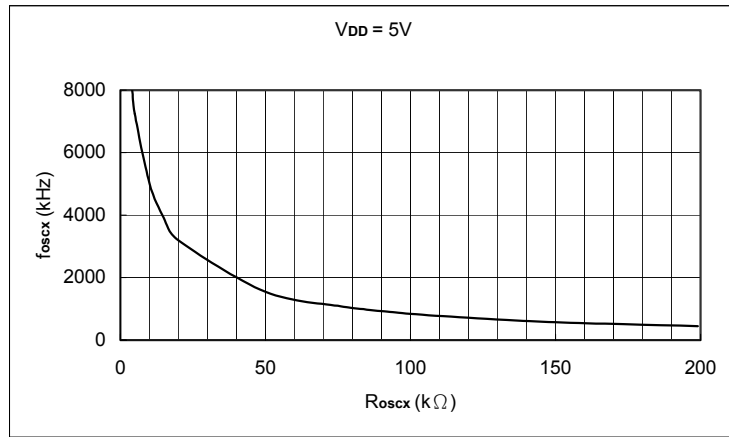
Resistor vs. fosc, VDD = 5.0V



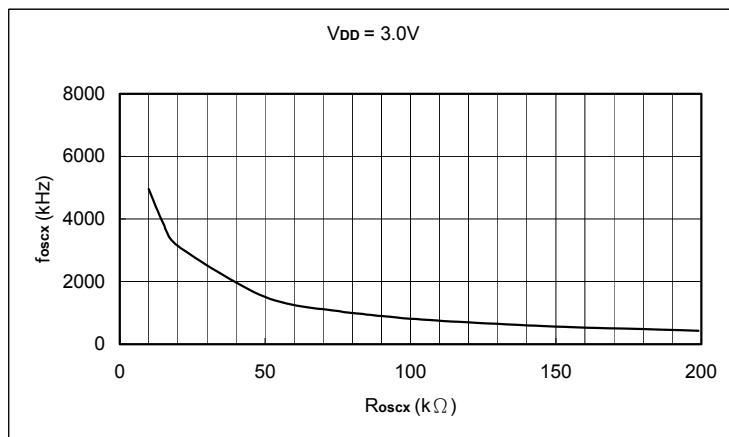
Resistor vs. fosc, VDD = 3.0V



(2) foscx vs. Roscx



Resistor vs. foscx, V_{DD} = 5.0V



Resistor vs. foscx, V_{DD} = 3.0V

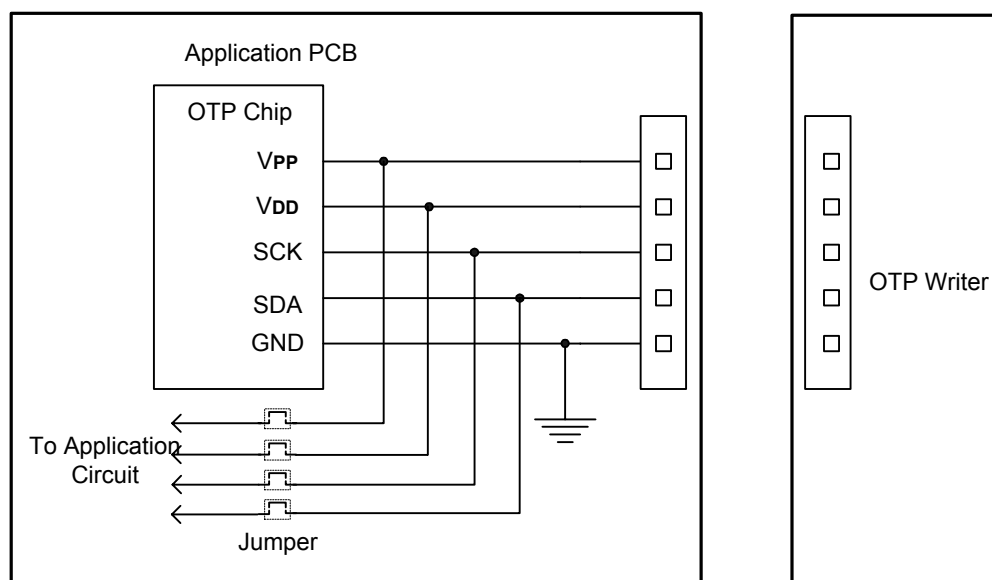


In System Programming Notice for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on the user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (VDD, VPP, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are as following:

- (1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.
- (2) Connect the programming interface with OTP writer and begin programming.
- (3) Disconnect OTP writer and short these jumpers when programming is complete.

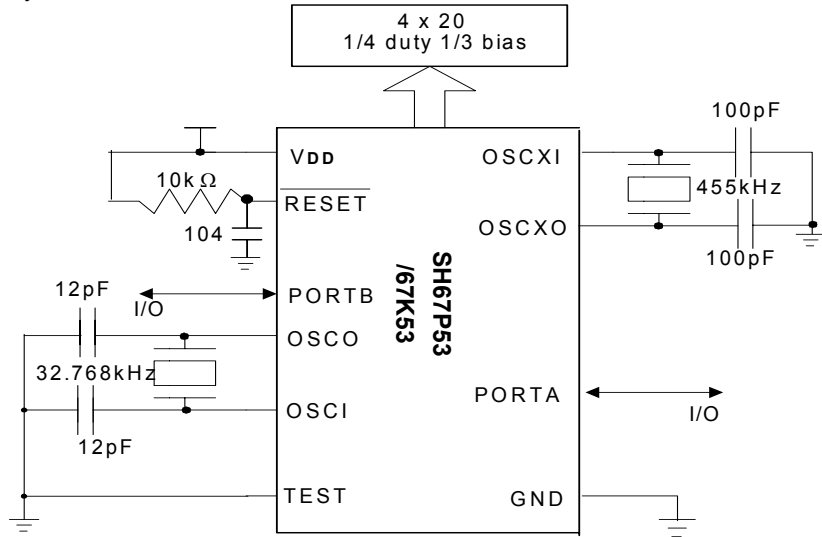
For more detail information, please refer to the OTP writer user manual.



Application Circuit (for reference only)

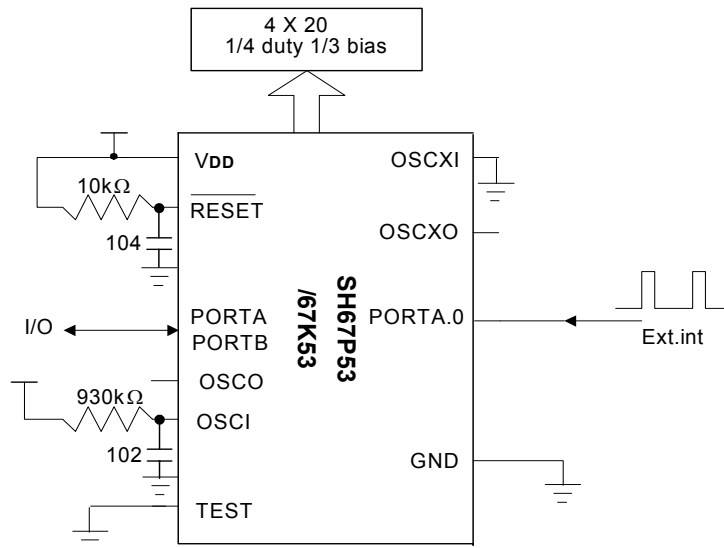
AP1:

V_{DD} = 3.0V
 OSC: Crystal oscillator 32.768kHz (Code Option)
 OSCX: Ceramic oscillator 455kHz
 PORTA, PORTB: I/O
 LCD: Internal LCD 1/4 duty, 1/3 bias



AP2:

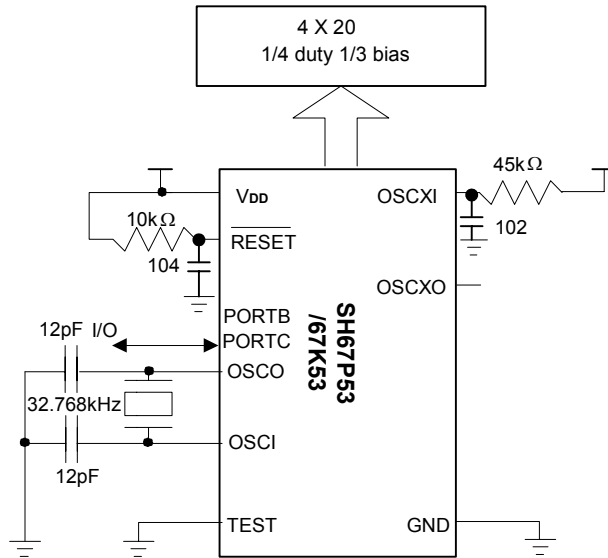
V_{DD} = 5.0V
 OSC: RC oscillator 262kHz (Code Option)
 LCD: Internal LCD 1/4 duty, 1/3 bias
 PORTA, PORTB: I/O
 PORTA.0: External interrupt





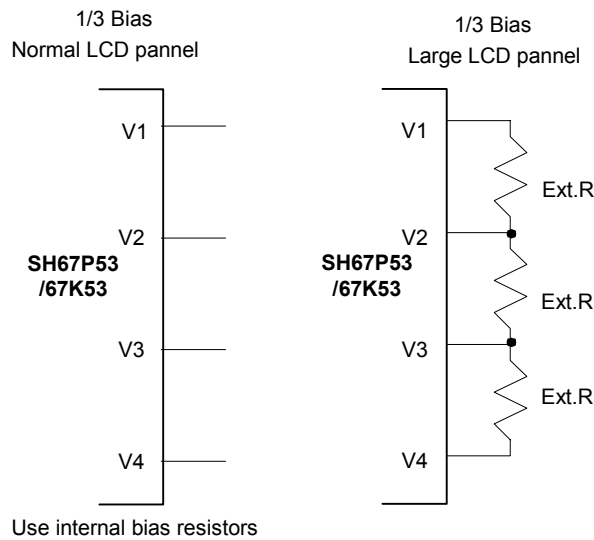
AP3:

V_{DD} = 5.0V
 OSC: Crystal oscillator 32.768kHz (Code Option)
 OSCX: RC oscillator 1.8MHz
 PORTB, PORTC: I/O



AP4:

Large LCD panel: If internal different bias resistor (10kΩ, 30kΩ, 90kΩ, 270kΩ) don't meet request, user can use External LCD bias





Ordering Information

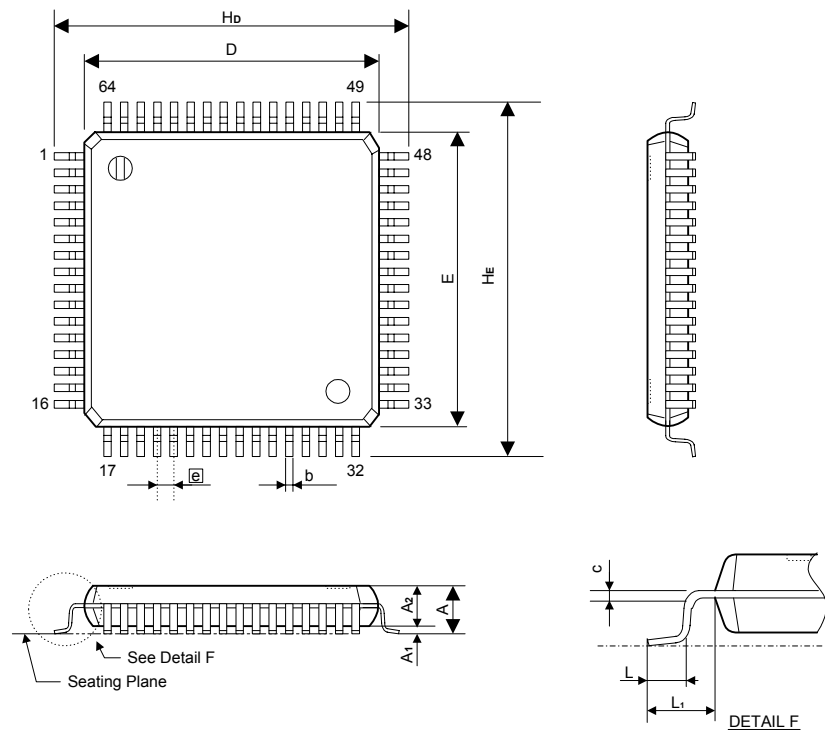
Part No.	Package
SH67P53H	CHIP FORM
SH67K53H	CHIP FORM
SH67P53P	LQFP 64
SH67K53P	LQFP 64



Package Information

LQFP64 Outline Dimensions (BODY SIZE: 10*10)

unit: inches/mm



Symbol	Dimensions in inch	Dimensions in mm
A	0.063 (MAX)	1.60 (MAX)
A1	0.002 (MIN.), 0.006(MAX.)	0.05 (MIN), 0.15 (MAX)
A2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.004 (MIN), 0.008 (MAX)	0.09 (MIN), 0.20 (MAX)
D	0.394 BASIC	10.00 BASIC
E	0.394 BASIC	10.00 BASIC
$\text{\textcircled{a}}$	0.020 BASIC	0.50 BASIC
H_b	0.472 BASIC	12.00 BASIC
H_E	0.472 BASIC	12.00 BASIC
L	0.024 ± 0.006	0.60 ± 0.15
L1	0.039 REF	1.00 REF

**Data Sheet Revision History**

Revision No.	History	Date
2.2	Update a content of the timer0 mode register	Feb. 2010
2.1	Add 64-pin LQFP Package	Feb. 2010
2.0	Package information update	May. 2009
1.0	Original	Jan. 2006