SH69K20A

1K 4-bit Micro-controller

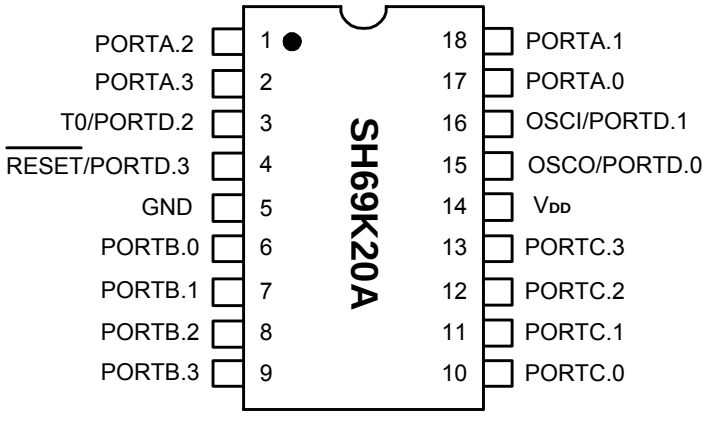
Features

- SH6610C-based single-chip 4-bit micro-controller
- ROM: 1K X 16 bits
- RAM: 96 X 4 bits
  - System register: 32 X 4 bits
  - Data memory: 64 X 4 bits
- Operation voltage:
  - f_{OSC} = 400kHz - 4MHz, V_{DD} = 2.0V - 5.5V
  - f_{OSC} = 4MHz - 8MHz, V_{DD} = 4.5V - 5.5V
- 15 CMOS bi-directional I/O pins and 1 CMOS input pin
- Built-in pull-high and pull-low resistor for PORTA, B, C, D (excluding PORTD.3 - no pull-high resistor)
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-load timer/counter, can be switched to external clock source
- Powerful interrupt sources:
  - Internal interrupt: Timer0
  - External 0 interrupt: PORTA.0
  - External 1 interrupt: PORTA.3
  - PORT's rising/falling edge interrupt: PORTBC
- Oscillator: (Code Option)
  - Crystal oscillator: 32.768kHz, 400kHz - 8MHz
  - Ceramic resonator: 400kHz - 8MHz
  - External RC oscillator: 400kHz - 8MHz
  - Internal RC oscillator: 2MHz/4MHz/6MHz
  - External clock: 30kHz - 8MHz
- Instruction cycle time:
  - 4/32.768kHz (≈ 122.1us) for 32.768kHz
  - 4/8MHz (= 0.5us) for 8MHz at V_{DD} = 5.0V
- Built-in 2MHz/4MHz/6MHz RC Oscillator (Code Option)
- Internal reliable reset circuit
- Low voltage reset function (LVR) (Code Option)
- Warm-up timer for power on reset
- Built-in watchdog timer (Code Option)
- Two low power operation modes: HALT and STOP
- MASK type
- 18-pin DIP/SOP Package

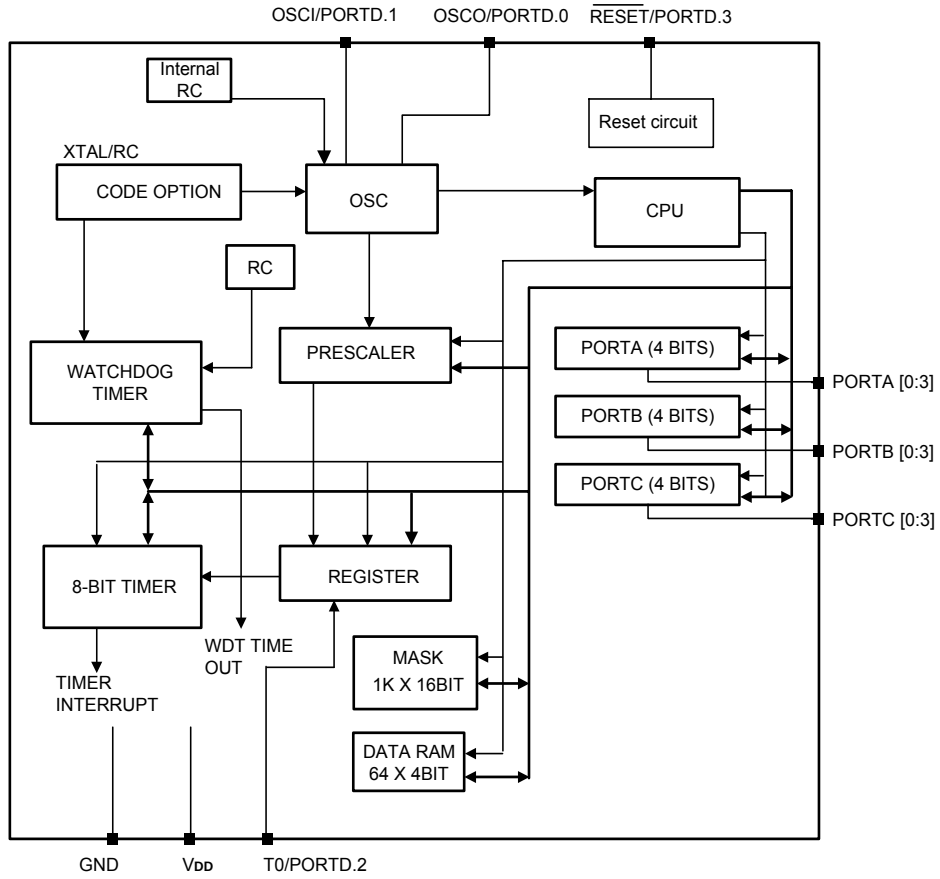
General Description

SH69K20A is a single-chip micro-controller integrated with SRAM, ROM, Timer and I/O port, with a built-in 2MHz/4MHz/6MHz RC oscillator.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Designation	I/O	Description
1	PORTA.2	I/O	Bit programmable bi-directional I/O port
2	PORTA.3	I/O I	Bit programmable bi-directional I/O port Schmitt Trigger input only when it is shared as External 1 interrupt
3	T0 /PORTD.2	I I/O	Timer Clock/Counter (Schmitt Trigger input) Shared with bit programmable bi-directional PORTD.2
4	$\overline{\text{RESET}}$ /PORTD.3	I I	Reset input (Active Low) When internal reset circuit is used, it is shared with PORTD.3 (Input only, Code Option)
5	GND	P	Ground pin
6 - 9	PORTB [0:3]	I/O I	Bit programmable bi-directional I/O port Vector Interrupt (Active rising or falling edge by system register setup)
10 - 13	PORTC [0:3]	I/O I	Bit programmable bi-directional I/O port Vector Interrupt (Active rising or falling edge by system register setup)
14	V_{DD}	P	Power supply pin
15	OSCO /PORTD.0	O I/O	Oscillator output pin, connect to crystal/ceramic oscillator When selecting internal/external RC oscillator or external clock input, it is shared with bit programmable bi-directional I/O port PORTD.0
16	OSCI /PORTD.1	I I/O	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of RC oscillator When selecting internal RC oscillator is used, it is shared with bit programmable bi-directional I/O PORTD.1
17	PORTA.0	I/O I	Bit programmable bi-directional I/O port Schmitt Trigger input only when it is shared as External 0 interrupt
18	PORTA.1	I/O	Bit programmable bi-directional I/O port

Function Description

1. CPU

The CPU contains the following function blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator (AC), Table Branch Register (TBR), Data Pointer (INX, DPH, DPM, and DPL), and Stacks.

1.1 PC

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2 ALU and CY

ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that generates the arithmetic operation. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3 Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4 Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5 Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, and RAM address bit9 - bit0 comes from DPH, DPM and DPL.

1.6 Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceed 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. ROM

The ROM can address 1K X 16 bits of program area from $000 to $3FF.

2.1 Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP instruction	Jump to RESET service routine
$001	JMP Instruction	Jump to External 0 interrupt service routine
$002	JMP instruction	Jump to TIMER0 interrupt service routine
$003	JMP Instruction	Jump to External 1 interrupt service routine
$004	JMP instruction	Jump to PORTBC interrupt service routine

*JMP instruction can be replaced by any instruction.

3. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT mode.

3.1 RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
System register and I/O: $000 - $01F
Data memory: $020 - $05F

3.2 Configuration of System Register

System Register $00-$1F RAM Map:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	IEX0	IET0	IEX1	IEP	R/W	Interrupt enable flags
$01	IRQX0	IRQT0	IRQX1	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06 - $07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C - $0D	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13 - $14	-	-	-	-	-	Reserved
$15	-	PD2OUT	PD1OUT	PD0OUT	R/W	PORTD input/output control
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	PORTA input/output control
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	PORTB input/output control
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	PORTC input/output control
$19	PULLEN	PH/PL	PBCFR	EINFR	R/W	Bit0: External 0/External 1 interrupt (PORTA.0/PORTA.3) rising/falling edge set Bit1: PORTBC interrupt rising/falling edge set Bit2: Port pull-high/pull-low set Bit3: Port pull-high/pull-low enable control
$1A - $1B	-	-	-	-	-	Reserved
$1C	-	-	T0S	T0E	R/W	Bit0: T0 signal edge, Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
$1F	-	-	-	-	-	Reserved

4. Initial State

4.1 System Register initial State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$00	IEX0	IET0	IEX1	IEP	0000	0000
$01	IRQX0	IRQT0	IRQX1	IRQP	0000	0000
$02	-	TM0.2	TM0.1	TM0.0	-000	-000
$04	TL0.3	TL0.2	TL0.1	TL0.0	xxxx	xxxx
$05	TH0.3	TH0.2	TH0.1	TH0.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	1111	1111
$09	PB.3	PB.2	PB.1	PB.0	1111	1111
$0A	PC.3	PC.2	PC.1	PC.0	1111	1111
$0B	PD.3	PD.2	PD.1	PD.0	1111	1111
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$15	-	PD2OUT	PD1OUT	PD0OUT	-000	-000
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	0000	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	0000	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	0000	0000
$19	PULLEN	PH/PL	PBCFR	EINFR	0100	0100
$1C	-	-	T0S	T0E	--00	--00
$1E	WD	WDT.2	WDT.1	WDT.0	0000	1000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2 Other Initial States:

Others	After power on reset
Program counter	$000
CY	Undefined
Data memory	Undefined
AC	Undefined
WDT Counter	0

5. System Clock and Oscillator

SH69K20A has one clock source. Oscillator is determined by Code Option. The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock = fosc/4.

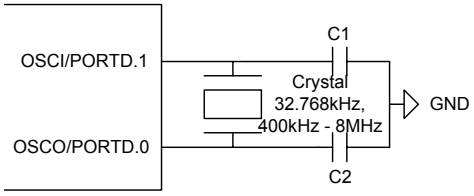
5.1 Instruction Cycle Time

(1) 4/32.768kHz (≈ 122.1μs) for 32.768kHz oscillator.

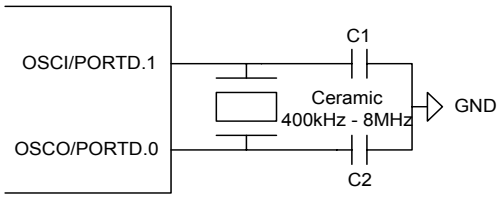
(2) 4/8MHz (= 0.5μs) for 8MHz oscillator.

5.2 Oscillator Type

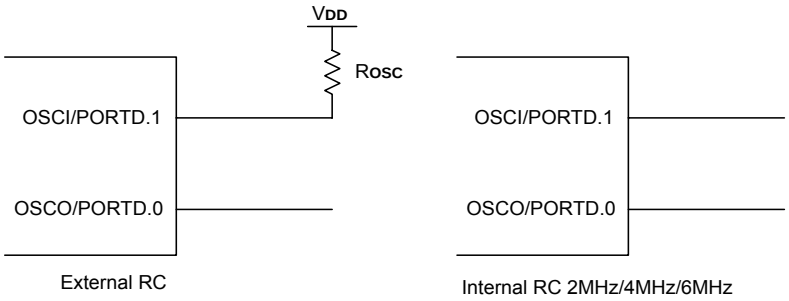
(1) Crystal oscillator: 32.768kHz, 400kHz - 8MHz.



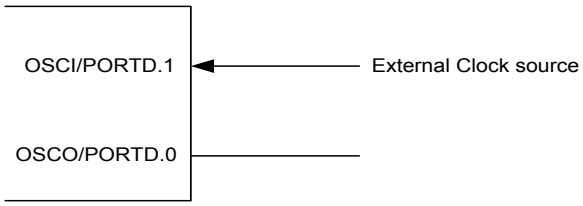
(2) Ceramic resonator: 400kHz - 8MHz.



(3) RC oscillator: 400kHz - 8MHz.



(4) External input clock: 30kHz - 8MHz.



Note:

- If selecting External RC oscillator (Code Option) or External input clock (Code Option), OSCO pin is shared with PORTD.0.
- If selecting Internal RC oscillator (Code Option), OSCI pin is shared with PORTD.1 and OSCO pin is shared with PORTD.0.

6. Timer0

SH69K20A has one 8-bit timer. The timer/counter has the following features:
- 8-bit up-counting timer/counter.
- Automatically re-load counter.
- 8-bit prescaler.
- Internal and external clock option.
- Interrupt on overflow from $FF to $00.
- Edge option for external event.

The following is a simplified timer block diagram:

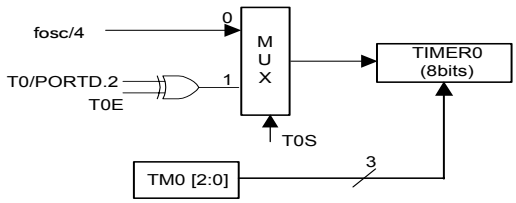


Figure 1. Timer block Diagram

6.1 Configuration and Operation

Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digit and high order digit. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.
Load register programming: The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflowing from $FF to $00.

Timer Load Register: Since register H controls the physical READ and WRITE operations. Please follow the following steps:

Write Operation:

Low nibble first;

High nibble to update the counter

Read Operation:

High nibble first;

Low nibble followed.

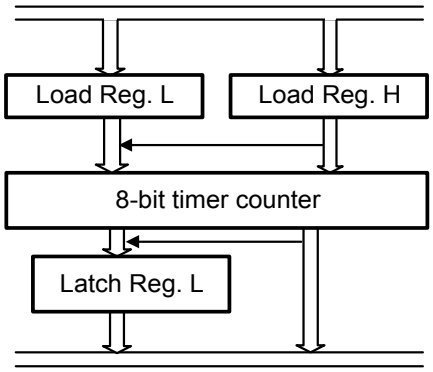


Figure 2. Timer Load Register Configure

6.2 Timer0 Mode Register

The timer can be programmed in several different prescaler ratios by setting Timer Mode Register (TM0).

The 8-bit counter prescaler overflows output pulses. The TIMER mode register (TM0) is a 3-bit register used for timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

6.3 External Clock/Event T0 as Timer0 Source

When external clock/event T0 inputs as Timer0 source, it is synchronized with the CPU system clock. Therefore the external source must follow certain constraints. The system clock samples it in frame cycle instruction. Therefore it is necessary to be set the value between high (at least 2 tosc) and low (at least 2 tosc). When the prescaler ratio selects /20, it is the same as the system clock input.

The requirement is as follows:

T0H (T0 high time) $\geq$ 2 X tosc + ΔT

T0L (T0 low time) $\geq$ 2 X tosc + ΔT; ΔT= 20ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter, so the prescaler output is symmetrical. Then:

$$\text{T0 high time} = \text{T0 low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = prescaler value

The requirement is:

$\frac{N*T0}{2} \geq 2*tosc+\Delta T$ or $T0 \geq \frac{4*tosc+2*\Delta T}{N}$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4*tosc+2*\Delta T}{N}$$

Systems register $1C: (T0)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	-	-	T0S	T0E	R/W	Bit0: T0 signal edge Bit1: T0 signal source
	-	-	X	0	R/W	Increment on low-to-high transition T0 pin
	-	-	X	1	R/W	Increment on high-to-low transition T0 pin
	-	-	0	X	R/W	Shared with PORTD.2, Timer0 source is system clock
	-	-	1	X	R/W	Shared with T0 input, Timer0 source is T0 input clock

7. I/O PORT

The SH69K20A provides up to 16 I/O pins (PORTD.3 can only be shared as input pin). When every I/O is used as an input port, the port control register controls ON/OFF of the output buffer. Sections below show the circuit configuration of I/O ports.

Each of these ports contains 4 bits I/O pins. The port control register can control ON/OFF of the output buffer for port.

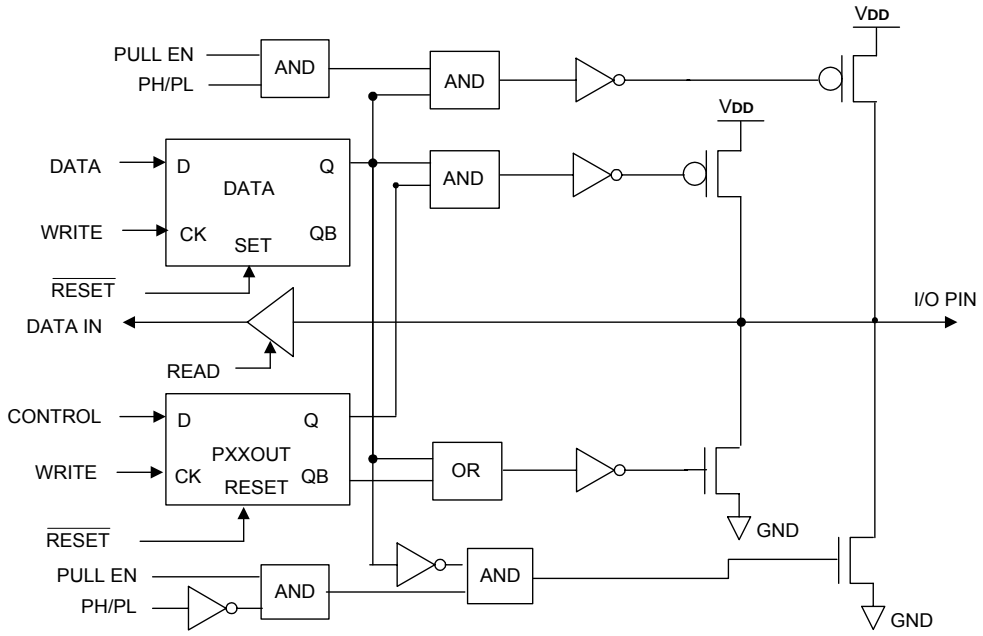
Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD

Notice:

PORTD.3 is shared with $\overline{\text{RESET}}$ pin. It can only be shared as input pin when selecting “Reset pin used as PORTD.3” by Code Option. It only has pull-low resistor control. So it is no use for PORTD.3 when PH/PL is set to “1”.

Equivalent circuit for a single I/O pin:



System Register $15 - $19

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	-	PD2OUT	PD1OUT	PD0OUT	R/W	Set PORTD to be output port
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	Set PORTA to be output port
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	Set PORTB to be output port
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	Set PORTC to be output port
$19	PULLEN	PH/PL	PBCFR	EINFR	R/W	Bit0: External 0/External 1 interrupt (PORTA.0/PORTA.3) rising/falling edge set Bit1: PORTBC interrupt rising/falling edge set Bit2: Port pull-high/pull-low set Bit3: Port pull-high/pull-low enable control

I/O control register:
PAXOUT, PBXOUT, PCXOUT (X = 0, 1, 2, 3), PDXOUT (X = 0, 1, 2)
1: Set I/O as an output buffer
0: Set I/O as an input buffer (power-on initial)

EINFR:	1: External Rising Edge interrupt	0: External Falling Edge interrupt,
PBCFR:	1: Rising Edge interrupt	0: Falling Edge interrupt,
PH/PL:	1: Port pull-high resister ON	0: Port pull-low resister ON,
PULLEN:	1: Port pull-high / pull-low enable	0: Port pull-high / pull-low disable (power-on initial)

8. Interrupt

Four interrupt sources are available on SH69K20A:
- Timer0 interrupt
- PORTBC interrupts (Rising/Falling edge)
- External 0 interrupt (Rising/Falling edge)
- External 1 interrupt (Rising/Falling edge)

8.1 Interrupt Control Bits and Interrupt Service

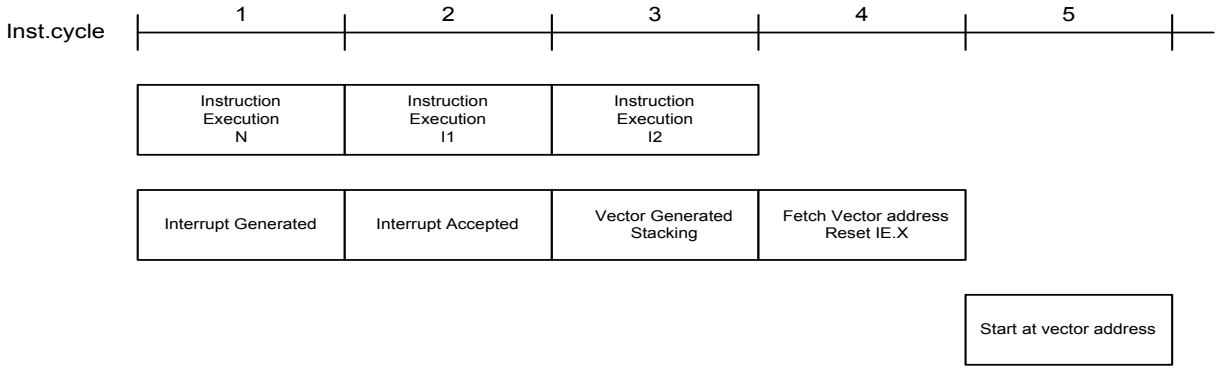
The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to “0” at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX0	IET0	IEX1	IEP	R/W	Interrupt enable flags
$01	IRQX0	IRQT0	IRQX1	IRQP	R/W	Interrupt request flags

When IEx is set to “1” and the interrupt request is generated (IRQx is “1”), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to “0” automatically, so when IRQx is “1” and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:

Interrupt Nesting:



During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instructions executed. However, if instruction I1 or instruction I2 disables the interrupt request or enables flag, then the interrupt service will be terminated.

8.2 External Interrupt

External 0 interrupt is shared with the PORTA.0 and External 1 interrupt is shared with PORTA.3, falling/rising edge active. When the bit3 of the register $00 (IEX0) is set to “1”, the external 0 interrupt is enabled; when the bit1 of the register $00 (IEX1) is set to “1”, the external1 interrupt is enabled.

If user wants to generate an External Interrupt when a Rising Edge from GND to V_{DD}, the following must be executed:
(1) Set the PORTA.0/PORTA.3 as input port;
(2) Pull-low the port (Use external pull-low resistance or set PULLEN to “1” and clear PH/PL to “0”).
(3) Set Rising Edge register. (Set EINFR to “1”)

And further rising edge transition would not be able to make interrupt request until PORTA.0 / PORTA.3 return to GND.

If user wants to generate an External Interrupt when a Falling Edge from V_{DD} to GND, the following must be executed:
(1) Set the PORTA.0/PORTA.3 as input port;
(2) Pull-high the port (Use external pull-high resistance or set PULLEN to “1” and set PH/PL to “1”).
(3) Set Falling Edge register. (clear EINFR to “0”)

And further falling edge transition would not be able to make interrupt request until PORTA.0 / PORTA.3 return to V_{DD}.

8.3 Timer0 Interrupt

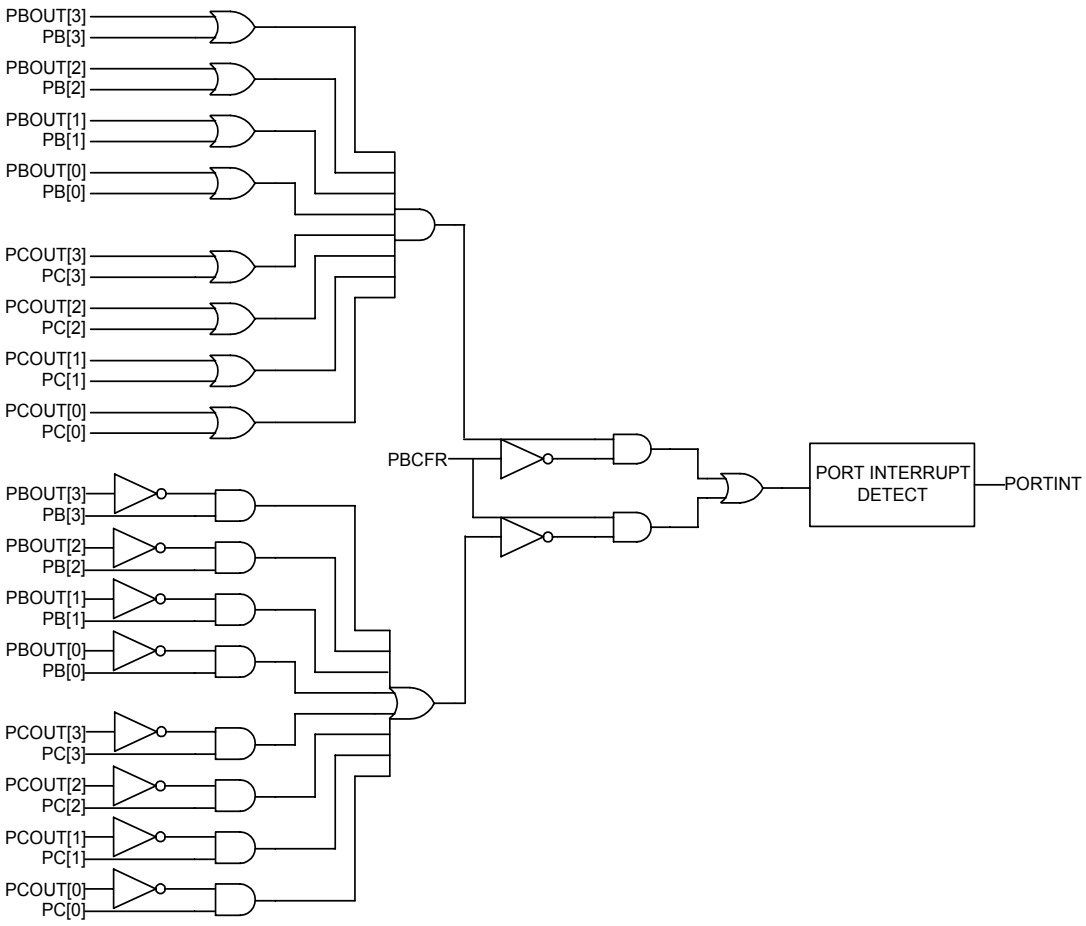
The input clock of Timer0 is based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1), If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

8.4 Port Interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is bit programmable I/O, so only the input port can generate an external interrupt.

When PBCFR is cleared to “0”, any one of the PORTB and PORTC input pin transitions from V_{DD} to GND will generate an interrupt request. And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD}.

When PBCFR is set to “1”, any one of the PORTB and PORTC input pin transitions from GND to V_{DD} will generate an interrupt request. And further rising edge transition would not be able to make interrupt request until all of the pins return to GND.



9. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and to generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by Code Option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$.

Here, V_{DD}: power supply voltage, V_{LVR}: LVR detect voltage. There are two levels of LVR voltage selected by Code Option:

Level 1: 1.4V - 2.0V, typical 1.7V

Level 2: 3.6V - 4.2V, typical 3.9V

LVR voltage level 2 can be enabled or disabled permanently by Code Option, but LVR voltage level 1 is always enabled, user can't disable it.

10. HALT and STOP Mode

After the execution of HALT instruction, the device will enter HALT mode. In the HALT mode, the CPU will stop operating, but the peripheral circuit (Timer0 and watchdog timer) will keep operating.

After the execution of STOP instruction, the device will enter STOP mode. In the STOP mode, the whole chip (including oscillator) will stop operating without watchdog timer, if it is enabled.

In HALT mode, SH69K20A can be waked up if any interrupt occurs.

In STOP mode, SH69K20A can be waked up if external interrupt or port interrupt occurs or watchdog timer overflows (if watchdog is enabled).

11. WDT (Watchdog Timer)

Watchdog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that the WDT will always run even in the STOP mode (if it is enabled). The watchdog timer automatically generates a device reset when it overflows. Code Option can enable and disable this function. The watchdog timer control registers (WDT bit2 - 0) select different overflow frequencies. WDT bit3 is watchdog timer overflow flag.

If the Watchdog timer is enabled, the CPU will be reset and the WDT bit3 is automatically set to "1" by hardware when watchdog timer overflows. Repeat reads or writes WDT register ($1E), the watchdog timer should re-count before the overflow happens.

System Register $1E: (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
	X	0	0	0		Watchdog timer-out period = 4096ms
	X	0	0	1		Watchdog timer-out period = 1024ms
	X	0	1	0		Watchdog timer-out period = 256ms
	X	0	1	1		Watchdog timer-out period = 128ms
	X	1	0	0		Watchdog timer-out period = 64ms
	X	1	0	1		Watchdog timer-out period = 16ms
	X	1	1	0		Watchdog timer-out period = 4ms
	X	1	1	1		Watchdog timer-out period = 1ms
	0	X	X	X		No watchdog timer overflow reset
	1	X	X	X		Watchdog timer overflow, WDT reset happens

12. Warm-up Timer

The device builds in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

12.1 Power on Reset and Low Voltage Reset Warm-up Time Interval:

(1) When the fosc range from 30kHz - 1MHz, the warm-up counter prescaler is divided by 2^{12} (4096).

(2) When the fosc range from 1MHz - 8MHz, the warm-up counter prescaler is divided by 2^{15} (32768).

12.2 Other Warm-up Time Interval:

- Low Voltage Reset (High voltage)
- Wake-up from stop mode

The warm-up counter prescaler is permanently divided by 2^{12} (4096).

Instructions

All instructions are one-cycle and one-word instructions having the characteristics of the memory-oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR X (, B)	11110 0000 000 0000	0 → AC [3]; AC [0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X (, B)	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not including p)	
RTNW H; L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input/Output Voltage . . . . . GND -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 4.5V - 5.5V GND = 0V, TA = 25℃, f_{OSC} = 4MHz Crystal, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	
Operating Current	I_{OP}	-	1.3	1.5	mA	Execute NOP instruction, All output pins unloaded
Stand by Current (HALT)	I_{SB1}	-	-	500	μA	All output pins unload, WDT off (If WDT on, I_{SB1} = I_{SB1} + 20μA)
Stand by Current (HALT) OSC = 32.768kHz Crystal	I_{SB32k}	-	7	10	μA	All output pins unload, WDT off LPD off (If WDT on, I_{SB32K} = I_{SB1} + 20μA)
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unloaded, LPD off, WDT off
Input Low Voltage	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports, pins tri-state
Input Low Voltage	V_{IL2}	GND		0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, OSCI, PORTA.0, PORTA.3 (Schmitt Trigger input when used as external interrupt)
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports, pins tri-state
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, OSCI (Schmitt Trigger input) PORTA.0, PORTA.3 (Schmitt Trigger input when used as external interrupt)
Input Leakage Current	I_{IL1}	-1	-	1	μA	I/O Ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5	-	-	μA	$V_{\overline{RESET}}$ = GND + 0.25V
Input Leakage Current	I_{IL3}	-	1	5	μA	$V_{\overline{RESET}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < V_{T0} < V_{DD}
pull-high/pull-low Resistor	R_P	-	150	-	kΩ	pull-high/pull-low resistor
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, I_{OH} = -10mA
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O Ports, I_{OL} = 20mA

DC Electrical Characteristics (V_{DD} = 2.0V - 4.5V GND = 0V, TA = 25℃, f_{OSC} = 4MHz Crystal, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.0	3.0	4.5	V	
Operating Current	I_{OP}	-	0.8	1.2	mA	Execute NOP instruction, All output pins unloaded
Stand by Current (HALT)	I_{SB1}	-	-	300	μA	All output pins unload, WDT off (If WDT on, I_{SB1} = I_{SB1} + 20μA)
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unloaded, LPD off, WDT off

User Notice:

Max current into V_{DD} pin = 100mA.
Max current out of GND pin = 150mA.
Max. output current sunk by any I/O pin = 50mA.
Max. output current sourced by any I/O pin = 40mA.

AC Electrical Characteristics

V_{DD} = 2.0V - 5.5V, GND = 0V, TA = -40°C to +85°C, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	T_{CY}	0.5	-	133	μs	f_{OSC} = 30kHz - 8MHz
T0 input width	t_{IW}	(T_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio.
Input pulse width	t_{IPW}	$t_{IW/2}$	-	-	ns	

V_{DD} = 2.0V - 5.5V, GND = 0V, TA = -40°C to +85°C, f_{OSC} = 30kHz - 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width (low)	T_{RESET}	10	-	-	μs	V_{DD} = 5V, Low active
Oscillator Start Time	T_{OSC1}	-	-	2	s	Crystal OSC = 32.768kHz
WDT Period	T_{WDT}	1	-	-	ms	V_{DD} = 5.0V, TA = 25°C
External Rosc Oscillator frequency Variation	|ΔF|/F	-	-	20	%	f_{OSC} = 400kHz - 4MHz, V_{DD} = 2.0V - 5.5V f_{OSC} = 4MHz - 8MHz, V_{DD} = 4.5V - 5.5V Include voltage and chip-to-chip variation Bias resistance accuracy within 1%
Internal Rosc Oscillator frequency Variation	|ΔF|/F	-	-	50	%	f_{OSC} = 2MHz/4MHz, V_{DD} = 2.4V - 5.5V f_{OSC} = 6MHz, V_{DD} = 4.5V - 5.5V Include voltage and chip-to-chip variation

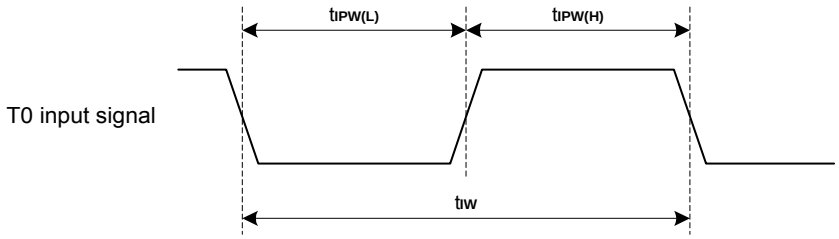
Low Voltage Reset Electrical Characteristics

V_{DD} =2.0V - 5.5V, GND = 0V, TA = 25°C, f_{OSC} = 30kHz - 8MHz, unless otherwise specified.

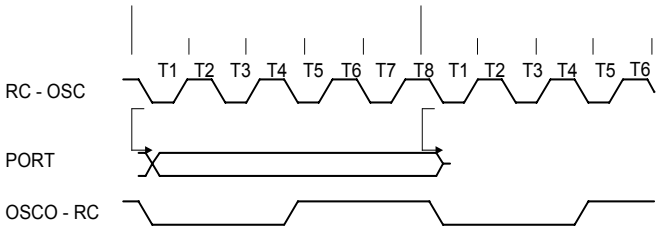
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage (High)	V_{LVR1}	3.6	3.9	4.2	V	LVR enable
LVR Voltage (Low)	V_{LVR2}	1.4	1.7	2.0	V	-

Timing Waveform

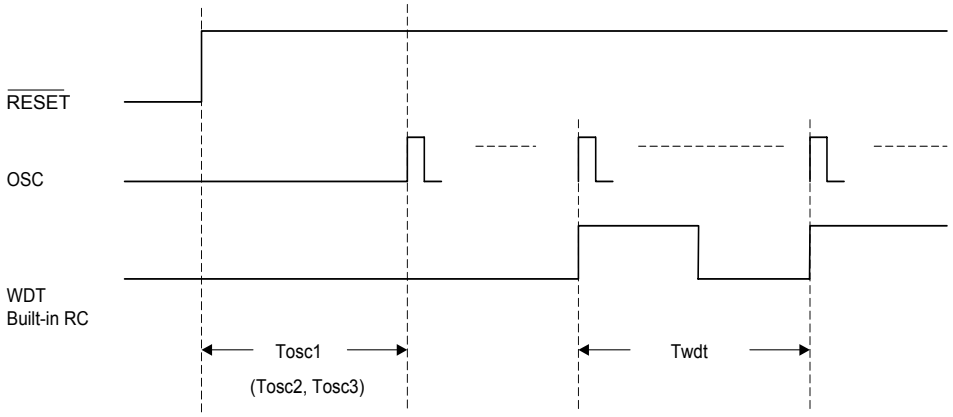
T0 Input Waveform:



RC OSCO Timing Waveform

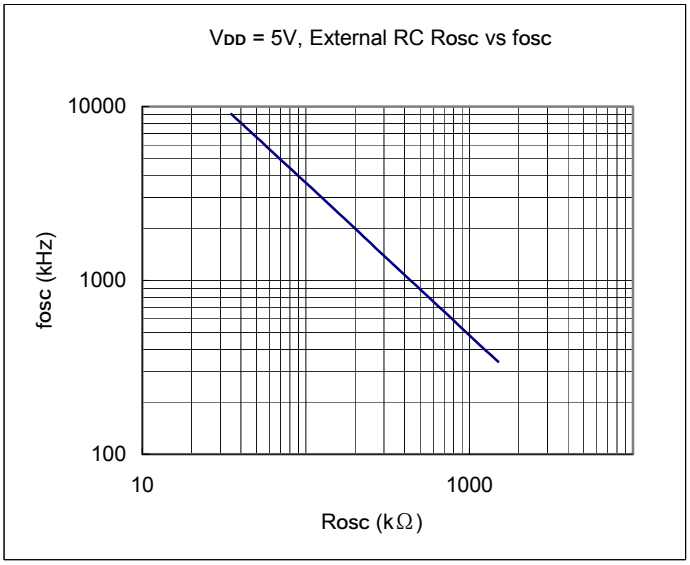


Built-in RC Oscillator (Only use for Watchdog)

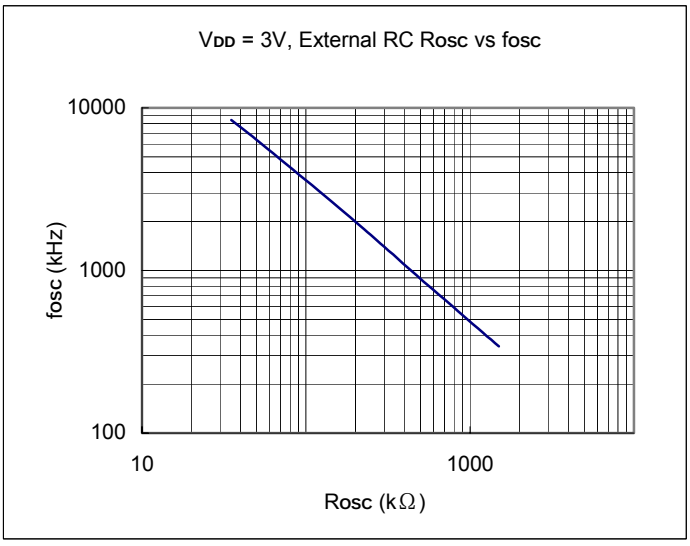


RC Oscillator Characteristics Graphs (for reference only)

Typical External RC oscillator Resistor vs. Frequency:

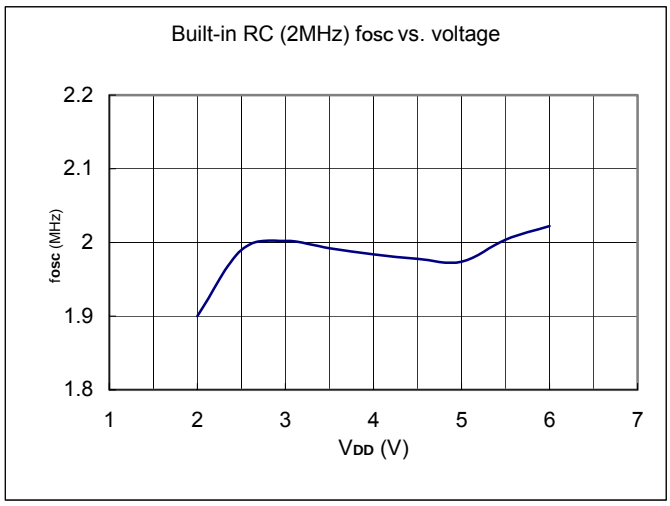


Graph 1. External RC Rosc vs. fosc (V_{DD} = 5V)

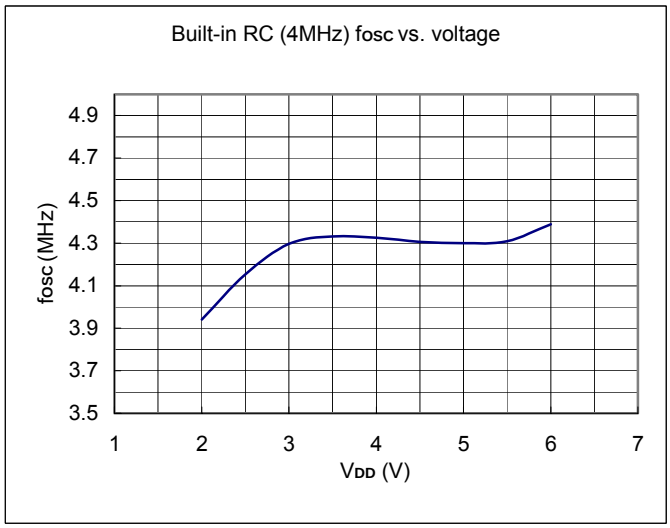


Graph 2. External RC Rosc vs. fosc (V_{DD} = 3V)

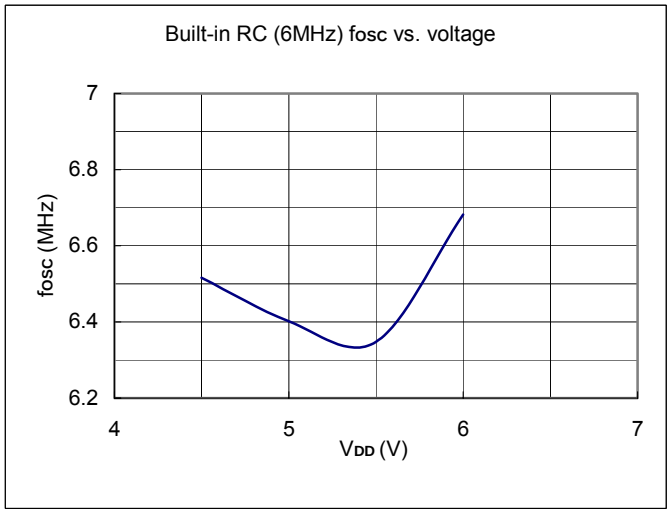
Typical Internal RC oscillator Frequency vs. Operating Voltage:



Graph 3. Built-in RC (2MHz) fosc vs. voltage



Graph 4. Built-in RC (4MHz) fosc vs. voltage

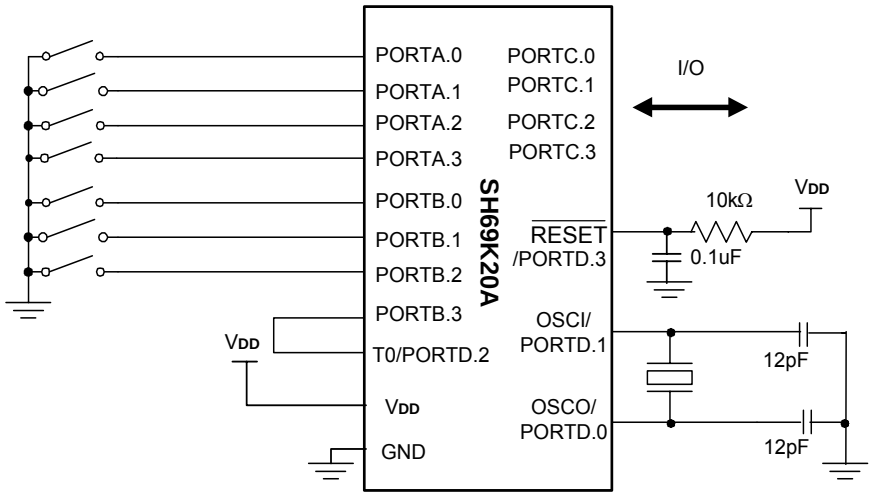


Graph 5. Built-in RC (6MHz) fosc vs. voltage

Application Circuits (for reference only)

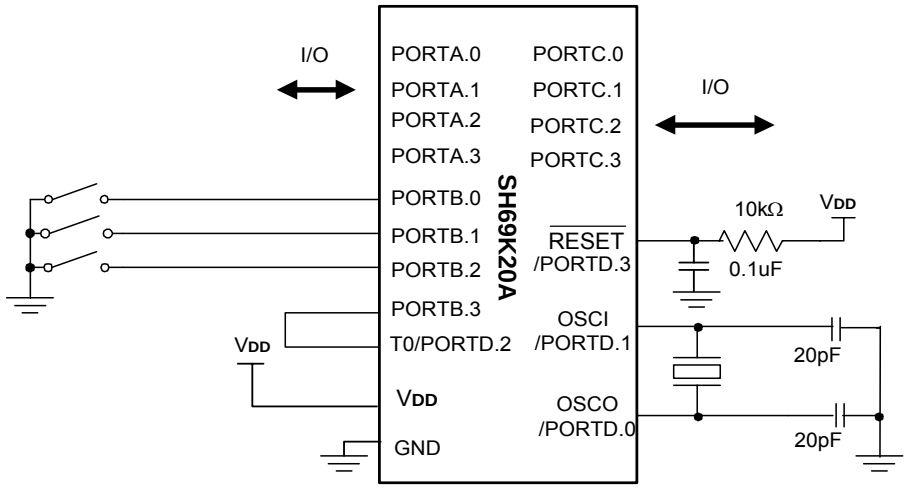
AP1:

(1) Operating voltage: 3.0V
(2) Oscillator: Crystal 32.768kHz
(3) PORTA - B: Input (pull-high ON)
(4) PORTC: I/O



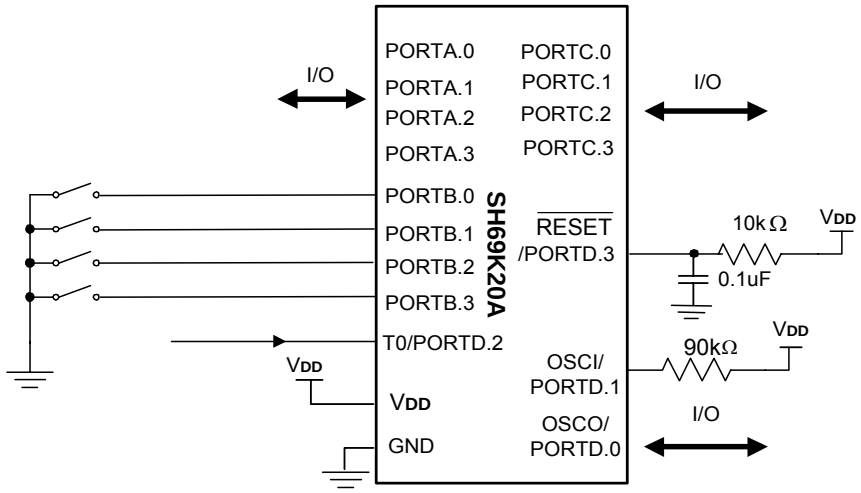
AP2:

(1) Operating voltage: 5.0V
(2) Oscillator: Crystal 4MHz
(3) PORTA & PORTC: I/O
(4) PORTB [0:2]: Input (pull-high ON)



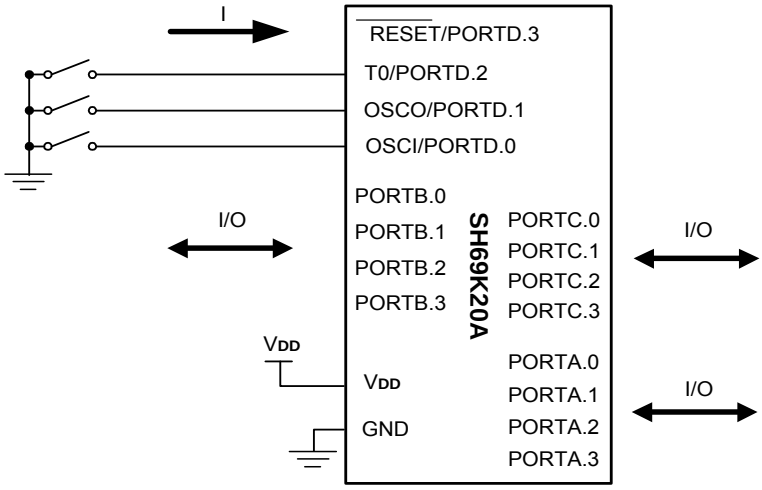
AP3:

(1) Operating voltage: 5.0V
(2) Oscillator: External RC 4MHz
(3) PORTA - C & PORTD.0: I/O (pull-high ON)
(4). Timer0 input: T0

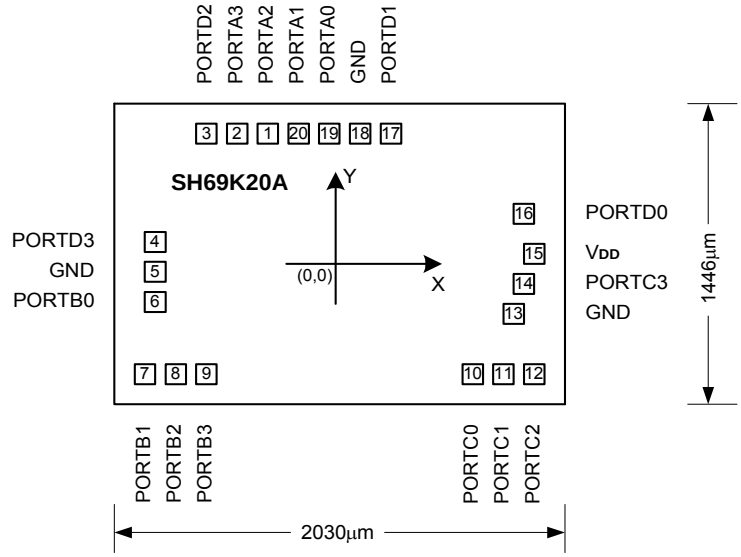


AP4:

(1) Operating voltage: 5.0V
(2) Oscillator: Internal RC 4MHz
(3) Internal Reset circuit
(4) PORTA - C: I/O. (pull-high ON)
(5) PORT [0:2]: (pull-high ON)
(6) PORTD.3: Input only (no pull-high resistor)



Bonding Diagram



Note: Substratum connects to GND.

Unit: μm

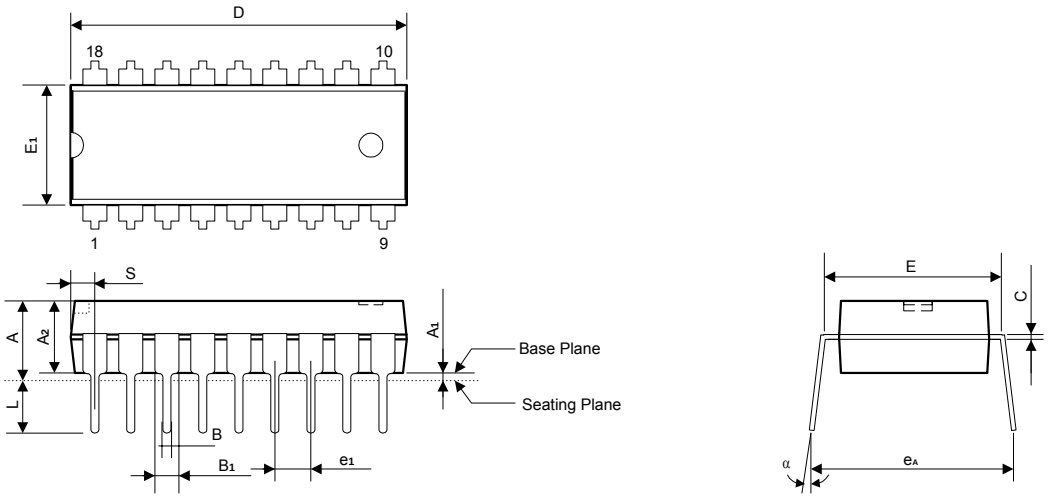
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTA.2	-299.15	571.95	11	PORTC.1	763	-571.95
2	PORTA.3	-429.15	571.95	12	PORTC.2	893	-571.95
3	T0/PORTD.2	-559.15	571.95	13	GND	813.95	-317.15
4	$\overline{\text{RESET}}$ /PORTD.3	-863.95	-45.05	14	PORTC.3	863.95	-187.15
5	GND	-863.95	-165.05	15	VDD	897	-57.15
6	PORTB.0	-863.95	-305.05	16	OSCO/PORTD.0	863.95	101.9
7	PORTB.1	-893	-571.95	17	OSCI/PORTD.1	220.85	571.95
8	PORTB.2	-763	-571.95	18	GND	90.85	571.95
9	PORTB.3	-633	-571.95	19	PORTA.0	-39.15	571.95
10	PORTC.0	633	-571.95	20	PORTA.1	-169.15	571.95

Ordering Information

Part No.	Package
SH69K20AH	CHIP FORM
SH69K20A	18L DIP
SH69K20AM	18L SOP

Package Information

DIP 18L Outline Dimensions unit: inches/mm

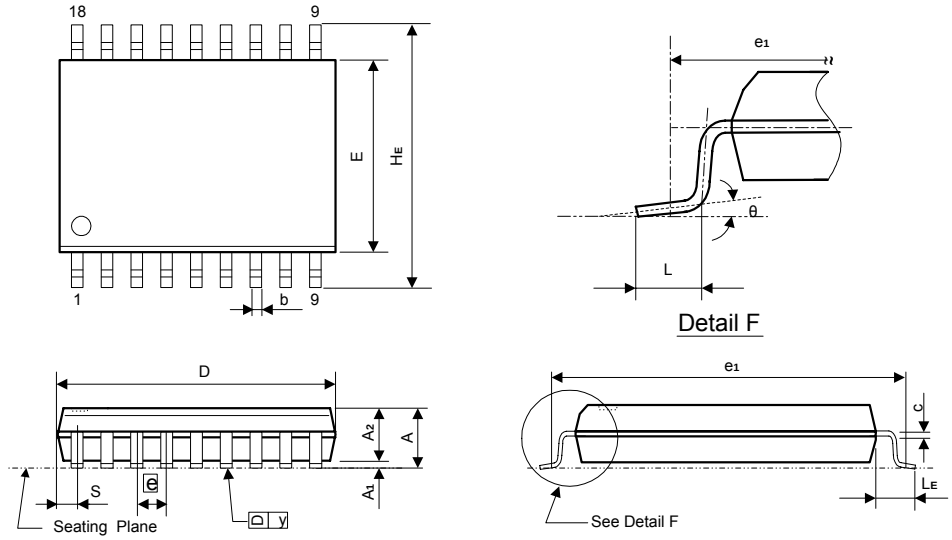


Symbol	Dimensions in inches	Dimension in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.900 Typ. (0.920 Max.)	22.86 Typ. (23.37 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.055 Max.	1.40 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP 18L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.455 ± 0.015	11.56 ± 0.38
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.030 ± 0.008	0.76 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.037 Max.	0.94 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
1.0	Original	Nov. 2004