SH69P55A/K55A

OTP/MASK 8K 4-Bit Micro-controller With LCD Driver & 10-bit SAR ADC

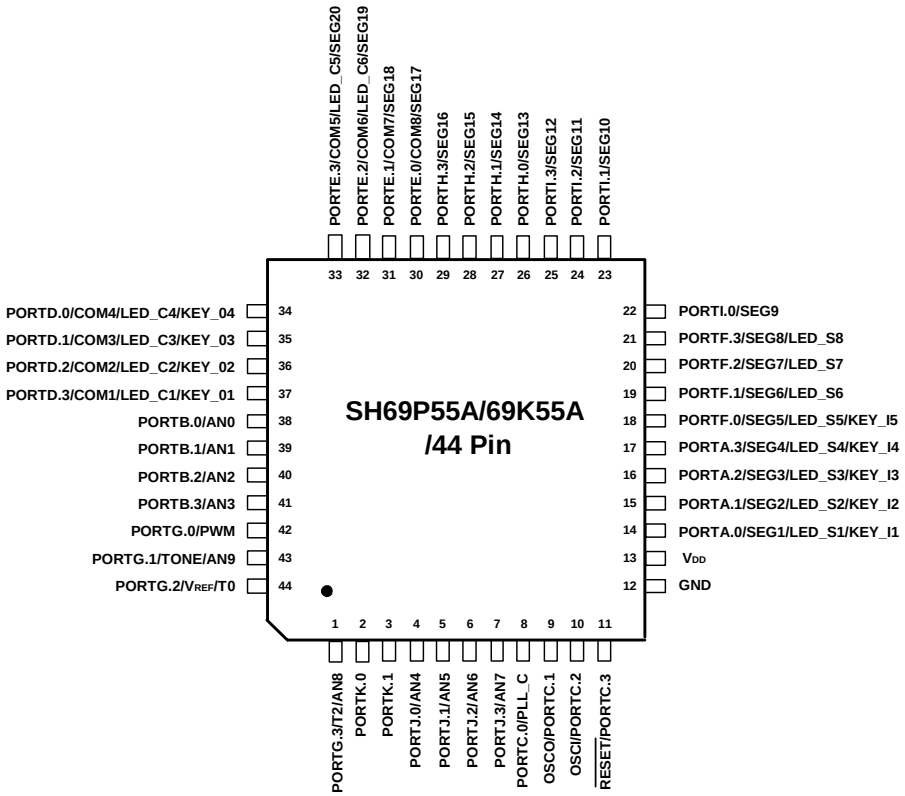
Features

- SH6610D-Based Single-Chip 4-bit Micro-Controller With LCD Driver & 10-bit SAR ADC
- OTP ROM: 8K X 16 bits (SH69P55A)
- MASK ROM: 8K X 16 bits (SH69K55A)
- RAM: 515X 4 bits
  - 99 System Control Register
  - 376 Data Memory
  - 40 LCD RAM
- Operation Voltage: 2.4V - 5.5V
  - f_{OSC} = 30k- 4MHz, V_{DD} = 2.4V - 5.5V
  - f_{OSC} = 30k - 8MHz, V_{DD} = 4.5V - 5.5V
- 42 CMOS Bi-directional I/O Pins (Including one open-drain output PortC.3)
- Built-in Pull-high Resistor For PORTA - PORTK
- 8-Level Stack (Including Interrupts)
- Two 8-bit and One 16-bit Auto Re-loaded Timer/Counter
- LCD Driver:
  - 16 SEG X 8 COM (1/8 Duty, 1/4 Bias)
  - 18 SEG X 6 COM (1/6 Duty, 1/3 Bias)
  - 20 SEG X 4 COM (1/4 Duty, 1/3 Bias)
- LED Driver:
  - 8 SEG X 6 COM (1/6 Duty)
  - 8 SEG X 5 COM (1/5 Duty)
  - 8 SEG X 4 COM (1/4 Duty)
- Powerful Interrupt Sources:
  - Timer0 Interrupt
  - Timer1 Interrupt
  - Timer2 Interrupt
  - External Interrupts (PORTB & PORTC Falling Edge Interrupts, A/D Interrupt, Key Scan Interrupt)
- Oscillator (Code Option)
  - Crystal Oscillator: 32.768kHz, 400kHz - 8MHz
  - Ceramic Resonator: 400kHz - 8MHz
  - External RC Oscillator: 400kHz - 8MHz
  - Internal RC Oscillator: 4MHz ±5%
- One Built-in PLL Oscillator (1, 2, 4, 8MHz)
- Instruction Cycle Time (4/f_{OSC})
- 10 Channels 10-Bit Resolution Analog/Digital Converter (ADC)
- 2 Channel Tone Generators
- Built-in Automatic Key Scanner
- Zero Cross Detect Function for AC Power Line
- Read ROM Data Table Function (RDT)
- One Channel 8+2Bit PWM Output
- Reset
  - Built-in Watchdog Timer (WDT) [(Code Option)]
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR) [(Code Option)]
- Two-Level Low Voltage Reset (LVR) (Code Option)
- Two Low Power Operation Modes: HALT and STOP
- OTP Type/Code Protection (SH69P55A)
- MASK Type (SH69K55A)
- 28-pin SOP package; 44-pin QFP package; 32-pin DIP package

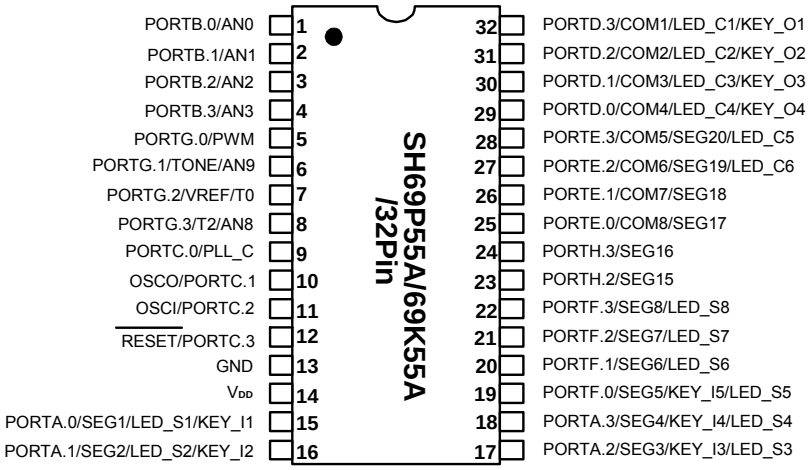
General Description

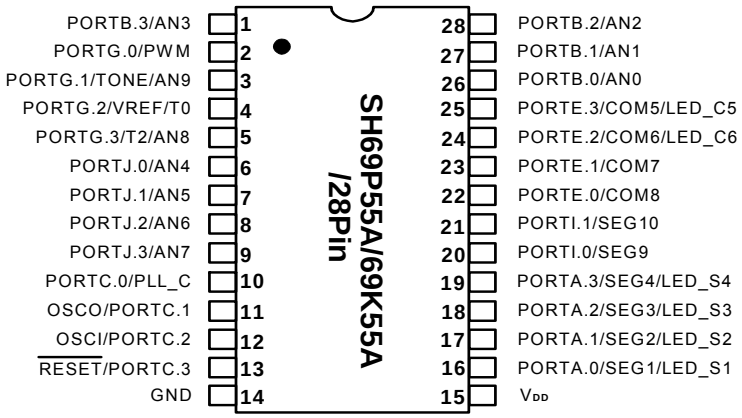
SH69P55A/69K55A is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, RAM, ROM, timer, LCD/LED driver, I/O ports, watchdog timer, 10 channels 10-bit resolution ADC, low voltage reset, automatic key scan, PLL and Zero Cross Detect function. The SH69P55A/69K55A is suitable for washing machine and micro-wave oven etc. application.

Pin Configuration (44 Pin)

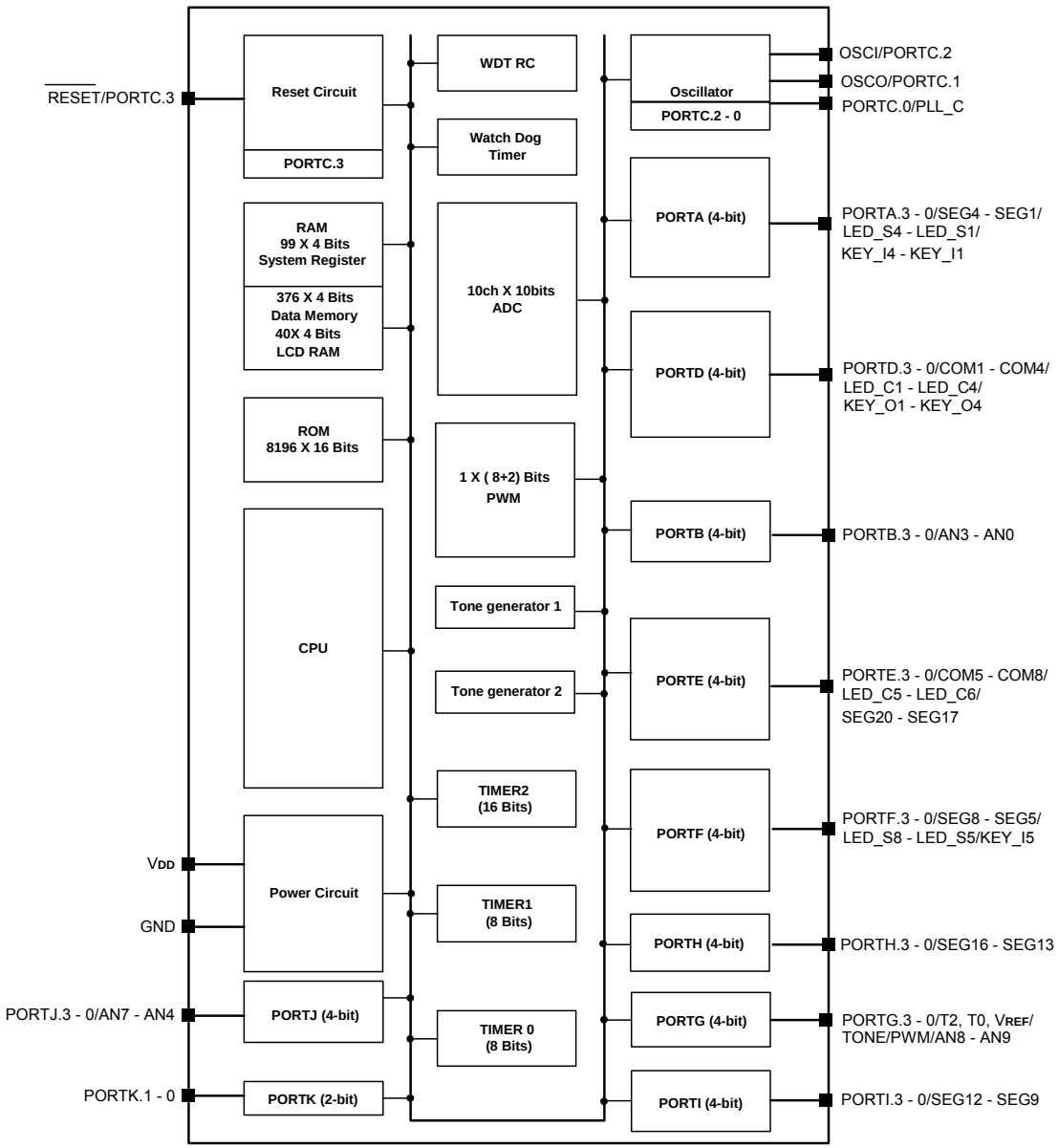


Pin Configuration (32 Pin & 28 Pin)





Block Diagram



Pin Descriptions

Pin No.			Pad No.	Pin Name	I/O	Description
44 pin	28 pin	32 pin				
44	4	7	1	PORTG.2 /T0 /VREF	I/O I I	Bit programmable I/O Timer0 Clock/Counter input pin. (Schmitt trigger input) External ADC VREF input
1	5	8	2	PORTG.3 /T2 /AN8	I/O I I	Bit programmable I/O Timer2 Clock/Counter input pin. (Schmitt trigger input) ADC input channel 8
3 - 2	-	-	4 - 3	PORTK.1 - 0	I/O	Bit programmable I/O
7 - 4	9 - 6	-	8 - 5	PORTJ.3 - 0 /AN7 - AN4	I/O I	Bit programmable I/O ADC input channel 7 - 4
8	10	9	10	PORTC.0 /PLL_C	I/O I P	Bit programmable I/O (code option) Vector Interrupt (Active falling edge by system register setup) Built-in PLL Connect with external capacitor
9	11	10	11	PORTC.1 /OSCO	I/O I I/O	Bit programmable I/O (code option) Vector Interrupt (Active falling edge by system register setup) OSC output pin. No output in RC mode
10	12	11	12	PORTC.2 /OSCI	I/O I I	Bit programmable I/O (code option) Vector Interrupt (Active falling edge by system register setup) OSC input pin, connected to a crystal, ceramic or external resistor
11	13	12	13	$\overline{\text{RESET}}$ /PORTC.3	I I I/O	Reset pin input (active low, Schmitt trigger input) Vector Interrupt (Active falling edge by system register setup) Bit programmable I/O, open-drain
12	14	13	9, 14, 35, 36, 43	GND	P	Ground pin
13	15	14	15,16	VDD	P	Power supply pin
17 - 14	19 - 16	18 - 15	20 - 17	PORTA.3 - 0 /SEG4 - SEG1 /LED_S4 - LED_S1 /KEY_I4 - KEY_I1	I/O O O I	Bit programmable I/O SEG4 - SEG1 signal output for LCD display SEG4 - SEG1 signal output for LED display Input for automatic key scan
18	-	19	21	PORTF.0 /SEG5 /LED_S5 /KEY_I5	I/O O O I	Bit programmable I/O SEG5 signal output for LCD display SEG5 signal output for LED display Input for automatic key scan
21 - 19	-	22 - 20	24 - 22	PORTF.3 - 1 /SEG8 - SEG6 /LED_S8 - LED_S6	I/O O O	Bit programmable I/O SEG8 - SEG6 signal output for LCD display SEG8 - SEG6 signal output for LED display
23 - 22	21 - 20	-	26- 25	PORTI.1 - 0 /SEG10 - SEG9	I/O O	Bit programmable I/O SEG10 - SEG9 signal output for LCD display
25 - 24	-	-	28 - 27	PORTI.3 - 2 /SEG12 - SEG11	I/O O	Bit programmable I/O SEG12 - SEG11 signal output for LCD display
27 - 26	-	-	30 - 29	PORTH.1 - 0 /SEG14 - SEG13	I/O O	Bit programmable I/O SEG14 - SEG13 signal output for LCD display
29 - 28	-	24 - 23	32 - 31	PORTH.3 - 2 /SEG16 - SEG15	I/O O	Bit programmable I/O SEG16 - SEG15 signal output for LCD display
31 - 30	23 - 22	26 - 25	34 - 33	PORTE.1 - 0 /COM7 - COM8 /SEG18 - SEG17	I/O O O	Bit programmable I/O COM7 - COM8 signal output for LCD display SEG18 - SEG17 signal output for LCD display

Pin Descriptions (continued)

Pin No.			Pad No.	Pin Name	I/O	Description
44 pin	28 pin	32 pin				
33 - 32	25 - 24	28 - 27	38 - 37	PORTE.3 - 2 /COM5 - COM6 /SEG20 - SEG19 /LED_C5 - LED_C6	I/O O O O	Bit programmable I/O COM5 - COM6 signal output for LCD display SEG20 - SEG19 signal output for LCD display COM5 - COM6 signal output for LED display
37 - 34	-	32 - 29	42 - 39	PORTD.3 - 0 /COM1 - COM4 /LED_C1 - LED_C4 /KEY_O1 - KEY_O4	I/O O O O	Bit programmable I/O COM1 - COM4 signal output for LCD display COM1 - COM4 signal output for LED display Output for automatic key scan
40 - 38	28 - 26	3 - 1	46 - 44	PORTB.2 - 0 /AN2 - AN0	I/O I I	Bit programmable I/O Vector Interrupt (Active falling edge by system register setup) ADC input channel 2 - 0
41	1	4	47	PORTB.3 /AN3	I/O I I	Bit programmable I/O Vector Interrupt (Active falling edge by system register setup) ADC input channel 3
42	2	5	48	PORTG.0 /PWM	I/O O	Bit programmable I/O PWM output
43	3	6	49	PORTG.1 /TONE /AN9	I/O O I	Bit programmable I/O TONE Generator output ADC input channel 9

Which, I: Input; O: Output; P: Power; Z: High impedance

OTP Programming Pin Description* (OTP Program Mode)

Pin No.			Pad No.	Symbol	I/O	Sharing Pin	Description
44 pin	28 pin	32 pin					
13	15	14	14, 15	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
11	13	12	12	V_{PP}	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11V)
12	14	13	13	GND	P	GND	Ground
10	12	11	11	SCK	I	OSCI	Programming Clock input pin
14	16	15	16	SDA	I/O	PORTA.0	Programming Data pin

*: Only SH69P55A has the OTP Program Mode, SH69K55A has not the OTP Program Mode.

Functional Descriptions

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range is 000H--3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $02F, $380 - $3AF, $3C0 - $3C2
Data memory: $030 - $1A7
LCD RAM space: $300 - $313, $320 - $333

RAM Bank Table:

Bank 0 B = 0	**Bank 1** B = 1	**Bank 2** B = 2	**Bank 3** B = 3	**Bank 4** B = 4	**Bank 5** B = 5	**Bank 6** B = 6	**Bank 7** B = 7
$000 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3AF, $3C0 - $3C2

Where, B: RAM bank bit use in instructions

2.2. Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IET0	IET1	IET2	IEEX	R/W	Interrupt enable flags register
$01	IRQT0	IRQT1	IRQT2	IRQEX	R/W	Interrupt request flags register
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register Bit3: T0 signal source select register
$03	T0E	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register Bit3: T0 signal edge select register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter high nibble register
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter low nibble register
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter high nibble register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	VREF	ACR2	ACR1	ACR0	R/W	Bit2-0: A/D port configuration control register Bit3: Select Internal/External reference voltage register
$14	ADCON	CH2	CH1	CH0	R/W	Bit2-0: ADC channel control register Bit3: ADC module operate control register
$15	T2E	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 pre-scaler register Bit3: T2 external signal edge select register
$16	FS1	FS0	OXS	OXON	R/W	Bit0: Turn on PLL register Bit1: clock source select (1: PLL, 0: 32.768kHz) register Bit3-2: PLL Frequency select register
$17	LVR	-	-	-	R/W	Bit3: Low Voltage Reset flag register (Read and Write 0 only)
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control register
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watch dog timer control register Bit3: Watchdog timer overflow flag register (Read only)
$1F	-	-	BNK1	BNK0	R/W	Bit1-0: ROM Bank register

Configuration of System Register (continued1):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWMS	TCK1	TCK0	PWM_EN	R/W	Bit0: PWM output enable control register Bit2-1: PWM clock control register Bit3: PWM output mode of duty cycle control register
$21	PP.3	PP.2	PP.1	PP.0	R/W	PWM period low nibble register
$22	PP.7	PP.6	PP.5	PP.4	R/W	PWM period high nibble register
$23	-	FSTP	-	-	R/W	Bit2: 32.768kHz oscillator is closed in the stop
$24	-	-	PDF.1	PDF.0	R/W	PWM duty fine-tune bits register (2 bits)
$25	PD.3	PD.2	PD.1	PD.0	R/W	PWM duty low nibble register (4 bits)
$26	PD.7	PD.6	PD.5	PD.4	R/W	PWM duty high nibble register (4bits)
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select register Bit2: Select directive edge active enable register Bit3: Set Timer2 function start register
$28	KEYNUM1	KEYNUM0	KEYEND	KEYEN	R/W R	Bit0: key scan enable register Bit1: key scan end/processing register Bit3-2: key scan result register
$29	LCDON	DUTY2	DUTY1	DUTY0	R/W	Bit2-0: Set duty and com register Bit3: LCD display on control register
$2A	-	-	-	-	R/W	Reserved
$2B	LEDEN	LEDON	EDUTY1	EDUTY0	R/W	Bit1-0: Set duty register Bit2: Turn on LED driver register Bit3: Enable LED driver register
$2C	KEYC3	KEYC2	KEYC1	KEYC0	R	Bit3-0: the result of key scan on KEY_O4 - 1 register
$2D	KEYL3	KEYL2	KEYL1	KEYL0	R	Bit3-0: the result of key scan on KEY_I5 - 1 register
$2E	RLCD	PS2	PS1	PS0	R/W	Bit2-0: Configuration the segment register Bit3: LCD bias resistor set register
$2F	GO/$\overline{\text{DONE}}$	TADC1	TADC0	-	R/W	Bit2-1: A/D Conversion Time control register Bit3: ADC startup/status flag register
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register
$384	T2D.3	T2D.2	T2D.1	T2D.0	R/W	Timer2 load/counter low nibble register
$385	T2D.7	T2D.6	T2D.5	T2D.4	R/W	Timer2 load/counter middle_L nibble register
$386	T2D.11	T2D.10	T2D.9	T2D.8	R/W	Timer2 load/counter middle_H nibble register
$387	T2D.15	T2D.14	T2D.13	T2D.12	R/W	Timer2 load/counter high nibble register
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags register
$389	PBIF.3	PBIF.2	PBGIF.1	PBIF.0	R/W	PORTB interrupt request flags register
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	R/W	PORTC interrupt enable flags register
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	R/W	PORTC interrupt request flags register
$38C	-	-	KEYIE	ADIE	R/W	Bit0: AD interrupt enable flag register Bit1: Key scan interrupt enable flag register
$38D	-	-	KEYIF	ADIF	R/W	Bit0: AD interrupt request flag register Bit1: Key scan interrupt request flag register
$38E	PG.3	PG.2	PG.1	PG.0	R/W	PORTG data register
$38F	PH.3	PH.2	PH.1	PH.0	R/W	PORTH data register

Configuration of System Register (continued2):

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$390	PI.3	PI.2	PI.1	PI.0	R/W	PORTI data register
$391	PJ.3	PJ.2	PJ.1	PJ.0	R/W	PORTJ data register
$392	-	-	PK.1	PK.0	R/W	PORTK data register
$393	PGCR.3	PGCR.2	PGCR.1	PGCR.0	R/W	PORTG input/output control register
$394	PHCR.3	PHCR.2	PHCR.1	PHCR.0	R/W	PORTH input/output control register
$395	PICR.3	PICR.2	PICR.1	PICR.0	R/W	PORTI input/output control register
$396	PJCR.3	PJCR.2	PJCR.1	PJCR.0	R/W	PORTJ input/output control register
$397	-	-	PKCR.1	PKCR.0	R/W	PORTK input/output control register
$398	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull high control register
$399	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull high control register
$39A	-	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull high control register
$39B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull high control register
$39C	PPECR.3	PPECR.2	PPECR.1	PPECR.0	R/W	PORTE pull high control register
$39D	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	R/W	PORTF pull high control register
$39E	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	R/W	PORTG pull high control register
$39F	PPHCR.3	PPHCR.2	PPHCR.1	PPHCR.0	R/W	PORTH pull high control register
$3A0	PPICR.3	PPICR.2	PPICR.1	PPICR.0	R/W	PORTI pull high control register
$3A1	PPJCR.3	PPJCR.2	PPJCR.1	PPJCR.0	R/W	PORTJ pull high control register
$3A2	-	-	PPKCR.1	PPKCR.0	R/W	PORTK pull high control register
$3A3	TG1.3	TG1.2	TG1.1	TG1.0	R/W	Tone generator 1 low nibble register
$3A4	TG1.7	TG1.6	TG1.5	TG1.4	R/W	Tone generator 1 middle nibble register
$3A5	TG1.11	TG1.10	TG1.9	TG1.8	R/W	Tone generator 1 high nibble register
$3A6	TG2.3	TG2.2	TG2.1	TG2.0	R/W	Tone generator 2 low nibble register
$3A7	TG2.7	TG2.6	TG2.5	TG2.4	R/W	Tone generator 2 middle nibble register
$3A8	TG2.11	TG2.10	TG2.9	TG2.8	R/W	Tone generator 2 high nibble register
$3A9	TV1.3	TV1.2	TV1.1	TV1.0	R/W	Tone generator 1 volume low nibble register
$3AA	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Bit2-0: Tone generator 1 volume high nibble register Bit3: Tone generator 1 enable register
$3AB	TV2.3	TV2.2	TV2.1	TV2.0	R/W	Tone generator 2 volume low nibble register
$3AC	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Bit2-0: Tone generator 2 volume high nibble register Bit3: Tone generator 2 enable register
$3AD	-	-	A1	A0	R	ADC data low nibble register
$3AE	A5	A4	A3	A2	R	ADC data middle nibble register
$3AF	A9	A8	A7	A6	R	ADC data high nibble register
$3C0	T1S	-	-	-	R/W	T1 signal source select register
$3C1	LPS3	LPS2	LPS1	LPS0	R/W	Bit3-0: LCD frame frequency control register
$3C2	ACR3	CH3	-	-	R/W	Bit3: A/D port configuration control register Bit2: ADC channel control register

3. ROM

The ROM can address 8192 X 16 bits of program area from $000 to $1FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to TIMER0 interrupt service routine
$002	JMP*	Jump to TIMER1 interrupt service routine
$003	JMP*	Jump to TIMER2 interrupt service routine
$004	JMP*	Jump to External interrupts service routine

* JMP instruction can be replaced by any instruction.

3.2. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The bank switch technique is used to extend the CPU address space. The lower 2K of the CPU address space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU address space maps to one of the three banks (BNK3-0 = 0, 1, 2) of the upper 6K of ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space		
	BNK = $00	BNK = $01	BNK = $02
Low 2K address	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
Upper 2K address	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)

4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset	WDT Reset /Low Voltage Reset
$00	IET0	IET1	IET2	IEEX	0000	0000
$01	IRQT0	IRQT1	IRQT2	IRQEX	0000	0000
$02	T0S	T0M.2	T0M.1	T0M.0	0000	uuuu
$03	T0E	T1M.2	T1M.1	T1M.0	0000	uuuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	VREF	ACR2	ACR1	ACR0	0000	uuuu
$14	ADCON	CH2	CH1	CH0	0000	0uuu
$15	T2E	T2SC.2	T2SC.1	T2SC.0	0000	uuuu
$16	FS1	FS0	OXS	OXON	0000	uuuu
$17	LVR	-	-	-	0---	*---
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	0000	0000
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	#000
$1F	-	-	BNK1	BNK0	--00	--00
$20	PWMS	TCK1	TCK0	PWM_EN	0000	uuu0
$21	PP.3	PP.2	PP.1	PP.0	xxxx	uuuu
$22	PP.7	PP.6	PP.5	PP.4	xxxx	uuuu
$23	-	FSTP			-0--	-0--

System Register State (Continued1):

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset	WDT Reset /Low Voltage Reset
$24			PDF.1	PDF.0	--xx	--uu
$25	PD.3	PD.2	PD.1	PD.0	xxxx	uuuu
$26	PD.7	PD.6	PD.5	PD.4	xxxx	uuuu
$27	T2GO	DEC	TM2S1	TM2S0	0000	0uuu
$28	KEYNUM1	KEYNUM0	KEYEND	KEYEN	0000	000u
$29	LCDON	DUTY2	DUTY1	DUTY0	0000	uuuu
$2A	-	-	-	-	----	----
$2B	LEDEN	LEDON	EDUTY1	EDUTY0	0000	uuuu
$2C	KEYC3	KEYC2	KEYC1	KEYC0	0000	uuuu
$2D	KEYL3	KEYL2	KEYL1	KEYL0	0000	uuuu
$2E	RLCD	PS2	PS1	PS0	0000	uuuu
$2F	GO/$\overline{\text{DONE}}$	TADC1	TADC0	-	000-	0uu-
$380	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$381	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$382	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$383	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu
$384	T2D.3	T2D.2	T2D.1	T2D.0	xxxx	xxxx
$385	T2D.7	T2D.6	T2D.5	T2D.4	xxxx	xxxx
$386	T2D.11	T2D.10	T2D.9	T2D.8	xxxx	xxxx
$387	T2D.15	T2D.14	T2D.13	T2D.12	xxxx	xxxx
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	0000	0000
$389	PBIF.3	PBIF.2	PBIF.1	PBIF.0	0000	0000
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	0000	0000
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	0000	0000
$38C	-		KEYIE	ADIE	--00	--00
$38D	-	-	KEYIF	ADIF	--00	--00
$38E	PG.3	PG.2	PG.1	PG.0	0000	0000
$38F	PH.3	PH.2	PH.1	PH.0	0000	0000
$390	PI.3	PI.2	PI.1	PI.0	0000	0000
$391	PJ.3	PJ.2	PJ.1	PJ.0	0000	0000
$392	-	-	PK.1	PK.0	--00	--00
$393	PGCR.3	PGCR.2	PGCR.1	PGCR.0	0000	0000
$394	PHCR.3	PHCR.2	PHCR.1	PHCR.0	0000	0000
$395	PICR.3	PICR.2	PICR.1	PICR.0	0000	0000
$396	PJCR.3	PJCR.2	PJCR.1	PJCR.0	0000	0000
$397	-	-	PKCR.1	PKCR.0	--00	--00
$398	PPACR.3	PPACR.2	PPACR.1	PPACR.0	0000	0000

System Register State (Continued2):

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset	WDT Reset /Low Voltage Reset
$399	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	0000	0000
$39A	-	PPCCR.2	PPCCR.1	PPCCR.0	-000	-000
$39B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	0000	0000
$39C	PPECR.3	PPECR.2	PPECR.1	PPECR.0	0000	0000
$39D	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	0000	0000
$39E	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	0000	0000
$39F	PPHCR.3	PPHCR.2	PPHCR.1	PPHCR.0	0000	0000
$3A0	PPICR.3	PPICR.2	PPICR.1	PPICR.0	0000	0000
$3A1	PPJCR.3	PPJCR.2	PPJCR.1	PPJCR.0	0000	0000
$3A2	-	-	PPKCR.1	PPKCR.0	--00	--00
$3A3	TG1.3	TG1.2	TG1.1	TG1.0	xxxx	uuuu
$3A4	TG1.7	TG1.6	TG1.5	TG1.4	xxxx	uuuu
$3A5	TG1.11	TG1.10	TG1.9	TG1.8	xxxx	uuuu
$3A6	TG2.3	TG2.2	TG2.1	TG2.0	xxxx	uuuu
$3A7	TG2.7	TG2.6	TG2.5	TG2.4	xxxx	uuuu
$3A8	TG2.11	TG2.10	TG2.9	TG2.8	xxxx	uuuu
$3A9	TV1.3	TV1.2	TV1.1	TV1.0	xxxx	uuuu
$3AA	TG1EN	TV1.6	TV1.5	TV1.4	xxxx	uuuu
$3AB	TV2.3	TV2.2	TV2.1	TV2.0	xxxx	uuuu
$3AC	TG2EN	TV2.6	TV2.5	TV2.4	xxxx	uuuu
$3AD	-	-	A1	A0	--xx	--uu
$3AE	A5	A4	A3	A2	xxxx	uuuu
$3AF	A9	A8	A7	A6	xxxx	uuuu
$3C0	T1S	-	-	-	0---	u---
$3C1	LPS3	LPS2	LPS1	LPS0	0000	uuuu
$3C2	ACR3	CH3	-	-	00--	uu--

Legend: x = unknown; u = unchanged; - = unimplemented read as '0'.

*, #: For the detail information, refer to the following table:

	WDT Reset	LVR Reset	WDT Reset & LVR Reset	Power on Reset/Pin Reset
*	0	1	1	0
#	1	0	1	0

4.2. Others Initial State:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

SH69P55A/69K55A has one clock source, which is determined in Code options. The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

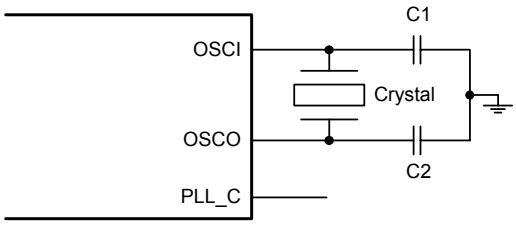
System clock fSYS = fosc/4.

5.1. Instruction Cycle Time:

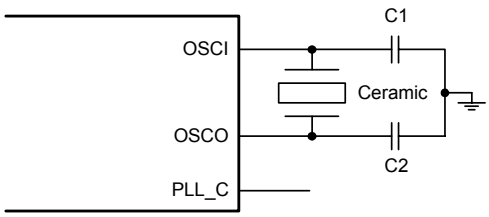
(1) 4/32.768kHz (≈ 122μs) for 32.768kHz oscillator.
(2) 4/8MHz (= 0.5μs) for 8 MHz oscillator.

5.2. Oscillator Type

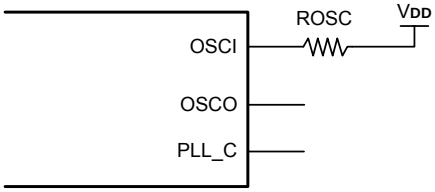
(1) Crystal Oscillator: 32.768kHz or 400kHz - 8MHz



(2) Ceramic Resonator: 400kHz - 8MHz

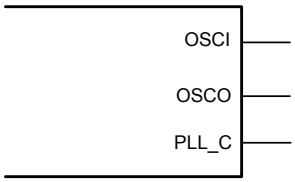


(3) RC Oscillator: 400kHz - 8MHz



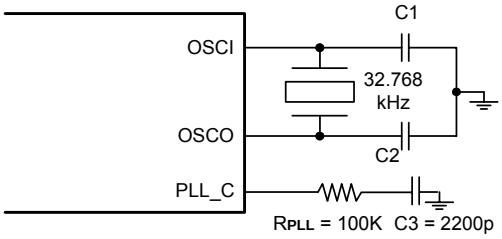
External RC

(4) RC Oscillator: 4MHz



Internal RC

(5) PLL Oscillator (1, 2, 4, 8MHz)



Note:

- If the external RC oscillator is selected, OSCO pin is used as the I/O port (PORTC.1).
- If the internal RC oscillator is selected, OSCO pin is used as the I/O port (PORTC.1) and OSCI pin is used as the I/O port (PORTC.2).
- If the PLL is disabled, PLL_C is used as the I/O port (PORTC.0).

5.3. Control of Phase Locked Loop Clock Source (PLL)

A phase locked loop (PLL) is built in SH69P55A/69K55A, which can provide up to 8MHz clock source when the 32.768kHz oscillator is selected. PLL control register can decide whether PLL enable or disable. When PLL is enabled, PORTC.0 is shared as PLL capacitor connecting port, which is connected with a RC network. When PLL is disabled, PORTC.0 is shared as a normal I/O.

PLL Control Register $16

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	FS1	FS0	OXS	OXON	R/W	Bit0: Turn on PLL register Bit1: clock source select (1: PLL, 0: 32.768kHz) register Bit3 - 2: PLL Frequency select register
	X	X	X	0	R/W	Turn off PLL
	X	X	X	1	R/W	Turn on PLL, when 32.768kHz oscillator is selected in code option
	X	X	0	X	R/W	Clock source is selected as 32.768kHz oscillator
	X	X	1	1	R/W	Clock source is selected as PLL
	0	0	1	1	R/W	PLL provides 8.126MHz clock signal for clock source (LVR voltage range must be selected as 4V in the code option)
	0	1	1	1	R/W	PLL provides 4.063MHz clock signal for clock source
	1	0	1	1	R/W	PLL provides 2.031MHz clock signal for clock source
	1	1	1	1	R/W	PLL provides 1.016MHz clock signal for clock source

Note:

1. Usage of PLL:
   First, configure the FS1 and FS0 in PLL control register.
   Second, set OXON = 1 and turn on the PLL.
   Third, wait at least 2ms.
   Last, set OXS = 1 and select PLL as the system clock source.
2. If LVR voltage range is selected as 2.5V in the code option, the PLL only provides 1, 2, 4MHz clock signal for clock source.

System Register $23

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$23	-	FSTP	-	-	R/W	Bit2: 32.768kHz oscillator is closed in the stop
	X	1	X	X	R/W	32.768kHz oscillator is closed in the stop, if 32.768kHz is selected in the code option
	X	0	X	X	R/W	32.768kHz oscillator is not closed in the stop, if 32.768kHz oscillator is selected in the code option

5.4. Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
455kHz	47 - 100pF	47 - 100pF	ZTB 455KHz	Vectron International
			ZT 455E	Shenzhen DGJB Electronic Co.,Ltd.
3.58MHz	-	-	ZTT 3.580M	Vectron International
			ZT 3.58M*	Shenzhen DGJB Electronic Co.,Ltd.
4MHz	-	-	ZTT 4.000M	Vectron International
			ZT 4M*	Shenzhen DGJB Electronic Co.,Ltd.

*- The specified ceramic resonator has internal built-in load capacity

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	**C1**	**C2**		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ3x8)	KDS
			φ3x8 - 32.768KHz	Vectron International
4MHz	8 - 15pF	8 - 15pF	HC-49U/S 4.000MHz	Vectron International
			49S-4.000M-F16E	Shenzhen DGJB Electronic Co.,Ltd.
8MHz	8 - 15pF	8 - 15pF	HC-49U/S 8.000MHz	Vectron International
			49S-8.000M-F16E	Shenzhen DGJB Electronic Co.,Ltd.

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures

6. I/O Port

The SH69P55A/69K55A provides 42 bi-directional I/O ports including one open-drain output. The PORT data is put in register $08 - $0D and $38E - $392. The PORT control register ($18 - $1D and $393 - $397) controls the PORT as input or output. Each I/O port (excluding those open drain output ports) contains pull-high resistor, which is controlled by the value of the corresponding bit in the port pull-high control register ($398 - $3A2), independently.

- When the port is selected as an input port, write “1” to the relevant bit in the port pull-high control register ($398 - $3A2) could turn on the pull high resistor and write “0” could turn off the pull high resistor.
- When the port is selected as output port, the pull high resistor will be turned off automatically, regardless the value of the corresponding bit in the port pull high control register ($398 - $3A2).
- When PORTB and PORTC are selected as the digital input direction, they can active port interrupt by falling edge (if port interrupt is enabled).

System Register $08 - $0D, $38E - $392: Port Data Register (PDR)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF data register
$38E	PG.3	PG.2	PG.1	PG.0	R/W	PORTG data register
$38F	PH.3	PH.2	PH.1	PH.0	R/W	PORTH data register
$390	PI.3	PI.2	PI.1	PI.0	R/W	PORTI data register
$391	PJ.3	PJ.2	PJ.1	PJ.0	R/W	PORTJ data register
$392	-	-	PK.1	PK.0	R/W	PORTK data register

System Register $18 - $1D, $393 - $397: Port Control Register (PCR)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control register
$393	PGCR.3	PGCR.2	PGCR.1	PGCR.0	R/W	PORTG input/output control register
$394	PHCR.3	PHCR.2	PHCR.1	PHCR.0	R/W	PORTH input/output control register
$395	PICR.3	PICR.2	PICR.1	PICR.0	R/W	PORTI input/output control register
$396	PJCR.3	PJCR.2	PJCR.1	PJCR.0	R/W	PORTJ input/output control register
$397	-	-	PKCR.1	PKCR.0	R/W	PORTK input/output control register

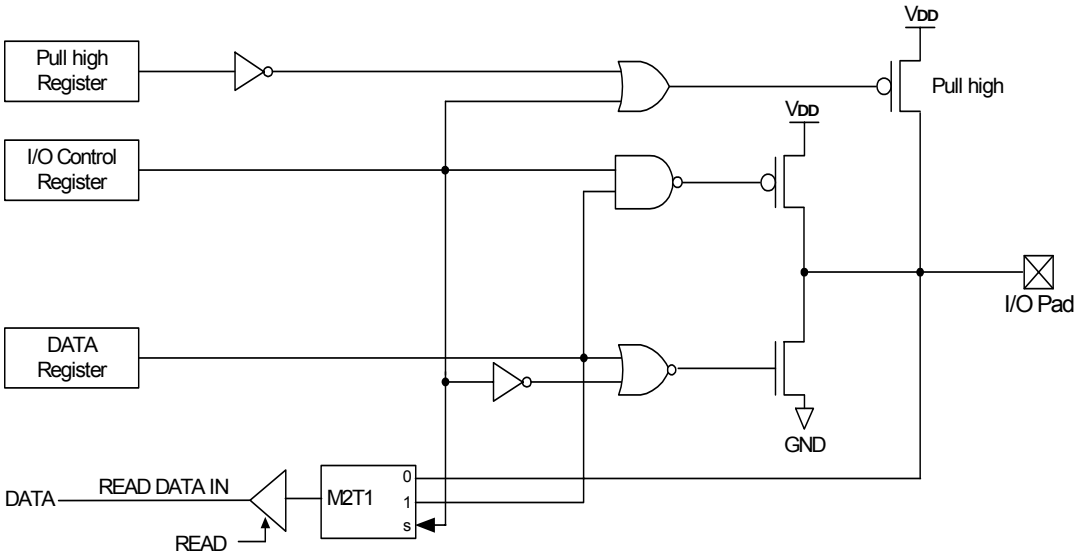
PA (/B/C/D/E/F/G/H/I/J) PCR.n, (n = 0, 1, 2, 3), PKPCR.n (n = 0, 1)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

System Register $398 - $3A2: Port Pull-high Control Register (PPCR)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$398	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull high control register
$399	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull high control register
$39A	-	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull high control register
$39B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull high control register
$39C	PPECR.3	PPECR.2	PPECR.1	PPECR.0	R/W	PORTE pull high control register
$39D	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	R/W	PORTF pull high control register
$39E	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	R/W	PORTG pull high control register
$39F	PPHCR.3	PPHCR.2	PPHCR.1	PPHCR.0	R/W	PORTH pull high control register
$3A0	PPICR.3	PPICR.2	PPICR.1	PPICR.0	R/W	PORTI pull high control register
$3A1	PPJCR.3	PPJCR.2	PPJCR.1	PPJCR.0	R/W	PORTJ pull high control register
$3A2	-	-	PPKCR.1	PPKCR.0	R/W	PORTK pull high control register

PA (/B/D/E/F/G/H/I/J) CR.n, (n = 0, 1, 2, 3), PKCR.n (n = 0, 1), PCCR.n (n = 0, 1, 2)
0: Disable internal pull-high resistor. (Power on initial)
1: Enable internal pull-high resistor.

Equivalent Circuit for a Single I/O Pin



PORTA.3 - 0 can be shared with SEG4 - SEG1 signal output for LCD or LED display, KEY_I4 - KEY_I1 input for automatic key scan.

PORTB.3 - 0 can be shared with ADC AN3 - 0 input channel.

PORTC.0 can be shared with PLL_C (code option), if PLL is enabled, a RC network must be connected with this port.

The OSCO pin can be shared with PORTC.1 if the SH69P55A/69K55A uses the external clock or the RC oscillator as the system oscillation.

The OSCI pin can be shared with PORTC.2, if the SH69P55A/69K55A uses the internal RC oscillator as the system oscillation.

The RESET pin can be shared with PORTC.3 controlled by the code option. PORTC.3 is open-drain output.

PORTD.3 - 0 can be shared with COM1 - COM4 signal output for LCD or LED display, KEY_O1 - KEY_O4 output for automatic key scan.

PORTE.3 - 0 can be shared with COM5 - COM8 or SEG20 - SEG17 signal output for LCD display, and PORTE.3 - 2 can be shared with COM5 - 6 signal output for LED display.

PORTF.3 - 0 can be shared with SEG8 - SEG5 signal output for LCD or LED display, and PORTF0 can be shared with KEY_I5 input for automatic key scan.

PORTG.0 can be shared with PWM output.

PORTG.1 can be shared with TONE output or ADC AN9.

PORTG.2 can be shared with T0 input or external ADC V_{REF} input.

PORTG.3 can be shared with T2 input or ADC AN8.

PORTH.3 - 0 can be shared with SEG16 - SEG13 signal output for LCD display.

PORTI.3 - 0 can be shared with SEG12 - SEG9 signal output for LCD display.

PORTJ.3 - 0 can be shared with ADC AN7 - 4 input channels.

IMPORTANT:

- In 32pin package, PORTH.0, PORTH.1 and PORTI - K must be selected to be output '0' (Port Control Register (PCR): $394 = xx11B, $395 - $396 = 1111B, $397 = 0011B and Port Data Register (PDR): $38F = xx00B and $390 - $391 = 0000B, $392 = 0000B).
- In 28pin package, PORTD, PORTF, PORTH, PORTI.3 - 2 and PORTK must be selected to be output '0' (Port Control Register (PCR): $1B $1D, $394 = 1111B, $395 = 11xxB, $397 = 0011B and Port Data Register (PDR): $0B $0D, $38F = 0000B, $390 = 00xxB, $392 = 0000B).
- In SH69P55A/69K55A, each output port contains a latch, which can hold the output data. Writing the port data register (PDR) under the output mode can directly transfers data to the corresponding pin. All input ports do not have latches, so the external input data should be held externally until the input data is get from outside. The contents of the port control register (PCR) determines each bi-directional I/O port to be an input or output port, where writing '0' to port control register (PCR) represents the input mode and '1' for the output mode. When a digital I/O port is selected to be an output port, the value of the associated port bit actually represents the value of the output data latch, not the voltage on the pin. When a digital I/O port is selected to be input, the value of the associated port bit represents the status on the corresponding pin. The output data latch can be written all the while, regardless of the state of the port control register (PCR). Therefore, when using ports in a mixture of input and output modes, the contents of the output latches for those ports that are selected as inputs may be rewritten by execution of logical instructions. So it is strongly recommended that writing proper data to the port data register (PDR) before changing the corresponding bits in the port control register (PCR) from the input mode to the output mode can avoid glitches on the relevant pins.

■ **Port Interrupt**

The PORTB and PORTC are used as port interrupt sources. Since PORTB and PORTC are bit programmable I/Os, only when the PORTB and PORTC are selected as normal I/O input, the voltage transition from V_{DD} to GND applying to the digital input port can generate a port interrupt. When they are selected as analog input (such as ADC input), Port interrupt request cannot be generated.

The interrupt control flags are mapped on $388 - $38A of the system register. They can be accessed by the read/write operation. Those flags are clear to '0' at the initialization by the chip reset.

Port interrupts can be used to wake up the CPU from the HALT or the STOP mode.

System Register $388, $38A: Port Interrupt Enable Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags register
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	R/W	PORTC interrupt enable flags register

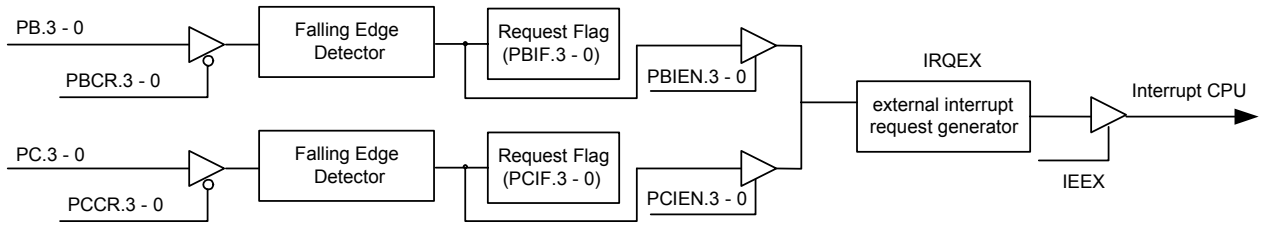
PB/CIEN.n, (n = 0, 1, 2, 3)
0: Disable port interrupt. (Power on initial)
1: Enable port interrupt.

System Register $389, $38B: Port Interrupt Request Flags Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$389	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags register
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	R/W	PORTC interrupt request flags register

PB/CIF.n, (n = 0, 1, 2, 3)
0: Port interrupt is not presented. (Power on initial)
1: Port interrupt is presented.
Only writing these bits to "0" is available.

Following is the port interrupt function block-diagram for reference.



Port Interrupt Programming Notes:

- Any one of PORTB & PORTC input pin transitions from V_{DD} to GND would set PBIF.x or PCIF.x to "1", in spite of level of the other pin of PORTB and PORTC.
- If PBIEN.x (or PCIEN.x) = 1and IEEX = 1, the x of PORTB (or PORTC) input pin transitions from V_{DD} to GND would generate an interrupt request (PBIF.x = 1 or PCIF.x = 1) and interrupt the CPU, in spite of level of the other pin of PORTB (or PORTC).

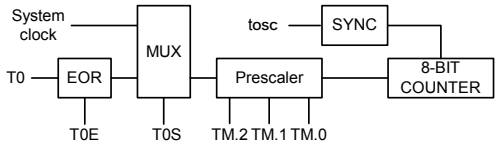
7. Timer

SH69P55A/69K55A has three timers: two 8-bit timers (Timer0, Timer1) and one 16-bit timer (Timer2).

The 8-bit timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer0/Timer1 block diagram.



The Timer0/Timer1 provides the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

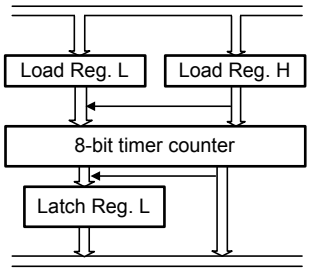
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



7.2. Timer0 and Timer1 Mode Register

The Timer can be programmed in several different prescalers by setting Timer Mode register (T0M, T1M).

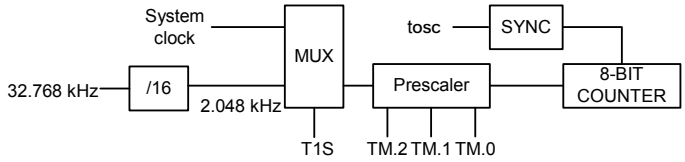
The clock source pre-scale by the 8-level counter first, then generate the output plus to timer counter. The Timer Mode registers (T0M, T1M) are 3-bit registers used for the timer control as shown in Table 1 and Table 2.

Table 1. Timer0 Mode Register ($02)

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

Table 2. Timer1 Mode Register ($03)

T1M.2	T1M.1	T1M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/2.048kHz
0	0	1	$/2^{9}$	System clock/2.048kHz
0	1	0	$/2^{7}$	System clock/2.048kHz
0	1	1	$/2^{5}$	System clock/2.048kHz
1	0	0	$/2^{3}$	System clock/2.048kHz
1	0	1	$/2^{2}$	System clock/2.048kHz
1	1	0	$/2^{1}$	System clock/2.048kHz
1	1	1	$/2^{0}$	System clock/2.048kHz



Also the clock source of Timer0 and Timer1 is set in timer control registers, as shown blow:

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0S	-	-	-	R/W	Bit3: T0 signal source select register
	0	X	X	X	R/W	Timer0 source is system clock
	1	X	X	X	R/W	Timer0 source is T0 input clock

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$03	T0E	-	-	-	R/W	Bit3: T0 signal edge select register
	0	X	X	X	R/W	Increment on high-to-low transition T0 input
	1	X	X	X	R/W	Increment on low-to-high transition T0 input

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C0	T1S	-	-	-	R/W	Bit3: T1 signal source select register*
	0	X	X	X	R/W	Timer1 source is system clock*
	1	X	X	X	R/W	Timer1 source is 2.048kHz*

*: The T1S register is available when the oscillator type is selected as 32.768kHz. Otherwise, the T1S register must be cleared to '0'.

7.3. External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer0 source, it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 tosc) and low (at least 2 tosc). When the prescaler ratio selects $/2^0$, it is the same as the system clock input.

The requirement is as follows:

T0H (T0 high time) $\geq$ 2 * tosc + ΔT

T0L (T0 low time) $\geq$ 2 * tosc + ΔT ; ΔT= 20ns

When another prescaler ratio is selected, the T0M is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$T0\ \text{high time} = T0\ \text{low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = prescaler value

The requirement is:

$$\frac{N * T0}{2} \geq 2 * t_{OSC} + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * t_{OSC} + 2 * \Delta T}{N}$$

So, the limitation is applied to the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

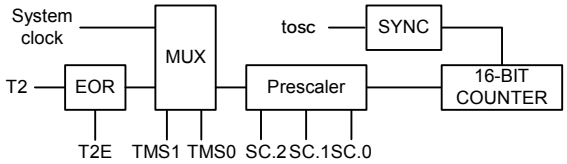
$$T0 = \text{Timer0 period} \geq \frac{4 * t_{OSC} + 2 * \Delta T}{N}$$

7.4. Timer2

Timer2 is a 16-bit timer and it has the following features:

- 16-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FFFF to $0000.

The following is a simplified Timer2 block diagram.



The Timer2 provides the following functions:

- Programmable interval timer function.
- Read counter value.

7.5. Timer2 Configuration and Operation

Timer2 consists of a 16-bit write-only timer load register (TL2L, TL2ML, TL2MH, TL2H) and a 16-bit read-only timer counter (TC2L, TC2ML, TC2MH, TC2H). Each of them has low-order digits and high-order digits. Writing data into the timer load register (TL2L, TL2ML, TL2MH, TL2H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FFFF to $0000.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

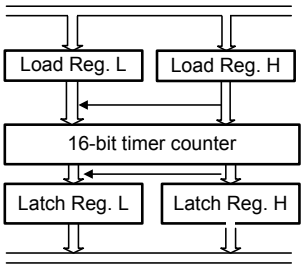
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.6. Timer2 Control Register

The Timer2 can be programmed in several different modes: timer, external event counter, and external trigger timer and pulse width measurement.

Timer2 Control Register: $27

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select register Bit3: Set Timer2 function start register
	X	X	0	0	R/W	Timer with internal system clock
	X	X	0	1	R/W	Event counter with external clock (T2 pin input)
	X	X	1	0	R/W	Timer with external trigger (T2 pin input)
	X	X	1	1	R/W	Pulse width measurement (T2 pin input)
	0	X	X	X	R/W	Timer/counter stops (Read: status; Write: command) (default)
	1	X	X	X	R/W	Timer/counter starts (Read: status; Write: command)

Note:

Before using event counter mode, timer with external trigger mode or pulse width measurement mode, the $3C2 bit3 must be cleared to 0.

(1) Timer Mode

In this mode, Timer2 is performed using the internal system clock. The contents of the Timer2 load register ($384 - $387) are loaded into the up-counter while the highest nibble ($387) has been written. The up-counter will start counting if the Timer2 control register ($27) T2GO (bit3) is set to 1. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) IET2 (bit1) is set to 1.

After the Timer2 control register ($27) T2GO (bit3) has been set to 1, writing the Timer2 load register ($384 - $387) can not affect the up-counter operating anymore. Only when the Timer2 control register ($27) T2GO (bit3) has been cleared to 0, the contents of the Timer2 load register ($384 - $387) will be loaded into the up-counter while the highest nibble ($387) is written.

Timer2 Pre-scaler Register: $15

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	T2E	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 pre-scaler register Bit3: T2 external signal edge select register
	X	0	0	0	R/W	Timer clock source: $f_{SYS}/2^{11}$
	X	0	0	1	R/W	Timer clock source: $f_{SYS}/2^{9}$
	X	0	1	0	R/W	Timer clock source: $f_{SYS}/2^{7}$
	X	0	1	1	R/W	Timer clock source: $f_{SYS}/2^{5}$
	X	1	0	0	R/W	Timer clock source: $f_{SYS}/2^{3}$
	X	1	0	1	R/W	Timer clock source: $f_{SYS}/2^{2}$
	X	1	1	0	R/W	Timer clock source: $f_{SYS}/2^{1}$
	X	1	1	1	R/W	Timer clock source: $f_{SYS}/2^{0}$
	0	X	X	X	R/W	Increment on high-to-low transition T2 input
	1	X	X	X	R/W	Increment on low-to-high transition T2 input

(2) External Event Counter Mode

In this mode, Timer2 is performed using the external clock via T2 pin (shared with PORTG3). Either the rising or falling edge can be selected with the external trigger controlled by the Timer2 pre-scaler register ($15) T2E (bit3). The contents of the Timer2 load register ($384 - $387) are loaded into the up-counter while the highest nibble ($387) has been written. The up-counter will start counting if the Timer2 control register ($27) T2GO (bit3) is set to 1. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) IET2 (bit1) is set to 1.

After the Timer2 control register ($27) T2GO (bit3) has been set to 1, writing the Timer2 load register ($384 - $387) can not affect the up-counter operating anymore. Only when the Timer2 control register ($27) T2GO (bit3) has been cleared to 0, the contents of the Timer2 load register ($384 - $387) will be loaded into the up-counter while the highest nibble ($387) is written.

The external clock source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high at least 2 t_{OSC} and low at least 2 t_{OSC}. In this mode, the pre-scaler circuit will not affect the external clock input. That means the input clock will bypass the pre-scaler circuit and disregards the value in Timer2 pre-scaler register. So, the limitation is applied to the external clock period time (T_E) described as follows:

$$T_E \text{ (period time)} \geq 4 * t_{OSC} + 2 * \Delta T \qquad ; \Delta T = 20ns$$

(3) External Trigger Timer Mode

In this mode, the counting is triggered by an external signal via T2 pin (shared with PORTG3). Either the rising or falling edge can be selected by setting the Timer2 pre-scaler register ($15) T2E (bit3). But the clock source of the up-counter is the internal system clock. The contents of the Timer2 load register ($384 - $387) are loaded into the up-counter while the highest nibble ($387) has been written. Only after the Timer2 control register ($27) T2GO (bit3) has been set to 1, a valid edge signal on the T2 input pin can start counting. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) IET2 (bit1) is set to 1. When the Timer2 interrupt is generated the up-counter is halted. The up-counter is restarted by the next valid edge of the T2 pin input.

When the Timer2 control register ($27) DEC (bit2) is set to 1, a valid rising (falling) edge signal on the T2 input pin can start counting, a valid falling (rising) edge signal on the T2 input pin will stop counting and The contents of the Timer2 load register ($384 - $387) are reloaded into the up-counter. Inputting a proper width pulse can generate interrupts. When the Timer2 control register ($27) DEC (bit2) is cleared to 0, the reverse directive edge input is ignored. The another valid edge input from T2 pin before the up-counter overflowing is also ignored.

After the Timer2 control register ($27) T2GO (bit3) is set to 1, writing the Timer2 counter register ($384 - $387) can not affect the up-counter operating anymore. Only when the Timer2 control register ($27) T2GO (bit3) has been cleared to 0, the contents of the Timer2 load register ($384 - $387) will be loaded into the up-counter while the highest nibble ($387) is written.

The T2 pin input signal must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high at least 1/2 $t_{Timer\ clock}$ and low at least 1/2 $t_{Timer\ clock}$. In this mode, the Timer clock is selected by the Timer2 pre-scaler register. So, the limitation is applied to the external clock period time (T_E) described as follows:

$$T_E \text{ (period time)} \geq 1 * t_{Timer\ clock} + 2 * \Delta T \quad ; \Delta T = 20ns$$

$$T_E \text{ (period time)} \geq (M * t_{OSC}) + 2 * \Delta T$$

where M = 2^3, 2^4, 2^5, 2^6, 2^8, 2^{10}, 2^{12} or 2^{14}

Timer2 Control Register: $27 (under the external trigger timer mode)

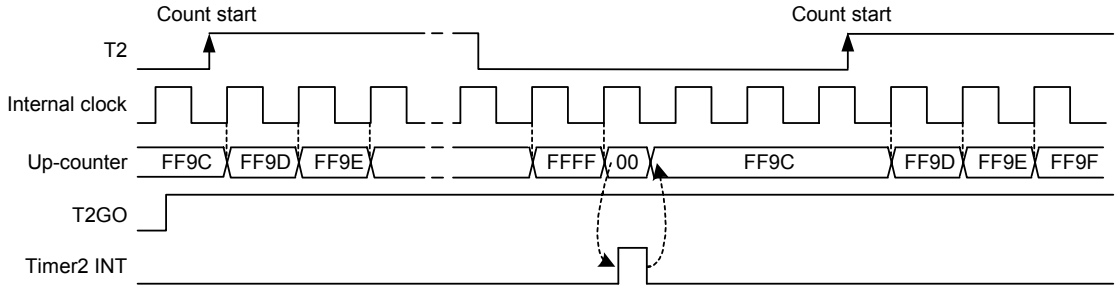
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select register Bit2: Reverse directive edge input control register
	X	0	1	0	R/W	Reverse directive edge input is ignored
	X	1	1	0	R/W	Reverse directive edge input reloads internal up-counter

Timer2 Pre-scaler Register: $15 (under the external trigger timer mode and pulse width measurement mode)

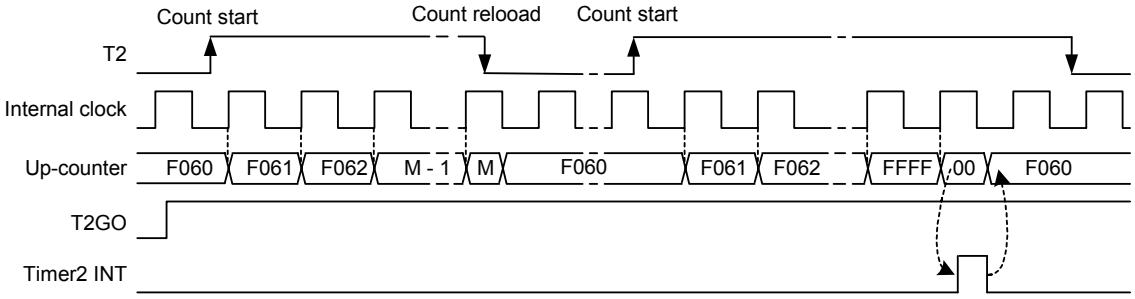
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	T2E	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 pre-scaler register Bit3: T2 external signal edge select
	X	0	0	0	R/W	Timer clock source: $f_{SYS}/2^{12}$
	X	0	0	1	R/W	Timer clock source: $f_{SYS}/2^{10}$
	X	0	1	0	R/W	Timer clock: source $f_{SYS}/2^8$
	X	0	1	1	R/W	Timer clock: source $f_{SYS}/2^6$
	X	1	0	0	R/W	Timer clock source: $f_{SYS}/2^4$
	X	1	0	1	R/W	Timer clock source: $f_{SYS}/2^3$
	X	1	1	0	R/W	Timer clock source: $f_{SYS}/2^2$
	X	1	1	1	R/W	Timer clock source: $f_{SYS}/2^1$
	0	X	X	X	R/W	T2 input falling edge active (Default)
	1	X	X	X	R/W	T2 input rising edge active

Timer2 Counter Register: $384 - $387

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$384	T2D.3	T2D.2	T2D.1	T2D.0	R/W	Timer2 load/counter low nibble register
$385	T2D.7	T2D.6	T2D.5	T2D.4	R/W	Timer2 load/counter middle_L nibble register
$386	T2D.11	T2D.10	T2D.9	T2D.8	R/W	Timer2 load/counter middle_H nibble register
$387	T2D.15	T2D.14	T2D.13	T2D.12	R/W	Timer2 load/counter high nibble register



Trigger Start (DEC = 0)



Trigger Start and Stop (DEC = 1)

(4) Pulse Width Measurement Mode

In this mode, Timer2 is performed using a special function under the timer mode in which counting is started on an valid edge of pulse that is input to the T2 pin. It is possible to measure the width of the pulse by reading the up-counter values. The rising or falling edge of the T2 pin input is selected by the Timer2 pre-scaler register ($15) T2E (bit3). But the clock source of the up-counter is the system internal clock selected by the Timer2 pre-scaler register ($15) T2SC (bit2-0). When the Timer2 control register ($27) T2GO (bit3) is set to 1, the contents of the up-counter is reset to “0000H”, automatically. Then a rising (falling) edge signal on the T2 input pin triggers the up-counter to start counting. At the next falling (rising) edge, the counter value is loaded to the Timer2 load register ($384 - $387), individually. Simultaneously, the Timer2 interrupt is generated if the Interrupt enable register ($00) IET2 (bit1) is set to 1.

When the Timer2 control register ($27) DEC (bit2) is cleared to 0, the Timer2 is in the one-edge capture mode. If the rising edge is selected as the counter-triggering signal, at the next falling edge, the Timer2 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer2 load register ($384 - $387) at first, then will be cleared again and the counter is halted. When the next rising edge applies to the T2 input pin, the up-counter starts counting for another measurement cycle.

When the Timer2 control register ($27) DEC (bit2) is set to 1, the Timer2 is in the double-edge capture mode. If the rising edge is selected as the counter-triggering signal, at the next falling edge, the Timer2 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer2 load register ($384 - $387) at first, then the counter continues counting. When the next rising edge applies to the T2 input pin, the Timer2 interrupt request is also generated. At this time, the contents of the up-counter must be loaded to the Timer2 load register ($384 - $387) again, then the counter is cleared and can be continued to start counting following measurement cycles.

In this mode, writing the Timer2 load register ($384 - $387) at any time cannot affect the up-counter operating anymore.

In this mode, the T2 pin input signal must follow certain constraints as in the external trigger timer mode. So, the limitation is applied for the external clock period time (T_E) described as follows:

$$T_E \text{ (period time)} \geq 1 * t_{\text{Timer clock}} + 2 * \Delta T; \qquad \Delta T = 20ns$$

$$T_E \text{ (period time)} \geq (M * t_{OSC}) + 2 * \Delta T$$

Where M (pre-scaler value for Timer2 internal clock) = 2^3, 2^4, 2^5, 2^6, 2^8, 2^{10}, 2^{12}or 2^{14}

But, in order to correctly get the pulse measurement value in programming, a sufficient wait period must be needed for the relevant Timer2 interrupt subroutine program.

So, if the Timer2 control register ($27) DEC (bit2) is 0, the Timer2 is in the one-edge capture mode. The limitation is applied for the external clock period (T_E) time described as follows:

T_E (period time) ≥ 14 * $t_{System\ clock}$

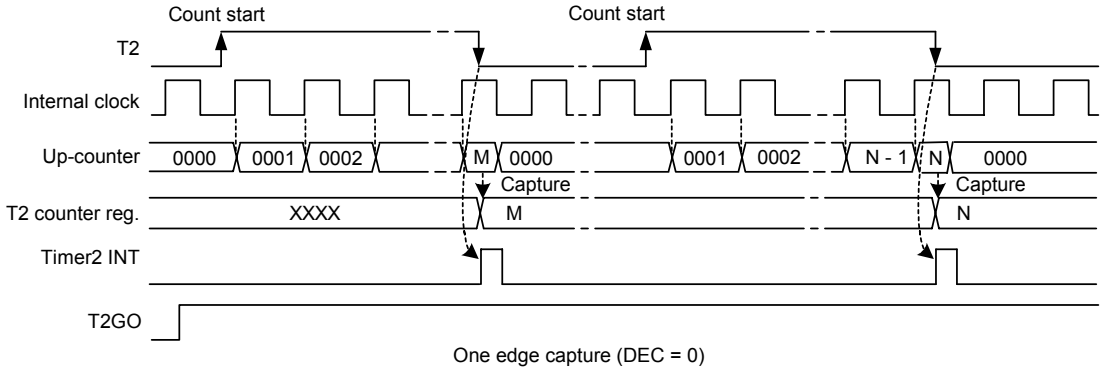
T_E (period time) ≥ 14 * 4 * t_{OSC}

The maximum value of these two equations shown above is valid to the proper application.

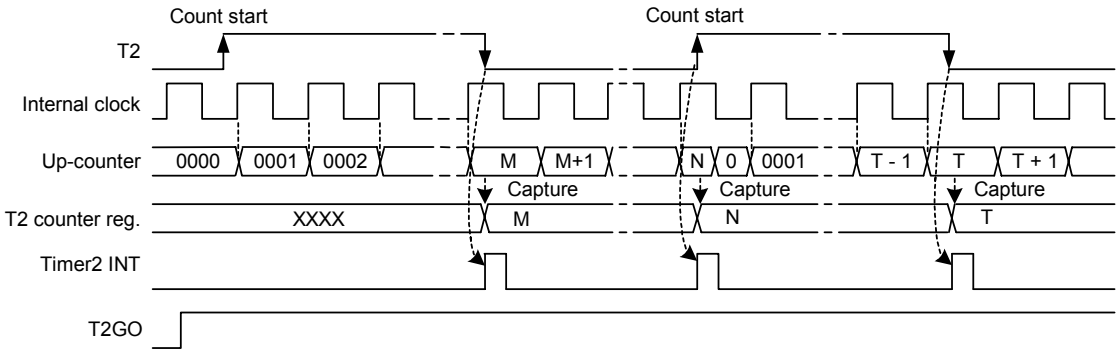
If the Timer2 control register ($27) DEC (bit2) is 1, the Timer2 is in the double-edge capture operation. The limitation is applied for the T2 input signal high or low level period described as follows:

T_E (high or low level period time) ≥ 14 * $t_{System\ clock}$

T_E (high or low level period time) ≥ 14 * 4 * t_{OSC}



One edge capture (DEC = 0)



Double edge capture (DEC = 1)

Timer2 Control Register: $27 (under the pulse width measurement mode)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select register Bit2: Capture edge select register
	X	0	1	1	R/W	One edge capture
	X	1	1	1	R/W	Double edge capture

8. LCD Driver

The LCD driver contains a controller, a voltage generator, 4-8 common driver pins/pads and 16-20 segment driver pins/pads. There are three different driving programmable modes: 1/4 duty & 1/3 bias, 1/6 duty & 1/3 bias and 1/8 duty & 1/4 bias. The driving mode is controlled by the system register $29. When 1/4 duty and 1/3 bias mode are used, COM8-5 are used as SEG17-20. When 1/6 duty and 1/3 bias mode are used, COM8-7 are used as SEG17-18. The controller consists of display data RAM and a duty generator.

The LCD SEG1-20 can also be used as output port, which is selected by the bit2-0 of the system register $2E. When SEG1-20 are selected to be output port, one should write data to bit3-0 at the same addresses ($08 - $0C, $38E - $390). The LCD COM1-8 can also be used as I/O port (PORTD, PORTE), which is selected by bit2 of the system register $29. The LCD COM1-6 and SEG1-8 can also be shared to LED application. LCD RAM could be used as data memory if needed.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When LCD off, both common and segment output low.

Before use the LCD driver, LEDEN (bit3 in $2B) must be cleared.

LCD Control Register $29

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$29	LCDON	DUTY2	DUTY1	DUTY0	R/W	Bit2-0: Set duty and com register Bit3: LCD display on control register
	0	X	X	X	R/W	LCD OFF
	1	X	X	X	R/W	LCD ON
	X	0	X	X	R/W	PORTD and PORTE as I/O ports
	X	1	0	0	R/W	Set 1/4 duty. PORTD3 - 0 as COM1 - 4, PORTE as I/O ports
	X	1	0	1	R/W	Set 1/4 duty. PORTE3 - 0 as COM5 - 8, PORTD as I/O ports
	X	1	1	0	R/W	Set 1/6 duty. PORTD3 - 0 as COM1 - 4, PORTE3 - 2 as COM5 - 6 and PORTE1 - 0 as I/O ports
	X	1	1	1	R/W	Set 1/8 duty. PORTD3 - 0 as COM1 - 4, PORTE3 - 0 as COM5 - 8

LCD Frame Frequency Control Register $3C1

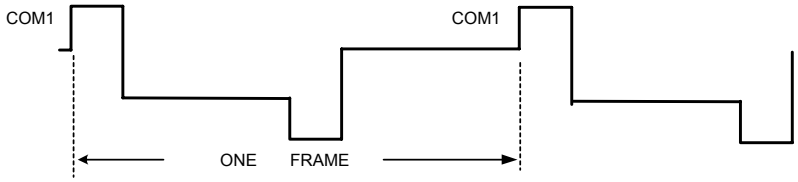
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C1	LPS3	LPS2	LPS1	LPS0	R/W	LCD frame frequency control register

Note:

1. If the $3C1≠0000B, the LCD Frame Frequency is controlled by $3C1.

COM	FOSC Code Option	Osc Range	LCD Frame Frequency
4	00	4M-8M	fosc/(20480*(LPS+1))
	01	2M-4M	fosc/(10240*(LPS+1))
	10	1M-2M	fosc/(5120*(LPS+1))
	11	400k-1M	fosc/(2560*(LPS+1))
	xx	32.768k	fosc/(160*(LPS+1))
6	00	4M-8M	fosc/(28672*(LPS+1))
	01	2M-4M	fosc/(14336*(LPS+1))
	10	1M-2M	fosc/(7168*(LPS+1))
	11	400k-1M	fosc/(3584*(LPS+1))
	xx	32.768k	fosc/(224*(LPS+1))
8	00	4M-8M	fosc/(36864*(LPS+1))
	10	2M-4M	fosc/(18432*(LPS+1))
	01	1M-2M	fosc/(9216*(LPS+1))
	11	400k-1M	fosc/(4608*(LPS+1))
	xx	32.768k	fosc/(288*(LPS+1))

*: LPS = LPS3 - LPS0



LCD Output Frame

The following table is the recommended setting.

OSC CLK	OTP OPTION	LPS	8COM F_{LCD} (Hz)	LPS	6COM F_{LCD} (Hz)	LPS	4COM F_{LCD} (Hz)
8M	00	05H	36	07H	35	0AH	35
7M	00	04H	38	06H	35	0BH	34
6M	00	03H	40	05H	35	07H	36
5M	00	03H	33	04H	35	06H	35
4.0001M	00	02H	36	03H	35	04H	39
4M	01	05H	36	07H	35	0AH	35
3M	01	03H	40	05H	35	07H	36
2.0001M	01	02H	36	03H	35	04H	39
2M	10	05H	36	07H	35	0AH	35
1.0001M	10	02H	36	03H	35	04H	39
1M	11	05H	36	07H	35	0AH	35
500k	11	02H	36	03H	35	04H	39
32.768k	xx	02H	38	03H	36	05H	34

2. If the $3C1 = 0000B. The LCD clock is divided from OSC, so LCD frame frequency will change in proportion to the variation of OSC frequency in spite of OSC type and the FOSC Code Option (See Page 56 for detail).

COM	FOSC Code Option	LCD Frame Frequency	Osc Range	EXAMPLE
4	00	fosc/40,960	4M - 8M	f_{OSC} = 4M, f_{LCD} = 97.5Hz
	01	fosc/20,480	2M - 4M	f_{OSC} = 2M, f_{LCD} = 97.5Hz
	10	fosc/10,240	1M - 2M	f_{OSC} = 1M, f_{LCD} = 97.5Hz
	11	fosc/5,120	400k - 1M	f_{OSC} = 500k, f_{LCD} = 97.5Hz
	xx	fosc/320	32.768k	f_{OSC} = 32.768k, f_{LCD} = 102.4Hz
6	00	fosc/57,344	4M - 8M	f_{OSC} = 4M, f_{LCD} = 69.5Hz
	01	fosc/28,672	2M - 4M	f_{OSC} = 2M, f_{LCD} = 69.5Hz
	10	fosc/14,336	1M - 2M	f_{OSC} = 1M, f_{LCD} = 69.5Hz
	11	fosc/7,168	400k - 1M	f_{OSC} = 500k, f_{LCD} = 69.5Hz
	xx	fosc/448	32.768k	f_{OSC} = 32.768k, f_{LCD} = 73Hz
8	00	fosc/73,728	4M - 8M	f_{OSC} = 4M, f_{LCD} = 54Hz
	10	fosc/36,864	2M - 4M	f_{OSC} = 2M, f_{LCD} = 54Hz
	01	fosc/18,432	1M - 2M	f_{OSC} = 1M, f_{LCD} = 54Hz
	11	fosc/9,216	400k - 1M	f_{OSC} = 500k, f_{LCD} = 54Hz
	xx	fosc/576	32.768k	f_{OSC} = 32.768k, f_{LCD} = 57Hz

3. SH69P55A/69K55A both has LCD driver and LED driver, and only one is valid at one time. If LEDEN = 1, the LCD driver is disabled; if LEDEN = 0, the LED driver is disabled.

SEG Configuration Register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	RLCD	PS2	PS1	PS0	R/W	Bit2 - 0: Configuration the segment (See the following table) Bit3: LCD bias resistor set register

PS2	PS1	PS0	PE.3	PE.2	PE.1	PE.0	PH.3	PH.2	PH.1	PH.0	PI.3	PI.2	PI.1	PI.0	PF.3	PF.2	PF.1	PF.0	PA.3	PA.2	PA.1	PA.0
0	0	0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
0	0	1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	S5	S4	S3	S2	S1
0	1	0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	S6	S5	S4	S3	S2	S1
0	1	1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	S7	S6	S5	S4	S3	S2	S1
1	0	0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	S8	S7	S6	S5	S4	S3	S2	S1
1	0	1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
1	1	0	I/O	I/O	I/O	I/O	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
1	1	1	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1

*Sx = SEGx

If the PORTE3 - 0 are shared as the COM5 - 8 for LCD display, then the PORTE3 - 0 cannot shared as the SEG20 - 17 for LCD display.

SEGs and COMs shall be configured correctly before the LCD is turned on.

Configuration of LCD RAM Area: (LCD 1/4 duty, 1/3 bias, COM uses COM1 - 4, SEG uses SEG1 - 20)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$30A	SEG11	SEG11	SEG11	SEG11
$301	SEG2	SEG2	SEG2	SEG2	$30B	SEG12	SEG12	SEG12	SEG12
$302	SEG3	SEG3	SEG3	SEG3	$30C	SEG13	SEG13	SEG13	SEG13
$303	SEG4	SEG4	SEG4	SEG4	$30D	SEG14	SEG14	SEG14	SEG14
$304	SEG5	SEG5	SEG5	SEG5	$30E	SEG15	SEG15	SEG15	SEG15
$305	SEG6	SEG6	SEG6	SEG6	$30F	SEG16	SEG16	SEG16	SEG16
$306	SEG7	SEG7	SEG7	SEG7	$310	SEG17	SEG17	SEG17	SEG17
$307	SEG8	SEG8	SEG8	SEG8	$311	SEG18	SEG18	SEG18	SEG18
$308	SEG9	SEG9	SEG9	SEG9	$312	SEG19	SEG19	SEG19	SEG19
$309	SEG10	SEG10	SEG10	SEG10	$313	SEG20	SEG20	SEG20	SEG20

Configuration of LCD RAM Area: (LCD 1/4 duty, 1/3 bias, COM uses COM5 - 8, SEG uses SEG1 - 16)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM8	COM7	COM6	COM5		COM8	COM7	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$308	SEG9	SEG9	SEG9	SEG9
$301	SEG2	SEG2	SEG2	SEG2	$309	SEG10	SEG10	SEG10	SEG10
$302	SEG3	SEG3	SEG3	SEG3	$30A	SEG11	SEG11	SEG11	SEG11
$303	SEG4	SEG4	SEG4	SEG4	$30B	SEG12	SEG12	SEG12	SEG12
$304	SEG5	SEG5	SEG5	SEG5	$30C	SEG13	SEG13	SEG13	SEG13
$305	SEG6	SEG6	SEG6	SEG6	$30D	SEG14	SEG14	SEG14	SEG14
$306	SEG7	SEG7	SEG7	SEG7	$30E	SEG15	SEG15	SEG15	SEG15
$307	SEG8	SEG8	SEG8	SEG8	$30F	SEG16	SEG16	SEG16	SEG16

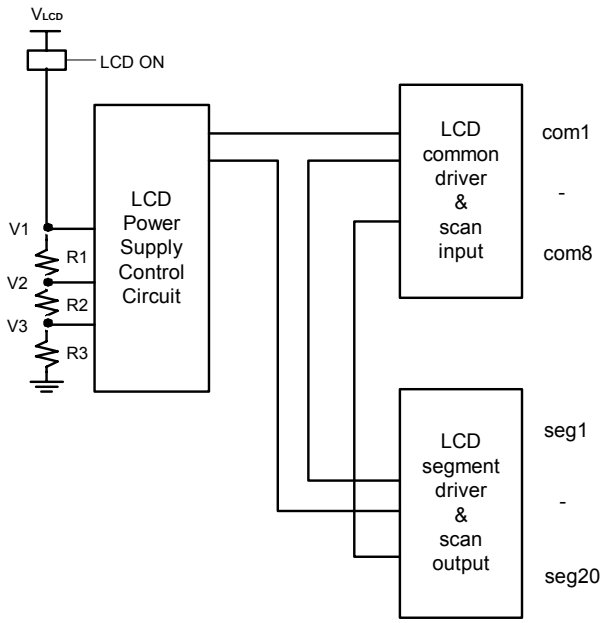
Configuration of LCD RAM Area: (LCD 1/6 duty, 1/3 bias, COM uses COM1 - 6, SEG uses SEG1 - 18)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	-	-	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	-	-	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	-	-	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	-	-	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	-	-	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	-	-	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	-	-	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	-	-	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	-	-	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	-	-	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	-	-	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	-	-	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	-	-	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	-	-	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	-	-	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	-	-	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$330	-	-	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$331	-	-	SEG18	SEG18

Configuration of LCD RAM Area: (LCD 1/8 duty, 1/4 bias, COM uses COM1 - 8, SEG uses SEG1 - 16)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM8	COM7	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	SEG1	SEG1	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	SEG2	SEG2	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	SEG3	SEG3	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	SEG4	SEG4	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	SEG5	SEG5	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	SEG6	SEG6	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	SEG7	SEG7	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	SEG8	SEG8	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	SEG9	SEG9	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	SEG10	SEG10	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	SEG11	SEG11	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	SEG12	SEG12	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	SEG13	SEG13	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	SEG14	SEG14	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	SEG15	SEG15	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	SEG16	SEG16	SEG16	SEG16

LCD Power



SEG Configuration Register: $2E

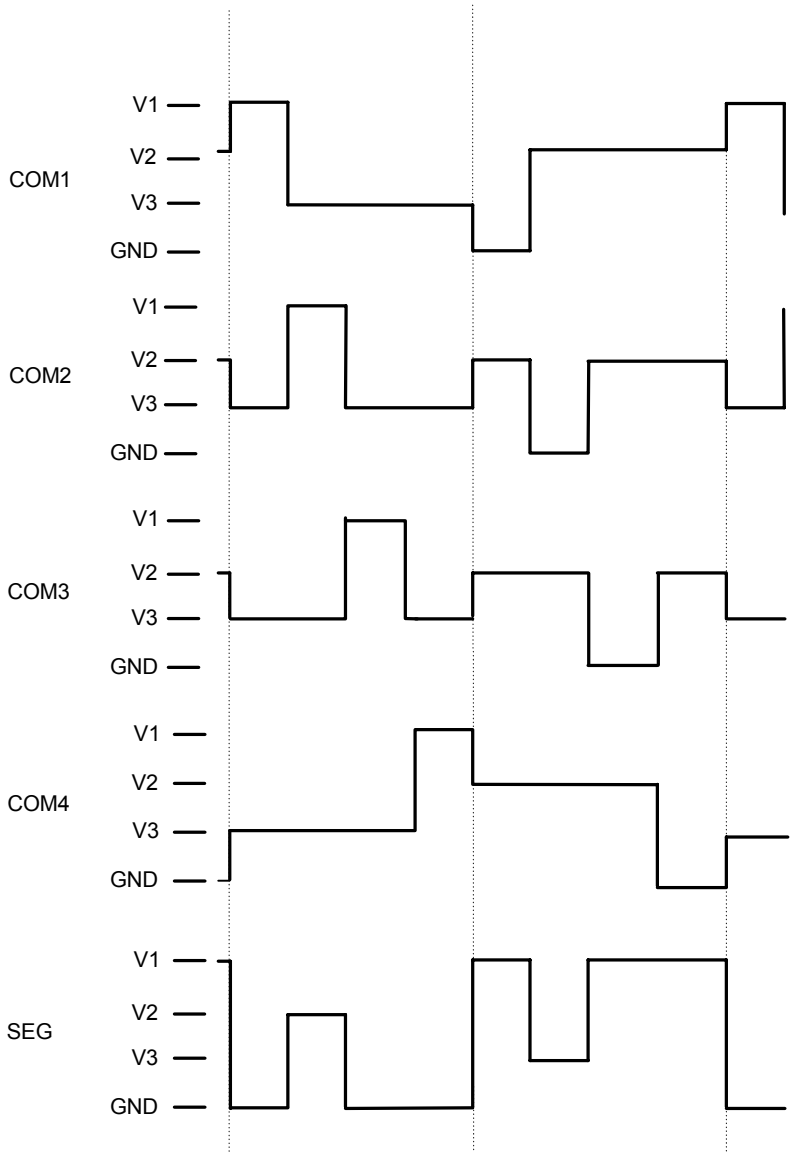
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	RLCD	-	-	-	R/W	Bit3: Set LCD bias resistor register
	0	X	X	X	R/W	R1 = R2 = R3 = 90k
	1	X	X	X	R/W	R1 = R2 = R3 = 10k
	X	X	X	X	R/W	R1 = R2 = R3 = 3k, if KEYEN = 1

When a large LCD panel is used, user can set the value of $2E to increase the bias current for better LCD performance. But it will cost more power, when the smaller divider resistances are used.

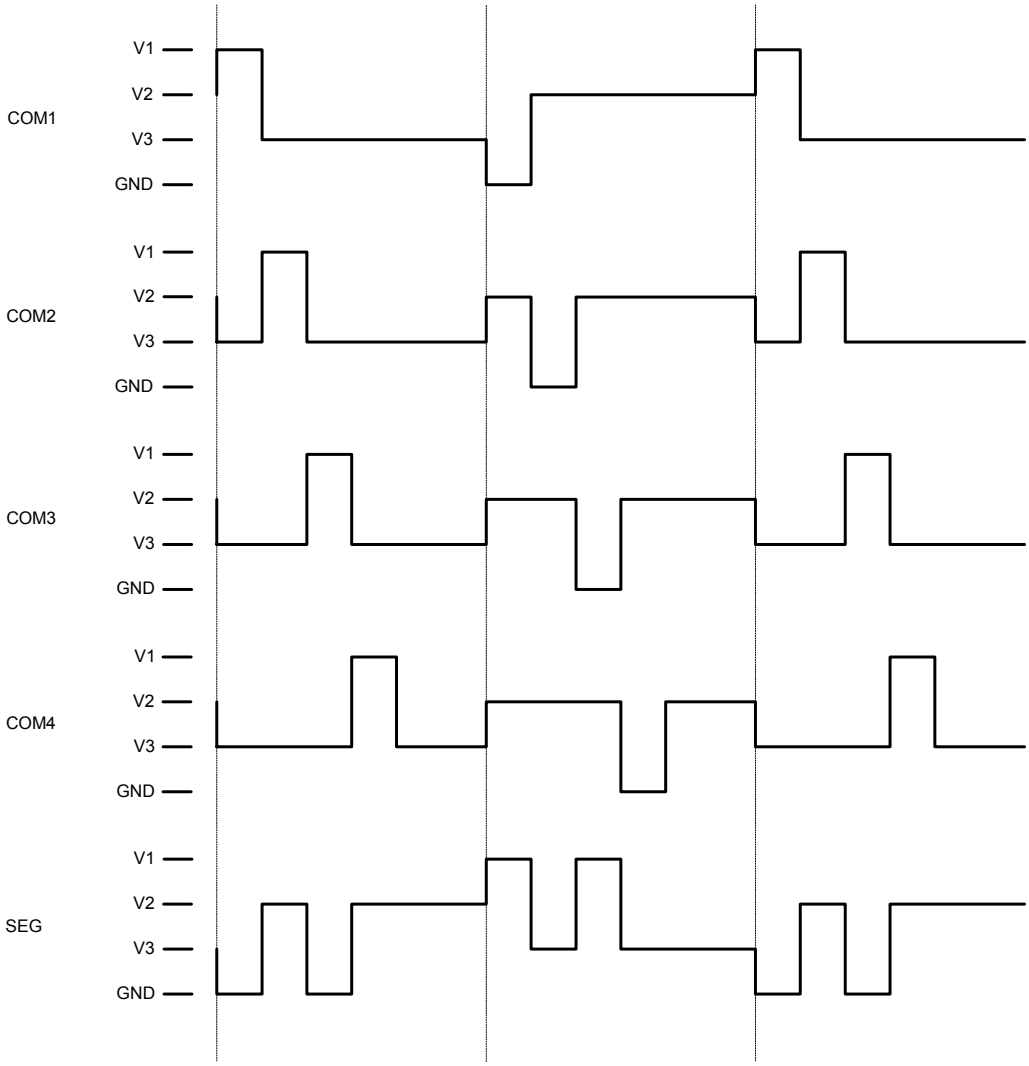
When the CPU is in STOP mode, the COM1-8 and SEG1-20 are pulled low.

LCD Waveform

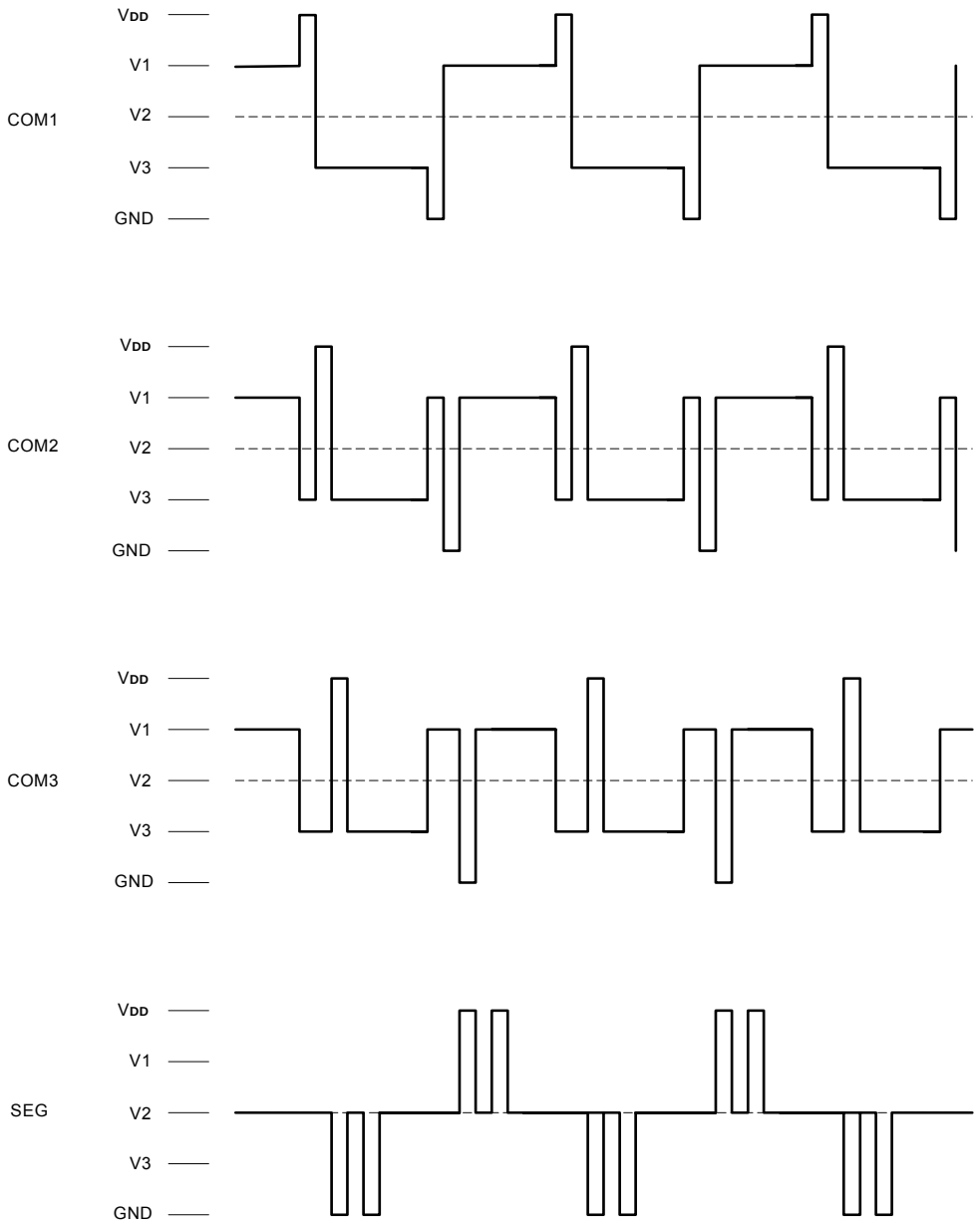
1/4 duty, 1/3 bias LCD Waveform



1/6 duty, 1/3 bias LCD Waveform



1/8 duty, 1/4 bias LCD Waveform



9. LED Driver

The LED driver contains a controller, 4-6 common driver pins and 8 segment driver pins. There are three different driving programmable modes: 1/4 duty, 1/5 duty and 1/6 duty. The driving mode is controlled by the system register $2B. The controller consists of display data RAM and a duty generator.

The LED SEG1-8 can also be used as output port, which is selected by the bit2-0 of the system register $2E. When SEG1-8 are selected to be output port, one should write “0” to bit2-0 at the address $2E. The LED COM1-6 can also be used as I/O port (PORTD, PORTE), which is selected by bit1-0 of the system register $2B.

The built-in LED driver has so powerful drive ability that it can drive LED directly. COM can source at least 200mA current. For detail information, please reference the application circuit. Before use the LED driver, LEDEN must be set to 1.

LED driver duty control register: $2B

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2B	LEDEN	LEDON	EDUTY1	EDUTY0	R/W	Bit1-0: Set duty register Bit2: Turn on LED driver register Bit3: Enable LED driver register
	0	X	X	X	R/W	LCD enable
	1	X	X	X	R/W	LED enable
	1	0	X	X	R/W	LED driver off
	1	1	X	X	R/W	LED driver on
	1	X	0	0	R/W	PORTD and PORTE are normal I/O port
	1	X	0	1	R/W	1/4 duty, PORTD3 - 0 is shared as COM1 - 4 for LED display and PORTE3 - 2 is normal I/O port
	1	X	1	0	R/W	1/5 duty, PORTD3 - 0 and PORTE3 is shared as COM1 - 5 for LED display and PORTE2 is normal I/O port
	1	X	1	1	R/W	1/6 duty, PORTD3 - 0 and PORTE3 - 2 is shared as COM1 - 6 for LED display

Note:

SH69P55A/69K55A both has LCD driver and LED driver, and just only one is valid at one time. If LEDEN = 1, the LCD driver is disabled; if LEDEN = 0, the LED driver is disabled.

SEG configuration register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	RLCD	PS2	PS1	PS0	R/W	Bit2-0: Configuration the segment register (See the following table)

PS2	PS1	PS0	PF3	PF2	PF1	PF0	PA3	PA2	PA1	PA0
0	0	0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
0	0	1	I/O	I/O	I/O	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1
0	1	0	I/O	I/O	LED_S6	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1
0	1	1	I/O	LED_S7	LED_S6	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1
1	0	0	LED_S8	LED_S7	LED_S6	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1

Configuration of LED RAM

Configuration of LCD RAM Area: (LED 1/4 duty, COM1 - 4, SEG1 - 8)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$304	SEG5	SEG5	SEG5	SEG5
$301	SEG2	SEG2	SEG2	SEG2	$305	SEG6	SEG6	SEG6	SEG6
$302	SEG3	SEG3	SEG3	SEG3	$306	SEG7	SEG7	SEG7	SEG7
$303	SEG4	SEG4	SEG4	SEG4	$307	SEG8	SEG8	SEG8	SEG8

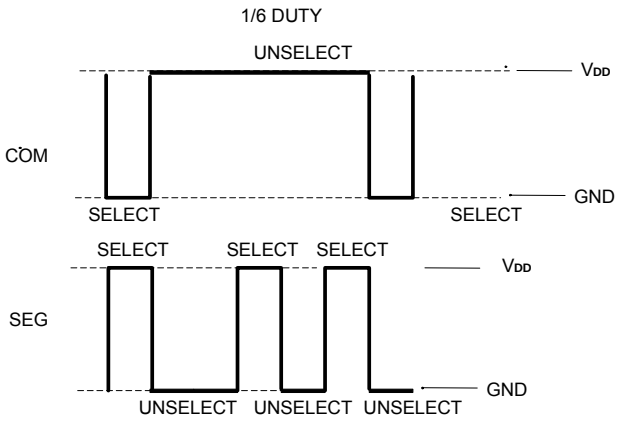
Configuration of LCD RAM Area: (1/5 duty, COM1 - 5, SEG1 - 8)

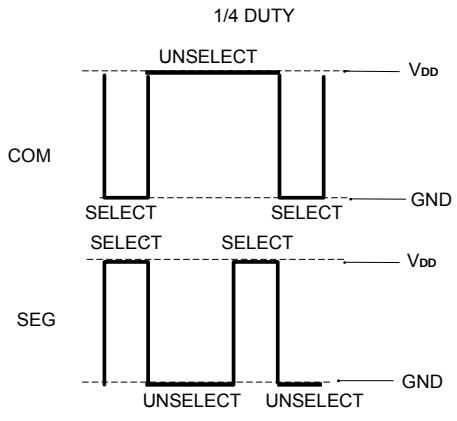
Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	-	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	-	-	-	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	-	-	-	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	-	-	-	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	-	-	-	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	-	-	-	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	-	-	-	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	-	-	-	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	-	-	-	SEG8

Configuration of LCD RAM Area: (1/6 duty, COM1 - 6, SEG1 - 8)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	-	-	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	-	-	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	-	-	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	-	-	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	-	-	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	-	-	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	-	-	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	-	-	SEG8	SEG8

LED Waveform





10. Key Scan

There is a key scanner built in the SH69P55A/69K55A, which can automatic detect the key-press. It includes four outputs (KEY_O1 - 4, shared with COM1 - COM4), five inputs (KEY_I5 - 1, shared with SEG1 - SEG5), and it can detect 20 individual keys. The key scan function must be shared with LCD or LED function, so the key scan must work in proper LCD or LED mode.

Since the LCD/LED drive waveform integrates the key scan waveform, the LCD/LED drive waveform is enlarged by a duty period compared with the traditional waveform. For instance, 1/4 duty would be enlarged to1/5 duty. The additional duty period is used to scan keys, and it would be inserted into the end of the frame automatically. The LCD waveform scans keys one time every one frame. The key scanner only works a duty period for each frame and it does not work for the rest duty periods of the frame. It scans keys during the last duty period of the first half frame, but it does not work during the last duty period of the last half frame. For instance in 1/4 duty mode the key scanner only works during the last duty period of the first half frame, but it does not work during the rest 9 duty periods of the frame. The LED waveform scans keys one time every two frame. The key scanner only works a duty period for every two frames and it does not work for the rest duty periods of the two frames. It scans keys during the last duty period of one frame, but it does not work during the last duty period of the next frame. For instance in 1/4 duty mode the key scanner only works a duty period for every two frames and it does not work during the rest 9 duty periods of the two frames.

Once the end of the key scan reaches, the key interrupt request flag would be set (KEYIF) whether a key is pressed or not. In LCD mode the key interrupt request flag is set every one frame. In LED mode the key interrupt request flag is set every 2 frames.

Key Scan Control Register: $28

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$28	KEYNUM1	KEYNUM0	KEYEND	KEYEN	R/W R	Bit0: key scan enable register Bit1: key scan end/processing register Bit3 - 2: key scan result register
	X	X	X	0	R/W	Disable key scan
	X	X	X	1	R/W	Enable key scan
	X	X	0	1	R	Key scan end
	X	X	1	1	R	Key scan processing
	X	0	X	1	R	No key-press
	X	1	X	1	R	Key-press occur
	0	X	X	1	R	One key-press occur, at the same time
	1	X	X	1	R	More than one key-press occur, at the same time

Key Scan Data Register1: $2C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2C	KEYC3	KEYC2	KEYC1	KEYC0	R	Bit3 - 0: the result of key scan on KEY_O4 - 1
	0	0	0	1	R	Key-press occur on KEY_O1
	0	0	1	0	R	Key-press occur on KEY_O2
	0	1	0	0	R	Key-press occur on KEY_O3
	1	0	0	0	R	Key-press occur on KEY_O4

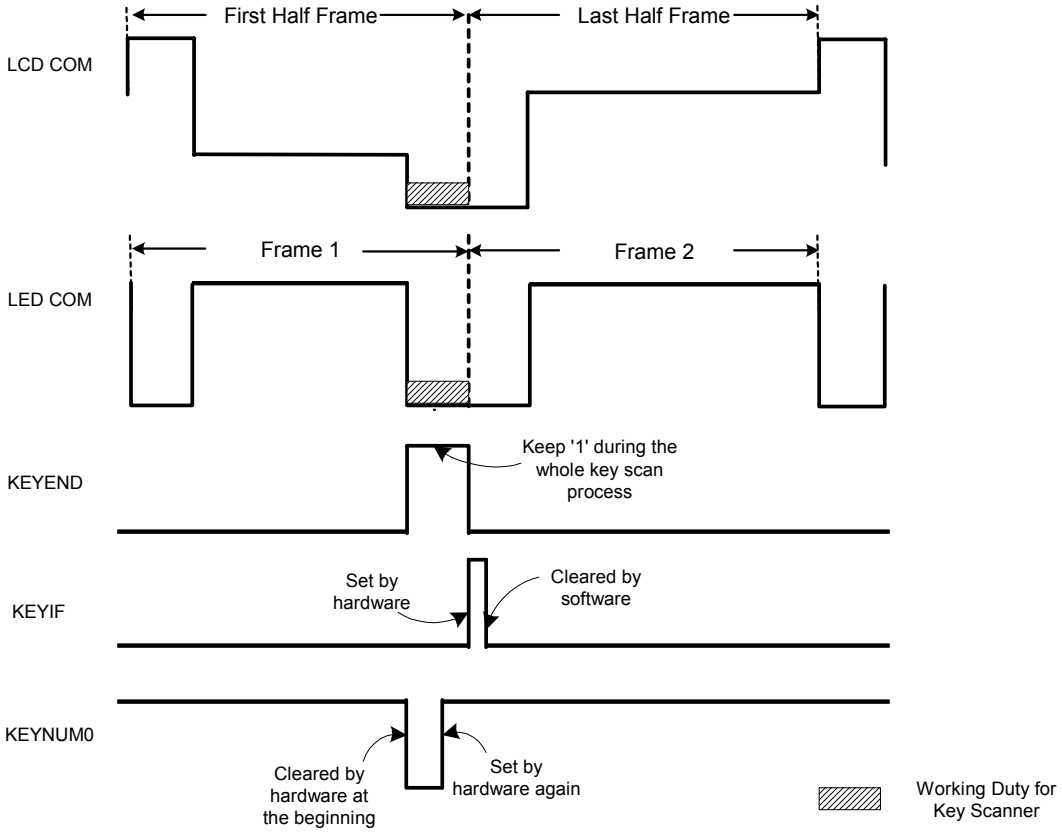
Key Scan Data Register2: $2D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2D	KEYL3	KEYL2	KEYL1	KEYL0	R	Bit3 - 0: the result of key scan on KEY_I5 - 1
	0	0	0	0	R	Key-press occur on KEY_I1
	0	0	0	1	R	Key-press occur on KEY_I2
	0	0	1	0	R	Key-press occur on KEY_I3
	0	1	0	0	R	Key-press occur on KEY_I4
	1	0	0	0	R	Key-press occur on KEY_I5

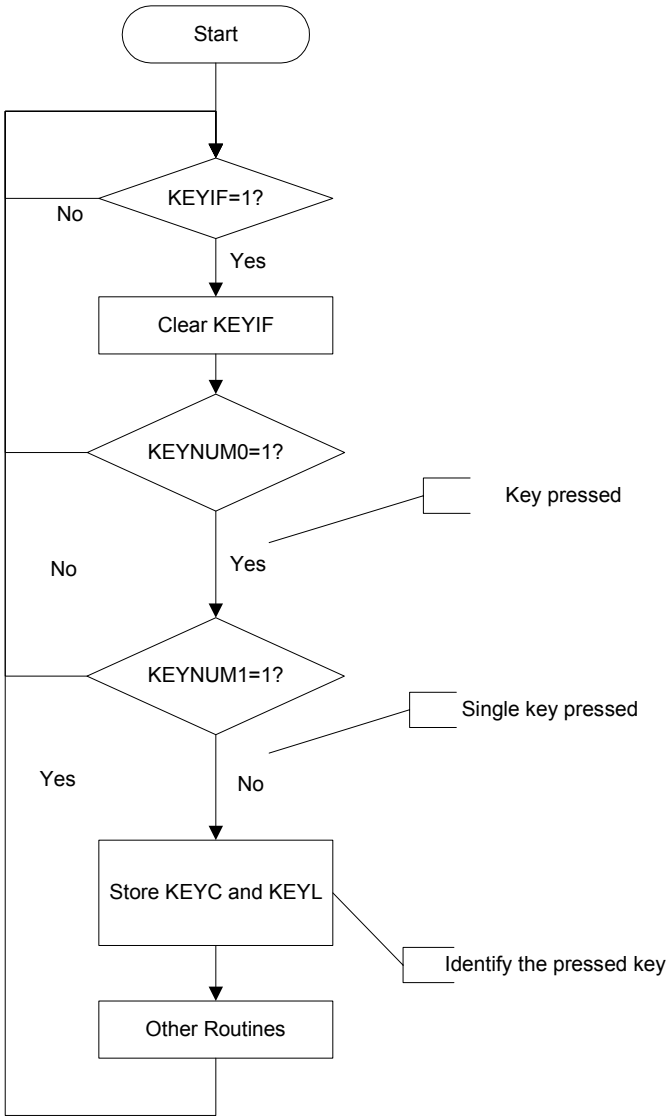
Note:

1. If key scan function is shared with LCD function, the LCD function must be selected as 4com, 6com or 8com. It is important that if the LCD function is selected as 4com, PORTD must be selected as COM port (the LCD control register $29 bit2 - 0 can be selected as '100', '110' and '111'). PORTA3 - 0, PORTF0 must be selected as SEG output (SEG configuration register $2E bit2 - 0 can't be '000').
2. If key scan function is shared with LED function, the LED function must be selected as 4com, 5com or 6com (LED driver duty control register $2B bit1 - 0 can be '01', '10' and '11'). PORTA3 - 0, PORTF0 must be selected as SEG output (SEG configuration register $2E bit2 - 0 can't be '000').
3. In the correct mode, although the LCD or LED is turned off, the automatic key scan is also valid.
4. The key scanner would clear KEYNUM0 and KEYNUM1 flags at the beginning of the key scan process. KEYEND flag would keep '1' during the whole key scan process and it would be cleared at the end of the scan process. For instance in 1/4 duty mode KEYEND keeps '1' during the working duty period and keeps '0' during the rest 9 duty periods. KEYNUM0 and KEYNUM1 would be cleared at the beginning of the working duty period and would be set or cleared again according to the key scan result. KEYNUM0 and KEYNUM1 would keep the key scan result for the rest 9 duty periods.
5. If and only if one key is pressed at the same time, the result of the key scan is valid; otherwise the result of key scan is invalid.

In 1/4 duty mode, the waveforms of key scan when a key is pressed



An Example of the program flow of customer applications



11. Analog/Digital Converter (ADC)

The 10 channels and 10-bit resolution A/D converter are implemented in this micro-controller.

The ADC control registers can be used to define the A/D channel number, select analog channel, reference voltage and conversion clock, start A/D conversion, and set the end of A/D conversion flag. The A/D conversion result register byte is read-only.

The approach for A/D conversion:

- Set analog input channels and select the reference voltage. (When using the external reference voltage, please keep in mind that any analog input voltage must not exceed V_{REF})
- Operating ADC module and select the converted analog channel.
- Set A/D conversion clock source.
- GO/$\overline{DONE}$ = 1, start the A/D conversion.

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: A/D port configuration control register Bit3: Select Internal/External reference voltage register
	X	0	0	0	R/W	Set analog channels
	0	X	X	X	R/W	Internal reference voltage (V_{REF} = V_{DD})
	1	X	X	X	R/W	External reference voltage

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3C2	ACR3	CH3	-	-	R/W	Bit2: ADC channel control register Bit3: A/D port configuration control register
	1	X	-	-	R/W	Set analog channels
	X	1	-	-	R/W	ADC channels control register

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	ADCON	CH2	CH1	CH0	R/W	Bit2-0: ADC channel control register Bit3: ADC module operate control register
	0	X	X	X	R/W	Disable ADC module
	1	X	X	X	R/W	Enable ADC module

Set Analog Channels

ACR3	ACR2	ACR1	ACR0	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PG1	PG3	PJ3	PJ2	PJ1	PJ0	PB3	PB2	PB1	PB0
0	0	0	1	PG1	PG3	PJ3	PJ2	PJ1	PJ0	PB3	PB2	PB1	AN0
0	0	1	0	PG1	PG3	PJ3	PJ2	PJ1	PJ0	PB3	PB2	AN1	AN0
0	0	1	1	PG1	PG3	PJ3	PJ2	PJ1	PJ0	PB3	AN2	AN1	AN0
0	1	0	0	PG1	PG3	PJ3	PJ2	PJ1	PJ0	AN3	AN2	AN1	AN0
0	1	0	1	PG1	PG3	PJ3	PJ2	PJ1	AN4	AN3	AN2	AN1	AN0
0	1	1	0	PG1	PG3	PJ3	PJ2	AN5	AN4	AN3	AN2	AN1	AN0
0	1	1	1	PG1	PG3	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	x	x	0	PG1	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	x	x	1	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Note:

The analog channels AN8 and AN9 are shared with digital I/O PORTG.3 and PORTG.1. They are also shared with T2 input pin and tone output pin. If user wants to use T2 input function, the control bit ACR3 must be clear to 0. If user wants to use tone generator function, the control bits ACR3 - 0 can't be 1xx1B.

ADC Channels Control

CH3	CH2	CH1	CH0	Remarks
0	0	0	0	ADC Channel AN0
0	0	0	1	ADC Channel AN1
0	0	1	0	ADC Channel AN2
0	0	1	1	ADC Channel AN3
0	1	0	0	ADC Channel AN4
0	1	0	1	ADC Channel AN5
0	1	1	0	ADC Channel AN6
0	1	1	1	ADC Channel AN7
1	x	x	0	ADC Channel AN8
1	x	x	1	ADC Channel AN9

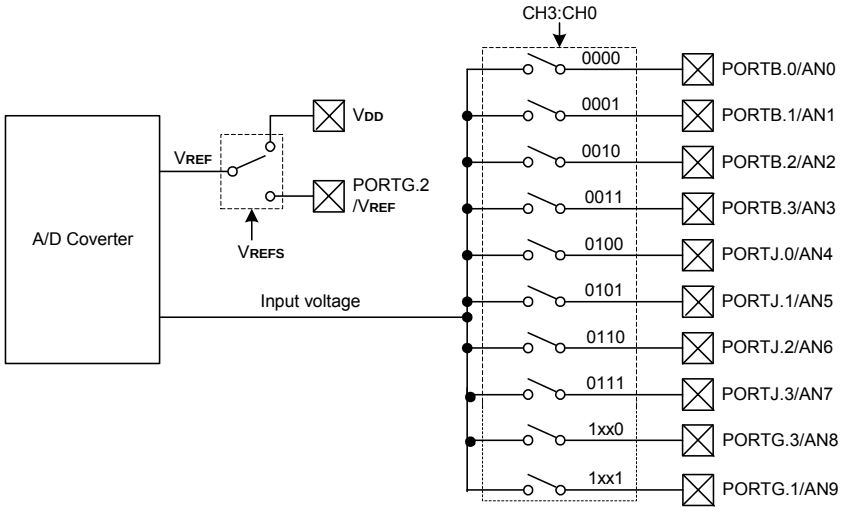
Systems Register for ADC Data:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3AD	-	-	A1	A0	R	ADC data low nibble register
$3AE	A5	A4	A3	A2	R	ADC data middle nibble register
$3AF	A9	A8	A7	A6	R	ADC data high nibble register

Systems Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2F	GO/$\overline{\text{DONE}}$	TADC1	TADC0	-	R/W	Bit2-1: A/D Conversion Time control register Bit3: ADC startup/status flag register
	X	0	0	X	R/W	A/D Conversion Time = 13 tosc*
	X	0	1	X	R/W	A/D Conversion Time = 52 tosc*
	X	1	0	X	R/W	A/D Conversion Time = 208 tosc*
	X	1	1	X	R/W	A/D Conversion Time = 416 tosc*
	0	X	X	X	R/W	A/D conversion is complete or not in processing
	1	X	X	X	R/W	Set 1 to start A/D conversion, keep GO/$\overline{\text{DONE}}$ = 1 when A/D conversion is in processing

*: tosc is the OSC clock. If the PLL is enable, tosc is the PLL frequency otherwise tosc is the OSC clock.



A/D Converter Block Diagram

Notes:

- Select A/D Conversion Time, make sure that A/D Conversion Time ≧ 25μs.
- When the A/D conversion is complete, an ADC interrupt occurs (if the ADC interrupt is enabled).
- The analog input channels must have their corresponding PXCR (X = B, J, G) bits selected as inputs.
- If select I/O port as analog input, the I/O functions and pull-high resistor are disabled.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the A/D conversion is complete.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion.
- The A/D result register will NOT be updated with the partially completed A/D conversion sample.
- 4tosc wait is required before the next acquisition is started.
- The ADC could keep on working in the HALT mode, and would stop automatic while executing “STOP” instruction.
- The ADC could wake-up the device from the HALT mode (if the ADC interrupt is enabled).

Application Notes:

When the External reference voltage is selected, the SH69P55A/69K55A ADC needs a little current, which is input into SH69P55A/69K55A from the V_{REF} pin to maintain the A/D normal running. The methods that show in figure 1 and figure 2 to set up the External reference voltage are recommended. If the A/D Conversion Time is between 25μs and 50μs, a capacitance (10μF) can be added between the V_{REF} pin and the GND pin to provide the current input into the SH69P55A/69K55A from the V_{REF} pin (figure 3). The method that shows in figure 4 also can set up the External reference voltage but the current consume of the hole system will increase obviously (V_{DD} = 5.0V, R1 + R2 = 500Ω, 10mA increases) (the dashed frames in all the figures are 0.1μF capacitances in order to reducing the disturbance in the V_{REF} pin).

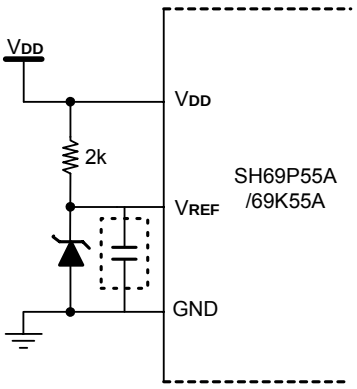


Figure 1.

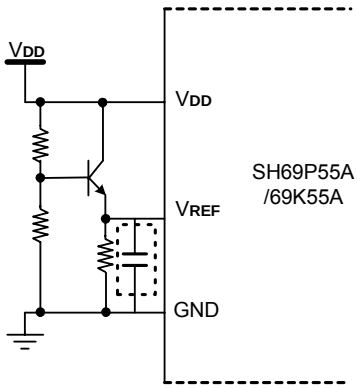


Figure 2.

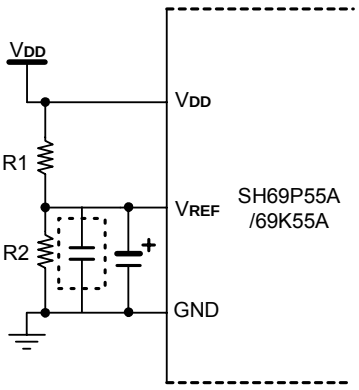


Figure 3. (R1+R2≧50kΩ)

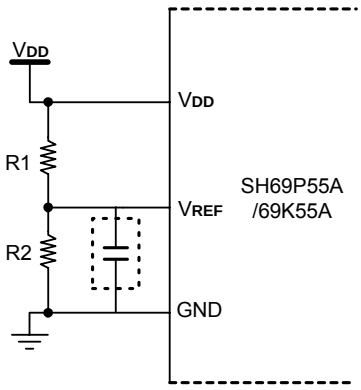


Figure 4. (R1+R2≦500Ω)

12. Pulse Width Modulation (PWM)

The SH69P55A/69K55A consists of one 8+2 bit PWM module. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMP is used to control the period cycle of the PWM module output. And the PWMD is used to control the duty in the waveform of the PWM module output.

Systems Register$20: PWM Control Register (PWMC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWMS	TCK1	TCK0	PWM_EN	R/W	Bit0: PWM output enable control register Bit2-1: PWM clock control register Bit3: PWM output mode of duty cycle control register
	X	X	X	0	R/W	Disable PWM (Default)
	X	X	X	1	R/W	Enable PWM
	X	0	0	X	R/W	PWM clock = tosc* (Default)
	X	0	1	X	R/W	PWM clock = 2 tosc*
	X	1	0	X	R/W	PWM clock = 4 tosc*
	X	1	1	X	R/W	PWM clock = 8 tosc*
	0	X	X	X	R/W	PWM output normal mode of duty cycle (high active) (Default)
	1	X	X	X	R/W	PWM output negative mode of duty cycle (low active)

The PWM output pin is shared with PORTG.0

*: tosc is the OSC clock. If the PLL is enable, tosc is the PLL frequency otherwise tosc is the OSC clock.

Systems Register $21 - $22: PWM Period Control Register (PWMP)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PP.3	PP.2	PP.1	PP.0	R/W	PWM period low nibble register
$22	PP.7	PP.6	PP.5	PP.4	R/W	PWM period high nibble register

PWM output period cycle = [PP.7, PP.0] X PWM clock.

When [PP.7, PP.0] = 00H, PWM outputs GND if the PWMS bit is cleared to 0.

When [PP.7, PP.0] = 00H, PWM outputs high level if the PWMS bit is set to 1.

Systems Register $24 - $26: PWM Duty Control Register (PWMD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	-	-	PDF.1	PDF.0	R/W	PWM duty fine-tune bits register
$25	PD.3	PD.2	PD.1	PD.0	R/W	PWM duty low nibble register
$26	PD.7	PD.6	PD.5	PD.4	R/W	PWM duty high nibble register

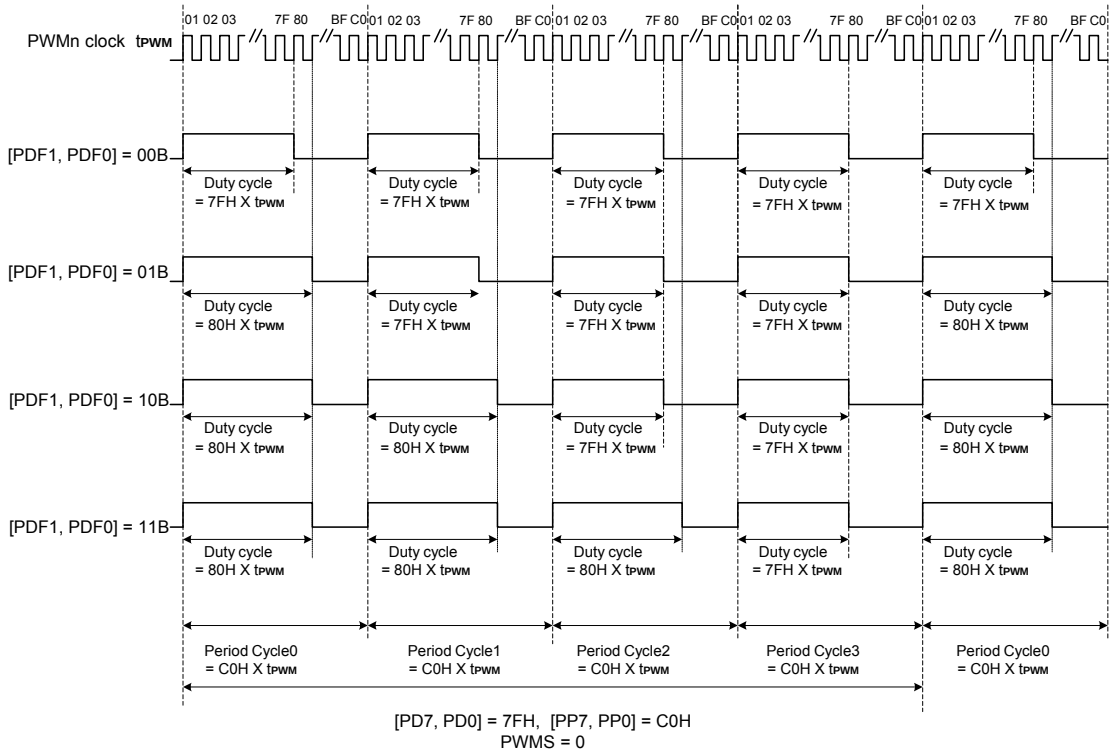
Average PWM output duty cycle = ([PD.7, PD.0] + [PDF.1, PDF.0]/4) X PWM clock.

If [PP.7, PP.0] ≤ [PD.7, PD.0], PWM outputs high when the PWMS bit is cleared to 0.

If [PP.7, PP.0] ≤ [PD.7, PD.0], PWM outputs GND level when the PWMS bit is set to 1.

System Register $24: PWM Duty Fine Control Register (PWMDF)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	-	-	PDF.1	PDF.0	R/W	Bit1-0: PWM duty f fine-tune bits register
	-	-	0	0	R/W	Duty cycle = [PD.7, PD0] in Period cycle0, 1, 2, 3
	-	-	0	1	R/W	Duty cycle = [PD.7, PD0]+1 in Period cycle0 Duty cycle = [PD.7, PD0] in Period cycle1, 2, 3
	-	-	1	0	R/W	Duty cycle = [PD.7, PD0]+1 in Period cycle0, 1 Duty cycle = [PD.7, PD0] in Period cycle 2, 3
	-	-	1	1	R/W	Duty cycle = [PD.7, PD0]+1 in Period cycle0, 1, 2 Duty cycle = [PD.7, PD0] in Period cycle 3



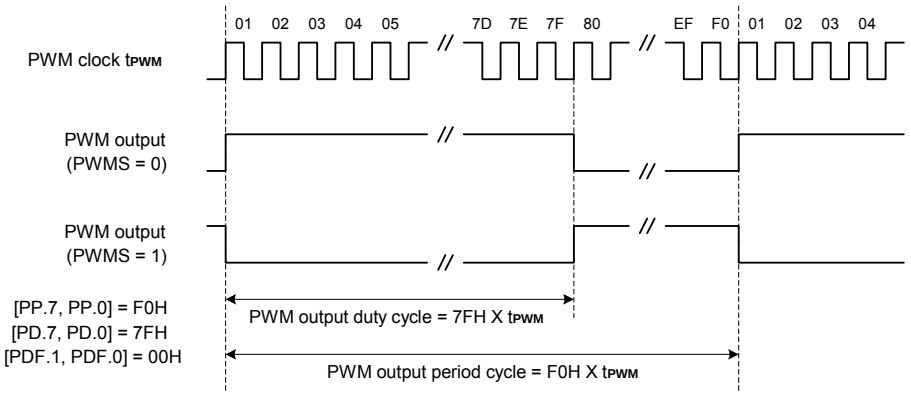
8+2 bit PWM Waveform

Programming Notes:

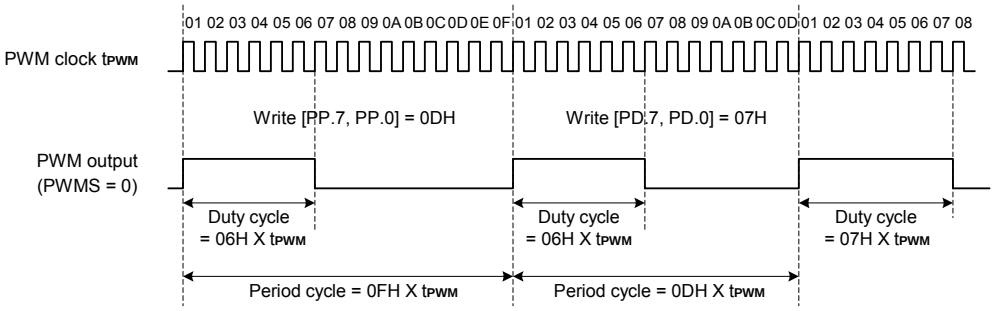
1. Select the PWM module system clock.
2. Set the PWM period cycle by writing proper value to the PWM period control register (PWMP). First set the low nibble, then the middle nibble and the last set the high nibble.
3. Set the PWM duty cycle by writing proper value to the PWM duty control register (PWMD). First set the fine tune nibble, then the low nibble, then the middle nibble and the last set the high nibble.
4. Select the PWM output mode of the duty cycle by writing the PWMS bit in the PWM control register (PWMC).
5. To output the desired PWM waveform, enable the PWM module by writing “1” to the PWM_EN bit in the PWM control register (PWMC).
6. If the PWM period cycle or duty cycle is needed to be changed, the writing flow should be followed as described in step 1 or step 2. Then the revised data are loaded into the re-load counter and the PWM module starts counting at next period.

Note:

- If the I/O port (PORTG.0) is selected as the PWM output, the I/O functions and pull-high resistor are disabled.
- The PWM could keep on working in the HALT mode, and would stop automatic when the “STOP” instruction is executed.



PWM Output Example



PWM Output Period or Duty Cycle Changing Example

13. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where heavy loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by the code option.

The LVR circuit has the following functions when the LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$
- Cancels the system reset when $V_{DD} > V_{LVR}$

Here, V_{LVR} which is LVR detect voltage has two level select by code option.

LVR flag will always keep '1' when the LVR happens; LVR flag must be cleared to '0' by software.

System Register: $17

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	LVR	-	-	-	R/W	Bit3: Low Voltage Reset flag register (Read and Write 0 only)
	0	X	X	X	R/W	No Low Voltage Reset
	1	X	X	X	R/W	Low Voltage Reset

14. ROM Data Table (RDT)

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 13-bit write-only PC address load register (RDT.12 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should fill 0 to higher 3 bit (bit 15 - 13) first, then write the ROM table address to RDT register (high nibble first then low nibble), after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

15. Dual Tone

SH69P55A/69K55A has two 12-bit tone generators. The tone generators generate the specific frequency of tone with square wave.

Tone Generator Control Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3A3	TG1.3	TG1.2	TG1.1	TG1.0	R/W	Tone generator 1 low nibble register
$3A4	TG1.7	TG1.6	TG1.5	TG1.4	R/W	Tone generator 1 middle nibble register
$3A5	TG1.11	TG1.10	TG1.9	TG1.8	R/W	Tone generator 1 high nibble register
$3A6	TG2.3	TG2.2	TG2.1	TG2.0	R/W	Tone generator 2 low nibble register
$3A7	TG2.7	TG2.6	TG2.5	TG2.4	R/W	Tone generator 2 middle nibble register
$3A8	TG2.11	TG2.10	TG2.9	TG2.8	R/W	Tone generator 2 high nibble register

Tone Generator Volume Control Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3A9	TV1.3	TV1.2	TV1.1	TV1.0	R/W	Tone generator 1 volume low nibble register
$3AA	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Bit2-0: Tone generator 1 volume high nibble register Bit3: Tone generator 1 enable register
$3AB	TV2.3	TV2.2	TV2.1	TV2.0	R/W	Tone generator 2 volume low nibble register
$3AC	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Bit2-0: Tone generator 2 volume high nibble register Bit3: Tone generator 2 enable register

The volume control register is 7-bit register used to control the output level of the tone generator.

TGxEN: Tone generator x enabl

0: Tone generator x disable (default)

1: Tone generator x enable

Note: x = 1 or 2

Programming Notes:

Before using tone generators functions, the $3C2 bit3 (ACR3) and $13 bit2 - 0(ACR2 - ACR0) can't be 1xx1B.

While the Tone Generators are operating, to reduce the power consumption never execute the "HALT" or "STOP" instruction.

Don't enable two-tone channels together to produce one tone. Or else, it will produce some unpredicted errors. If it is necessary to use 2 channels together (Ex. To play two-channel melody), Don't try to keep the score be the same tones as much as possible, then the unpredicted errors will not occur or it will be ignored through user's hearing.

The tone generator outputs frequency is divided from OSC frequency,

$$\text{Tone output frequency} = \frac{\text{fosc}}{8XN}$$

where N = FFFH - TGCR (TGx.11 - TGx.0)

x = 1 or 2

Music Table 1

Following is the music scale reference table for the Tone Generator channel 1 (or channel 2) under OSX = 4MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B2	123.47	4050	02E	123.46	-0.01	#F5	739.99	676	D5C	739.64	-0.05
C3	130.81	3822	112	130.82	0.01	G5	783.99	638	D82	783.70	-0.04
#C3	138.59	3608	1E8	138.58	-0.01	#G5	830.61	602	DA6	830.56	-0.01
D3	146.83	3405	2B3	146.84	0.01	A5	880.00	568	DC8	880.28	0.03
#D3	155.56	3214	372	155.57	0.00	#A5	932.33	536	DE8	932.84	0.06
E3	164.81	3034	426	164.80	-0.01	B5	987.77	506	E06	988.14	0.04
F3	174.61	2863	4D1	174.64	0.02	C6	1046.5	478	E22	1046.0	-0.05
#F3	185.00	2703	571	184.98	-0.01	#C6	1108.7	451	E3D	1108.7	-0.01
G3	196.00	2551	609	196.00	0.00	D6	1174.7	426	E56	1173.7	-0.08
#G3	207.65	2408	698	207.64	-0.01	#D6	1244.5	402	E6E	1243.8	-0.06
A3	220.00	2273	71F	219.97	-0.01	E6	1318.5	379	E85	1319.3	0.06
#A3	233.08	2145	79F	233.10	0.01	F6	1396.9	358	E9A	1396.7	-0.02
B3	246.94	2025	817	246.91	-0.01	#F6	1480.0	338	EAE	1479.3	-0.05
C4	261.63	1911	889	261.64	0.01	G6	1568.0	319	EC1	1567.4	-0.04
#C4	277.18	1804	8F4	277.16	-0.01	#G6	1661.2	301	ED3	1661.1	-0.01
D4	293.66	1703	959	293.60	-0.02	A6	1760.0	284	EE4	1760.6	0.03
#D4	311.13	1607	9B9	311.14	0.00	#A6	1864.7	268	EF4	1865.7	0.05
E4	329.63	1517	A13	329.60	-0.01	B6	1975.5	253	F03	1976.3	0.04
F4	349.23	1432	A68	349.16	-0.02	C7	2093.0	239	F11	2092.1	-0.05
#F4	369.99	1351	AB9	370.10	0.03	#C7	2217.5	225	F1F	2222.2	0.22
G4	392.00	1276	B04	391.85	-0.04	D7	2349.3	213	F2B	2347.4	-0.08
#G4	415.30	1204	B4C	415.28	-0.01	#D7	2489.0	201	F37	2487.6	-0.06
A4	440.00	1136	B90	440.14	0.03	E7	2637.0	190	F42	2631.6	-0.21
#A4	466.16	1073	BCF	465.98	-0.04	F7	2793.8	179	F4D	2793.3	-0.02
B4	493.88	1012	C0C	494.07	0.04	#F7	2960.0	169	F57	2958.6	-0.05
C5	523.25	956	C44	523.01	-0.05	G7	3136.0	159	F61	3144.7	0.28
#C5	554.37	902	C7A	554.32	-0.01	#G7	3322.4	150	F6A	3333.3	0.33
D5	587.33	851	CAD	587.54	0.04	A7	3520.0	142	F72	3521.1	0.03
#D5	622.25	804	CDC	621.89	-0.06	#A7	3729.3	134	F7A	3731.3	0.05
E5	659.26	758	D0A	659.63	0.06	B7	3951.1	127	F81	3937.0	-0.36
F5	698.46	716	D34	698.32	-0.02	C8	4186.0	119	F89	4201.7	0.37

Music Table 2

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSX = 2MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B1	61.73	4050	2E	61.73	0.00	C5	523.25	478	E22	523.01	-0.05
C2	65.10	3840	100	65.10	0.00	#C5	554.37	451	E3D	554.32	-0.01
#C2	69.29	3608	1E8	69.29	0.00	D5	587.33	426	E56	586.85	-0.08
D2	73.42	3405	2B3	73.42	0.00	#D5	622.25	402	E6E	621.89	-0.06
#D2	77.78	3214	372	77.78	0.00	E5	659.26	379	E85	659.63	0.06
E2	82.41	3034	426	82.40	-0.01	F5	698.46	358	E9A	698.32	-0.02
F2	87.31	2863	4D1	87.32	0.01	#F5	739.99	338	EAE	739.64	-0.05
#F2	92.50	2703	571	92.49	-0.01	G5	783.99	319	EC1	783.70	-0.04
G2	98.00	2551	609	98.00	0.00	#G5	830.61	301	ED3	830.56	-0.01
#G2	103.82	2408	698	103.82	0.00	A5	880.00	284	EE4	880.28	0.03
A2	110.00	2273	71F	109.99	-0.01	#A5	932.33	268	EF4	932.84	0.06
#A2	116.54	2145	79F	116.55	0.01	B5	987.77	253	F03	988.14	0.04
B2	123.47	2025	817	123.46	-0.01	C6	1046.5	239	F11	1046.0	-0.05
C3	130.81	1911	889	130.82	0.01	#C6	1108.7	225	F1F	1111.1	0.22
#C3	138.59	1804	8F4	138.58	-0.01	D6	1174.7	213	F2B	1173.7	-0.08
D3	146.83	1703	959	146.80	-0.02	#D6	1244.5	201	F37	1243.8	-0.06
#D3	155.56	1607	9B9	155.57	0.00	E6	1318.5	190	F42	1315.8	-0.21
E3	164.81	1517	A13	164.80	-0.01	F6	1396.9	179	F4D	1396.7	-0.02
F3	174.61	1432	A68	174.58	-0.02	#F6	1480.0	169	F57	1479.3	-0.05
#F3	185.00	1351	AB9	185.05	0.03	G6	1568.0	159	F61	1572.3	0.28
G3	196.00	1276	B04	195.92	-0.04	#G6	1661.2	150	F6A	1666.7	0.33
#G3	207.65	1204	B4C	207.64	-0.01	A6	1760.0	142	F72	1760.6	0.03
A3	220.00	1136	B90	220.07	0.03	#A6	1864.7	134	F7A	1865.7	0.05
#A3	233.08	1073	BCF	232.99	-0.04	B6	1975.5	127	F81	1968.5	-0.36
B3	246.94	1012	C0C	247.04	0.04	C7	2093.0	119	F89	2100.8	0.37
C4	261.63	956	C44	261.51	-0.04	#C7	2217.5	113	F8F	2212.4	-0.23
#C4	277.18	902	C7A	277.16	-0.01	D7	2349.3	106	F96	2358.5	0.39
D4	293.66	851	CAD	293.77	0.04	#D7	2489.0	100	F9C	2500.0	0.44
#D4	311.13	804	CDC	310.95	-0.06	E7	2637.0	95	FA1	2631.6	-0.21
E4	329.63	758	D0A	329.82	0.06	F7	2793.8	89	FA7	2809.0	0.54
F4	349.23	716	D34	349.16	-0.02	#F7	2960.0	84	FAC	2976.2	0.55
#F4	369.99	676	D5C	369.82	-0.05	G7	3136.0	80	FB0	3125.0	-0.35
G4	392.00	638	D82	391.85	-0.04	#G7	3322.4	75	FB5	3333.3	0.33
#G4	415.30	602	DA6	415.28	-0.01	A7	3520.0	71	FB9	3521.1	0.03
A4	440.00	568	DC8	440.14	0.03	#A7	3729.3	67	FBD	3731.3	0.05
#A4	466.16	536	DE8	466.42	0.06	B7	3951.1	63	FC1	3968.3	0.44
B4	493.88	506	E06	494.07	0.04	C8	4186.0	60	FC4	4166.7	-0.46

16. Watch Dog Timer (WDT)

Watch dog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that the WDT will always run even in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E bit2 - 0) are used to select different overflow frequency. WDT bit3 is the watchdog timer overflow flag. The watchdog timer overflow flag ($1E bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watch dog timer control register Bit3: Watchdog timer overflow flag register (read only)
	X	0	0	0	R/W	Watch dog timer-out period = 4096ms
	X	0	0	1	R/W	Watch dog timer-out period = 1024ms
	X	0	1	0	R/W	Watch dog timer-out period = 256ms
	X	0	1	1	R/W	Watch dog timer-out period = 128ms
	X	1	0	0	R/W	Watch dog timer-out period = 64ms
	X	1	0	1	R/W	Watch dog timer-out period = 16ms
	X	1	1	0	R/W	Watch dog timer-out period = 4ms
	X	1	1	1	R/W	Watch dog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow resets
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note:

Watchdog timer-out period valid for V_{DD} = 5V.

17. Interrupt

Four interrupt sources are available on SH69P55A/69K55A:
- Timer0 interrupt
- Timer1 interrupt
- Timer2 interrupt
- External interrupts (include PORTB, PORTC interrupts (Falling edge), AD interrupt, Key scan interrupt)

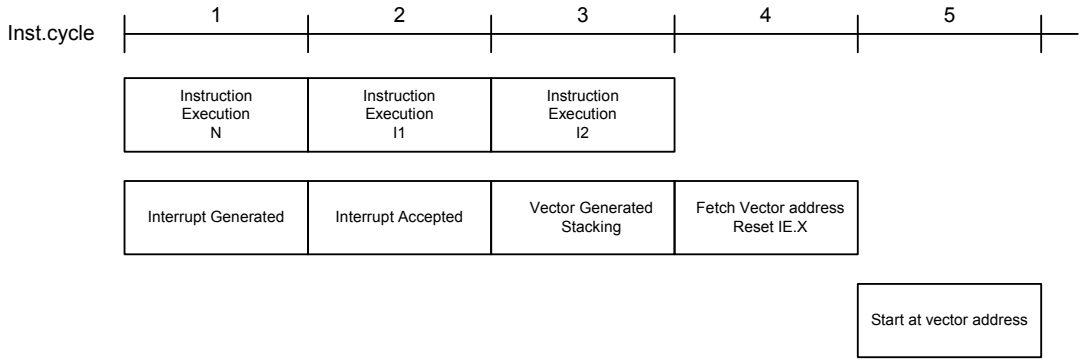
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed by the program. Those flags are cleared to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IET0	IET1	IET2	IEEX	R/W	Interrupt enable flags register
$01	IRQT0	IRQT1	IRQT2	IRQEX	R/W	Interrupt request flags register

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into the stack memory and jump to the interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the SH6610D CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

Timer (Timer0, Timer1, Timer2) Interrupt

The input clock of Timer0, Timer1 and Timer2 are based on system clocks or external clock/event T0 input as Timer0 source and T2 input as Timer2 source. The timer overflow from $FF to $00 (from $FFFF to $0000 for Timer2) will generate an internal interrupt request (IRQT0, IRQT1 = 1 or IRQT2 = 1), If the interrupt enable flag is enabled (IET0, IET1 = 1 or IET2 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from the HALT mode.

External Interrupts

External interrupts include PORTB, PORTC falling edge interrupt; ADC interrupt and Key scan interrupt. Any external interrupt occur, an internal interrupt request (IRQEX) will be generated, if the interrupt enable flag is enabled (IEEX), an external interrupt service routine will start.

■ **PORTB, PORTC falling Edge Interrupt**

The PORTB and PORTC are used as external port interrupt sources. Since PORTB and PORTC are bit programmable I/Os, only when the PORTB and PORTC are selected as normal I/O input, the voltage transition from VDD to GND applying to the digital input port can generate a port interrupt. When they are selected as analog input (such as ADC input), Port interrupt request cannot be generated.

The interrupt control flags are mapped on $388, $38A, $38C of the system register. They can be accessed or tested by the read/write operation. Those flags are cleared to 0 at the initialization by the chip reset. Port Interrupts can be used to wake up the CPU from the HALT or the STOP mode.

Port Interrupt Enable Flags Register: $388, $38A

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags register
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	R/W	PORTC interrupt enable flags register

PB/CIEN.n, (n = 0, 1, 2, 3)
0: Disable port interrupt. (Default)
1: Enable port interrupt.

Port Interrupt Request Flags Register: $389, $38B

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$389	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags register
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	R/W	PORTC interrupt request flags register

PB/CIF.n, (n = 0, 1, 2, 3)
0: Port interrupt is not presented. (Default)
1: Port interrupt is presented.
Only writing these bits to 0 is available.

Application Notes:

Any one of PORTB & PORTC input pin transitions from V_{DD} to GND would set PBIF.x or PCIF.x to “1”, in spite of level of the other pin of PORTB and PORTC.

If PBIEN.x (or PCIEN.x) = 1and IEEX = 1, the x of PORTB (or PORTC) input pin transitions from V_{DD} to GND would generate an interrupt request (PBIF.x = 1 or PCIF.x = 1) and interrupt the CPU, in spite of level of the other pin of PORTB (or PORTC).

■ **ADC Interrupt**

When the A/D conversion is complete, it will generate an interrupt request (ADIF = 1), if the ADC interrupt is enabled (ADIE = 1), an external interrupt service routine will start. The ADC interrupt can be used to wake the CPU from HALT mode.

■ **Key Scan Interrupt**

When the Key scan is complete, it will generate an interrupt request (KEYIF = 1), if the Key scan interrupt is enabled (KEYIE = 1), an External interrupt service routine will start. The KEY scan interrupt can be used to wake the CPU from HALT mode.

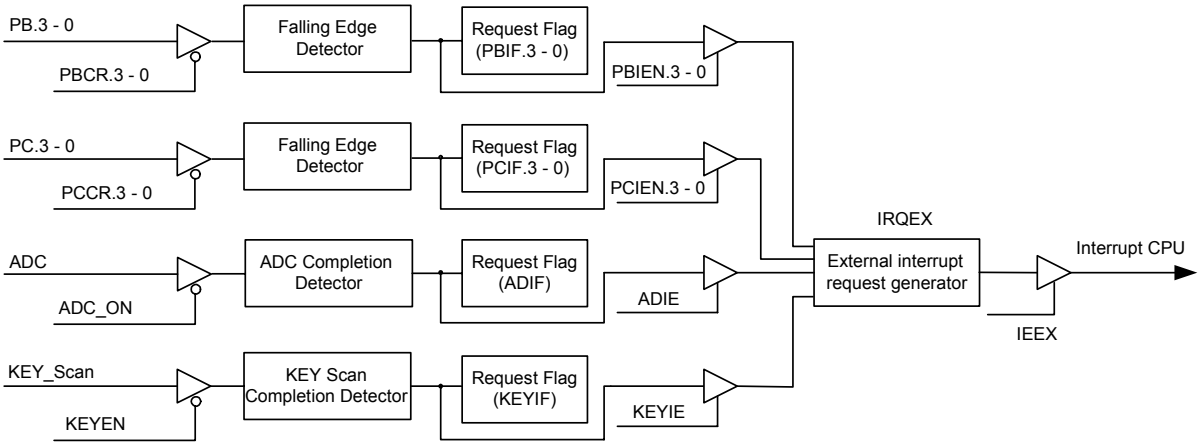
Other External Interrupt Enable Flags Register: $38C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38C	-	-	KEYIE	ADIE	R/W	Bit0: ADC interrupt enable flag register Bit1: Key scan interrupt enable flag register

Other External Interrupt Request Flags Register: $38D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38D	-	-	KEYIF	ADIF	R/W	Bit0: ADC interrupt request flag register Bit1: Key scan interrupt request flag register

Only writing these bits to 0 is available.



Port (including other external sources) Interrupt Function Block-diagram

18. HALT and STOP Mode

After the execution of HALT instruction, SH69P55A/69K55A will enter the HALT mode. In the HALT mode, CPU will stop operating but peripheral circuits (Timer0, Timer1, Timer2, ADC, PWM and watchdog timer) will keep status.

After the execution of STOP instruction, SH69P55A/69K55A will enter the STOP mode. The whole chip (If the OSC is not 32.768kHz, the oscillator will stop in STOP mode. If the OSC is 32.768kHz, the oscillator ON/OFF in STOP mode will be controlled by the register $23) will stop operating without watchdog timer if it is enabled.

In the HALT mode, SH69P55A/69K55A can be waked up if any interrupt occurs.

In the STOP mode, SH69P55A/69K55A can be waked up if any port interrupt occurs or watchdog timer overflows (WDT is enabled).

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

19. Warm-up Timer

The device has a build-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

A. Power-on Reset

(1) In Internal RC oscillator mode, fosc = 4MHz, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).
(2) In External RC oscillator mode, fosc = 400kHz - 8MHz, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).
(3) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).
(4) In 32.768kHz mode, the warm-up counter prescaler divide ratio is $1/2^{13}$ (8192).

B. WDT Reset, LVR Reset, Pin Reset

(1) In Internal RC oscillator mode, fosc = 4MHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128).
(2) In External RC oscillator mode, fosc = 400kHz - 8MHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128).
(3) In crystal oscillator or ceramic resonator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(4) In 32.768kHz mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

C. Wake up from STOP Mode

(1) In Internal RC oscillator mode, fosc = 4MHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128).
(2) In External RC oscillator mode, fosc = 400kHz - 8MHz, the warm-up counter prescaler divide ratio is $1/2^{7}$ (128).
(3) In crystal oscillator or ceramic resonator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(4) In 32.768kHz mode, the warm-up counter prescaler divide ratio is as follows:

System Clock	32.768kHz in Stop	Warm-up counter prescaler divide ratio
PLL	On	$1/2^{7}$
	Off	$1/2^{12}$
32.768kHz	On	$1/2^{2}$
	Off	$1/2^{12}$

20. Code Option

(a) Oscillator Type:

OSC[2:0]:

000 = Internal RC Oscillator (Select OSCO pin as PORTC1 and OSCI pin as PORTC2 for normal I/O ports.) (default)
001 = External RC Oscillator (400kHz - 8MHz) (Select OSCO pin as PORTC1 for a normal I/O port.)
010 = Ceramic Resonator (400kHz - 8MHz)
011 = Crystal Oscillator (400kHz - 8MHz)
100 = 32.768kHz Crystal Oscillator

(b) Watch Dog Timer:

WDT:

0 = Enable WDT function. (default)
1 = Disable WDT function.

(c) Low Voltage Reset:

LVR:

0 = Disable LVR function. (default)
1 = Enable LVR function.

(d) LVR voltage Range:

LVR0:

0 = 4V LVR voltage (default)
1 = 2.5V LVR voltage

(e) Chip Pin Reset:

RST:

0 = Enable (default)
1 = Disable (Select RESET pin as PORTC3.)

(f) OSC Clock Range Select:

FOSC[1:0]:

00 = 4MHz < OSC Clock <= 8MHz (default)
01 = 2MHz < OSC Clock <= 4MHz
10 = 1MHz < OSC Clock <= 2MHz
11 = 400kHz < OSC Clock <= 1MHz

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
P	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

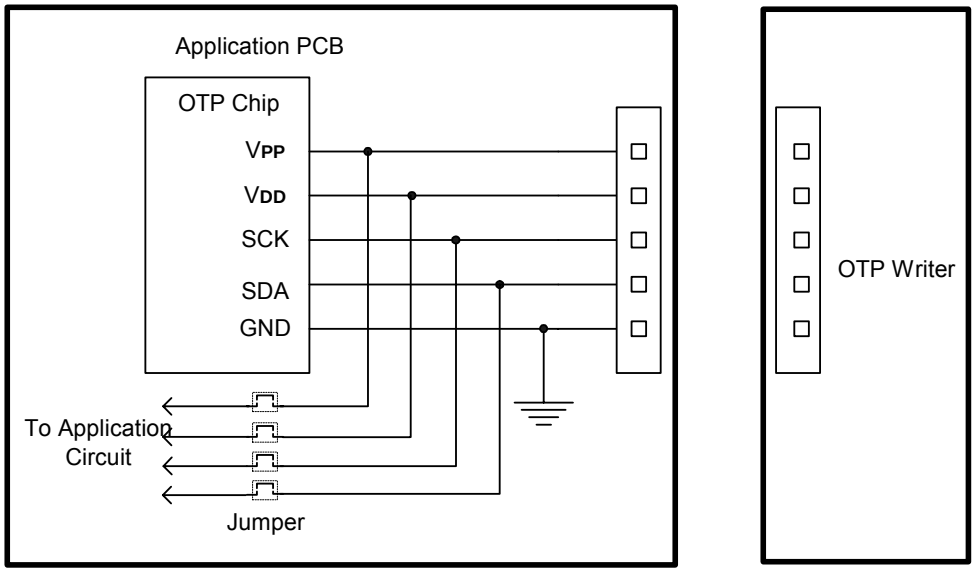
In System Programming Note for OTP

The In System Programming technology is valid for OTP chip (SH69P55A).

The Programming Interface of the OTP chip must be set on the user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.

For few OTP chip with more V_{DD} pads, the V_{DD} pads should be connected together.



The recommended step is the followings:

(1) The jumper is Open to separate the programming pins from the application circuit before programming the chip.

(2) Connect the programming interface with OTP Writer and begin Programming.

(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . .-40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 2.4 - 5.5V GND = 0V, T_A = -40℃ to +85℃, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	30kHz ≤ fosc ≤ 8MHz
		2.4	5.0	5.5	V	30kHz ≤ fosc ≤ 4MHz
Low Voltage Reset Voltage	V_{LVR}	3.8	-	4.2	V	LVR (4V) enable
		2.3	-	2.7	V	LVR (2.5V) enable
Operating Current	I_{OP}	-	2	3	mA	fosc = 8MHz, V_{DD} = 5.0V All output pins unloaded, Execute NOP instruction (WDT off, ADC disable, LVR off, LCD off, Key scan disable)
		-	1.0	1.5	mA	fosc = 4MHz, V_{DD} = 5.0V All output pins unloaded, Execute NOP instruction (WDT off, ADC disable, LVR off, LCD off, Key scan disable)
			12	20	μA	fosc = 32.768kHz, V_{DD} = 5.0V All output pins unloaded, Execute NOP instruction (WDT off, ADC disable, LVR off, LCD off, Key scan disable)
Stand by Current1 (HALT)	I_{SB1}	-	-	1.8	mA	fosc = 8MHz, V_{DD} = 5.0V All output pins unloaded (all input pins is not floating) CPU stop (HALT mode), WDT off, LVR off, LCD off
		-	-	1.3	mA	fosc = 4MHz, V_{DD} = 5.0V All output pins unloaded (all input pins is not floating) CPU stop (HALT mode), WDT off, LVR off, LCD off
			8	15	μA	fosc = 32.768kHz, V_{DD} = 5.0V All output pins unloaded (all input pins is not floating) CPU stop (HALT mode), WDT off, LVR off, LCD off
Stand by Current2 (STOP)	I_{SB2}	-	-	10	μA	fosc = 32.768kHz V_{DD} = 5.0V All output pins unloaded (all input pins is not floating) CPU stop (STOP mode) WDT off, ADC disable LCD off, 32.768kHz on
		-	-	1	μA	V_{DD} = 5.0V All output pins unloaded (all input pins is not floating) CPU stop (STOP mode) LCD off, LVR off, WDT off
Input Low Voltage	V_{IL}	GND	-	V_{DD} X0.3	V	I/O Ports pins tri-state
		GND	-	V_{DD} X0.2	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger)
Input High Voltage	V_{IH}	V_{DD} X0.7	-	V_{DD}	V	I/O Ports, pins tri-state
		V_{DD} X0.8	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger)
Input Leakage Current	I_{IL}	-1	-	1	μA	I/O ports, V_{IN} = V_{DD} or GND
Pull-high Resistor	R_{PH}	-	30	-	kΩ	Pull-high resistor (V_{DD} = 5.0V)

DC Electrical Characteristics (Continued)
(V_{DD} = 2.4 - 5.5V GND = 0V, T_A = -40℃ to +85℃, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output High Voltage	V_{OH}	V_{DD}-0.7	-	-	V	I/O ports, I_{OH} = -10mA (V_{DD} = 5.0V)
Output Low Voltage	V_{OL}	-	-	GND+0.6	V	I/O ports, I_{OL} = 20mA (exclude PORTD, PORTE.2-3, V_{DD} = 5.0V)
		-	-	GND+1.5	V	I/O ports, I_{OL} = 200mA (PORTD, PORTE.2-3, V_{DD} = 5.0V)
WDT Current	I_{WDT}	-	-	20	μA	V_{DD} = 5.0V
LCD Driving on Resistor	R_{ON}	-	5	-	kΩ	LCD COMx, LCD SEGx, the voltage variation of V1, V2, V3, is less than 0.2V
LCD Voltage Divider Resistor	R_{LCD}	-	90 10	-	kΩ	RLCD = 0 RLCD = 1

Note:
Max. Current into V_{DD} = 200mA
Max. Current out of V_{SS} = 250mA
*: Data in "Typ." column is at 5.0V, 25°C, unless otherwise specified.

AC Electrical Characteristics (V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified.)

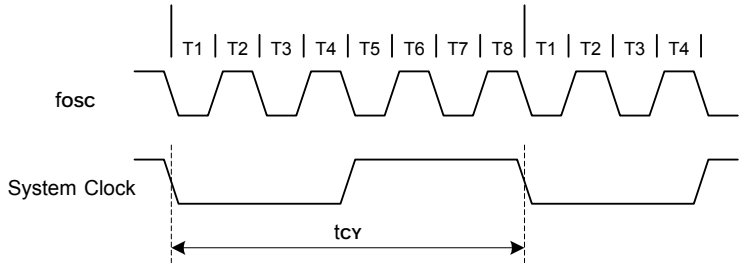
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	t_{CY}	0.5	-	133.4	μs	30kHz ≤ f_{OSC} ≤ 8MHz
T0/T2 input width	t_{IW}	(T_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	
RESET pulse width	t_{RESET}	10	-	-	μs	Low active V_{DD} = 5.0V
WDT Period	t_{WDT}	1	-	-	ms	V_{DD} = 5.0V
PLL Frequency Variation	|ΔF|/F			0.6	%	Average frequency of continuous 256 clocks
Frequency Stability (RC)	|ΔF|/F	-	-	15	%	External R_{OSC} Oscillator, Include chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)
Frequency Stability (RC)	|ΔF|/F	-	-	5	%	Internal R_{OSC} Oscillator, f_{OSC} = 4MHz. Include chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)

A/D Converter Electrical Characteristics
(V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = 25℃, f_{OSC} = 30kHz - 8MHz, unless otherwise specified.)

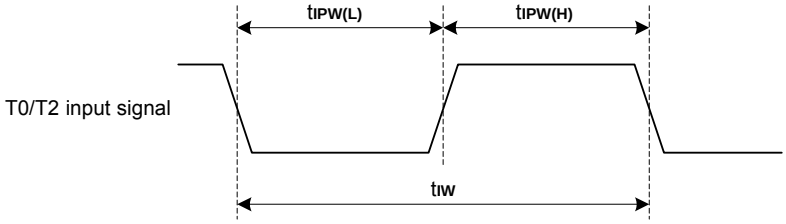
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	N_R	-	10	-	bit	GND ≤ V_{AIN} ≤ V_{REF}
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor	R_{AIN}	2	1000	-	MΩ	V_{IN} = 5.0V
A/D conversion current	I_{AD}	-	1	3	mA	A/D converter module operating, V_{DD} = 5.0V
A/D Input current	I_{ADIN}			10	μA	V_{DD} = 5.0V
Differential linearity error	D_{LE}	-	-	±1	LSB	V_{REF} = V_{DD} = 5.12V, f_{OSC} = 8MHz
Integral linearity error	I_{LE}			±2	LSB	V_{REF} = V_{DD} = 5.12V, f_{OSC} = 8MHz
Full scale error	E_F	-	±3	-	LSB	V_{REF} = V_{DD} = 5.12V, f_{OSC} = 8MHz
Offset error	E_Z	-	±0.5	±2	LSB	V_{REF} = V_{DD} = 5.12V, f_{OSC} = 8MHz
Total Absolute error	E_{AD}	-	±3	-	LSB	V_{REF} = V_{DD} = 5.12V, f_{OSC} = 8MHz
Conversion time	T_{CON}	25	-	-	μs	10 bit resolution and f_{OSC} = 8MHz

Timing Waveform

(a) System Clock Timing Waveform

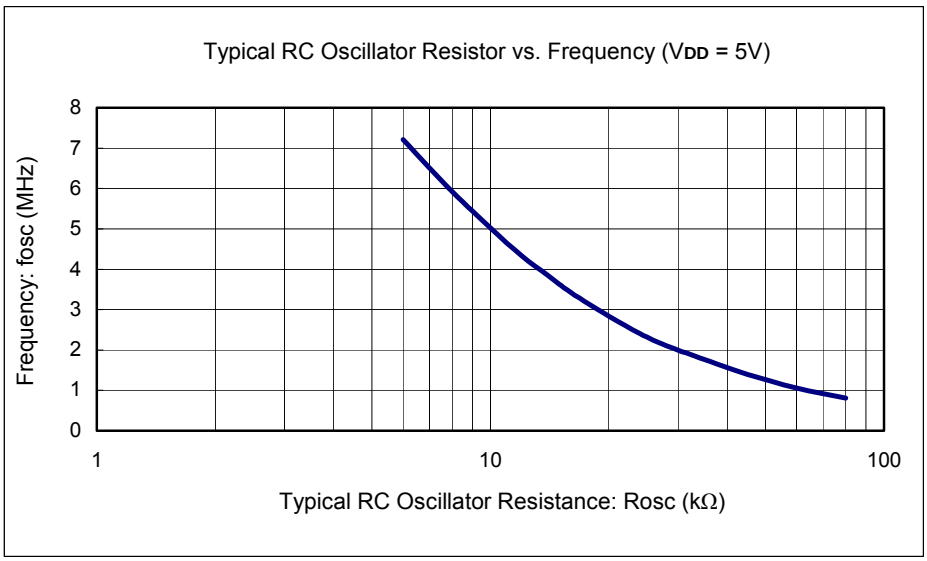


(b) T0/T2 Input Waveform

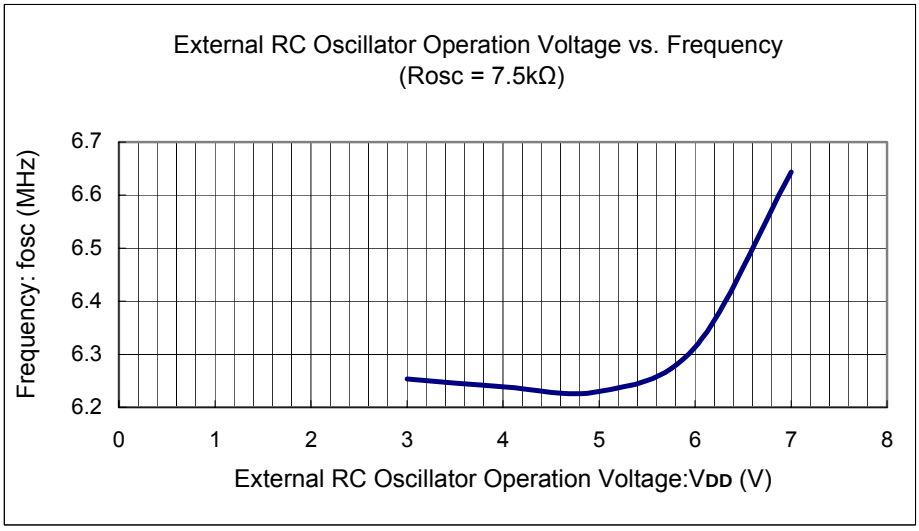


RC Oscillator Characteristics Graphs (for reference only)

(a) External RC Oscillator Resistor vs. Frequency:



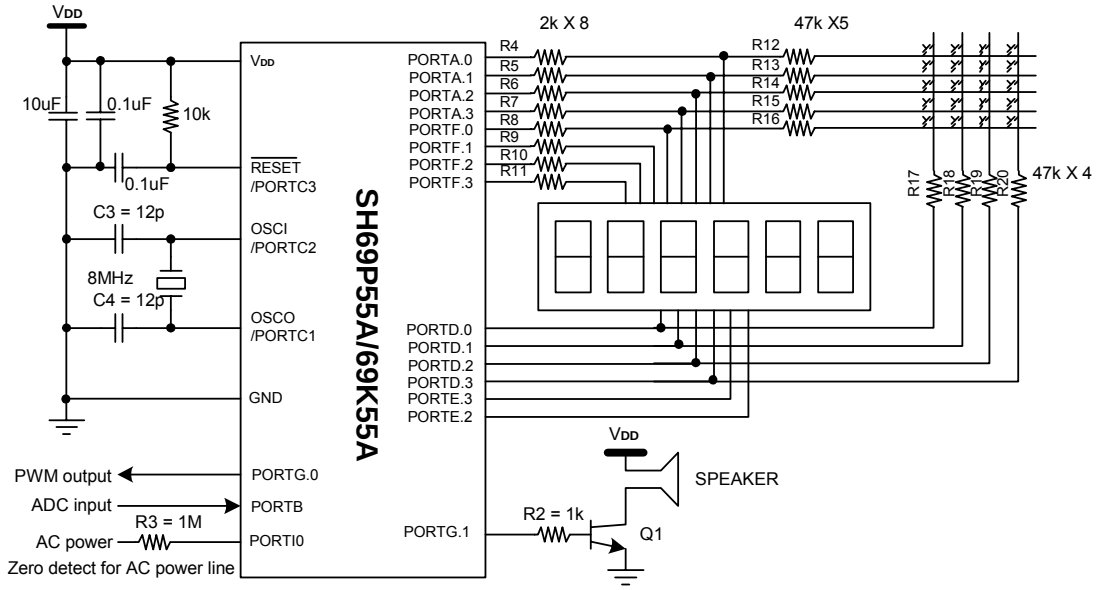
(b) External RC Oscillator Operation Voltage vs. Frequency:



Application Circuit (for reference only)

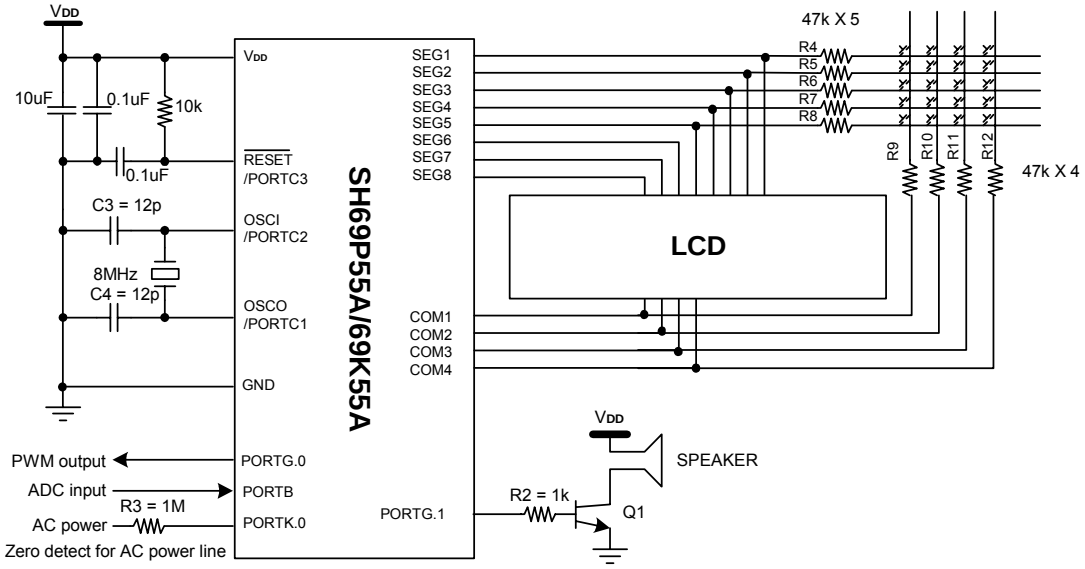
AP1:

(1) Operating voltage: 5.0V
(2) Oscillator: Crystal 8MHz
(3) PORTA, PORTF: LED SEG1-8.
PORTD, PORTE.3, PORTE.2: LEDCOM1-6.
PORTA, PORTD are shared as keyscan ports.
PORTG.1 is used as tone output.
PORTI.0 is used as Zero Cross Detect function for AC Power line.
PORTG.0 is used as PWM output.
PORTB are used as ADC ports.



AP2:

(1) Operating voltage: 5.0V
(2) Oscillator: Crystal 8MHz
(3) PORTA, PORTF: LCD SEG1-8.
PORTD: LCD COM1-4.
PORTA, PORTD are shared as keyscan ports.
PORTG.1 is used as tone output.
PORTK.0 is used as Zero Cross Detect function for AC Power line.
PORTG.0 is used as PWM output.
PORTB are used as ADC ports.

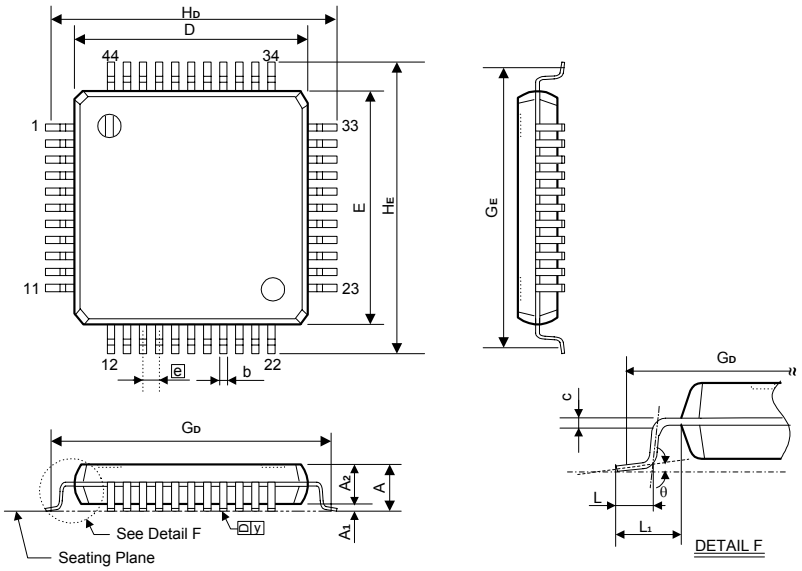


Ordering Information

Part No.	Package
SH69P55AF/SH69K55AF	44 QFP
SH69P55AM/SH69K55AM	28 SOP
SH69P55A/SH69K55A	32 DIP

Package Information

QFP 44 Outline Dimensions unit: inch/mm

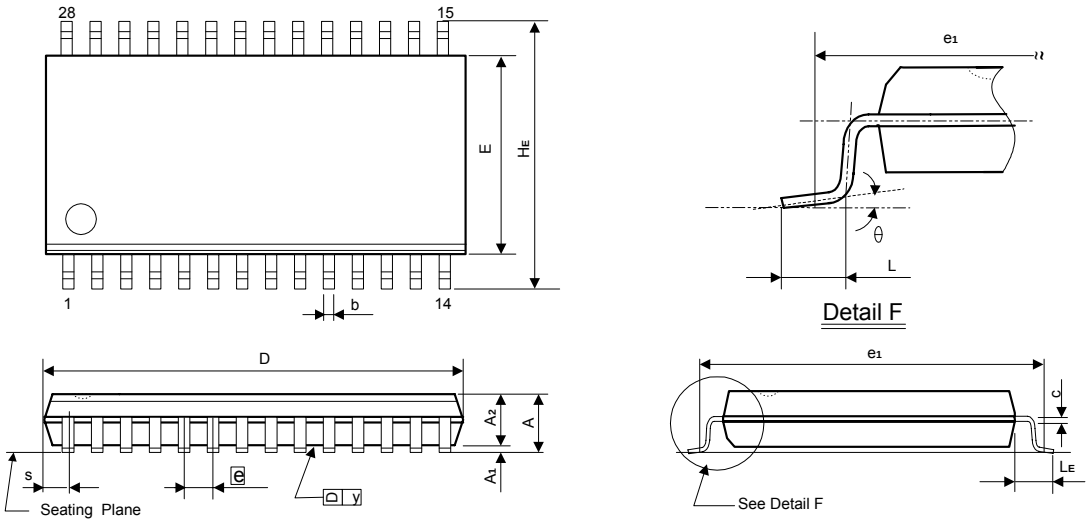


Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.70 Max.
A_1	0.01 Min.0.02Max.	0.25 Min.0.50Max.
A_2	0.079+0.008 -0.004	2.00+0.2 -0.1
b	0.012 Typ.	0.30 Typ.
c	0.006 ± 0.002	0.15 ± 0.05
D	0.394 ± 0.004	10.00 ± 0.10
E	0.394 ± 0.004	10.00 ± 0.10
e	0.031 Typ.	0.80 Typ.
G_D	0.488 NOM.	12.40 NOM.
G_E	0.488 NOM.	12.40 NOM.
H_D	0.519 ± 0.008	13.20 ± 0.20
H_E	0.519 ± 0.008	13.20 ± 0.20
L	0.035+0.002 -0.006	0.88+0.05 -0.15
L_1	0.063 Typ.	1.60 Typ.
y	0.004 Max.	0.10 Max.
θ	0° - 7°	0° - 7°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

SOP (W.B.) 28L Outline Dimensions unit: inches/mm

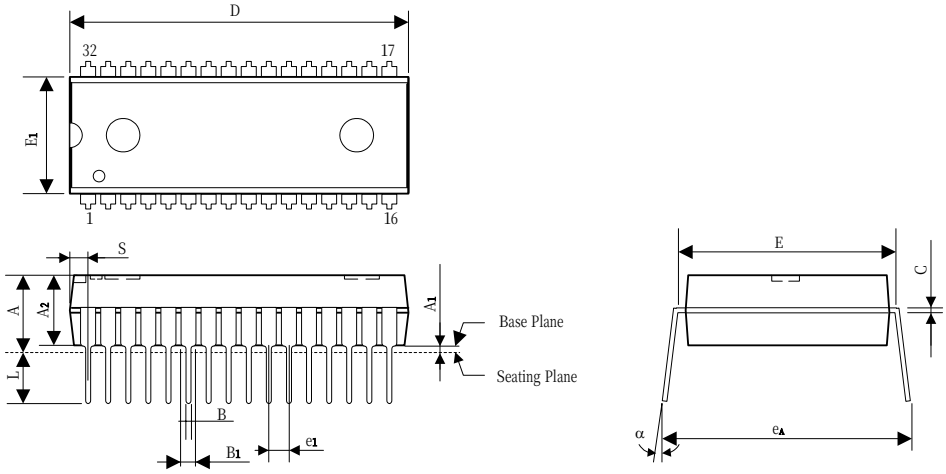


Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.093 ± 0.005	2.36 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.705 ± 0.020	17.91 ± 0.51
E	0.291 - 0.299	7.39 - 7.59
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.40 NOM.
H_E	0.394 - 0.417	10.01 - 10.60
L	0.036 ± 0.008	0.91 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.043 Max.	1.09 Max.
y	0.004 Max.	0.10 Max.
θ	0° - 10°	0° - 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

P-DIP 32L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.155 ± 0.010	3.94 ± 0.25
B	0.018+0.004 -0.002	0.46+0.10 -0.05
B_1	0.050+0.004 -0.002	1.27+0.10 -0.05
C	0.010+0.004 -0.002	0.25+0.11 -0.05
D	1.650 Typ. (1.670 Max.)	41.91 Typ. (42.42 Max.)
E	0.600 ± 0.010	15.24 ± 0.25
E_1	0.550 Typ. (0.562 Max.)	13.97 Typ. (14.27 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.655 ± 0.035	16.64 ± 0.89
S	0.090 Max.	2.29 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.2	Add keyscan description	Jan. 2011
2.1	Ordering information updated	Dec. 2008
2.0	Ordering information updated	Mar. 2008
1.0	Original	Jan. 2008