SINO WEALTH

SH69P20

PRELIMINARY

OTP 4-bit Microcontroller

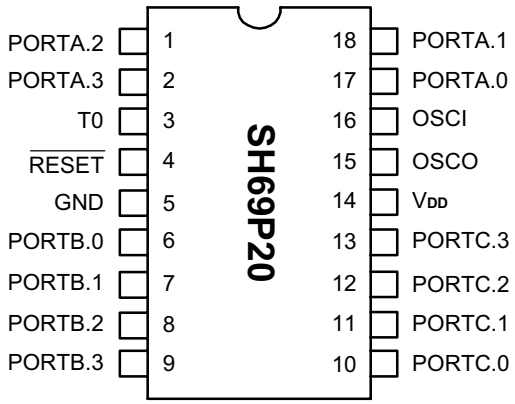
Features

- SH6610C-based single-chip 4-bit microcontroller
- ROM: 1K X 16 bits
- RAM: 64 X 4 bits (Data memory)
- Operation voltage: 3.3V - 6.0V (Typical 5.0V)
- 12 CMOS bi-directional I/O pins
- Built in pull-up and pull-low resistor for PortB and PortC
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-load timer/counter
- Warm-up timer for power on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0)
  - External interrupts: PortB & PortC (Rising or Falling edge)
- Oscillator (user option)
  - X`tal oscillator: 32.768KHz ~ 4MHz
  - Ceramic resonator: 400K ~ 4MHz
  - RC oscillator: 400K ~ 4MHz
  - External clock: 30K ~ 4MHz
- Instruction cycle time:
  - 4/32.768KHz (≈ 122us) for 32.768KHz OSC clock
  - 4/4MHz (= 1us) for 4MHz OSC clock
- Two low power operation modes: HALT and STOP
- OTP type
- Code protection
- Built-in watchdog timer

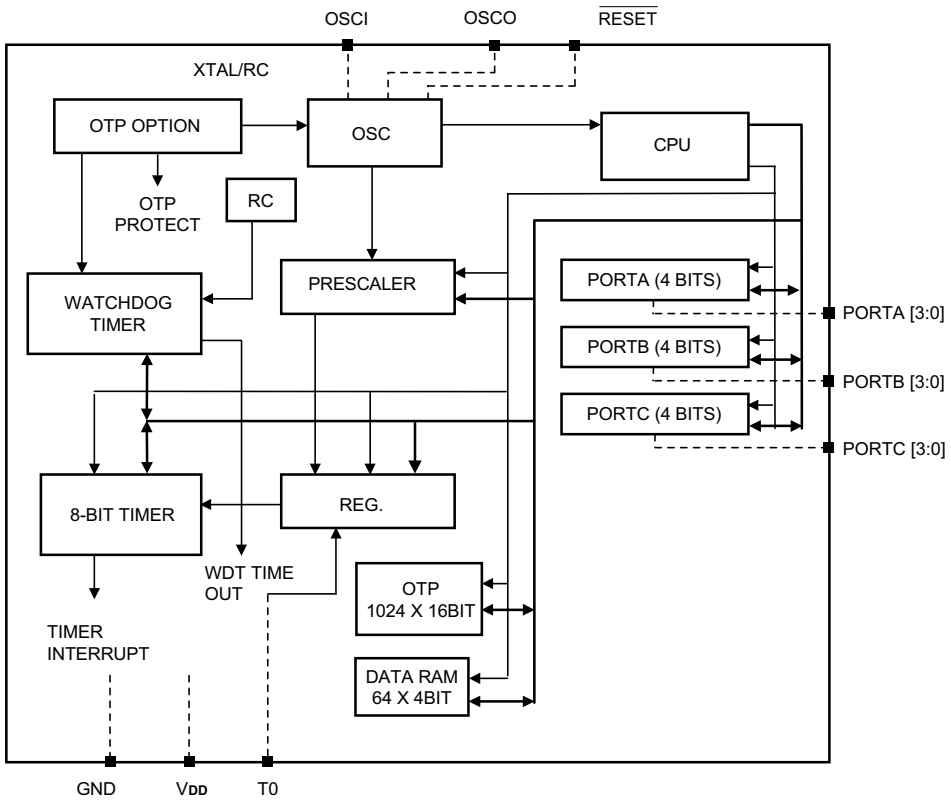
General Description

SH69P20 is a 4-bit microcontroller. This chip integrates the SH6610C 4-bit CPU core with SRAM, 1K program ROM, Timer and I/O Port.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Designation	I/O	Description
1 - 2	PORTA2, 3	I/O	Bit programmable I/O
3	T0	I	Timer Clock/Counter (Schmitt Trigger input)
4	$\overline{\text{RESET}}$	I	Reset input (Active Low)
5	GND	P	Ground pin
6 - 9	PORTB0 - 3	I/O	Bit programmable I/O, Vector Interrupt (Active rising or falling edge by system register setup)
10 - 13	PORTC0 - 3	I/O	Bit programmable I/O, Vector Interrupt (Active rising or falling edge by system register setup)
14	V_{DD}	P	Power supply pin
15	OSCO	O	OSC output pin. There is a signal with a frequency of Fosc/4 for RC mode
16	OSCI	I	OSC input pin can be connected to crystal、ceramic or external resistor
17 - 18	PORTA0, 1	I/O	Bit programmable I/O

Note: The all pins excluding pin15 are shared with OTP programming.

Function Description

1. CPU

The CPU contains the following function blocks: Program Counter, Arithmetic Logic Unit (ALU), Carry Flag, Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL), and Stack.

1.1. PC (Program Counter)

The Program Counter is used to address the 1K program ROM. It consists of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BNC),

(2) When executing a subroutine call instruction (CALL),

(3) When an interrupt occurs,

(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2. ALU and CY

The ALU performs arithmetic and logic operations. It provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjust for addition/subtraction (DAA, DAS) Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BAZ, BNC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow which the arithmetic operation generates. During an interrupt servicing or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator

The Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data transfer between the accumulator and system register, or data memory can be performed.

1.4. Stack

This group of registers is used to save the contents of CY & PC (11 - 0) sequentially with each subroutine call or interrupt. It is organized to 13 bits X 4 levels. The MSB is saved for CY. Four levels are the maximum allowed total for subroutine calls and interrupts.

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine call and interrupt requests. Note that program execution may enter an abnormal state if the number of calls and interrupt requests exceed 4, where then the bottom of stack will be shifted out.

2. ROM

The SH69P20 can address up to 1024 X 16 bit of program area from $000 to $3FF.
Service routine such as starting vector address.

Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Function
$000H	JMP instruction	Jump to RESET service routine
$001H	NOP	Reserved
$002H	JMP instruction	Jump to TIMER0 service routine
$003H	NOP	Reserved
$004H	JMP instruction	Jump to PBC service routine

3. RAM

Built-in RAM consists of general-purpose data memory and system register. Direct addressing in one instruction can accessed data memory and system register.

The following is the memory allocation map:

$000 - $01F: System register and I/O.
$020 - $05F: Data memory (64 X 4 bits).

The Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$00	-	IET0	-	IEP	R/W	Interrupt enable flags	- 0 - 0
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags	- 0 - 0
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)	- 000
$03	-	-	-	-	-	Reserved	-
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low digit	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high digit	0000
$06 - $07	-	-	-	-	-	Reserved	-
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	1111
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	1111
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	1111
$0B - $0D	-	-	-	-	-	Reserved	-
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register	-
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register	-
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble	-
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble	-
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble	-
$13 - $15	-	-	-	-	-	Reserved	-
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port	0000
$19	PULLEN	PH/PL	PBCFR	-	R/W	Bit1:PBC interrupt rising / failing edge set Bit2:Port pull-hi/low set Bit3: Port pull-up/low enable control	010 -
$1A - $1B	-	-	-	-	-	Reserved.	-
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge, Bit1: T0 signal source	- - 00
$1D	-	-	-	-	-	Reserved	-
$1E	WDT	-	-	-	W	Bit3: WDT time-out bit (write one only)	-
$1F	-	-	-	-	-	Reserved	-

* System Register $00 - $12 (Please refer to "SH6610C User's manual").

4. Low Power Detection (LPD)

The LPD function is to monitor the supply voltage and applies an internal reset in the microcontroller at the time of battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by software control.

- High reliability is not required
- Power supply voltage V_{DD} = 3.3V to 6.0 V

4.1. Functions of LPD Circuit

The LPD circuit has the following functions:

- Generates an internal reset signal when $V_{DD} \leq V_{LPD}$
- Cancels the internal reset signal when $V_{DD} > V_{LPD}$

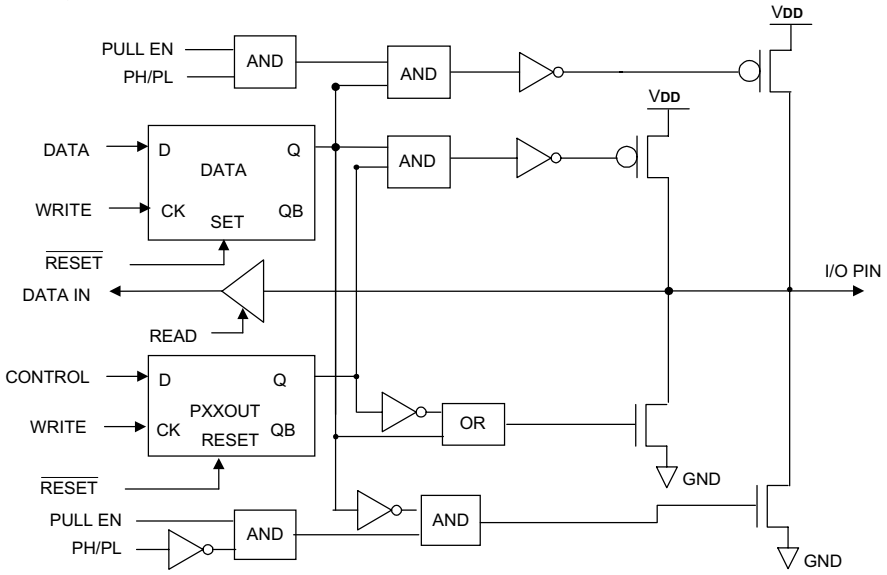
Here, V_{DD}: power supply voltage, V_{LPD}: LPD detect voltage, it is about 3.9 ± 0.5V
LPD can be enabled or disabled permanently by user option.

5. I/O Ports

The SH69P20 provides 12 I/O pins. When every I/O is used as an input port, the port control register controls ON/OFF of the output buffer. Sections below show the circuit configuration of I/O ports.
Each of these ports contains 4 bits I/O pins. ON/OFF of the output buffer for port can be controlled by the port control register.
Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Power On
$08	PORT A.3	PORT A.2	PORT A.1	PORT A.0	R/W	1111
$09	PORT B.3	PORT B.2	PORT B.1	PORT B.0	R/W	1111
$0A	PORT C.3	PORT C.2	PORT C.1	PORT C.0	R/W	1111

Equivalent circuit for a single I/O pin



System Register $15 - $18

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description	Power On
$16	PA3OUT	PA2OUT	PA1OUT	PA0OUT	W	Set PORTA to be output port	0000
$17	PB3OUT	PB2OUT	PB1OUT	PB0OUT	W	Set PORTB to be output port	0000
$18	PC3OUT	PC2OUT	PC1OUT	PC0OUT	W	Set PORTC to be output port	0000
$19	PULLEN	PH/PL	PBCFR	-	RW	Bit1:PBC interrupt rising / failing edge set Bit2:Port pull-hi/low set Bit3: Port pull-up/low enable control	010 -

I/O control register:
PAXOUT, PBXOUT, PCXOUT (X = 0, 1, 2, 3)
1: Set I/O as an output buffer
0: Set I/O as an input buffer (initial power-on)
PBCFR: 1: Rising Edge interrupt 0: Falling Edge interrupt,
PH/PL: 1: Port Pull up resister ON, 0: Port Pull low resister ON,
PULLEN: 1: Port Pull up /Pull low enable, 0: Port Pull up /Pull low disable (power-on initial)

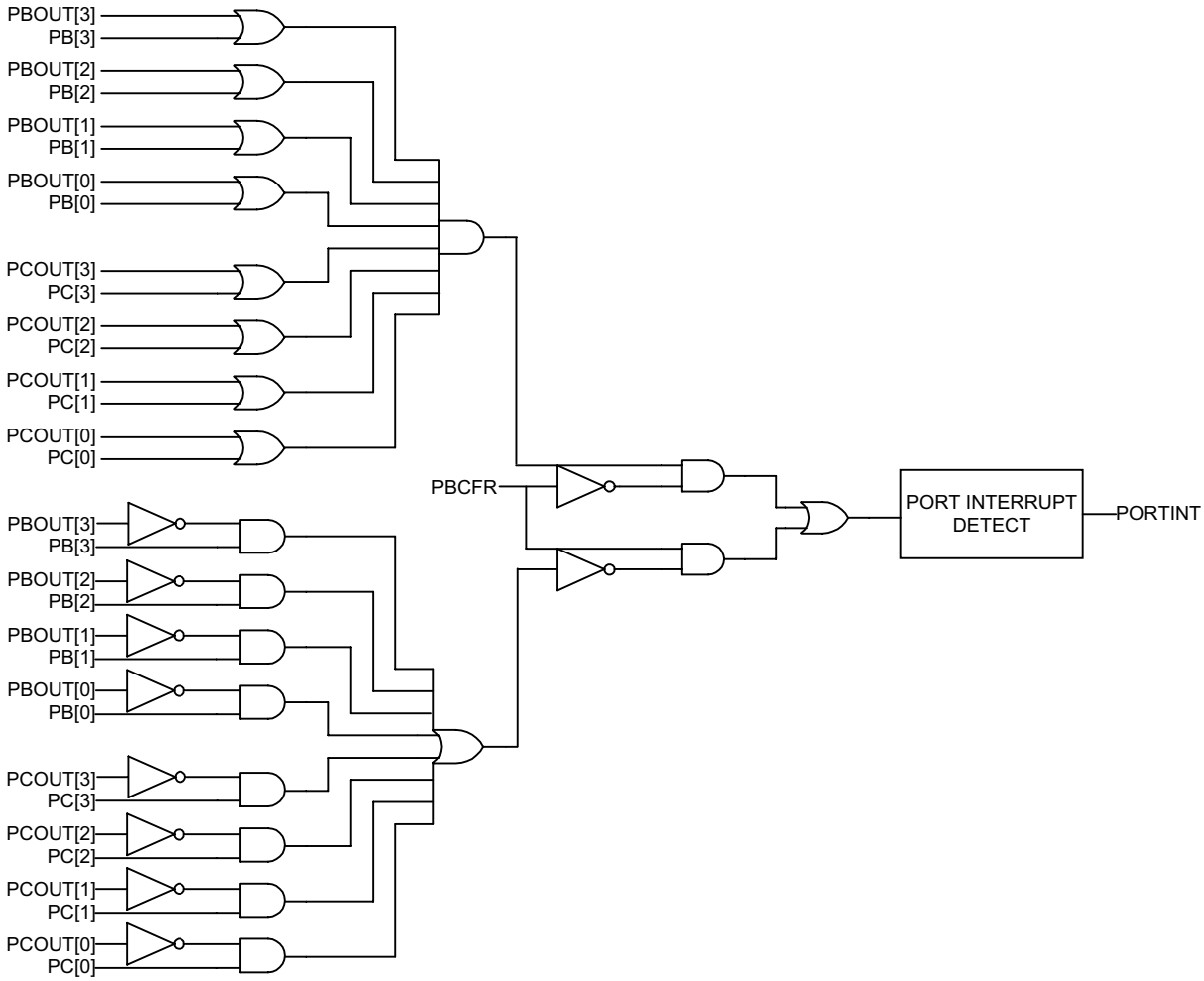
PORTB & PORTC interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is bit programmable I/O, so only the input port can generate an external interrupt.

When PBCFR set to 1, any one of the PORTB and PORTC input pin transitions from V_{DD} to GND will generate an interrupt request. And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD}.

When PBCFR set to 0, any one of the PORTB and PORTC input pin transitions from GND to V_{DD} will generate an interrupt request. And further rising edge transition would not be able to make interrupt request until all of the pins return to GND.

Following is the port interrupt function block-diagram.



6. T0 & WDT

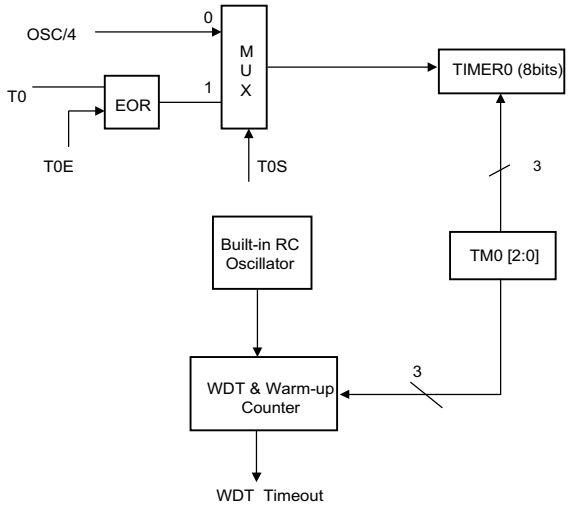
System Register $1C

Address	BIT3	BIT2	BIT1	BIT0	R/W	Remark	Power ON
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source	- - 00

T0E: T0 signal edge.
0: Increment on low-to-high transition T0 pin (initial power-on).
1: Increment on high-to-low transition T0 pin.

T0S: T0 signal source.
0: OSC 1/4 (initial power-on).
1: Transition on T0 pin.

T0, OSC1/4 & WDT



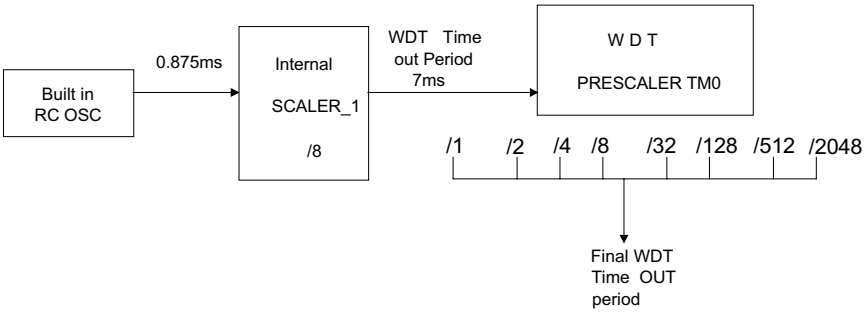
System Register $1E

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remark
$1E	WDT	-	-	-	W	Bit3: WDT time-out bit (write one only)

The input clock of watchdog timer is generated by a built-in RC oscillator, so that the WDT will always run even in the STOP mode. SH69P20 generates a RESET condition when watchdog times-out. Watchdog can be enabled or disabled permanently by user option. To prevent it from timing out and generating a device RESET condition, one can write this bit as "1" before timing-out. The WDT has a time-out period of more than 7ms (V_{DD} = 5V). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:2048 can be assigned to the WDT under software controlled by writing to the TM0 register.

Pre-scaler divide ratio (valid for V_{DD} = 5V):

TM0.2	TM0.1	TM0.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	7ms
1	1	0	1:2	14ms
1	0	1	1:4	28ms
1	0	0	1:8	56ms
0	1	1	1:32	224ms
0	1	0	1:128	896ms
0	0	1	1:512	3,584ms
0	0	0	1:2048 (Power on initial)	14,336ms

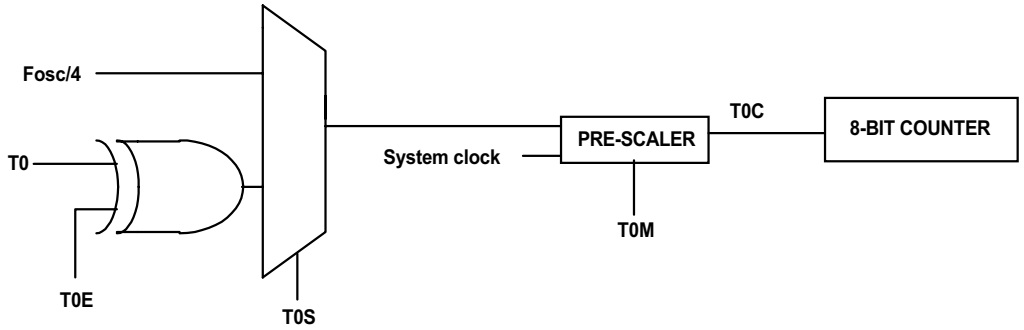


7. Timer0

SH69P20 has one 8-bit timer. The time/counter has the following features:

. 8-bit timer/counter
. Readable and writable
. Automatic reloadable counter
. 8-prescaller scale is available
. Internal and external clock select
. Interrupt on overflow from $FF to $00
. Edge select for external event

Following is a simplified timer block diagram:



7.1. Configuration and Operation

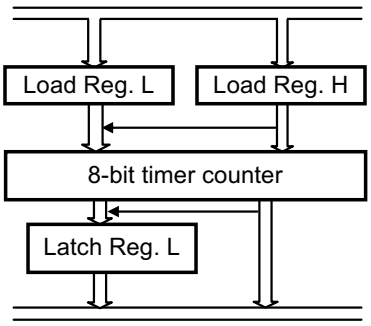
Timer-0 consists of an 8-bit write-only timer load register (TL0L, TL0H), and an 8-bit read-only timer counter (TC0L, TC0H). The counter and load register both have low order digits and high order digits. The timer counter can be initialized by writing data into the timer load register (TL0L, TL0H). Load register programming: write the low-order digit first and then the high-order digit. The timer counter is loaded with the content of load register automatically when the high order digit is written or counter counts overflow from $FF to $00.
Timer Load Register: Since the register H would control the physical READ and WRITE operation. Please follow these rules:

Write Operation:

Low nibble first;
High nibble to update the counter.

Read Operation:

High nibble first;
Low nibble followed.



7.2. Timer0 Interrupt

The timer overflow will generate an internal interrupt request, when the counter counts overflow from $FF to $00. If the interrupt enable flag is enabled, then a timer interrupt service routine will proceed. This can also be used to wake CPU from HALT mode.

7.3. Timer0 mode register

The timer can be programmed in several different prescaler ratio by setting Timer Mode register (TM0). The 8-bit counter counts prescaler overflow output pulses. The timer mode registers (TM0) are 3-bit registers used for timer control as shown in table1. These mode registers select the input pulse sources into the timer.

Timer 0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Ratio N
0	0	0	$/2^{11}$	2048 (initial)
0	0	1	$/2^{9}$	512
0	1	0	$/2^{7}$	128
0	1	1	$/2^{5}$	32
1	0	0	$/2^{3}$	8
1	0	1	$/2^{2}$	4
1	1	0	$/2^{1}$	2
1	1	1	$/2^{0}$	1

7.4. External Clock/Event T0 as TMR0 Source

When external clock/event input is used for TM0, it is synchronized with CPU system clock. Therefore the external source must follow certain constrains. The output from T0M multiplex is T0C. It is sampled by system clock in instruction frame cycle. Therefore it is necessary for T0C to be high at least 2 t**osc** and low at least 2 t**osc**. When prescaler ratio selects /20, T0C is the same as the system clock input. Therefore the requirement is as follows:

$$T0H = T0CH = T0 \text{ high time} \geq 2\ t_{osc} + \Delta T$$

$$T0L = T0CL = T0 \text{ low time} \geq 2\ t_{osc} + \Delta T$$

When other prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical.

Then:

$$T0C \text{ high time} = T0C \text{ low time} = \frac{N * T0}{2}$$

Where

T0 = Timer0 input period

N = prescaler value

The requirement is, therefore:

$$\frac{N * T0}{2} \geq 2\ tosc + \Delta T \text{ , or } T0 \geq \frac{4 * t_{osc} + 2\Delta T}{N}$$

The limitation is applied for T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * t_{osc} + 2\Delta T}{N}$$

8. Interrupt

Two interrupt sources are available on for:

- Timer0 overflow interrupt
- Port's rising/falling edge detection interrupt (PBC)

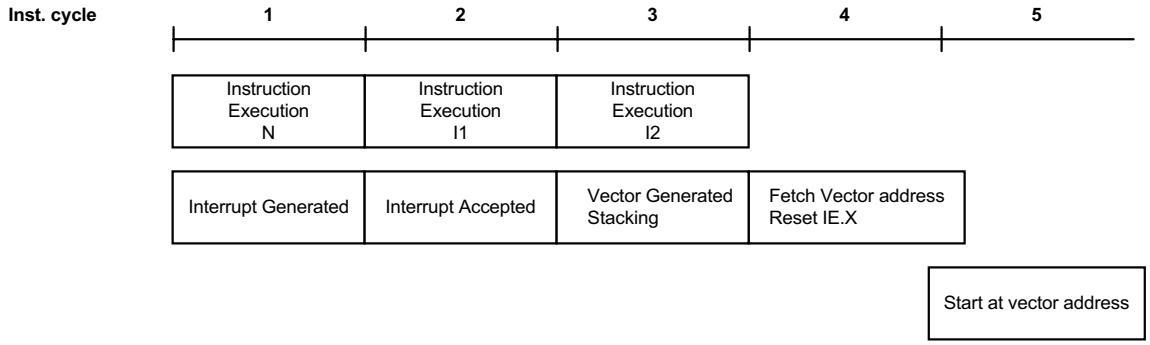
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 through $01 of the system register. They can be accessed or tested by program. Those flags are cleared to 0 at initialization by chip reset.

Address	Bit3	Bit2	Bit1	Bit0	Remarks	Power On
$00	-	IET0	-	IEP	Interrupt enable flags	- 0 - 0
$01	-	IRQT0	-	IRQP	Interrupt request flags	- 0 - 0

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

System Clock and Oscillator

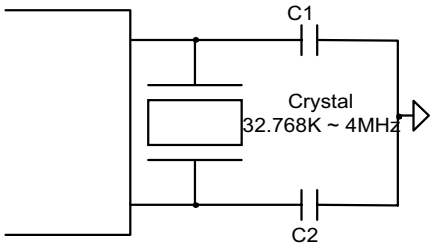
System clock generator produces the basic clock pulses that provide the system clock with CPU and peripherals.
Instruction cycle time

(1) 4/32.768KHz (≈ 122us) for 32.768KHz system clock.

(2) 4/4MHz (= 1us) for 4MHz system clock.

Oscillator

(1) Crystal oscillator: 32.768KHz - 4MHz.

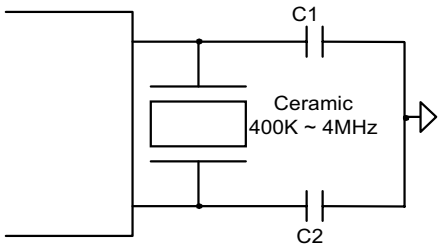


C1, C2 Setting :

Crystal 32.768KHz :
C1, C2 < 56p (V_{DD} = 5V);
C1, C2 < 56p (V_{DD} = 3V).

Crystal 4MHz :
C1, C2 < 33p (V_{DD} = 5V);
C1, C2 < 10p (V_{DD} = 3V).

(2) Ceramic resonator: 400KHz - 4MHz.

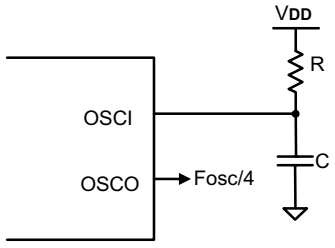


C1, C2 Setting :

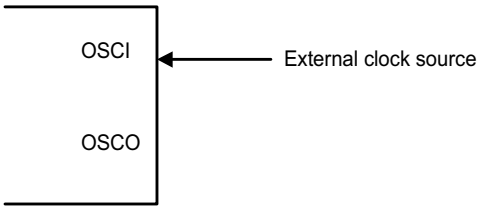
Ceramic 400KHz :
20p < C1, C2 < 470p (V_{DD} = 5V);
20p < C1, C2 < 150p (V_{DD} = 3V).

Ceramic 4MHz :
20p < C1, C2 < 100p (V_{DD} = 5V);
C1, C2 < 10p (V_{DD} = 3V).

(3) RC oscillator: 400KHz - 4MHz.



(4) External input clock: 30KHz - 4MHz.



Initial State

Hardware	After power on reset
Program counter	$000
CY	Undefined
Data memory	Undefined
System register	Undefined
AC	Undefined
Timer counter	0
Timer load register	0
WDT counter	0
WDT prescaler	0
I/O Ports	Input
T0S T0E	00
WDT	0
LPD	1010

Instruction Set

All instructions are one cycle and one word instructions. The characteristics is memory-oriented operation.
Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC + 1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC [3]; AC [0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM mnemonic is EORI. However, EORI has the same operation identical with EORIM. Same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC; Mx ← Decimal adjustment for add.	CY
DAS X	11001 1010 xxx xxxx	AC; Mx ← Decimal adjustment for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC + 1 PC ← X (Not including p)	
RTNW H; L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY; PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank = 000
p	ROM page = 0		
ST	Stack	TBR	Table Branch Register

.

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to + 7.0V

Input/Output Voltage . . . . . .GND -0.2V to V_{DD} + 0.2V

Operating Ambient Temperature . . . . . -40℃ to + 85℃

Storage Temperature . . . . . -55℃ to + 125℃

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

***Comments**

DC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, TA = 25℃, FOSC = 4MHz [Crystal], unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	3.3	5.0	6.0	V	LPD disabled
Low Power Detection Voltage	V_{LPD}	3.4	3.9	4.4	V	
Operating Current	I_{OP}	-	1.3	1.5	mA	All output pins unloaded (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	150	300	μA	All output pins unload, WDT off LPD off (If WDT on, I_{SB1} = I_{SB1} + 20μA)
Stand by Current (HALT) OSC = 32768Hz Crystal	I_{SB32k}	-	7	10	μA	All output pins unload, WDT off LPD off (If WDT on, I_{SB32k} = I_{SB1} + 20μA)
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unloaded, LPD off, WDT off (If WDT on, I_{SB2} = I_{SB2} + 20μA)
Input Low Voltage	V_{IL1}	GND	-	0.2 X V_{DD}	V	I/O Ports, pins tri-state
Input Low Voltage	V_{IL2}	GND	-	0.15 X V_{DD}	V	$\overline{RESET}$, T0 ,OSCI (Driven by external Clock)
Input High Voltage	V_{IH1}	0.8 X V_{DD}	-	V_{DD}	V	I/O Ports, pins tri-state
Input High Voltage	V_{IH2}	0.85 X V_{DD}	-	V_{DD}	V	$\overline{RESET}$, T0 ,OSCI (Driven by external Clock)
Input Leakage Current	I_{IL1}	-1	-	1	μA	I/O Ports, GND < $V_{I/O}$ < V_{DD}
Input Leakage Current	I_{IL2}	-5	-	-	μA	$V_{\overline{RESET}}$ = GND + 0.25V
Input Leakage Current	I_{IL3}	-	1	5	μA	$V_{\overline{RESET}}$ = V_{DD}
Input Leakage Current	I_{IL4}	-3	1	3	μA	T0, GND < V_{T0} < V_{DD}
Pull-up/ Pull-low Resistor	R_P	-	150	-	KΩ	PULL-UP/ PULL-LOW resistor
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, I_{OH} = -10mA OSCO, I_{OH} = -0.7mA
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O Ports, I_{OL} = 20mA OSCO, I_{OL} = 1.6mA

Notes:

Negative current is defined as the flowing out of the pin.
Max. current into V_{DD} = 50mA.
Max. current out of V_{SS} = 150mA.
Max. output current sunk by any I/O pin = 25mA.
Max. output current sourced by any I/O pin = 20mA.
Max. output current sunk by any I/O port = 50mA.
Max. output current sourced by any I/O port = 40mA.

AC Electrical Characteristics (V_{DD} = 5.0V GND = 0V, T_A = 25℃, unless otherwise specified.)

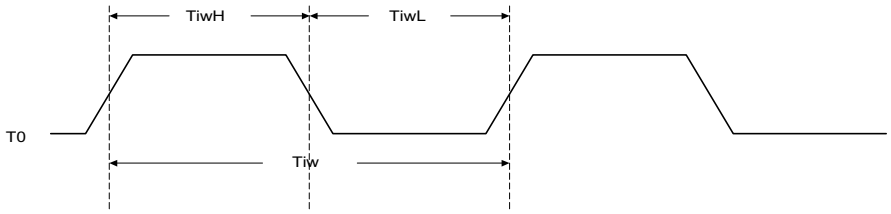
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start Time	T_{OSC1}			2	s	X'tal osc = 32.768KHz
RESET pulse width (low)	T_{RESET}	1			μs	V_{DD}=5V
WDT Period	T_{WDT}	7		15	ms	V_{DD}=5V
Frequency Stability (RC)	Δ F/F			20	%	RC oscillator: [F(5.0) - F(4.5)]/F(5.0)

AC Characteristics

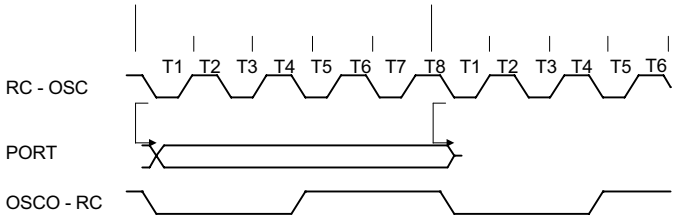
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CY}	Instruction cycle time	1		122	μs	
T_{IW}	T0 input width	(T_{CY} + 40)/N			ns	N = Prescaler divide ratio
T_{IWH}	High pulse width	1/2 t_{IW}			ns	
T_{IWL}	LOW pulse width	1/2 t_{IW}			ns	

Timing Waveform

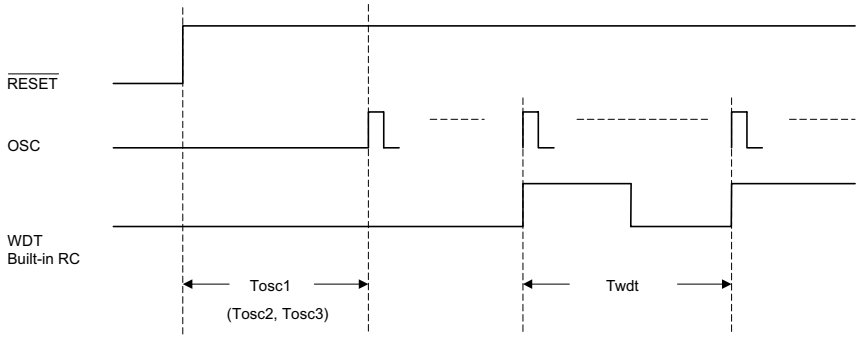
T0 Input Waveform



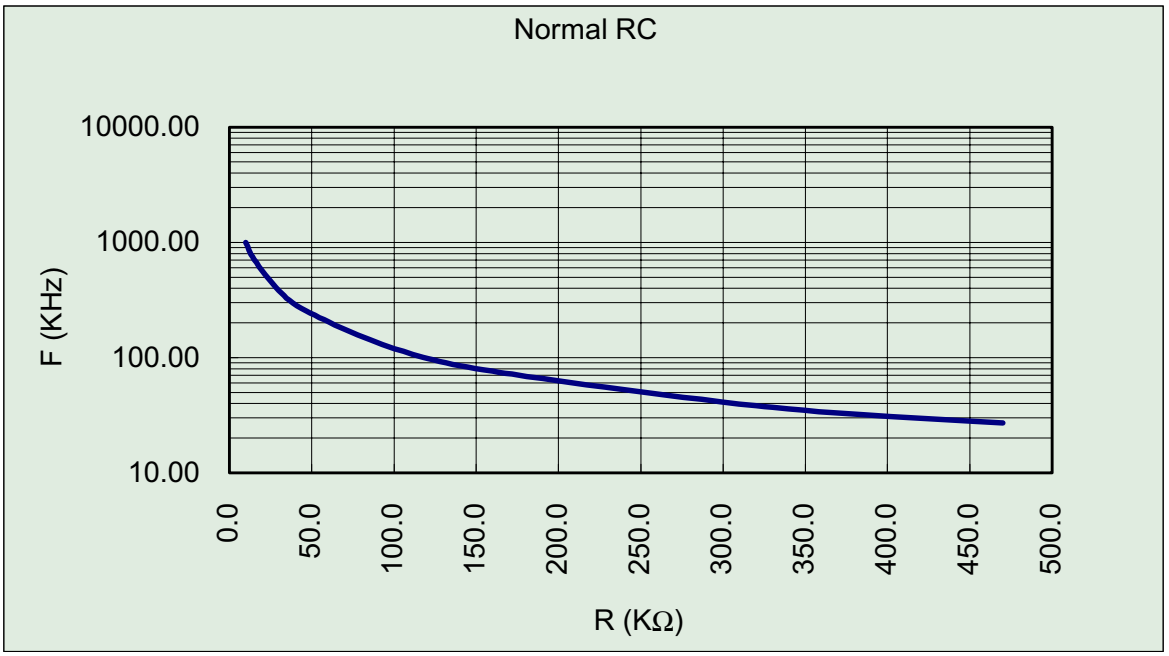
RC OSCO Timing Waveform

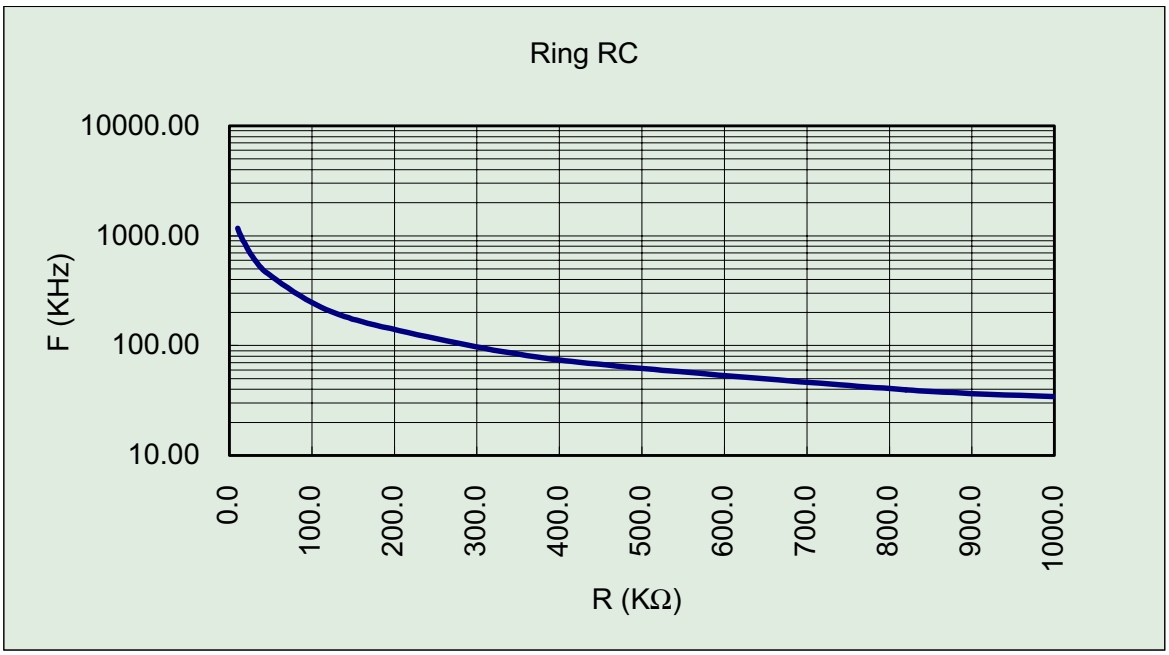


Built-in RC Oscillator (Only use for Watch Dog)



Typical RC oscillator Resistor vs. Frequency: (V_{DD} = 5V, for reference only)

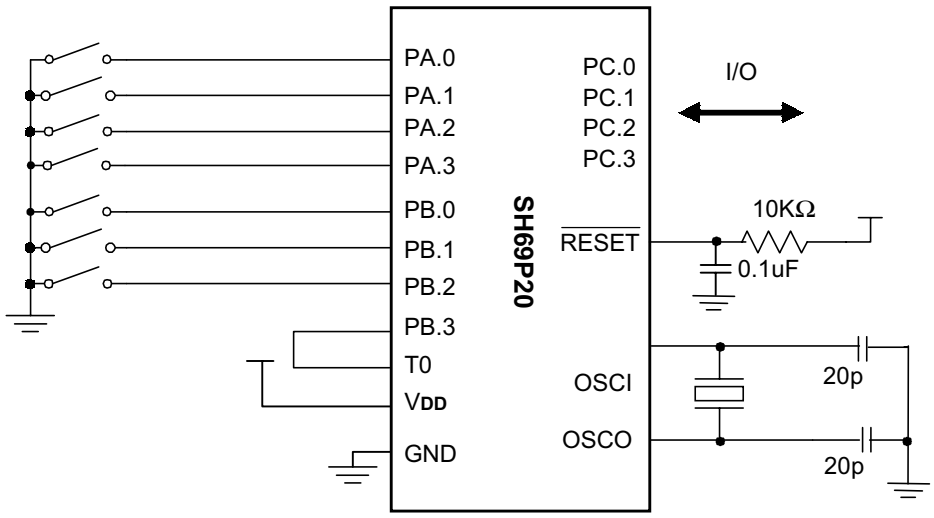




Application Circuits (for reference only)

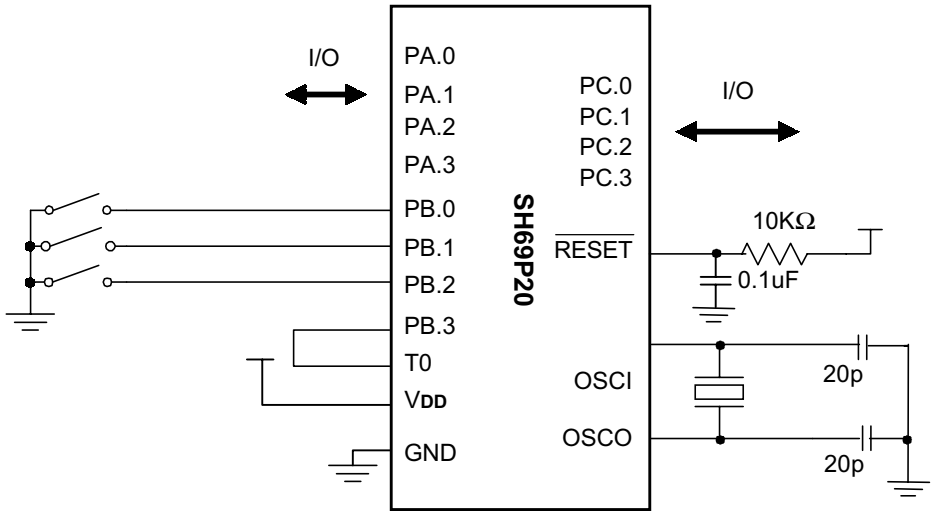
AP1:

a. Operating voltage: 3.0V.
b. Oscillator: Crystal 32.768KHz.
c. PORTA - C: I/O. (PULL UP ON)



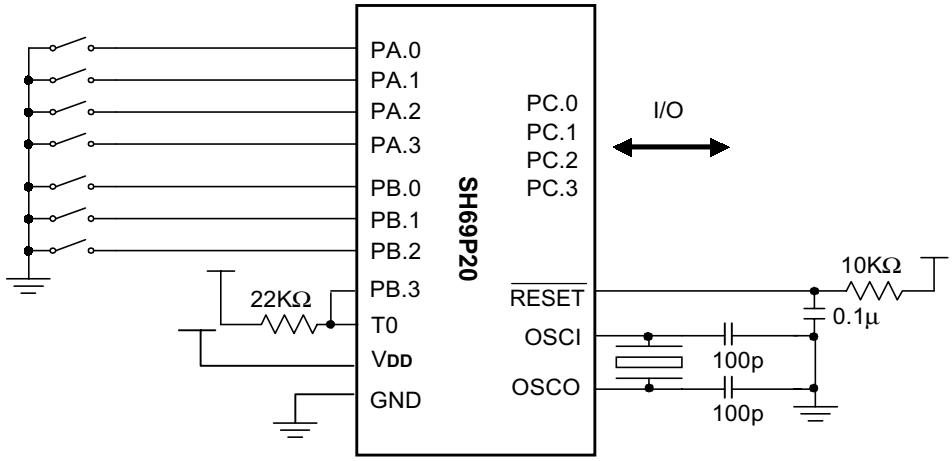
AP2:

a. Operating voltage: 5.0V.
b. Oscillator: Crystal 4MHz.
c. PORTA - C: I/O. (PULL UP ON)



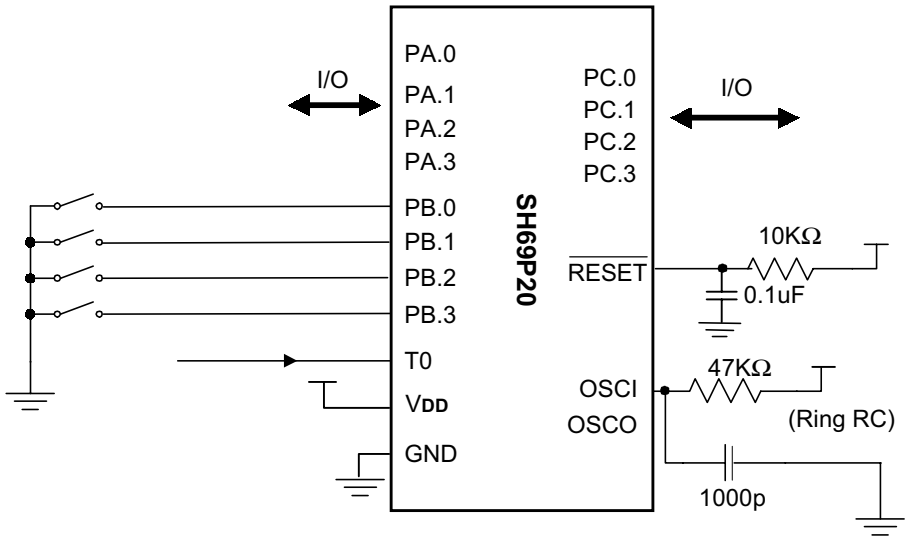
AP3:

a. Operating voltage: 5.0V.
b. Oscillator: Ceramic 400KHz.
c. PORTA - C: I/O. (PULL UP ON)

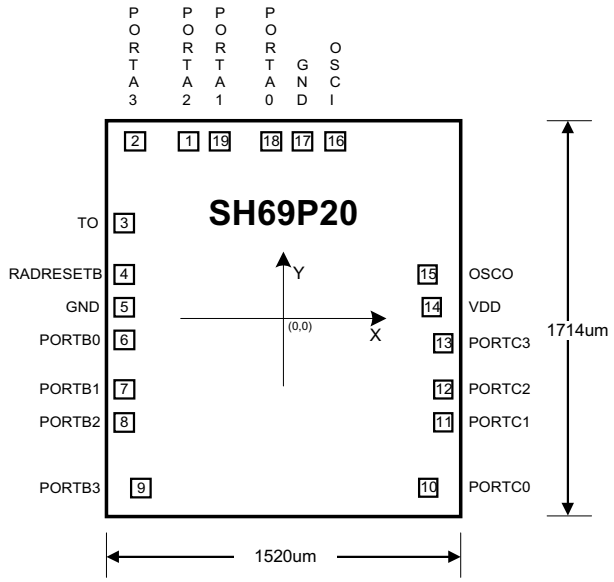


AP4:

a. Operating voltage: 5.0V.
b. Oscillator: RC 450KHz.(Ring RC)
c. PORTA – C: I/O. (PULL UP ON)
d. Timer0 input: T0.



Bonding Diagram



Pad Location **unit : μm**

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTA[2]	-415.75	786.3	11	PORTC[1]	690	-465.15
2	PORTA[3]	-648.85	786.3	12	PORTC[2]	690	-330.05
3	T0	-686.65	470.75	13	PORTC[3]	690	-99.25
4	PADRESETB	-684.65	225.45	14	VDD	641	72.75
5	GND	-690	66.9	15	OSCO	626.55	207.85
6	PORTB[0]	-690	-84.5	16	OSCI	250	786.3
7	PORTB[1]	-690	-317.9	17	GND	108.75	786.3
8	PORTB[2]	-690	-465.15	18	PORTA[0]	-45.65	786.3
9	PORTB[3]	-607.3	-728.7	19	PORTA[1]	-278.45	786.3
10	PORTC[0]	607.3	-728.7				

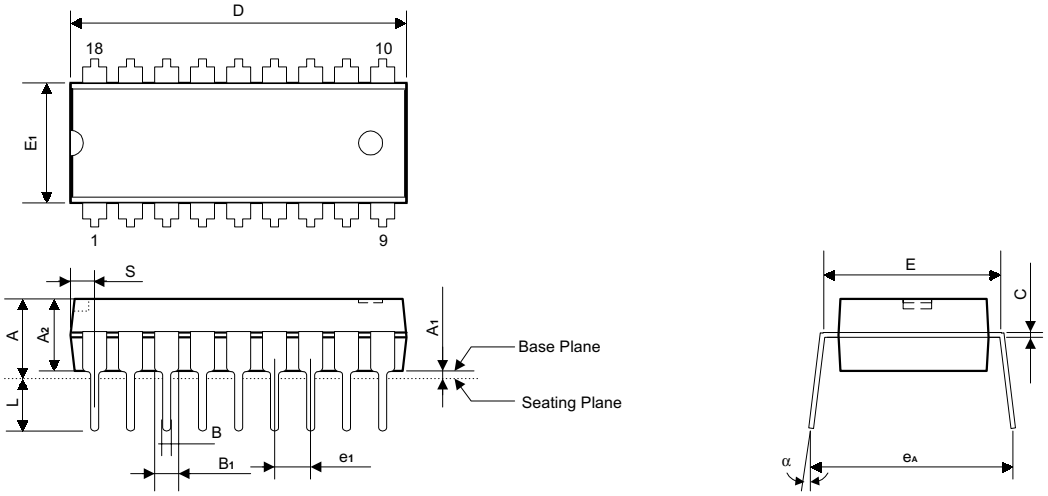
note: The all GND pins must be connected together outside the chip.

Ordering Informations

Part No.	Packages
SH69P20	18L DIP
SH69P20	18L SOP

Package Informations

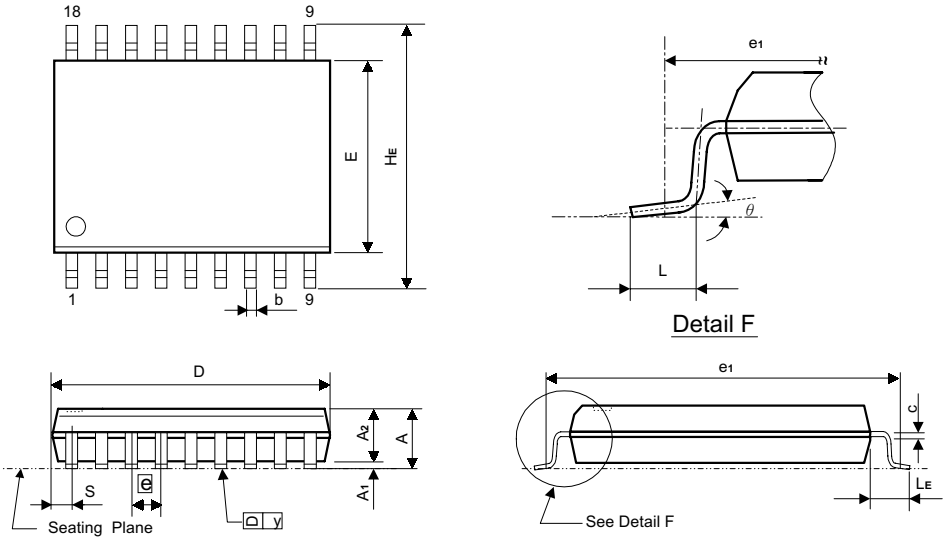
DIP 18L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimension in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.900 Typ. (0.920 Max.)	22.86 Typ. (23.37 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° ~ 15°	0° ~ 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.055 Max.	1.40 Max.

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP 18L (W.B.) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.110 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.455 ± 0.015	11.56 ± 0.38
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.030 ± 0.008	0.76 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.037 Max.	0.94 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Product Spec. Change Notice

SH69P20 Specification Revision History		
Version	**Content**	**Date**
0.1	Original	Aug.2002