SINO WEALTH

SH69P48

Preliminary

OTP 4-bit Microcontroller with SAR 10-bit A/D Converter

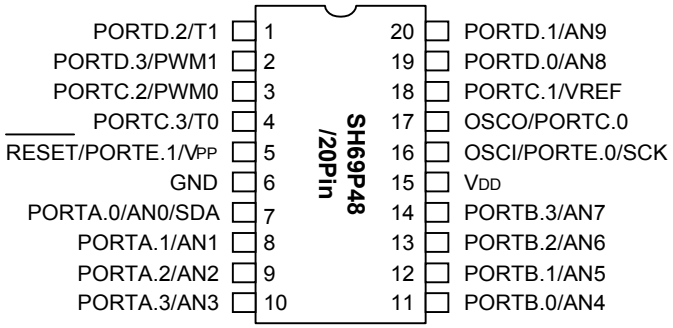
Features

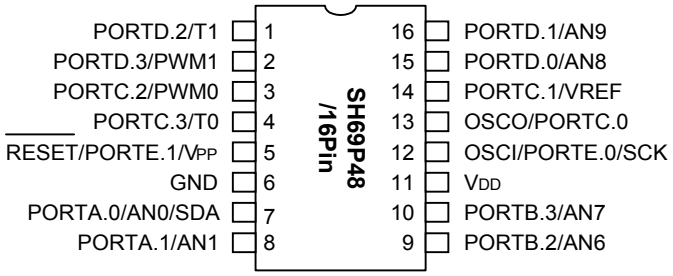
- SH6610D-based single-chip 4-bit microcontroller with 10-bit SAR A/D converter
- OTP ROM: 4K X 16 bits
- RAM: 253 X 4 bits
  - System register: 61 X 4 bits
  - Data memory: 192 X 4 bits
- Operation voltage:
  - f_{OSC}=30kHz - 4MHz, V_{DD}=2.4V - 5.5V
  - f_{OSC}=4MHz - 10MHz, V_{DD}=4.5V - 5.5V
- 17 CMOS bi-directional I/O pins (exclude 1 output only pin)
- Built in pull-up for I/O port
- Two 8-bit auto re-load timer/counter, One can switch to external clock source
- Read Rom Table function
- 8-level subroutine nesting (including interrupts)
- Powerful interrupt sources:
  - A/D interrupt
  - Internal interrupt (Timer1, Timer0)
  - External interrupts: Port B/D (Falling edge)
- Oscillator: (OTP option)
  - Crystal oscillator: 32768Hz, 400kHz ~ 10MHz
  - Ceramic resonator: 400k ~ 10MHz
  - External R_{OSC} RC oscillator: 400k ~ 10MHz
  - Internal R_{OSC} RC oscillator: 4MHz
  - External clock: 30k ~ 10MHz
- Instruction cycle time:
  - 4/32.768kHz (≈122μs) for 32.768kHz
  - 4/10MHz (= 0.4μs) for 10MHz at V_{DD}=5.0V
- 10 channels 10-bit resolution A/D converter
- 2 channels 8+2bit PWM output
- Warm-up timer for power on reset
- Low voltage reset function (LVR)
- Internal reliable reset circuit
- Built-in watchdog timer
- Two low power operation modes: HALT and STOP
- OTP type/Code protection
- 20-pin DIP/SOP package

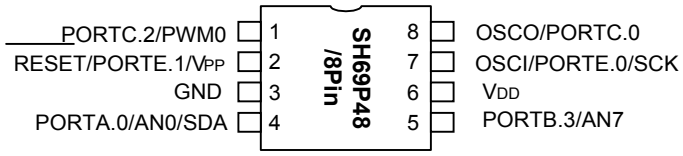
General Description

The SH69P48 is an advanced CMOS 4-bit microcontroller. It provide the following standard features: 4K words of OTP ROM, 253 nibbles of RAM, 8-bit timer/counter, 10-bit A/D converter, 8+2bit high speed PWM output, on-chip oscillator clock circuitry, on-chip watchdog timer, low voltage reset function and support power saving modes to reduce power consumption.

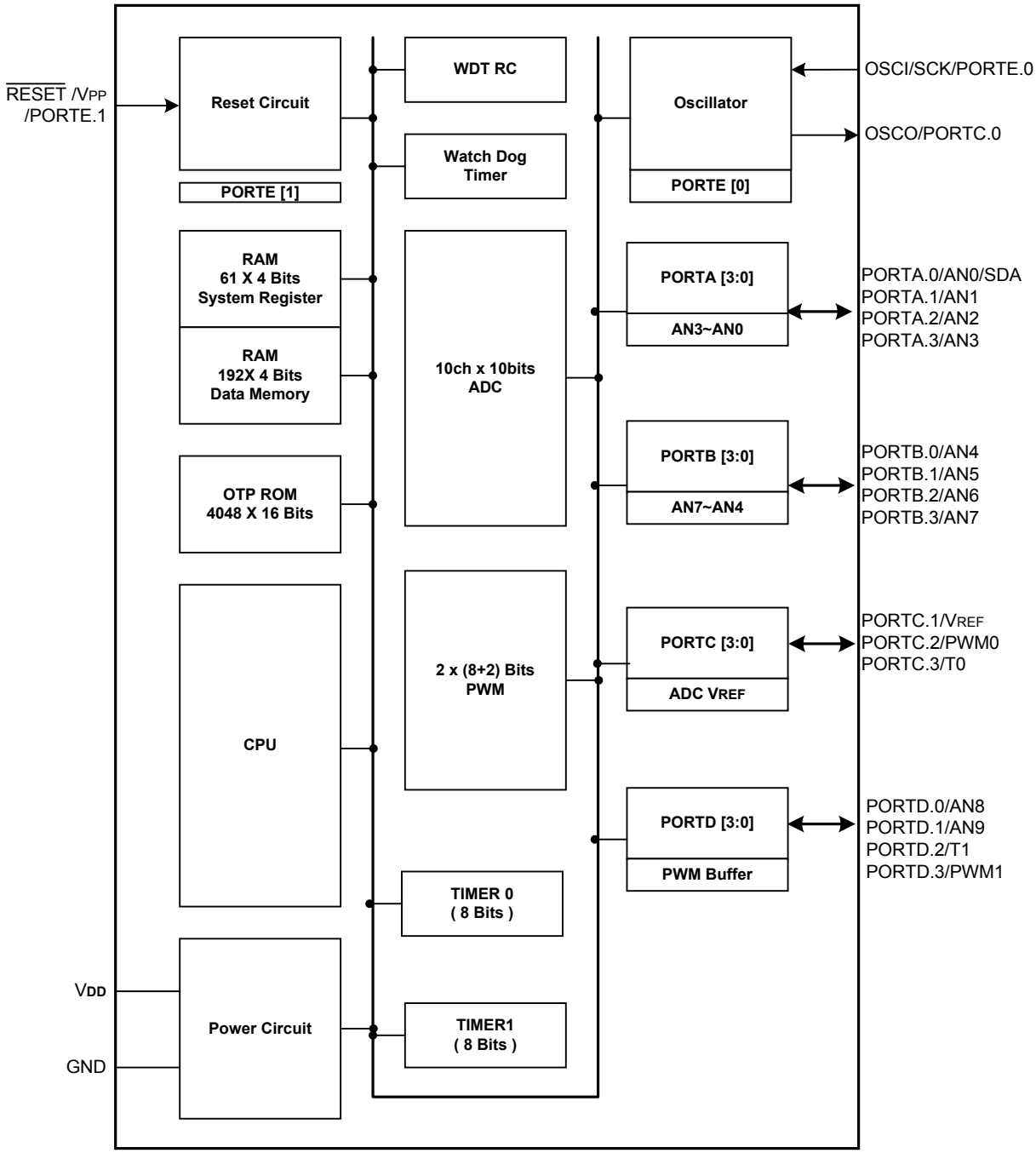
Pin Configuration







Block Diagram



Pin Descriptions:

1. SH69P48/20pin

Pin No.	Designation	I/O	Description
1	PORTD.2 /T1	I/O I I	Bit programmable Bi-directional I/O port Shared with Timer1 Input Capture Vector port interrupt. (falling edge active)
2	PORTD.3 /PWM1	I/O O I	Bit programmable Bi-directional I/O port Shared with PWM1 output Vector port interrupt. (falling edge active)
3	PORTC.2 /PWM0	I/O O	Bit programmable Bi-directional I/O port Shared with PWM0 output
4	PORTC.3 /T0	I/O I	Bit programmable Bi-directional I/O port Shared with Timer0 external clock input
5	$\overline{\text{RESET}}$ /PORTE.1	I O	Reset pin input, (low active) Output only (open drain type) (selected by code option)
6	GND	P	Ground pin
7,8,9,10	PORTA.0 ~ 3 /AN0 ~ 3	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN0 ~ AN3
11,12,13,14	PORTB.0 ~ 3 /AN4 ~ 7	I/O I I	Bit programmable bi-directional I/O port Shared with ADC input channel AN4 ~ AN7 Vector port interrupt. (falling edge active)
15	V_{DD}	P	Power supply pin
16	OSCI /PORTE.0	I I/O	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator. Shared with bi-directional I/O port in the internal RC code option
17	OSCO /PORTC.0	O I/O	Oscillator output pin, connect to crystal/ceramic oscillator. Shared with bi-directional I/O port in the RC oscillator code option
18	PORTC.1 /V_{REF}	I/O I	Bit programmable Bi-directional I/O port Shared with external ADC V_{REF} input
19	PORTD.0 /AN8	I/O I I	Bit programmable Bi-directional I/O port Shared with ADC input channel AN8 Vector port interrupt. (falling edge active)
20	PORTD.1 /AN9	I/O I	Bit programmable Bi-directional I/O port Shared with ADC input channel AN9 Vector port interrupt. (falling edge active)

Total 20 pins

OTP Programming Pin Description (OTP program mode)

Pin No.	Symbol	I/O	Shared by	Description
15	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
5	VPP	P	$\overline{\text{RESET}}$ /PORTE.1	Programming high voltage Power supply (+11V)
6	GND	P	GND	Ground
16	SCK	I	OSCI /PORTE.0	Programming Clock input pin
7	SDA	I/O	PORTA.0 AN0	Programming Data pin

2. SH69P48/16pin

Pin No.	Designation	I/O	Description
1	PORTD.2 /T1	I/O I I	Bit programmable Bi-directional I/O port Shared with Timer1 Input Capture Vector port interrupt. (falling edge active)
2	PORTD.3 /PWM1	I/O O I	Bit programmable Bi-directional I/O port Shared with PWM1 output Vector port interrupt. (falling edge active)
3	PORTC.2 /PWM0	I/O O	Bit programmable Bi-directional I/O port Shared with PWM0 output
4	PORTC.3 /T0	I/O I	Bit programmable Bi-directional I/O port Shared with Timer0 external clock input
5	$\overline{\text{RESET}}$ /PORTE.1	I O	Reset pin input, (low active) Output only (open drain type) (selected by code option)
6	GND	P	Ground pin
7,8	PORTA.0 ~ 1 /AN0 ~ 1	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN0 ~ AN1
9,10	PORTB.2 ~ 3 /AN6 ~ 7	I/O I I	Bit programmable bi-directional I/O port Shared with ADC input channel AN6 ~ AN7 Vector port interrupt. (falling edge active)
11	V_{DD}	P	Power supply pin
12	OSCI /PORTE.0	I I/O	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator. Shared with bi-directional I/O port in the internal RC code option
13	OSCO /PORTC.0	O I/O	Oscillator output pin, connect to crystal/ceramic oscillator. Shared with bi-directional I/O port in the RC oscillator code option
14	PORTC.1 /V_{REF}	I/O I	Bit programmable Bi-directional I/O port Shared with external ADC V_{REF} input

15	PORTD.0 /AN8	I/O I I	Bit programmable Bi-directional I/O port Shared with ADC input channel AN8 Vector port interrupt. (falling edge active)
16	PORTD.1 /AN9	I/O I	Bit programmable Bi-directional I/O port Shared with ADC input channel AN9 Vector port interrupt. (falling edge active)

Total 20 pins

OTP Programming Pin Description (OTP program mode)

Pin No.	Symbol	I/O	Shared by	Description
11	VDD	P	VDD	Programming Power supply (+5.5V)
5	VPP	P	$\overline{\text{RESET}}$ /PORTE.1	Programming high voltage Power supply (+11V)
6	GND	P	GND	Ground
12	SCK	I	OSCI /PORTE.0	Programming Clock input pin
7	SDA	I/O	PORTA.0 AN0	Programming Data pin

2. SH69P48/8Pin

Pin No.	Designation	I/O	Description
1	PORTC.2 /PWM0	I/O O	Bit programmable Bi-directional I/O port Shared with PWM0 output
2	$\overline{\text{RESET}}$ /PORTE.1	I O	Reset pin input, (low active) Output only (open drain type) (selected by code option)
3	GND	P	Ground pin
4	PORTA.0 /AN0	I/O I	Bit programmable bi-directional I/O port Shared with ADC input channel AN0
5	PORTB.3 /AN7	I/O I I	Bit programmable bi-directional I/O port Shared with ADC input channel AN7 Vector port interrupt. (falling edge active)
6	VDD	P	Power supply pin
7	OSCI /PORTE.0	I I/O	Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator. Shared with bi-directional I/O port in the internal RC code option
8	OSCO /PORTC.0	O I/O I	Oscillator output pin, connect to crystal/ceramic oscillator. Shared with bi-directional I/O port in the RC oscillator code option Vector port interrupt. (falling edge active)

Total 8 pins

OTP Programming Pin Description (OTP program mode)

Pin No.	Symbol	I/O	Shared by	Description
6	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
2	VPP	P	$\overline{\text{RESET}}$ /PORTE.1	Programming high voltage Power supply (+11V)
3	GND	P	GND	Ground
7	SCK	I	OSCI /PORTE.0	Programming Clock input pin
4	SDA	I/O	PORTA.0 AN0	Programming Data pin

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

(a) PC

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0). The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter cans only 4K program ROM address. (Refer to the ROM description).

(b) ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

(c) Accumulator

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

(d) Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

(e) Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

(f) Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:
The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. ROM

The SH69P48 can address 4096 X 16 bits of program area from $0000 to $0FFF. The Program Counter can only address a 4K program ROM. To address 4K size program ROM, use the bank switch.

(a) Vector Address Area ($0000 to $0004)

The program is sequentially executed. There is an area address $0000 through $0004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	JMP instruction	Jump to ADC interrupt service routine
002H	JMP instruction	Jump to TIMER0 interrupt service routine
003H	JMP instruction	Jump to TIMER1 interrupt service routine
004H	JMP instruction	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

(b) Table Data Reference

Table Data can be stored in the program memory and can be referenced by using the Table Branch (TJMP) and the Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) are placed by an offset address in the program ROM. The TJMP instruction branch is placed into address ((PC11 - PC8) X (28) + (TBR, A)). The address is determined by RTNW to return the look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

3. RAM

Built-in RAM contains of general-purpose data memory and system register.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

$000 - $02F, $380 ~ $38C: System register and I/O

$030 - $0EF: Data memory (192 X 4 bits)

(b) Data Memory

Data memory is organized as 192X 4 bits ($030 - $0EF). Because of its static nature, the RAM can keep data after the CPU enters the STOP or the HALT.

(c) Configuration of System Register:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQAD	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 pre-scaler select Bit3: T0 signal source
$03	T1E	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 pre-scaler select Bit3: T1 external signal edge select
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load / counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load / counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load / counter register (low nibble)
$07	T1H.3	T1H.2	T1H.2	T1H.0	R/W	Timer1 load / counter register (high nibble)
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE(PE.1 output only)
$0D	-	-	-	-	-	Reserved
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	T1GO	DEC	-	TM1S0	R/W	Bit0: Set Timer1 mode Bit2: Select directive edge active enable Bit3: Set Timer1 function start
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
$15	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set A/D Conversion Time Bit2, Bit1: Select A/D Clock Period Bit3: ADC status flag
$16	ACR3	ACR2	ACR1	ACR0	R/W	Bit3-0: A/D port configuration control
$17	CH3	CH2	CH1	CH0	R/W	Bit3-0: Select ADC channel
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	-	-	-	PECR.0	R/W	PORTE input/output control
$1D	-	-	-	-	-	Reserved
$1E	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watch dog timer control Bit3: Watchdog timer overflow flag (Read only)
$1F	-	-	-	-	-	Reserved
$20	PWM0S	T0CK1	T0CK0	PWM0_EN	R/W	Bit0: Set PWM0 Enable Bit2, Bit1: Select PWM0 clock Bit3: Set PWM0 output mode of duty cycle

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PWM1S	T1CK1	T1CK0	PWM1_EN	R/W	Bit0: Set PWM1 Enable Bit2, Bit1: Select PWM1 clock Bit3: Set PWM1 output mode of duty cycle
$22	PP0.3	PP0.2	PP0.1	PP0.0	R/W	PWM0 period low nibble
$23	PP0.7	PP0.6	PP0.5	PP0.4	R/W	PWM0 period high nibble
$24	-	-	PDF0.1	PDF0.0	R/W	PWM0 duty fine tune nibble
$25	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble
$26	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty high nibble
$27	PP1.3	PP1.2	PP1.1	PP1.0	R/W	PWM1 period low nibble
$28	PP1.7	PP1.6	PP1.5	PP1.4	R/W	PWM1 period high nibble
$29	-	-	PDF1.1	PDF1.0	R/W	PWM1 duty fine tune nibble
$2A	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble
$2B	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty high nibble
$2C	-	-	-	-	-	Reserved
$2D	-	-	A1	A0	R	ADC data low nibble (Read only)
$2E	A5	A4	A3	A2	R	ADC data medium nibble (Read only)
$2F	A9	A8	A7	A6	R	ADC data high nibble (Read only)
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address / data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address / data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address / data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address / data register
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable flags
$385	PDIF.3	PDIF.2	PDIF.1	PDIF.0	R/W	PORTD interrupt request flags
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags
$387	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags
$388	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull-up control
$389	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull-up control
$38A	PPCCR.3	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull-up control
$38B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull-up control
$38C	-	-	-	PPECR.0	R/W	PORTE pull-up control

4. Initial state

(a) System Register state:

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$00	IEAD	IET0	IET1	IEP	0000	0000
$01	IRQAD	IRQT0	IRQT1	IRQP	0000	0000
$02	T0S	T0M.2	T0M.1	T0M.0	0000	uuuu
$03	T1E	T1M.2	T1M.1	T1M.0	0000	uuuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	-	-	PE.1	PE.0	--10	--10
$0D	-	-	-	-	----	----
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	T1GO	DEC	-	TM1S0	00-0	0u-u
$14	VREFS	-	-	ADCON	0--0	u--0
$15	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	0000	0uuu
$16	ACR3	ACR2	ACR1	ACR0	0000	uuuu
$17	CH3	CH2	CH1	CH0	0000	uuuu
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	-	-	-	PECR.0	---0	---0
$1D	-	-	-	-	----	----
$1E	WD	WDT.2	WDT.1	WDT.0	0000	1000
$1F	-	-	-	-	----	----
$20	PWM0S	T0CK1	T0CK0	PWM0_EN	0000	uuu0
$21	PWM1S	T1CK1	T1CK0	PWM1_EN	0000	uuu0
$22	PP0.3	PP0.2	PP0.1	PP0.0	xxxx	uuuu

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset / Low Voltage Reset	WDT Reset
$23	PP0.7	PP0.6	PP0.5	PP0.4	xxxx	uuuu
$24	-	-	PDF0.1	PDF0.0	--xx	--uu
$25	PD0.3	PD0.2	PD0.1	PD0.0	xxxx	uuuu
$26	PD0.7	PD0.6	PD0.5	PD0.4	xxxx	uuuu
$27	PP1.3	PP1.2	PP1.1	PP1.0	xxxx	uuuu
$28	PP1.7	PP1.6	PP1.5	PP1.4	xxxx	uuuu
$29	-	-	PDF1.1	PDF1.0	--xx	--uu
$2A	PD1.3	PD1.2	PD1.1	PD1.0	xxxx	uuuu
$2B	PD1.7	PD1.6	PD1.5	PD1.4	xxxx	uuuu
$2C	-	-	-	-	----	----
$2D	-	-	A1	A0	xxxx	uuuu
$2E	A5	A4	A3	A2	xxxx	uuuu
$2F	A9	A8	A7	A6	xxxx	uuuu
$380	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$381	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$382	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$383	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	0000	0000
$385	PDIF.3	PDIF.2	PDIF.1	PDIF.0	0000	0000
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	0000	0000
$387	PBIF.3	PBIF.2	PBIF.1	PBIF.0	0000	0000
$388	PPACR.3	PPACR.2	PPACR.1	PPACR.0	0000	0000
$389	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	0000	0000
$38A	PPCCR.3	PPCCR.2	PPCCR.1	PPCCR.0	0000	0000
$38B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	0000	0000
$38C	-	-	-	PPECR.0	---0	---0

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

(d) Others initial state:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

SH69P48 has one clock source. Oscillator is determined by OTP options. The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock = $F_{OSC}/4$.

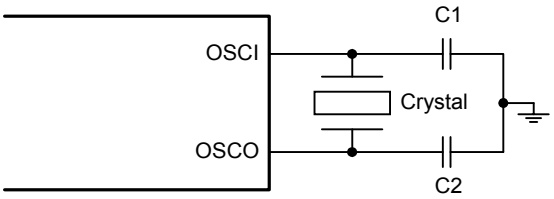
(a) Instruction cycle time:

(1) 4/32768Hz (≈122.1μs) for 32768Hz oscillator.

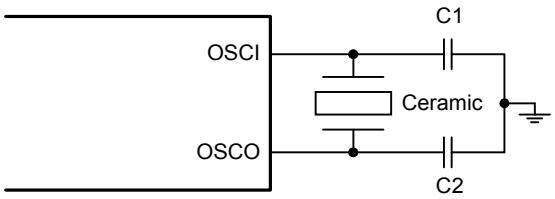
(2) 4/10MHz (=0.4μs) for 10MHz oscillator.

(b) Oscillator type

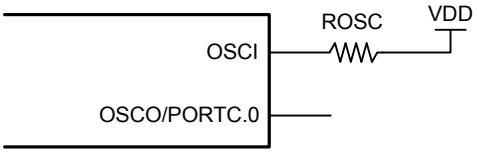
(1) Crystal oscillator: 32768Hz or 400KHz ~ 10MHz



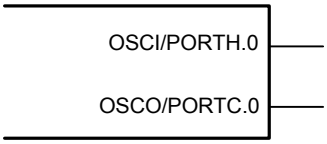
(2)Ceramic resonator: 400KHz ~ 10MHz



(3)RC oscillator: 400KHz - 10MHz

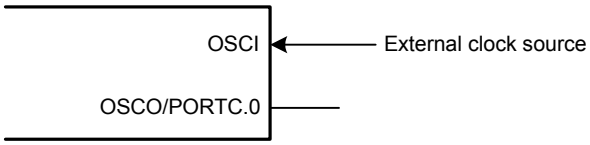


External R_{OSC} RC



Internal R_{OSC} RC (F_{OSC}= 4MHz)

(4)External input clock: 30KHz ~ 10MHz



Note:

- If the RC oscillator or the external input clock is selected, OSCO pin is used as the I/O port (PORTC.0).
- If the internal RC oscillator is selected, OSCO pin is used as the I/O port (PORTC.0) as well as OSCI pin is used as the PORTE.0.

6. I/O Port

The SH69P48 provides 17 programmable bi-directional I/O ports and one port for output only. Each I/O port contains pull-up MOS controllable by the program. Each pull-up MOS is controlled by the value of the corresponding bit in the port pull-up control register (PPCR), independently. When the port is selected as an input port (Write 1 to the relevant bit in the port pull-up control register (PPCR) could turn on the pull-up MOS and write 0 could turn off the pull-up MOS). So the pull-up MOS can be turned on and off individually. But when the port is selected as output port, the pull-up MOS must be turned off automatically, regardless the value of the corresponding bit in the port pull-up control register (PPCR). When PORTC/F are selected as the digital input direction, they can activate port interrupt by falling edge (if port interrupt is enabled).

PORTA.0~3 can be shared with ADC input channel (AN0~3).
PORTB.0~3 can be shared with ADC input channel (AN4~7).
PORTD.0~1 can be shared with ADC AN8~9 input channel (AN8~9).

A/D Converter Enable Register $14:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
	X	-	-	0	R/W	Disable the A/D converter module. (Default)
	X	-	-	1	R/W	Enable the A/D converter module.

When A/D converter is disabled, PORTA.0~3, PORTB.0~3 and PORTD.0~1are used as normal I/O port. When A/D converter is enabled, set A/D port configuration register($14) to select anyone of PORTA.0~3, PORTB.0~3 and PORTD.0~1as normal I/O port or A/D port. For detail, refer to A/D converter description.

PORTC.1 can be shared with the reference voltage input (VREF).

A/D Port Configuration Control Register $14:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
	0	-	-	X	R/W	Set PC1 as normal I/O port (Default)
	1	-	-	X	R/W	Set PC1 as the external reference voltage input

PORTC.2 can be shared with the PWM0 output (PWM0).

PWM0 Control Register $20:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWM0S	T0CK1	T0CK0	PWM0_EN	R/W	Bit0: Set PWM0 output enable Bit2, Bit1: Select PWM0 clock Bit3: Set PWM0 output mode of duty cycle
	X	X	X	0	R/W	Set PC2 as normal I/O port and disable PWM0 (Default)
	X	X	X	1	R/W	Set PC2 as PWM0 output and enable PWM0

PORTC.3 can be shared with the Timer0 external input (T0).

Timer0 pre-scaler select Register $02:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 pre-scaler select Bit3: T0 signal source
	0	X	X	X	R/W	Set PC3 as normal I/O port (Default)
	1	X	X	X	R/W	Set PC3 as T0 input (falling edge active)

PORTD.2 can be shared with the Timer1 input capture. (IC1)

Timer1 Control Register $13:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T1GO	DEC	-	TM1S0	R/W	Bit1-0: Timer1 mode select
	X	X	-	0	R/W	Set PD2 as normal I/O port (Default)
	X	X	-	1	R/W	Set PD2 as T1 input

PORTD.3 can be shared with the PWM1 output (PWM1).

PWM1 Control Register $21:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PWM1S	T1CK1	T1CK0	PWM1_EN	R/W	Bit0: Set PWM1 output enable Bit2, Bit1: Select PWM1 clock Bit3: Set PWM1 output mode of duty cycle
	X	X	X	0	R/W	Set PD3 as normal I/O port and disable PWM1 (Default)
	X	X	X	1	R/W	Set PD3 as PWM1 output and enable PWM1

The RESET pin can be shared with PORTE.1 for open drain output. (Refer to the OTP option (OP_RST).)

The OSCO pin can be shared with PORTC.0. When SH69P48 oscillating source is selected as the External clock or the RC oscillator, this pin is used as PORTC.0. (Refer to the OTP option (OP_OSC[2:0]).)

The OSCI pin can be shared with PORTE.0. When SH69P48 oscillating source is selected as the internal RC oscillator, this pin is used as PORTE.0. (Refer to the OTP option (OP_OSC[2:0]).)
In SH69P48, each output port contains a latch, which can hold the output data. Writing the port data register (PDR) under the output mode can directly transfers data to the corresponding pad. All input ports do not have latches, so the external input data should be held externally until the input data is read from outside or reading the port data register (PDR) under the input mode should be performed several times before the available processing. The contents of the port control register (PCR) determine each bi-directional I/O port to be either an input or output, where writing 0 to PCR registers represents the input mode and 1 for the output mode. When a digital I/O port is selected to be an output, the reading of the associated port bit actually represents the value of the output data latch, not the voltage on the pad. When a digital I/O port is selected to be an input, the reading of the associated port bit represents the status on the corresponding pad. The output data latch can always be written, regardless of the state of the port control register (PCR). Therefore, when using ports in a mixture of input and output modes, the contents of the output latches for those ports that are selected as inputs may be rewritten by execution of logical instructions. So it is strongly recommended that writing proper data to the port data register (PDR) before changing the corresponding bits in the port control register (PCR) from the input mode to the output mode can avoid glitches on the relevant pads.

As PORTC.1 can be shared with the pin RESET input controlled by the OTP option, it can only act as output port with open drain structure. So the value of reading from the PORTE.1 bit in the port data register (PDR) ($0C) is always fetched from the output latch.

Port Data Register (PDR): $08 ~ $0C

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE (PE.1 output only)

When the chip pin reset is selected as disable, (Refer to the OTP option), the RESET pin is used as the PORTE.1.

Port Control Register (PCR): $18 ~ $1C

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	-	-	-	PECR.0	R/W	PORTE input/output control

I/O control register:

PA(/B/C/D/E)CR.n, (n = 0, 1, 2, 3)

0: Set I/O as an input direction. (Default)

1: Set I/O as an output direction.

Port Pull-up Control Register (PPCR): $38D ~ $391

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$388	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull-up control
$389	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull-up control
$38A	PPCCR.3	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull-up control
$38B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull-up control
$38C	-	-	-	PPECR.0	R/W	PORTE pull-up control

0: Disable internal pull-up MOS. (Default)

1: Enable internal pull-up MOS.

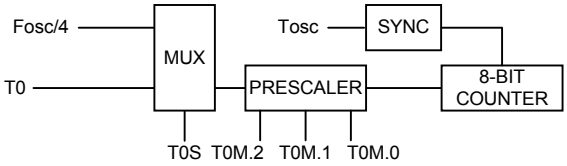
7. Timer

SH69P48 has two 8-bit timers.

The Timer0 has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer0 block diagram.



The Timer0 provides the following functions:

- Programmable interval timer function.
- Read counter value.

(a) Timer0 Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

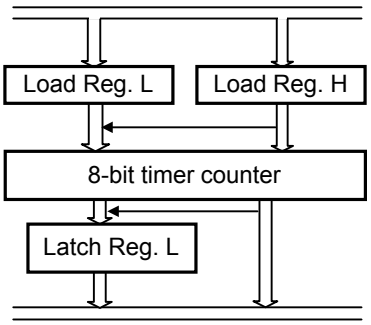
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



(b) Timer pre-scaler select Register

The Timer0 can be programmed in several different pre-scalers by setting Timer0 pre-scaler select register.
The 8-bit counter prescaler overflow outputs pulses. The Timer0 pre-scaler select register is 3-bit register used for the timer control as shown bellow. These bits select the input pulse sources into the timer.

Timer0 pre-scaler select Register: $02

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

(C) External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer0 source, it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t_{OSC}) and low (at least 2 t_{OSC}). When the prescaler ratio selects $/2^0$, it is the same as the system clock input.
The requirement is as follows

T0H (T0 high time) $\geq 2 * t_{OSC} + \Delta T$

T0L (T0 low time) $\geq 2 * t_{OSC} + \Delta T$; ΔT= 20ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$T0\ \text{high time} = T0\ \text{low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = prescaler value

The requirement is:

$$\frac{N * T0}{2} \geq 2 * tosc + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

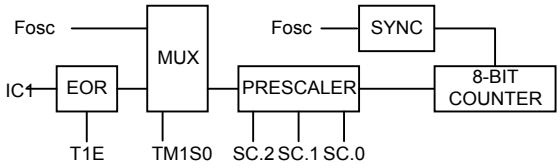
Timer0 pre-scaler select Register: $02

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit3: T0 signal source
	0	X	X	X	R/W	Shared with PortC.3, Timer0 source is system clock (Default)
	1	X	X	X	R/W	Shared with T0 input, Timer0 source is T0 input clock (Falling edge active)

The Timer1 has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer1 block diagram.



The Timer1 provides the following functions:

- Programmable interval timer function.
- Read counter value.

(c) Timer1 Configuration and Operation

Timer1 consists of a 8-bit write-only timer load register (TL1L, TL1H) and a 8-bit read-only timer counter (TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

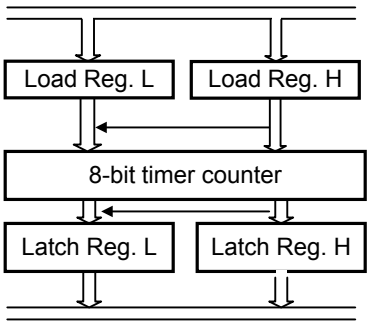
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



(d) Timer1 Control Register

The Timer1 can be programmed in two modes: timer and pulse width measurement.

Timer1 Control Register: $13

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T1GO	DEC	-	TM1S0	R/W	Bit0: Timer1 mode select
	X	X	-	0	R/W	Timer with internal system clock
	X	X	-	1	R/W	Pulse width measurement (T1 pin input)
	0	X	-	X	R/W	Timer/counter stops (Read: status; Write: command) (default)
	1	X	-	X	R/W	Timer/counter starts (Read: status; Write: command)

(1) Timer mode

In this mode, Timer1 is performed using the internal clock. The contents of the Timer1 counter register ($06 ~ $07) are loaded into the up-counter while the highest nibble ($07) has been written. The up-counter will start counting if the T1GO (bit3) in the Timer1 control register ($13) is set to 1. The Timer1 interrupt will issue when the up-counter overflows from $FF to $00 if the Interrupt enable register ($00) bit1 (IET1) is set to 1.

After the T1GO (bit3) in the Timer1 control register ($13) has been set to 1, writing the Timer1 counter register ($06 ~ $07) can not affect the up-counter operating anymore. Only when the T1GO (bit3) in the Timer1 control register ($13) has been reset to 0, the revised contents of the Timer1 counter register ($06 ~ $07) will be loaded into the up-counter while the highest nibble ($07) is written.

Timer1 pre-scaler select Register: $03

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$03	T1E	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 pre-scaler select Bit3: T1 external signal edge select
	X	0	0	0	R/W	Timer clock: OSC clock / 2^{11}
	X	0	0	1	R/W	Timer clock: OSC clock / 2^{9}
	X	0	1	0	R/W	Timer clock: OSC clock / 2^{7}
	X	0	1	1	R/W	Timer clock: OSC clock / 2^{5}
	X	1	0	0	R/W	Timer clock: OSC clock / 2^{3}
	X	1	0	1	R/W	Timer clock: OSC clock / 2^{2}
	X	1	1	0	R/W	Timer clock: OSC clock / 2^{1}
	X	1	1	1	R/W	Timer clock: OSC clock / 2^{0}
	0	X	X	X	R/W	T1 input falling edge active (Default)
	1	X	X	X	R/W	T1 input rising edge active

(2) Pulse width measurement mode

In this mode, Timer1 is performed using a special function under the timer mode in which counting is started on an edge of pulse waveform that is input to the T1 pin. It is possible to measure the width of the pulse waveform by reading the up-counter values on state transitions of the input to the T1 pin. The rising or falling edge of the T1 pin input is selected by setting the T1E (bit3) in the Timer1 pre-scaler register ($03). But the source clock of the up-counter is an internal clock selected by proper setting the T1M (bit2-0) in the Timer1 pre-scaler register ($03). When the T1GO (bit3) in the Timer1 control register ($13) is set to “1”, the contents of the up-counter must reset to “00H”, automatically. Then a rising (falling) edge signal on the T1 input pin triggers the up-counter to start counting. At the next falling (rising) edge, the counter value is loaded to the Timer1 counter register ($06 ~ $07), individually. Simultaneously, the Timer1 interrupt is generated if the Interrupt enable register ($00) bit1 (IET1) is set to 1.

When DEC (bit2) in the Timer1 control register ($13) is 0, the Timer1 is in the one-edge capture operation. If the rising edge is selected as the counter triggering signal, at the next falling edge, the Timer1 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer1 counter register ($06 ~ $07) at first, then will be cleared again and the counter is halted. When the next rising edge applies to the T1 input pin, the up-counter starts counting for another measurement cycle.

When DEC (bit2) in the Timer1 control register ($13) is 1, the Timer1 is in the double-edge capture operation. If the rising edge is selected as the counter triggering signal, at the next falling edge, the Timer1 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer1 counter register ($06 ~ $07) at first, then the counter continues counting. When the next rising edge applies to the T1 input pin, the Timer1 interrupt request is also generated. At this time, the contents of the up-counter must be loaded to the Timer1 counter register ($06 ~ $07) again, then the counter must be cleared and can be continued to start counting following measurement cycles.

In this mode, writing the Timer1 counter register ($06 ~ $07) at any time can not affect the up-counter operating anymore.

In this mode, the T1 pin input signal must follow certain constraints. So, the limitation is applied for the T1 period time described as follows:

$$T1\ (\text{period time}) \geq 1 * t_{\text{Timer clock}} + 2 * \Delta T \qquad ; \Delta T = 20ns$$

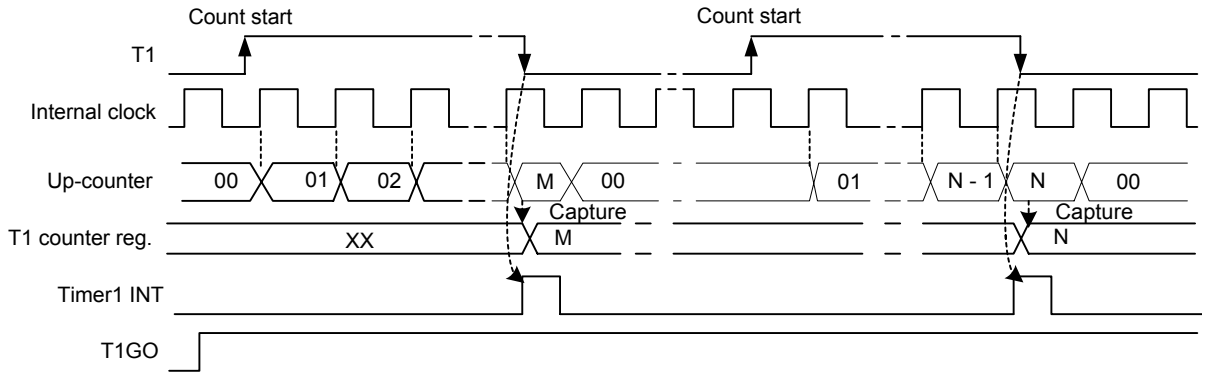
$$T1\ (\text{period time}) \geq (M * t_{OSC}) + 2 * \Delta T$$

where M (pre-scaler value for Timer1 internal clock) $=2^0, 2^1, 2^2, 2^3, 2^5, 2^7, 2^9$ or 2^{11}

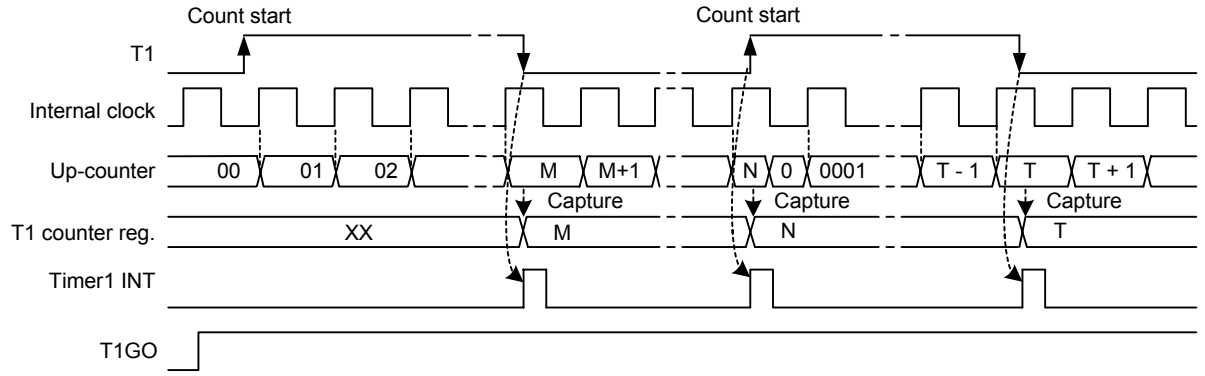
But, in order to correctly get the pulse measurement value in programming, a sufficient wait period must be needed for the relevant Timer1 interrupt subroutine program.

Timer1 Counter Register: $06 ~ $07

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load / counter register (low nibble)
$07	T1H.3	T1H.2	T1H.2	T1H.0	R/W	Timer1 load / counter register (high nibble)



One edge capture (DEC = 0)



Double edge capture (DEC = 1)

Timer1 Control Register: $13 (under the pulse width measurement mode)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T1GO	DEC	-	TM1S0	R/W	Bit0: Timer1 mode select
	X	0	-	1	R/W	Bit2: One edge capture.
	X	1	-	1	R/W	Bit2: Double edge capture.

8. Analog/Digital Converter (ADC)

The 10 channels and 10-bit resolution A/D converter are implemented in this microcontroller.

The A/D converter system registers are $14~$17 and $2D~$2F. The $14~$17 system registers are A/D converter control register, which defines the A/D channel number, analog channel select, reference voltage select, A/D conversion clock select, start A/D conversion control bit and the end of A/D conversion flag. The $2D~$2F system registers are A/D conversion result register byte and are read-only.

The approach for A/D conversion:

- Set analog channel and select reference voltage. (When using the external reference voltage, keep in mind that any analog input voltage must not exceed V_{REF})
- Operating A/D converter module and select the converted analog channel.
- Set A/D conversion clock source.
- GO/$\overline{DONE}$ =1, start A/D conversion.

(a) Systems register $14

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	VREFS	-	-	ADCON	R/W	Bit0: Set ADC module operate Bit3: Select Internal/External reference voltage
	X	X	X	0	R/W	A/D converter module not operating
	X	X	X	1	R/W	A/D converter module operating
	0	X	X	X	R/W	Internal reference voltage (V_{REF}=V_{DD})
	1	X	X	X	R/W	External reference voltage

(b) Systems register $16

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	ACR3	ACR2	ACR1	ACR0	R/W	Bit3-0: A/D port configuration control
	0	0	0	0	R/W	See the following table

Select analog channels from normal I/O ports

ACR3	ACR2	ACR1	ACR0	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PD1	PD0	PB3	PB2	PB1	PB0	PA3	PA2	PA1	PA0
0	0	0	1	PD1	PD0	PB3	PB2	PB1	PB0	PA3	PA2	PA1	AN0
0	0	1	0	PD1	PD0	PB3	PB2	PB1	PB0	PA3	PA2	AN1	AN0
0	0	1	1	PD1	PD0	PB3	PB2	PB1	PB0	PA3	AN2	AN1	AN0
0	1	0	0	PD1	PD0	PB3	PB2	PB1	PB0	AN3	AN2	AN1	AN0
0	1	0	1	PD1	PD0	PB3	PB2	PB1	AN4	AN3	AN2	AN1	AN0
0	1	1	0	PD1	PD0	PB3	PB2	AN5	AN4	AN3	AN2	AN1	AN0
0	1	1	1	PD1	PD0	PB3	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	X	0	0	PD1	PD0	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	X	0	1	PD1	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
1	X	1	X	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

(c) Systems register $17 for ADC channel selection

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	CH3	CH2	CH1	CH0	R/W	Bit3-0: Select ADC channel
	0	0	0	0	R/W	ADC channel AN0
	0	0	0	1	R/W	ADC channel AN1

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
	0	0	1	0	R/W	ADC channel AN2
	0	0	1	1	R/W	ADC channel AN3
	0	1	0	0	R/W	ADC channel AN4
	0	1	0	1	R/W	ADC channel AN5
	0	1	1	0	R/W	ADC channel AN6
	0	1	1	1	R/W	ADC channel AN7
	1	X	X	0	R/W	ADC channel AN8
	1	X	X	1	R/W	ADC channel AN9

(d) Systems register $2D ~ $2F for ADC data

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2D	X	X	A1	A0	R	ADC data low nibble (Read only)
$2E	A5	A4	A3	A2	R	ADC data medium nibble (Read only)
$2F	A9	A8	A7	A6	R	ADC data high nibble (Read only)

(e) Systems register $15

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: Set A/D Conversion Time Bit2, Bit1: Select A/D Clock Period Bit3: ADC status flag
	X	X	X	0	R/W	A/D Conversion Time = 204 t_{AD}
	X	X	X	1	R/W	A/D Conversion Time = 780 t_{AD}
	X	0	0	X	R/W	A/D Clock Period t_{AD} = t_{OSC}
	X	0	1	X	R/W	A/D Clock Period t_{AD} = 4 t_{OSC}
	X	1	0	X	R/W	A/D Clock Period t_{AD} = 8 t_{OSC}
	X	1	1	X	R/W	A/D Clock Period t_{AD} =16 t_{OSC}
	0	X	X	X	R/W	A/D conversion not in progress
	1	X	X	X	R/W	A/D conversion in progress, when ADCON=1

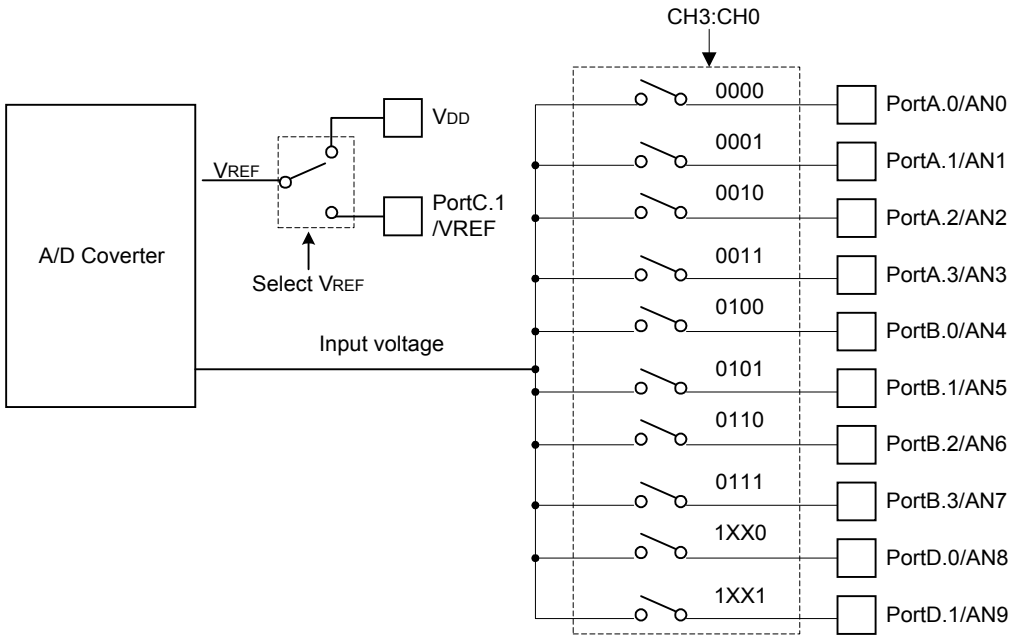


Figure 1 A/D Converter Block Diagram

Programming Notice:

- Select A/D clock period t_{AD}, make sure that $1\mu s \le t_{AD} \le 33.4\ \mu s$.
- When the A/D conversion is completed, an A/D converter interrupt occurs (if the A/D converter interrupt is enabled).
- The analog input channels must have their corresponding PXCR (X=A, B,D) bits selected as inputs.
- If an I/O port is selected as an analog input, the I/O port can not be accessed anymore.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the A/D conversion is completed.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current operation.
- The A/D result register will NOT be updated with the partially completed A/D conversion sample.
- 4-t_{OSC} wait is required before the next acquisition is started.
- The A/D converter could keep on working in the HALT mode, and would stop automatically when the "STOP" instruction is executed.
- The A/D converter could wake-up SH69P48 from the HALT mode (if the A/D converter interrupt is enabled).

9. Pulse Width Modulation (PWM)

The SH69P48 consists of two 8+2 bit PWM modules. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMP is used to control the period cycle of the PWM module output. And the PWMD is used to control the duty in the waveform of the PWM module output.

PWM Control Register $20, $21: (PWMC)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20, $21	PWMnS	TnCK1	TnCK0	PWMn_EN	R/W	Bit0: Set PWMn output enable Bit2, Bit1: Select PWMn clock Bit3: Set PWMn output mode of duty cycle
	X	X	X	0	R/W	Shared with I/O port (Default)
	X	X	X	1	R/W	Shared with PWMn, n=0 or 1
	X	0	0	X	R/W	PWMn clock = t_{OSC} (Default)
	X	0	1	X	R/W	PWMn clock = $2t_{OSC}$
	X	1	0	X	R/W	PWMn clock = $4t_{OSC}$
	X	1	1	X	R/W	PWMn clock = $8t_{OSC}$
	0	X	X	X	R/W	PWMn output normal mode of duty cycle (high active) (Default)
	1	X	X	X	R/W	PWMn output negative mode of duty cycle (low active)

n=0 or 1

The PWM0 output pin is shared with PORTC.2.

The PWM1 output pin is shared with PORTD.3.

PWM Period Control Register $22 ~ $23, $27 ~ $28: (PWMP)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$22, $27	PPn.3	PPn.2	PPn.1	PPn.0	R/W	PWMn period low nibble
$23, $28	PPn.7	PPn.6	PPn.5	PPn.4	R/W	PWMn period high nibble

n=0 or 1

PWM output period cycle = [PPn.7, PPn.0] x PWMn clock.

When [PPn.7, PPn.0]= 00H, PWMn outputs GND if the PWMnS bit is set to 0.

When [PPn.7, PPn.0]= 00H, PWMn outputs high level if the PWMnS bit is set to 1.

PWM Duty Control Register $24 ~ $26, $29 ~ $2B: (PWMD)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	-	-	PDF0.1	PDF0.0	R/W	PWM0 duty fine tune nibble
$25	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble
$26	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty high nibble
$29	-	-	PDF1.1	PDF1.0	R/W	PWM1 duty fine tune nibble
$2A	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble
$2B	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty high nibble

n=0 or 1

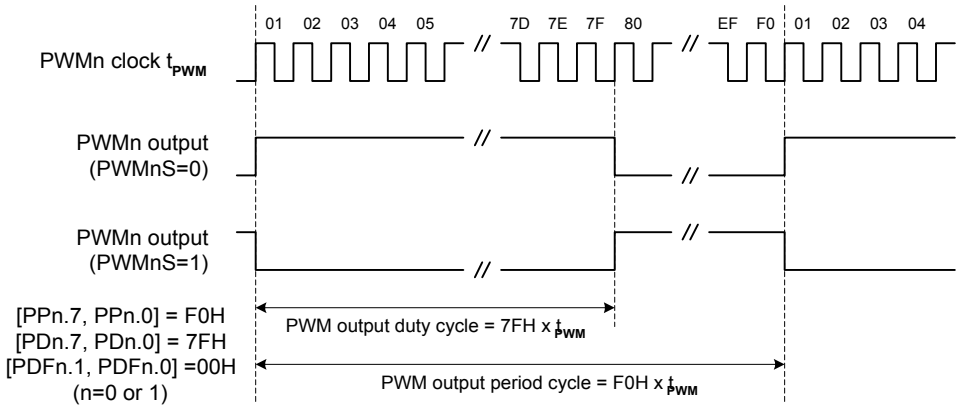
Average PWMn output duty cycle =([PDn.7, PDn.0] + [PDFn.1, PDFn.0] / 4) x PWMn clock.

If [PPn.7, PPn.0] ≤ [PDn.7, PDn.0], PWMn outputs high when the PWMnS bit is set to 0.

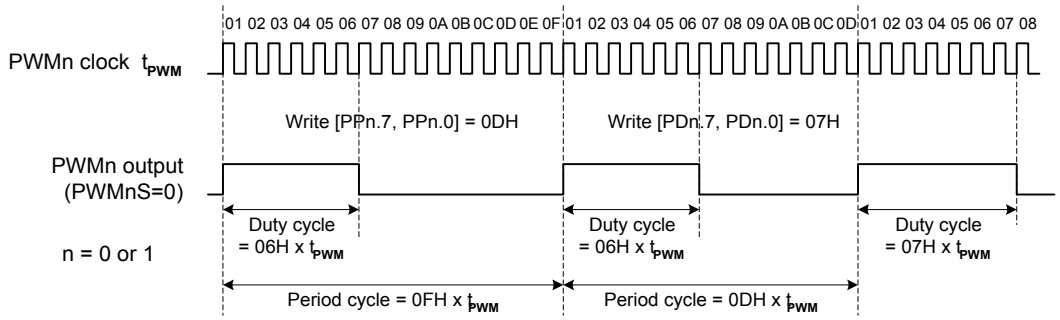
If [PPn.7, PPn.0] ≤ [PDn.7, PDn.0], PWMn outputs GND level when the PWMnS bit is set to 1.

Notice:

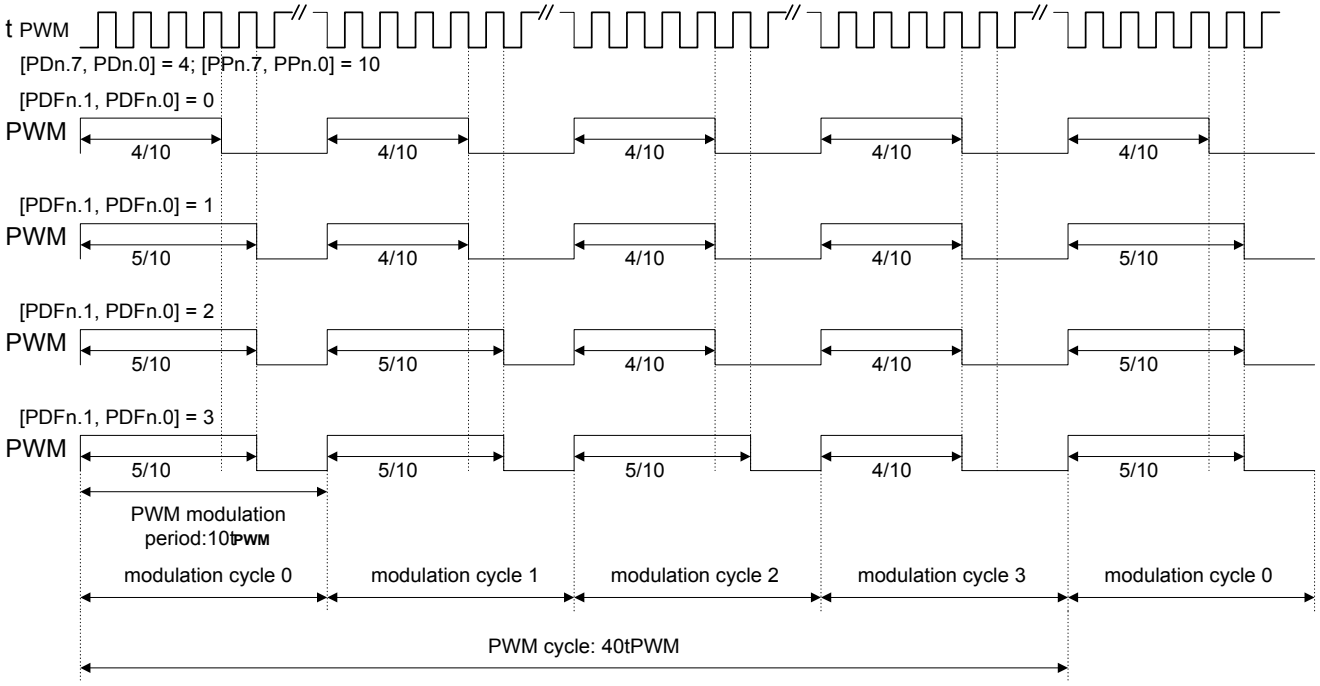
- If the I/O port is selected as the PWM output, the I/O functions and pull up resistor are disabled.
- The writing flow of the PWMn duty control register is described as follows. First set the fine tune nibble, then the low nibble and set the high nibble at last.
- The writing flow of the PWMn period control register is described as follows. First set the low nibble, then set the high nibble.
- After the high nibble of the PWMn period or duty control register is written, the data are loaded into the re-load counter and start counting at next period.
- The reading flow of the PWMn period or duty control register is at the reverse direction with that described above. First read the high nibble, then read the low nibble.
- PWM could keep on working in the HALT mode, and would stop automatic when the "STOP" instruction is executed.



PWM output example



PWM output Period or Duty cycle changing example



8+2 bit PWM waveform

In the 8+2 bit PWM waveform, A PWM cycle is divided into 4 modulation cycles(cycle 0 – cycle 3), each modulation cycle has certain period decided by period cycle registers(PWMP). The contents of duty cycle register(PWMD) is divided into two parts. The basic part of PWMD is PDn.7 – PDn.0. The extended part is PDFn.1 – PDFn.0. In a PWM cycle, the duty cycle of each modulation cycle is shown in the table.

Parameter	[PDFn.1, PDFn.0] (0-3)	Duty Cycle
Modulation Cycle I (I=0-3)	I<	([PDn.7, PDn.0] + 1)/ [PPn.7, PPn.0]
	I≥ [PDFn.1, PDFn.0]	[PDn.7, PDn.0] / [PPn.7, PPn.0]

The modulation period, cycle period and cycle duty of the PWM output signal are summarized in the following table.

PWM modulation period	PWM cycle period	PWM cycle duty
[PPn.7, PPn.0] * tpwm	4*[PPn.7, PPn.0] * tpwm	(4* [PDn.7, PDn.0] + [PDFn.1, PDFn.0])/(4*[PPn.7, PPn.0])

10. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where heavy loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by the OTP option.

The LVR circuit has the following functions when the LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq t_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$ and $t < t_{LVR}$.
-

11. ROM Data Table

ROM Data Table Register (RDT): $380 - $383

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address / data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address / data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address / data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address / data register

The RDT register consists of a 12-bit write-only PC address load register (RDT.11 – RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 – RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first then low nibble), then after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into $380 will start the data read-out action).

Programmer can put 16-bit data into one address by data allocation instruction “DW”. (Reference to UASM66 Cross Assembler User’s Guide.)

12. Interrupt

Four interrupt sources are available on SH69P48:

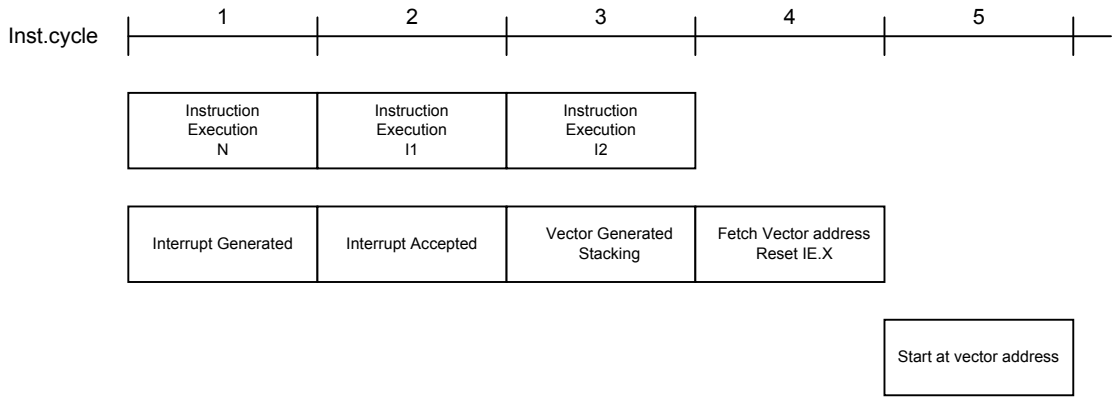
- A/D interrupt
- Timer0 interrupt
- Timer1 interrupt
- PortB/D interrupts (Falling edge)

(a) Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQAD	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the SH6610D CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

(b) A/D interrupt

Bit3 (IEAD) of system register $00 is the ADC interrupt enable flag. When the A/D conversion is complete, It will generate an interrupt request (IRQAD=1), if the ADC interrupt is enabled (IEAD=1), an ADC interrupt service routine will start. The A/D interrupt can be used to wake the CPU from HALT mode.

(c) Timer (Timer0, Timer1) Interrupt

The input clock of Timer0 and Timer1 are based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1=1), If the interrupt enable flag is enabled (IET0 or IET1=1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

(d) Port Interrupt

The PORTB/D are used as external port interrupt sources. Since PORTB/D are bit programmable I/Os, so only the voltage transition from VDD to GND applying to the digital input port can generate a port interrupt. The analog input can not generate any interrupt request.

The interrupt control flags are mapped on $384 - $387 of the system register. They can be accessed or tested by the read/write operation. Those flags are cleared to 0 at the initialization by the chip reset. Port Interrupts (including other external interrupt sources) can be used to wake up the CPU from the HALT or the STOP mode.

Port Interrupt Enable Flags Register: $384, $386

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$384	PDIEN.3	PDIEN.2	PDIEN.1	PDIEN.0	R/W	PORTD interrupt enable flags
$386	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags

PDIEN.n, PBIEN.n (n = 0, 1, 2, 3)

0: Disable port interrupt. (Default)

1: Enable port interrupt.

Port Interrupt Request Flags Register: $385, $387

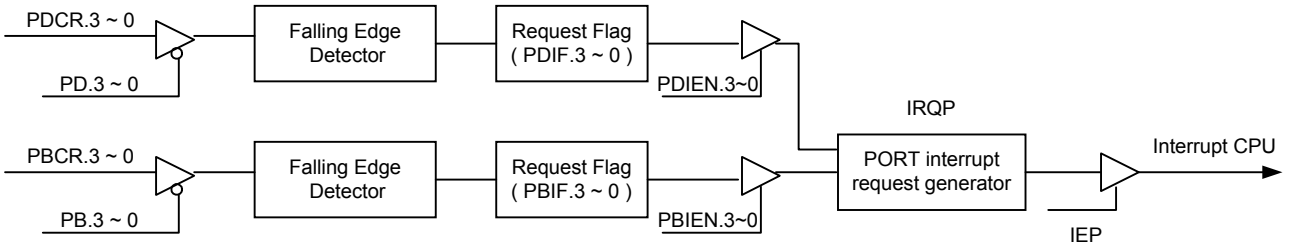
	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38A	PDIF.3	PDIF.2	PDIF.1	PDIF.0	R/W	PORTD interrupt request flags
$38C	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags

PDIF.n, PBIF.n (n = 0, 1, 2, 3)

0: Port interrupt is not presented. (Default)

1: Port interrupt is presented.

Only writing these bits to 0 is available.



Port Interrupt function block-diagram

14. Watch Dog Timer (WDT)

Watch dog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that the WDT will always run even in the STOP mode (if it is enabled). The watchdog timer automatically generates a device reset when it overflows. OTP option can enable and disable this function. The watchdog timer control registers (WDT bit2 ~ 0) is selects different overflow frequency. WDT bit3 is watchdog timer overflow flag.

If the Watchdog timer is enabled, the CPU will be reset when watchdog timer overflows. Repeat reads or writes WDT register ($1E), the watchdog timer should re-count before the overflow happens.

System Register $1E: (WDT)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watch dog timer control Bit3: Watchdog timer overflow flag (Read only)
	X	0	0	0	R/W	Watch dog timer-out period = 4096ms
	X	0	0	1	R/W	Watch dog timer-out period = 1024ms
	X	0	1	0	R/W	Watch dog timer-out period = 256ms
	X	0	1	1	R/W	Watch dog timer-out period = 128ms
	X	1	0	0	R/W	Watch dog timer-out period = 64ms
	X	1	0	1	R/W	Watch dog timer-out period = 16ms
	X	1	1	0	R/W	Watch dog timer-out period = 4ms
	X	1	1	1	R/W	Watch dog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer-out period valid for V_{DD} = 5V.

15. HALT and STOP Mode

After the execution of HALT instruction, The device will enter halt mode. In the halt mode, CPU will stop operating. But peripheral circuit (Timer0, Timer1, ADC and watchdog timer) will keep operating.
After the execution of STOP instruction, The device will enter stop mode. In the stop mode, the whole chip (including oscillator) will stop operating without watchdog timer, if it is enabled.
In HALT mode, SH69P48 can be waked up if any interrupt occurs.
In STOP mode, SH69P48 can be waked up if port interrupt occurs or watchdog timer overflow (WDT is enabled).

16. Warm-up Timer

The device builds in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

(a) Power on reset warm-up time interval

(1) When oscillator range is selected as 30kHz to 2MHz scope, the warm-up counter prescaler is divided by 2^{12} (4096).
(2) When oscillator range is selected as 2MHz to10MHz scope, the warm-up counter prescaler is divided by 2^{14} (16384).

(b) Others warm-up time interval

- Hardware reset
- Low voltage reset
- Wake-up from stop mode

(1) In RC oscillator or external clock mode, the warm-up counter prescaler is divided by 2^{7} (128).
(2) In crystal oscillator or ceramic resonator mode, the warm-up counter prescaler is divided by 2^{12} (4096).

17. OTP option

(a) Oscillator type:

OP_OSC [2:0]:

000 = External clock (Select OSCO pin as PORTC.0 for a normal I/O port) (Default)

001 = Internal ROSC RC oscillator (4MHz) (Select OSCO pin as PORTC.0 and OSCI pin as PORTE.0 for normal I/O ports)

010 = Internal ROSC RC oscillator (4MHz) (Select OSCO pin as PORTC.0 and OSCI pin as PORTE.0 for normal I/O ports)

011 = Internal ROSC RC oscillator (4MHz) (Select OSCO pin as PORTC.0 and OSCI pin as PORTE.0 for normal I/O ports)

100 = External R_{OSC} RC oscillator (400kHz ~ 10MHz) (Select OSCO pin as PORTC.0 for a normal I/O port)

101 = Ceramic resonator (400kHz ~ 10MHz)

110= Crystal oscillator (400kHz ~ 10MHz)

111 = 32.768kHz Crystal oscillator

(b) Oscillator range:

OP_OSC 3:

0 = 2MHz ~ 10MHz (Default)

1 = 30kHz ~ 2MHz

(c) Watch dog timer:

OP_WDT:

0 = Enable (Default)

1 = Disable

(d) Low Voltage Reset:

OP_LVR:

0 = Disable (Default)

1 = Enable

(e) LVR voltage Range:

OP_LVR0:

0 = High LVR voltage (Default)

1 = Low LVR voltage

(f) Chip pin Reset:

OP_RST:

0 = Enable chip pin reset (Default)

1 = Disable chip pin reset (Select RESET pin as PORTE.1 for an open drain output)

(g) Package:

OP_PKG [1:0]:

00 = 20 pin (Default)

01 = 16 pin

1X = 8pin

Instructions

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

(h) Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx □ ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx □ ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx □ ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx □ ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx □ ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx □ ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

(i) Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

2. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

3. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

4. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input / Output Voltage . . . . . GND-0.3V to VDD+0.3V

Operating Ambient Temperature . . . . . .-40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

1. DC Electrical Characteristics

(a) GND = 0V, T_A = -40℃ to +85℃, F_{OSC} = 10MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	30kHz ≤ F_{OSC} ≤ 10MHz
Operating Current	I_{OP}	-	3	4.5	mA	All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction) WDT off, ADC disable, LVR off
Stand by Current (HALT)	I_{SB1}	-	-	1.5	mA	All output pins unload, CPU off (execute HALT instruction), WDT off, ADC disable, LVR off
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unload, CPU off (execute STOP instruction), WDT off, ADC disable, LVR off
WDT Current	I_{WDT}	-	-	20	μA	All output pins unload, CPU off (execute STOP instruction) , WDT on, ADC disable, LVR off
Input Low Voltage	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input Low Voltage	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI (external clock)
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI (external clock)
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN}=V_{DD} or GND
Pull-up Resistor	R_{PH}	10	20	50	KΩ	V_{DD} =5.0V, V_{IN}=GND
Output Leakage Current	I_{OL}	-1	-	1	μA	Open drain output, V_{DD} =5.0V V_{OUT}=V_{DD} or GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, PWM0&1, I_{OH} = -10mA, V_{DD} =5.0V
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O Ports, PWM0&1, I_{OL} = 20mA, V_{DD} =5.0V

*: Data in “Typ.” column is at 5.0V, 25℃,unless otherwise specified.

Maximum value of the supply current to V_{DD} is 100mA.

Maximum value of the output current from GND is 150mA.

(b) GND = 0V, T_A = -40℃ to +85℃, F_{OSC} = 4MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	5.0	5.5	V	30kHz ≤ F_{OSC} ≤ 4MHz
Operating Current	I_{OP}	-	2	3	mA	All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction) WDT off, ADC disable, LVR off
Stand by Current (HALT)	I_{SB1}	-	-	1	mA	All output pins unload, CPU off (execute HALT instruction), WDT off, ADC disable, LVR off
Stand by Current (STOP)	I_{SB2}	-	-	1	μA	All output pins unload, CPU off (execute STOP instruction), WDT off, ADC disable, LVR off
WDT Current	I_{WDT}	-	-	20	μA	All output pins unload, CPU off (execute STOP instruction) , WDT on, ADC disable, LVR off
Input Low Voltage	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input Low Voltage	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, OSCI

*: Data in “Typ.” column is at 5.0V, 25℃,unless otherwise specified.

2. AC Electrical Characteristics

(a) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30KHz ~10MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	T_{CY}	0.4	-	133.4	μs	
T0 input width	t_{IW}	(T_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	

(b) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30KHz ~ 10MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width	t_{RESET}	10	-	-	μs	Low active
WDT Period	T_{WDT}	1	-	-	ms	
Frequency Variation	|ΔF|/F	-	-	15	%	External R_{OSC} Oscillator, Include supply voltage, temperature and chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)
Frequency Variation	|ΔF|/F	-	-	20	%	Internal R_{OSC} Oscillator, F_{OSC} = 4MHz Include supply voltage, temperature and chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)

3. A/D Converter Electrical Characteristics

V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30kHz ~ 10MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	NR	-	-	10	bit	$GND \le V_{AIN} \le V_{REF}$
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor	R_{AIN}	2000	-	-	KΩ	V_{IN}=5.0V
A/D conversion current	I_{AD}	-	500	1000	μA	A/D converter module operating, V_{DD}=5.0V
Nonlinear Error	E_{NL}	-	-	±2	LSB	$V_{REF} = V_{DD}$ = 5.0V
Full scale error	E_F	-	-	±1	LSB	$V_{REF} = V_{DD}$ = 5.0V
Offset error	E_Z	-	-	±1	LSB	$V_{REF} = V_{DD}$ = 5.0V
Total Absolute error	E_{AD}	-	±1	±2	LSB	$V_{REF} = V_{DD}$ = 5.0V
A/D Clock Period	t_{AD}	1	-	33.4	μs	F_{OSC} = 30kHz ~ 10MHz
A/D Conversion Time	t_{CNV1}	-	204	-	t_{AD}	Set ADCS=0
A/D Conversion Time	t_{CNV2}	-	780	-	t_{AD}	Set ADCS=1

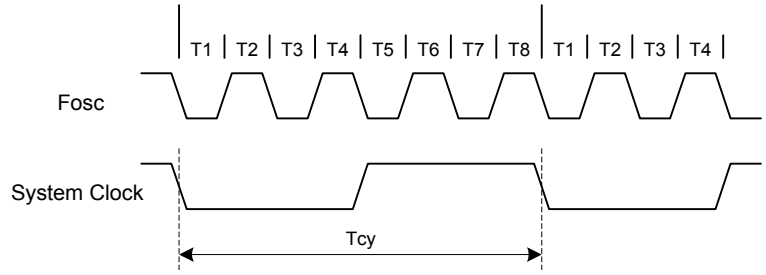
4. Low Voltage Reset Electrical Characteristics

V_{DD} = 3.0V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 32.768kHz ~ 10MHz, unless otherwise specified.

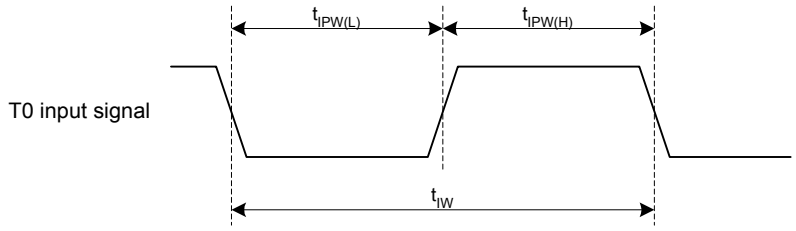
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage (High)	V_{LVR1}	3.8	-	4.2	V	LVR enable
LVR Voltage (Low)	V_{LVR2}	2.3	-	2.7	V	LVR enable
LVR Voltage Pulse Width	t_{LVR}	500	-	-	μs	$V_{DD} \le V_{LVR}$

5. Timing Waveform

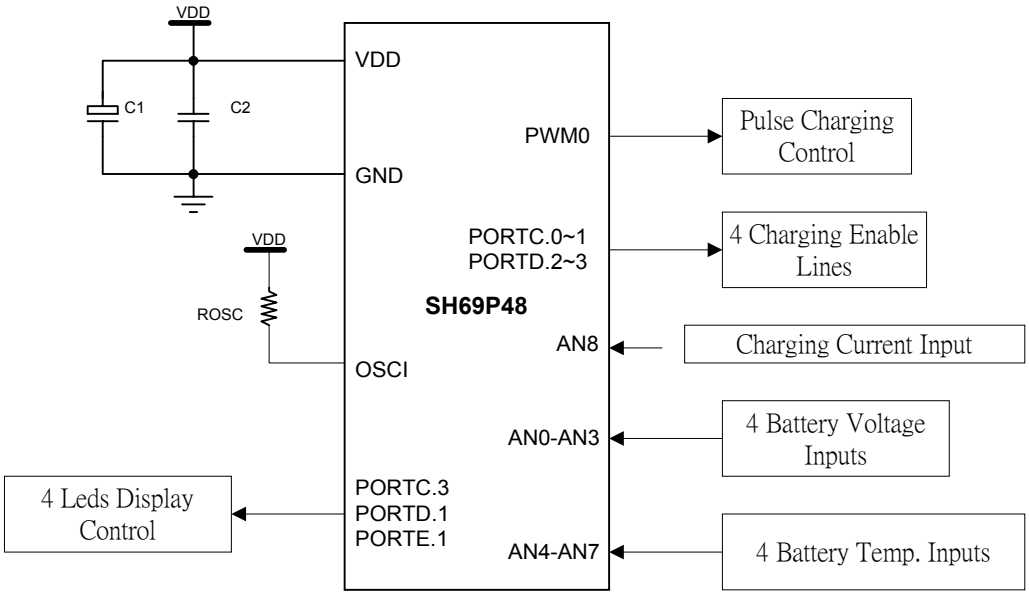
(c) System Clock Timing Waveform



(d) T0 Input Waveform



Application Circuits:



Product SPEC. Change Notice

SH69P48 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	June, 2004