SINO WEALTH

SH69P55

OTP 8K 4-Bit Micro-controller With SAR 10-bit A/D Converter & LCD Driver

Preliminary

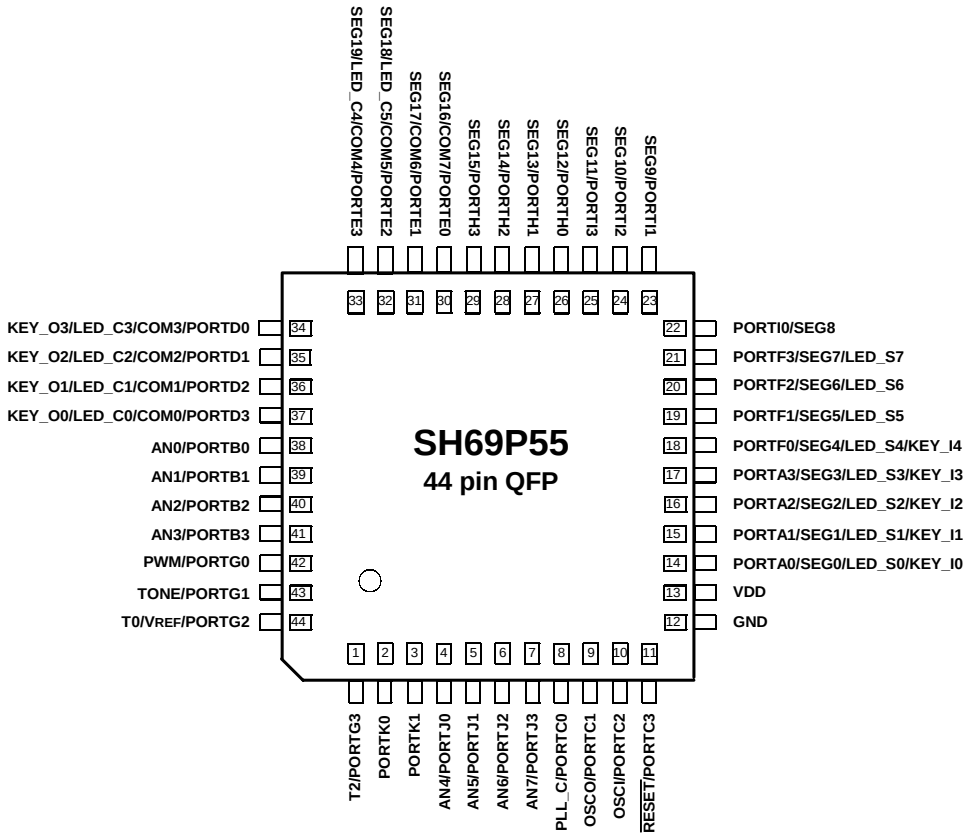
Features

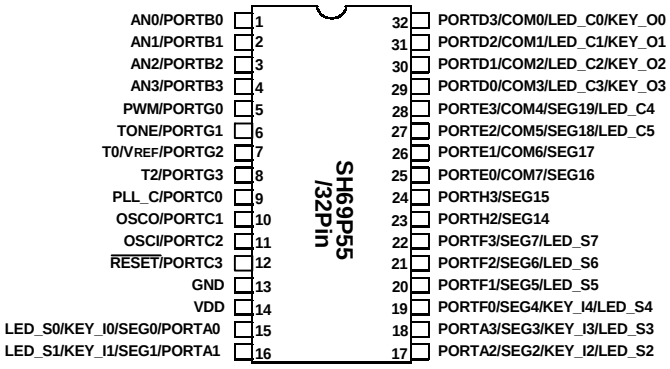
- SH6610D-Based Single-Chip 4-bit Micro-Controller
- OTP ROM: 8192X 16 bits
- RAM: 512 X 4 bits
  - System register: 96 X 4 bits
  - Data memory: 416 X 4 bits including LCD RAM
- Operation voltage:
  - fosc=32.768kHz, 400kHz - 4MHz, VDD=2.4V - 5.5V
  - fosc=4M - 8MHz, VDD=4.5V - 5.5V
- 26 CMOS bi-directional I/O pins (28 pin SKINNY)
- 30 CMOS bi-directional I/O pins (32 pin SDIP)
- 42 CMOS bi-directional I/O pins (44 pin QFP)
- Built-in pull-high for I/O port
- Two 8-Bit Auto Re-load Timer/Counter, one can switch to external clock source
- One 16-bit timer/counter for pulse measurement
- 8-Level Subroutine Nesting (including interrupts)
- Zero Cross Detect function for AC Power line
- LCD driver:
  - 8X16, 6X18 and 4X20
- LED driver which can drive LED directly:
  - 6X8, 5X8 and 4X8
- Powerful interrupt sources:
  - Internal interrupt (Timer2, Timer1, Timer0)
  - External interrupts (include PortB, PortC interrupts, AD interrupt, Key scan interrupt)
- Oscillator: (Code option)
  - Crystal oscillator: 32.768kHz, 400kHz - 8MHz
  - Ceramic resonator: 400kHz - 8MHz
  - External R_{OSC} RC oscillator: 400kHz - 8MHz
  - Internal R_{OSC} RC oscillator: 4MHz
- Instruction cycle time:
  - 4/32.768kHz (≈122μs) for 32.768kHz
  - 4/8MHz (= 0.5μs) for 8MHz at V_{DD}=5.0V
- 8 channels 10-bit resolution A/D converter
- One Built-in PLL
- 2 channel tone generators
- Built-in automatic Key Scanner
- Read ROM Table function
- One channel 8+2bit PWM output
- Warm-up timer for power on reset
- Low voltage reset function (LVR)
- Internal reliable reset circuit
- Built-in watchdog timer
- Built-in system clock monitor circuit
- Two low power operation modes: HALT and STOP
- OTP type/Code protection
- 28-pin SKINNY/32-pin SDIP/44-pin QFP package

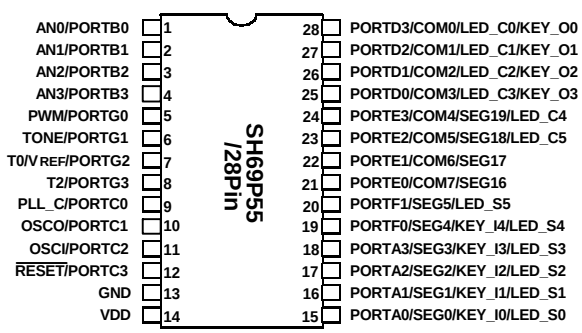
General Description

The SH69P55 is an advanced CMOS 4-bit micro-controller. It provides the following standard features: 8K words of OTP ROM, 512 nibbles of RAM, tow 8-bit timer/counter, one 16-bit timer/counter, LED driver, LCD driver, built-in automatic key scanner two channel tone generators, 10-bit A/D converter, on-chip oscillator clock circuitry, built-in PLL, Zero Cross Detect function, on-chip watchdog timer, low voltage reset function and a built-in dual-oscillator to enhance the total chip performance. It can support power saving modes to reduce the power consumption.

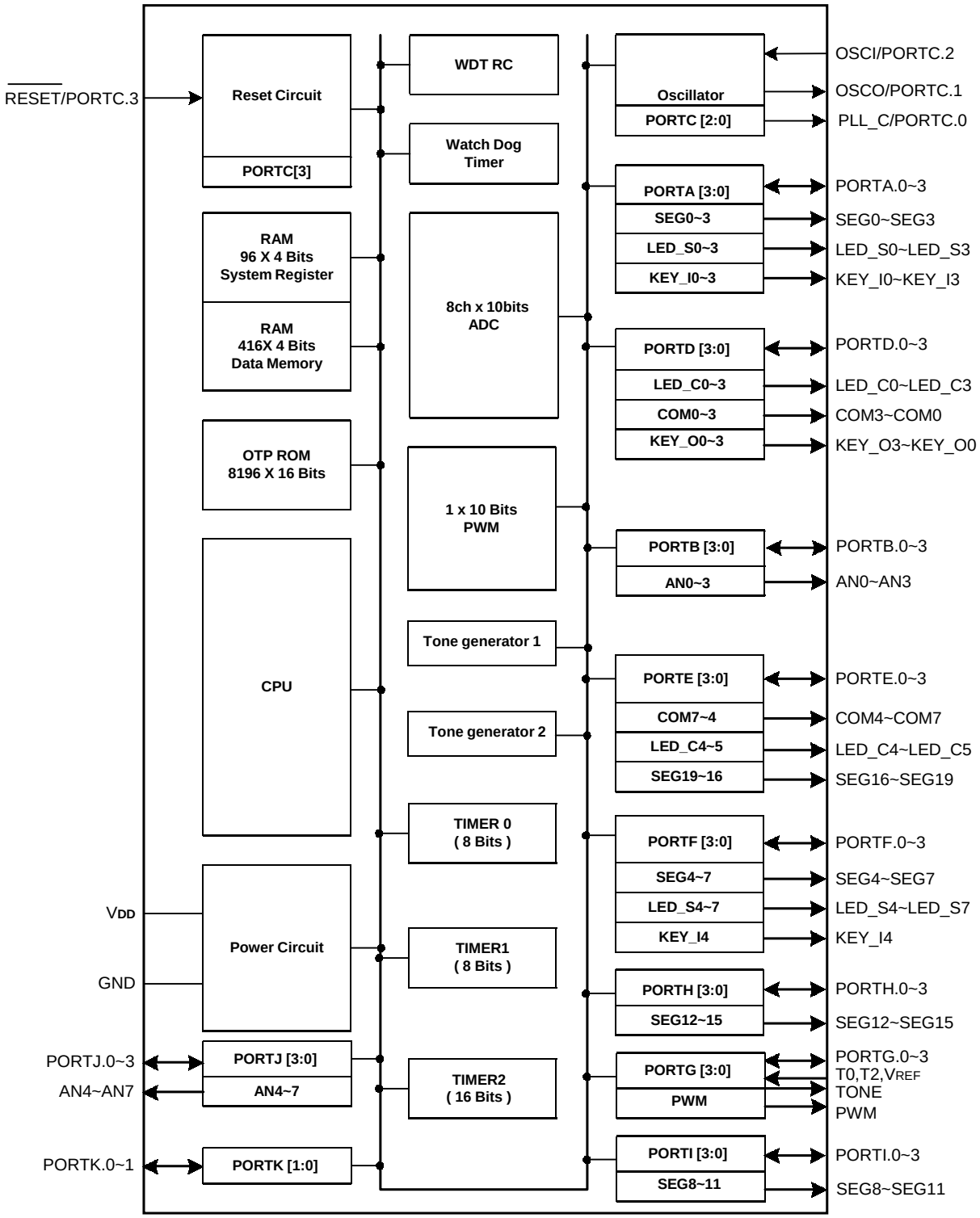
Pin Configuration







Block Diagram



Pin Descriptions (For 28 pin)

Pin No.	Designation	I/O	Description
1	PORTB.0 /AN0	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input0
2	PORTB.1 /AN1	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input1
3	PORTB.2 /AN2	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input2
4	PORTB.3 /AN3	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input3
5	PORTG..0 /PWM	I/O O	Bi-directional I/O port Shared with PWM output
6	PORTG.1 /TONE	I/O O	Bi-directional I/O port Shared with TONE generator output
7	PORTG.2 /T0 /VREF	I/O I I	Bi-directional I/O port Shared with Timer0 external clock input Shared with external ADC VREF input
8	PORTG.3 /T2	I/O I	Shared with bi-directional I/O port in the internal or external RC oscillator Code option Shared with Timer2 external clock input
9	PORTC.0 /PLL_C	I/O I P	Bi-directional I/O port (selected by Code option) Vector port interrupt. (falling edge active) Built-in PLL Connect with External Capacitor
10	PORTC.1 /OSCO	I/O I O	Shared with bi-directional I/O port in the internal or external RC oscillator Code option Vector port interrupt. (falling edge active) Oscillator output pin, connect to crystal/ceramic oscillator.
11	PORTC.2 /OSCI	I/O I I	Shared with bi-directional I/O port in the internal RC Code option Vector port interrupt. (falling edge active) Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator.
12	$\overline{\text{RESET}}$ /PORTC.3	I I I/O	Reset pin input, (low active) Vector port interrupt. (falling edge active) Bi-directional I/O port (Open drain output and no pull high for input)
13	GND	P	Ground pin
14	VDD	P	Power supply pin
15	PORTA.0 /SEG0 /LED_S0 /KEY_I0	I/O O O I	Bi-directional I/O port SEG0 signal output for LCD display SEG0 signal output for LED display Input for automatic key scan

Pin Descriptions (For 28 pin) (continued)

Pin No.	Designation	I/O	Description
16	PORTA.1	I/O	Bi-directional I/O port
	/SEG1	O	SEG1 signal output for LCD display
	/LED_S1	O	SEG1 signal output for LED display
	/KEY_I1	I	Input for automatic key scan
17	PORTA.2	I/O	Bi-directional I/O port
	/SEG2	O	SEG2 signal output for LCD display
	/LED_S2	O	SEG2 signal output for LED display
	/KEY_I2	I	Input for automatic key scan
18	PORTA.3	I/O	Bi-directional I/O port
	/SEG3	O	SEG3 signal output for LCD display
	/LED_S3	O	SEG3 signal output for LED display
	/KEY_I3	I	Input for automatic key scan
19	PORTF.0	I/O	Bi-directional I/O port
	/SEG4	O	SEG4 signal output for LCD display
	/LED_S4	O	SEG4 signal output for LED display
	/KEY_I4	I	Input for automatic key scan
20	PORTF.1	I/O	Bi-directional I/O port
	/SEG5	O	SEG5 signal output for LCD display
	/LED_S5	O	SEG5 signal output for LED display
21	PORTE.0	I/O	Bi-directional I/O port
	/COM7	O	COM7 signal output for LCD display
	/SEG16	O	SEG16 signal output for LCD display
22	PORTE.1	I/O	Bi-directional I/O port
	/COM6	O	COM6 signal output for LCD display
	/SEG17	O	SEG17 signal output for LCD display
23	PORTE.2	I/O	Bi-directional I/O port
	/COM5	O	COM5 signal output for LCD display
	/SEG18	O	SEG18 signal output for LCD display
	/LED_C5	O	COM5 signal output for LED display
24	PORTE.3	I/O	Bi-directional I/O port
	/COM4	O	COM4 signal output for LCD display
	/SEG19	O	SEG19 signal output for LCD display
	/LED_C4	O	COM4 signal output for LED display
25	PORTD.0	I/O	Bi-directional I/O port
	/COM3	O	COM3 signal output for LCD display
	/LED_C3	O	COM3 signal output for LED display
	/KEY_O3	O	Output for automatic key scan
26	PORTD.1	I/O	Bi-directional I/O port
	/COM2	O	COM2 signal output for LCD display
	/LED_C2	O	COM2 signal output for LED display
	/KEY_O2	O	Output for automatic key scan

Pin Descriptions (For 28 pin) (continued)

Pin No.	Designation	I/O	Description
27	PORTD.2	I/O	Bi-directional I/O port
	/COM1	O	COM1 signal output for LCD display
	/LED_C1	O	COM1 signal output for LED display
	/KEY_O1	O	Output for automatic key scan
28	PORTD.3	I/O	Bi-directional I/O port
	/COM0	O	COM0 signal output for LCD display
	/LED_C0	O	COM0 signal output for LED display
	/KEY_O0	O	Output for automatic key scan

Pin Descriptions (For 32 pin)

Pin No.	Designation	I/O	Description
1	PORTB.0 /AN0	I/O I O	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input2
2	PORTB.1 /AN1	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input1
3	PORTB.2 /AN2	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input2
4	PORTB.3 /AN2	I/O I I	Bi-directional I/O port Vector port interrupt. (falling edge active) Shared with ADC input3
5	PORTG.0 /PWM	I/O O	Bi-directional I/O port Shared with PWM output
6	PORTG.1 /TONE	I/O O	Bi-directional I/O port Shared with TONE generator output
7	PORTG.2 /T0 /VREF	I/O I I	Bi-directional I/O port Shared with Timer0 external clock input Shared with external ADC VREF input
8	PORTG.3 /T2	I/O I	Shared with bi-directional I/O port in the internal or external RC oscillator Code option Shared with Timer2 external clock input
9	PORTC.0 /PLL_C	I/O I P	Bi-directional I/O port (selected by Code option) Vector port interrupt. (falling edge active) Built-in PLL Connect with External Capacitor
10	PORTC.1 /OSCO	I/O I O	Shared with bi-directional I/O port in the internal or external RC oscillator Code option Vector port interrupt. (falling edge active) Oscillator output pin, connect to crystal/ceramic oscillator.
11	PORTC.2 /OSCI	I/O I I	Shared with bi-directional I/O port in the internal RC Code option Vector port interrupt. (falling edge active) Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator.
12	$\overline{\text{RESET}}$ /PORTC.3	I I I/O	Reset pin input, (low active) Vector port interrupt. (falling edge active) Bi-directional I/O port
13	GND	P	Ground pin
14	VDD	P	Power supply pin
15	PORTA.0 /SEG0 /LED_S0 /KEY_I0	I/O O O I	Bi-directional I/O port SEG0 signal output for LCD display SEG0 signal output for LED display Input for automatic key scan

Pin Descriptions (For 32 pin) (continued)

Pin No.	Designation	I/O	Description
16	PORTA.1	I/O	Bi-directional I/O port
	/SEG1	O	SEG1 signal output for LCD display
	/LED_S1	O	SEG1 signal output for LED display
	/KEY_I1	I	Input for automatic key scan
17	PORTA.2	I/O	Bi-directional I/O port
	/SEG2	O	SEG2 signal output for LCD display
	/LED_S2	O	SEG2 signal output for LED display
	/KEY_I2	I	Input for automatic key scan
18	PORTA.3	I/O	Bi-directional I/O port
	/SEG3	O	SEG3 signal output for LCD display
	/LED_S3	O	SEG3 signal output for LED display
	/KEY_I3	I	Input for automatic key scan
19	PORTF.0	I/O	Bi-directional I/O port
	/SEG4	O	SEG4 signal output for LCD display
	/LED_S4	O	SEG4 signal output for LED display
	/KEY_I4	I	Input for automatic key scan
20	PORTF.1	I/O	Bi-directional I/O port
	/SEG5	O	SEG5 signal output for LCD display
	/LED_S5	O	SEG5 signal output for LED display
21	PORTF.2	I/O	Bi-directional I/O port
	/SEG6	O	SEG6 signal output for LCD display
	/LED_S6	O	SEG6 signal output for LED display
22	PORTF.3	I/O	Bi-directional I/O port
	/SEG7	O	SEG7 signal output for LCD display
	/LED_S7	O	SEG7 signal output for LED display
23	PORTH.2	I/O	Bi-directional I/O port
	/SEG14	O	SEG14 signal output for LCD display
24	PORTH.3	I/O	Bi-directional I/O port
	/SEG15	O	SEG15 signal output for LCD display
25	PORTE0	I/O	Bi-directional I/O port
	/COM7	O	COM7 signal output for LCD display
	/SEG16	O	SEG16 signal output for LCD display
26	PORTE.1	I/O	Bi-directional I/O port
	/COM6	O	COM6 signal output for LCD display
	/SEG17	O	SEG17 signal output for LCD display
27	PORTE.2	I/O	Bi-directional I/O port
	/COM5	O	COM5 signal output for LCD display
	/SEG18	O	SEG18 signal output for LCD display
	/LED_C5	O	COM5 signal output for LED display

Pin Descriptions (For 32 pin) (continued)

Pin No.	Designation	I/O	Description
28	PORTE.3	I/O	Bi-directional I/O port
	/COM4	O	COM4 signal output for LCD display
	/SEG19	O	SEG19 signal output for LCD display
	/LED_C4	O	COM4 signal output for LED display
29	PORTD.0	I/O	Bi-directional I/O port
	/COM3	O	COM3 signal output for LCD display
	/LED_C3	O	COM3 signal output for LED display
	/KEY_O3	O	Output for automatic key scan
30	PORTD.1	I/O	Bi-directional I/O port
	/COM2	O	COM2 signal output for LCD display
	/LED_C2	O	COM2 signal output for LED display
	/KEY_O2	O	Output for automatic key scan
31	PORTD.2	I/O	Bi-directional I/O port
	/COM1	O	COM1 signal output for LCD display
	/LED_C1	O	COM1 signal output for LED display
	/KEY_O1	O	Output for automatic key scan
32	PORTD.3	I/O	Bi-directional I/O port
	/COM0	O	COM0 signal output for LCD display
	/LED_C0	O	COM0 signal output for LED display
	/KEY_O0	O	Output for automatic key scan

Pin Descriptions (For 44 pin)

Pin No.	Designation	I/O	Description
1	PORTG.3 /T2	I/O I	Shared with bi-directional I/O port in the internal or external RC oscillator Code option Shared with Timer2 external clock input
2	PORTK.0	I/O	Bi-directional I/O port
3	PORTK.1	I/O	Bi-directional I/O port
4	PORTJ.0 /AN4	I/O I	Bi-directional I/O port Shared with ADC input4
5	PORTJ.1 /AN5	I/O I	Bi-directional I/O port Shared with ADC input5
6	PORTJ.2 /AN6	I/O I	Bi-directional I/O port Shared with ADC input6
7	PORTJ.3 /AN7	I/O I	Bi-directional I/O port Shared with ADC input7
8	PORTC.0 /PLL_C	I/O I P	Bi-directional I/O port (selected by Code option) Vector port interrupt. (falling edge active) Built-in PLL Connect with External Capacitor
9	PORTC.1 /OSCO	I/O I O	Shared with bi-directional I/O port in the internal or external RC oscillator Code option Vector port interrupt. (falling edge active) Oscillator output pin, connect to crystal/ceramic oscillator.
10	PORTC.2 /OSCI	I/O I I	Shared with bi-directional I/O port in the internal RC Code option Vector port interrupt. (falling edge active) Oscillator input pin, connect to crystal/ceramic oscillator or external resistor of external RC oscillator.
11	$\overline{\text{RESET}}$ /PORTC.3	I I I/O	Reset pin input, (low active) Vector port interrupt. (falling edge active) Bi-directional I/O port
12	GND	P	Ground pin
13	VDD	P	Power supply pin
14	PORTA.0 /SEG0 /LED_S0 /KEY_I0	I/O O O I	Bi-directional I/O port SEG0 signal output for LCD display SEG0 signal output for LED display Input for automatic key scan
15	PORTA.1 /SEG1 /LED_S1 /KEY_I1	I/O O O I	Bi-directional I/O port SEG1 signal output for LCD display SEG1 signal output for LED display Input for automatic key scan
16	PORTA2 /SEG2 /LED_S2 /KEY_I2	I/O O O I	Bi-directional I/O port SEG2 signal output for LCD display SEG2 signal output for LED display Input for automatic key scan

Pin Descriptions (For 44 pin) (continued)

Pin No.	Designation	I/O	Description
17	PORTA.3	I/O	Bi-directional I/O port
	/SEG3	O	SEG3 signal output for LCD display
	/LED_S3	O	SEG3 signal output for LED display
	/KEY_I3	I	Input for automatic key scan
18	PORTF.0	I/O	Bi-directional I/O port
	/SEG4	O	SEG4 signal output for LCD display
	/LED_S4	O	SEG4 signal output for LED display
	/KEY_I4	I	Input for automatic key scan
19	PORTF.1	I/O	Bi-directional I/O port
	/SEG5	O	SEG5 signal output for LCD display
	/LED_S5	O	SEG5 signal output for LED display
20	PORTF.2	I/O	Bi-directional I/O port
	/SEG6	O	SEG6 signal output for LCD display
	/LED_S6	O	SEG6 signal output for LED display
21	PORTF.3	I/O	Bi-directional I/O port
	/SEG7	O	SEG7 signal output for LCD display
	/LED_S7	O	SEG7 signal output for LED display
22	PORTI.0	I/O	Bi-directional I/O port
	/SEG8	O	SEG8 signal output for LCD display
23	PORTI.1	I/O	Bi-directional I/O port
	/SEG9	O	SEG9 signal output for LCD display
24	PORTI.2	I/O	Bi-directional I/O port
	/SEG10	O	SEG10 signal output for LCD display
25	PORTI.3	I/O	Bi-directional I/O port
	/SEG11	O	SEG11 signal output for LCD display
26	PORTH.0	I/O	Bi-directional I/O port
	/SEG12	O	SEG12 signal output for LCD display
27	PORTH.1	I/O	Bi-directional I/O port
	/SEG13	O	SEG13 signal output for LCD display
28	PORTH.2	I/O	Bi-directional I/O port
	/SEG14	O	SEG14 signal output for LCD display
29	PORTH.3	I/O	Bi-directional I/O port
	/SEG15	O	SEG15 signal output for LCD display
30	PORTE.0	I/O	Bi-directional I/O port
	/COM7	O	COM7 signal output for LCD display
	/SEG16	O	SEG16 signal output for LCD display
31	PORTE.1	I/O	Bi-directional I/O port
	/COM6	O	COM6 signal output for LCD display
	/SEG17	O	SEG17 signal output for LCD display
32	PORTE.2	I/O	Bi-directional I/O port
	/COM5	O	COM5 signal output for LCD display
	/SEG18	O	SEG18 signal output for LCD display
	/LED_C5	O	COM5 signal output for LED display

Pin Descriptions (For 44 pin) (continued)

Pin No.	Designation	I/O	Description
33	PORTE.3	I/O	Bi-directional I/O port
	/COM4	O	COM4 signal output for LCD display
	/SEG19	O	SEG19 signal output for LCD display
	/LED_C4	O	COM4 signal output for LED display
34	PORTD.0	I/O	Bi-directional I/O port
	/COM3	O	COM3 signal output for LCD display
	/LED_C3	O	COM3 signal output for LED display
	/KEY_O3	O	Output for automatic key scan
35	PORTD.1	I/O	Bi-directional I/O port
	/COM2	O	COM2 signal output for LCD display
	/LED_C2	O	COM2 signal output for LED display
	/KEY_O2	O	Output for automatic key scan
36	PORTD.2	I/O	Bi-directional I/O port
	/COM1	O	COM1 signal output for LCD display
	/LED_C1	O	COM1 signal output for LED display
	/KEY_O1	O	Output for automatic key scan
37	PORTD.3	I/O	Bi-directional I/O port
	/COM0	O	COM0 signal output for LCD display
	/LED_C0	O	COM0 signal output for LED display
	/KEY_O0	O	Output for automatic key scan
38	PORTB.0	I/O	Bi-directional I/O port
	/AN0	I	Vector port interrupt. (falling edge active)
		I	Shared with ADC input2
39	PORTB.1	I/O	Bi-directional I/O port
	/AN1	I	Vector port interrupt. (falling edge active)
		I	Shared with ADC input1
40	PORTB.2	I/O	Bi-directional I/O port
	/AN2	I	Vector port interrupt. (falling edge active)
		I	Shared with ADC input2
41	PORTB.3	I/O	Bi-directional I/O port
	/AN2	I	Vector port interrupt. (falling edge active)
		I	Shared with ADC input3
42	PORTG.0	I/O	Bi-directional I/O port
	/PWM	O	Shared with PWM output
43	PORTG.1	I/O	Bi-directional I/O port
	/TONE	O	Shared with TONE generator output
44	PORTG.2	I/O	Bi-directional I/O port
	/T0	I	Shared with Timer0 external clock input
	/VREF	I	Shared with external ADC VREF input

OTP Programming Pin Description (OTP Program Mode)

(44 pin QFP)

Pin No.	Symbol	I/O	Shared by	Description
13	VDD	P	VDD	Programming Power supply (+5.5V)
11	VPP	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11V)
12	GND	P	GND	Ground
10	SCK	I	OSCI	Programming Clock input pin
14	SDA	I/O	PORTA 0	Programming Data pin

(32 pin SDIP)

Pin No.	Symbol	I/O	Shared by	Description
14	VDD	P	VDD	Programming Power supply (+5.5V)
12	VPP	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11V)
13	GND	P	GND	Ground
11	SCK	I	OSCI	Programming Clock input pin
15	SDA	I/O	PORTA 0	Programming Data pin

(28 pin SKINNY)

Pin No.	Symbol	I/O	Shared by	Description
14	VDD	P	VDD	Programming Power supply (+5.5V)
12	VPP	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11V)
13	GND	P	GND	Ground
11	SCK	I	OSCI	Programming Clock input pin
15	SDA	I/O	PORTA 0	Programming Data pin

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

(a) PC

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0). The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.
The program counter cans only 4K program ROM address. (Refer to the ROM description).

(b) ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:
Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BC)
Logic Shift (SHR)
The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

(c) Accumulator

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

(d) Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) is placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

(e) Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

(f) Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:
The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. ROM

The SH69P55 can address 8192 X 16 bits of program area from $0000 to $1FFF. The Program Counter can only address a 4K program ROM. To address 8K size program ROM, use the bank switch.

(a) Vector Address Area ($0000 to $0004)

The program is sequentially executed. There is an area address $0000 through $0004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$0000	JMP Instruction	Jump to RESET service routine
$0001	JMP Instruction	Jump to TIMER0 interrupt service routine
$0002	JMP Instruction	Jump to TIMER1 interrupt service routine
$0003	JMP Instruction	Jump to TIMER2 interrupt service routine
$0004	JMP Instruction	Jump to external interrupts service routine

*JMP instruction can be replaced by any instruction.

Bank Switch Mapping

The Program Counter (PC11 - PC0) can only address 4K ROM space. The Bank switch technique is used to extend the CPU address space. The lower 2K of the CPU addressing space maps to the lower 2K of ROM space (BANK0). The upper 2K of the CPU addressing space maps to one of the three banks (BNK 0, 1,2) of the upper 6K of ROM. (According to the Bank Register $1F)

The bank switch mapping is as follows:

CPU Address	ROM Space, BNK = 0	ROM Space, BNK = 1	ROM Space, BNK = 2
000 -7FF	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)	0000 - 07FF (BANK 0)
800 - FFF	0800 - 0FFF (BANK 1)	1000 - 17FF (BANK 2)	1800 - 1FFF (BANK 3)

(b) Table Data Reference

Table Data can be stored in the program memory and can be referenced by using the Table Branch (TJMP) and the Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) are placed by an offset address in the program ROM. The TJMP instruction branch is placed into address ((PC11 - PC8) X (28) + (TBR, A)). The address is determined by RTNW to return the look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

3. RAM

Built-in RAM contains of general-purpose data memory and system register.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

$000 - $02F: $380 - $3AF System register and I/O

$030 - $1A7: Data memory (376 X 4 bits)

$300 - $313, $320 - $333: LCD display (40 X 4 bits)

$314 - $319, $334 - $339: LED display (12 X 4 bits)

(b) Data Memory

Data memory is organized as 416 X 4 bits. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

(c) Configuration of System Register:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IET0	IET1	IET2	IEEX	R/W	Interrupt enable flags
$01	IRQT0	IRQT1	IRQT2	IRQEX	R/W	Interrupt request flags
$02	T0S	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register
$03	T0E	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load / counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load / counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load / counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load / counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: A/D port configuration control Bit3: Select Internal/External reference voltage
$14	ADCON	CH2	CH1	CH0	R/W	Bit2-0: Select ADC channel Bit3: Set ADC module operate
$15	T2E	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 pre-scaler register Bit3: T2 external signal edge select
$16	FS1	FS0	OXS	OXON	R/W	Bit0: Turn on PLL Bit1: System select (1: PLL, 0: 32.768kHz) Bit3~2:PLL Frequency select
$17	LVR	-	-	SCF	R/W	Bit3: Low Voltage Reset flag (Read and Write 0 only) Bit0: System clock fail flag(Read and Write 0 only)
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	R/W	PORTF input/output control
$1E	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
$1F	-	-	BNK1	BNK0	R/W	Bit1-0: Bank register for ROM
$20	PWMS	TCK1	TCK0	PWM_EN	R/W	Bit0: Set PWM0 Enable Bit2, Bit1: Select PWM0 clock Bit3: Set PWM0 output mode of duty cycle

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PP.3	PP.2	PP.1	PP.0	R/W	PWM period low nibble
$22	PP.7	PP.6	PP.5	PP.4	R/W	PWM period high nibble
$23	-	FSTP	FSR1	FSR0	R/W	Bit1~0: select external frequency of system clock Bit2: 32.768kHz is closed in the stop
$24	-	-	PDF.1	PDF.0	R/W	PWM duty low nibble
$25	PD.5	PD.4	PD.3	PD.2	R/W	PWM duty middle nibble
$26	PD.9	PD.8	PD.7	PD.6	R/W	PWM duty high nibble
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select Bit2: Select directive edge active enable Bit3: Set Timer2 function start
$28	KeyNUM1	KeyNUM0	KeyEND	KeyEN	R/W R R	Bit0: enable key scanner Bit1: one key scan end Bit3~2: key number0, 1
$29	LCDON	DUTY2	DUTY1	DUTY0	R/W	Bit2-0: Set duty and com Bit3: Turn on LCD
$2A	-	-	-	-	R/W	Reserved
$2B	LEDEN	LEDON	EDUTY1	EDUTY0	R/W	Bit1-0: Set duty Bit2: Turn on LED driver Bit3: Enable LED driver
$2C	KeyC3	KeyC2	KeyC1	KeyC0	R	Bit3~0: the result of key scan on KEY_O3~0
$2D	KeyL3	KeyL2	KeyL1	KeyL0	R	Bit3~0: the result of key scan on KEY_I4~0
$2E	RLCD	Ps2	Ps1	Ps0	R/W	Bit2~0: Configuration the segment Bit3:set LCD driver bias resistor
$2F	GO/$\overline{\text{DONE}}$	TADC1	TADC0	-	R/W	Bit2, Bit1: Select A/D Clock Period Bit3: ADC status flag
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address / data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address / data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address / data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address / data register
$384	T2D.3	T2D.2	T2D.1	T2D.0	R/W	Timer2 load / counter register (low nibble)
$385	T2D.7	T2D.6	T2D.5	T2D.4	R/W	Timer2 load / counter register (middle_L nibble)
$386	T2D.11	T2D.10	T2D.9	T2D.8	R/W	Timer2 load / counter register (middle_H nibble)
$387	T2D.15	T2D.14	T2D.13	T2D.12	R/W	Timer2 load / counter register (high nibble)
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags
$389	PBIF.3	PBIF.2	PBGIF.1	PBIF.0	R/W	PORTB interrupt request flags
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	R/W	PORTC interrupt enable flags
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	R/W	PORTC interrupt request flags
$38C	-	-	KEYIE	ADIE	R/W	Bit0: AD interrupt enable flag Bit1: Key scan interrupt enable flag
$38D	-	-	KEYIF	ADIF	R/W	Bit0: AD interrupt request flag Bit1: Key scan interrupt request flag
$38E	PG.3	PG.2	PG.1	PG.0	R/W	PORTG
$38F	PH.3	PH.2	PH.1	PH.0	R/W	PORTH
$390	PI.3	PI.2	PI.1	PI.0	R/W	PORTI
$391	PJ.3	PJ.2	PJ.1	PJ.0	R/W	PORTJ

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$392	-	-	PK.1	PK.0	R/W	PORTK
$393	PGCR.3	PGCR.2	PGCR.1	PGCR.0	R/W	PORTG input/output control
$394	PHCR.3	PHCR.2	PHCR.1	PHCR.0	R/W	PORTH input/output control
$395	PICR.3	PICR.2	PICR.1	PICR.0	R/W	PORTI input/output control
$396	PJCR.3	PJCR.2	PJCR.1	PJCR.0	R/W	PORTJ input/output control
$397	-	-	PKCR.1	PKCR.0	R/W	PORTK input/output control
$398	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull high control
$399	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull high control
$39A	-	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull high control
$39B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull high control
$39C	PPECR.3	PPECR.2	PPECR.1	PPECR.0	R/W	PORTE pull high control
$39D	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	R/W	PORTF pull high control
$39E	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	R/W	PORTG pull high control
$39F	PPHCR.3	PPHCR.2	PPHCR.1	PPHCR.0	R/W	PORTH pull high control
$3A0	PPICR.3	PPICR.2	PPICR.1	PPICR.0	R/W	PORTI pull high control
$3A1	PPJCR.3	PPJCR.2	PPJCR.1	PPJCR.0	R/W	PORTJ pull high control
$3A2	-	-	PPKCR.1	PPKCR.0	R/W	PORTK pull high control
$3A3	TG1.3	TG1.2	TG1.1	TG1.0	R/W	Tone generator 1 low nibble
$3A4	TG1.7	TG1.6	TG1.5	TG1.4	R/W	Tone generator 1 middle nibble
$3A5	TG1.11	TG1.10	TG1.9	TG1.8	R/W	Tone generator 1 high nibble
$3A6	TG2.3	TG2.2	TG2.1	TG2.0	R/W	Tone generator 2 low nibble
$3A7	TG2.7	TG2.6	TG2.5	TG2.4	R/W	Tone generator 2 middle nibble
$3A8	TG2.11	TG2.10	TG2.9	TG2.8	R/W	Tone generator 2 high nibble
$3A9	TV1.3	TV1.2	TV1.1	TV1.0	R/W	Tone generator 1 volume low nibble
$3AA	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Tone generator 1 volume high nibble TG1EN: Tone generator 1 enable
$3AB	TV2.3	TV2.2	TV2.1	TV2.0	R/W	Tone generator 2 volume low nibble
$3AC	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Tone generator 2 volume high nibble TG2EN: Tone generator 2 enable
$3AD	-	-	A1	A0	R	ADC data low nibble (Read only)
$3AE	A5	A4	A3	A2	R	ADC data middle nibble (Read only)
$3AF	A9	A8	A7	A6	R	ADC data high nibble (Read only)

4. Initial state

(a) System Register state:

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset	WDT Reset / Low Voltage Reset
$00	IET0	IET1	IET2	IEEX	0000	0000
$01	IRQT0	IRQT1	IRQT2	IRQEX	0000	0000
$02	T0S	T0M.2	T0M.1	T0M.0	0000	uuuu
$03	T0E	T1M.2	T1M.1	T1M.0	0000	uuuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	PF.3	PF.2	PF.1	PF.0	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	VREFS	ACR2	ACR1	ACR0	0000	uuuu
$14	ADCON	CH2	CH1	CH0	0000	0uuu
$15	T2E	T2SC.2	T2SC.1	T2SC.0	0000	uuuu
$16	FS1	FS0	OXS	OXON	0000	uuuu
$17	LVR	-	-	SCF	0--0	*--u
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1D	PFCR.3	PFCR.2	PFCR.1	PFCR.0	0000	0000
$1E	WD	WDT.2	WDT.1	WDT.0	0000	#000
$1F	-	-	BNK1	BNK0	--00	--00
$20	PWMS	TCK1	TCK0	PWM_EN	0000	uuu0
$21	PP.3	PP.2	PP.1	PP.0	xxxx	uuuu
$22	PP.7	PP.6	PP.5	PP.4	xxxx	uuuu

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset	WDT Reset / Low Voltage Reset
$23	-	FSTP	FS1	FS0	-000	-000
$24			PDF.1	PDF.0	--xx	--uu
$25	PD.5	PD.4	PD.3	PD.2	xxxx	uuuu
$26	PD.9	PD.8	PD.7	PD.6	xxxx	uuuu
$27	T2GO	DEC	TM2S1	TM2S0	0000	0uuu
$28	KeyNUM1	KeyNUM0	KeyEND	KeyEN	0000	000u
$29	LCDON	DUTY2	DUTY1	DUTY0	0000	uuuu
$2A	-	-	-	-	----	----
$2B	LEDEN	LEDON	EDUTY1	EDUTY0	0000	uuuu
$2C	KeyC3	KeyC2	KeyC1	KeyC0	0000	uuuu
$2D	KeyL3	KeyL2	KeyL1	KeyL0	0000	uuuu
$2E	RLCD	Ps2	Ps1	Ps0	0000	uuuu
$2F	GO/$\overline{\text{DONE}}$	TADC1	TADC0	-	000-	0uu-
$380	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$381	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$382	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$383	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu
$384	T2D.3	T2D.2	T2D.1	T2D.0	xxxx	xxxx
$385	T2D.7	T2D.6	T2D.5	T2D.4	xxxx	xxxx
$386	T2D.11	T2D.10	T2D.9	T2D.8	xxxx	xxxx
$387	T2D.15	T2D.14	T2D.13	T2D.12	xxxx	xxxx
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	0000	0000
$389	PBIF.3	PBIF.2	PBIF.1	PBIF.0	0000	0000
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	0000	0000
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	0000	0000
$38C	-		KEYIE	ADIE	--00	--00
$38D	-	-	KEYIF	ADIF	--00	--00
$38E	PG.3	PG.2	PG.1	PG.0	0000	0000
$38F	PH.3	PH.2	PH.1	PH.0	0000	0000
$390	PI.3	PI.2	PI.1	PI.0	0000	0000
$391	PJ.3	PJ.2	PJ.1	PJ.0	0000	0000
$392	-	-	PK.1	PK.0	--00	--00
$393	PGCR.3	PGCR.2	PGCR.1	PGCR.0	0000	0000
$394	PHCR.3	PHCR.2	PHCR.1	PHCR.0	0000	0000
$395	PICR.3	PICR.2	PICR.1	PICR.0	0000	0000
$396	PJCR.3	PJCR.2	PJCR.1	PJCR.0	0000	0000
$397	-	-	PKCR.1	PKCR.0	--00	--00

	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset	WDT Reset / Low Voltage Reset
$398	PPACR.3	PPACR.2	PPACR.1	PPACR.0	0000	0000
$399	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	0000	0000
$39A	-	PPCCR.2	PPCCR.1	PPCCR.0	-000	-000
$39B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	0000	0000
$39C	PPECR.3	PPECR.2	PPECR.1	PPECR.0	0000	0000
$39D	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	0000	0000
$39E	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	0000	0000
$39F	PPHCR.3	PPHCR.2	PPHCR.1	PPHCR.0	0000	0000
$3A0	PPICR.3	PPICR.2	PPICR.1	PPICR.0	0000	0000
$3A1	PPJCR.3	PPJCR.2	PPJCR.1	PPJCR.0	0-00	0-00
$3A2			PPKCR.1	PPKCR.0	--00	--00
$3A3	TG1.3	TG1.2	TG1.1	TG1.0	xxxx	uuuu
$3A4	TG1.7	TG1.6	TG1.5	TG1.4	xxxx	uuuu
$3A5	TG1.11	TG1.10	TG1.9	TG1.8	xxxx	uuuu
$3A6	TG2.3	TG2.2	TG2.1	TG2.0	xxxx	uuuu
$3A7	TG2.7	TG2.6	TG2.5	TG2.4	xxxx	uuuu
$3A8	TG2.11	TG2.10	TG2.9	TG2.8	xxxx	uuuu
$3A9	TV1.3	TV1.2	TV1.1	TV1.0	xxxx	uuuu
$3AA	TG1EN	TV1.6	TV1.5	TV1.4	xxxx	uuuu
$3AB	TV2.3	TV2.2	TV2.1	TV2.0	xxxx	uuuu
$3AC	TG2EN	TV2.6	TV2.5	TV2.4	xxxx	uuuu
$3AD	-	-	A1	A0	--xx	--uu
$3AE	A5	A4	A3	A2	xxxx	uuuu
$3AF	A9	A8	A7	A6	xxxx	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

*, #: For the detail information, refer to the following table:

	WDT reset	LVR reset	WDT reset & LVR reset	Power on reset /Pin reset
*	0	1	1	0
#	1	0	1	0

Others initial state:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

SH69P55 has one clock source, which is determined in Code options. The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals. A phase locked loop (PLL) is built-in SH69P55, which can provide up to 8MHz oscillator clock when the 32.768kHz oscillator is selected. PLL control register can decide whether PLL enable or disable. When PLL is enabled, PORTC0 is shared as PLL capacitor connect port, which is connected with a capacitor; when PLL is disabled, PORTC0 is shared as a normal I/O.

PLL control register ($) 16

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	FS1	FS0	OXS	OXON	R/W	Bit0: Turn on PLL Bit1: System select (1: PLL, 0: 32.768kHz) Bit3~2:PLL Frequency select
	X	X	X	0	R/W	Turn off PLL
	X	X	X	1	R/W	Turn on PLL, when 32.768kHz is selected in Code option
	X	X	0	X	R/W	System clock is selected as 32.768kHz
	X	X	1	1	R/W	System clock is selected as PLL
	0	0	1	1	R/W	PLL provides 8MHz clock signal for system clock, if LVR voltage range is not selected as 2.5V in the Code option.
	0	1	1	1	R/W	PLL provides 4MHz clock signal for system clock
	1	0	1	1	R/W	PLL provides 2MHz clock signal for system clock
	1	1	1	1	R/W	PLL provides 1MHz clock signal for system clock

Note:

1.Usage of PLL:

First, config the FS1 and FS0 in PLL control register

Second, set OXON=1 and turn on the PLL

Third, wait at least 2ms

Last, set OXS=1 and select PLL as the system clock source.

2.If LVR voltage range is selected as 2.5V in the Code option, the PLL can not provide 8MHZ clock signal for system clock.

If the 32.768kHz is not selected in the Code option, the following Frequency select register is must be set at the begin of the program. If the 32.768kHz is selected in the Code option, the following Frequency selection is invalid.

External Frequency select register $23

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$23	-	FSTP	FSR1	FSR0	R/W	Bit1~0: select external frequency of system clock Bit2: 32.768kHz is closed in the stop
	X	X	0	0	R/W	4MHz<System clock≦8MHz exclude internal RC, if 32.768kHz is not selected in the Code option
	X	X	0	1	R/W	2MHz<System clock≦4MHz exclude internal RC, if 32.768kHz is not selected in the Code option
	X	X	1	0	R/W	1MHz<System clock≦2MHz exclude internal RC, if 32.768kHz is not selected in the Code option
	X	X	1	1	R/W	400kHz<System clock≦1MHz exclude internal RC, if 32.768kHz is not selected in the Code option
	X	1	X	X	R/W	32.768kHz is closed in the stop, if 32.768kHz is selected in the Code option
	X	0	X	X	R/W	32.768kHz is not closed in the stop, if 32.768kHz is selected in the Code option

System clock = $F_{OSC}/4$.

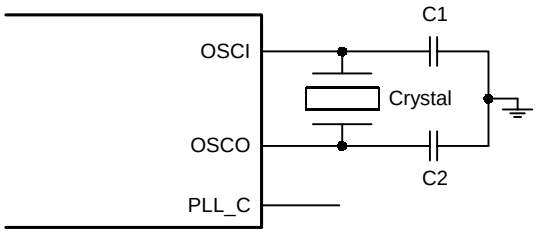
(a) Instruction cycle time:

(1) 4/32768Hz (≈122.1μs) for 32768Hz oscillator.

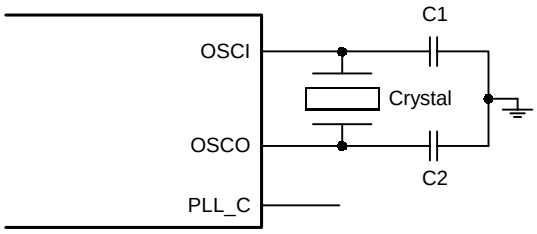
(2) 4/8MHz (=0.5μs) for 8 MHz oscillator.

(b) Oscillator type

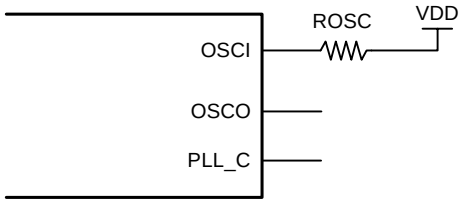
(1) Crystal oscillator: 32.768kHz or 400kHz ~ 8MHz



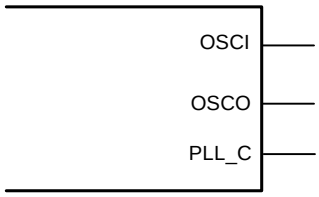
(2) Ceramic resonator: 400kHz ~ 8MHz



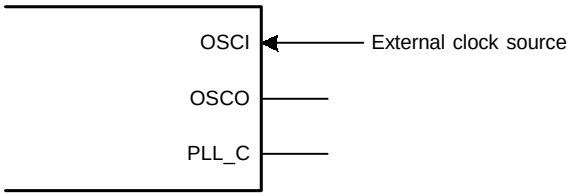
(3) External RC oscillator: 400kHz - 8MHz



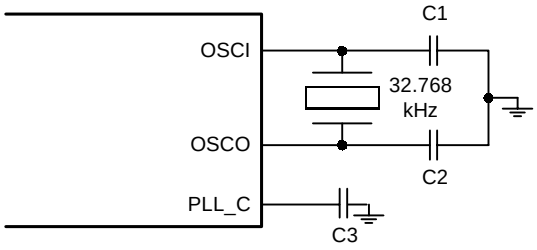
(4) Internal RC oscillator: 4MHz



(5) External input clock: 30kHz ~ 8MHz



(6) PLL enable



Note:

- If the RC oscillator or the external input clock is selected, OSCO pin is used as the I/O port (PORTC1).
- If the internal RC oscillator is selected, OSCO pin is used as the I/O port (PORTC1) as well as OSCI pin is used as the PORTC2.
- If the PLL is disabled, PLL_C is used as the I/O port (PORTC0).

6. I/O Port

The SH69P55 provides 42 programmable bi-directional I/O ports including one open-drain output. Each I/O port contains pull high MOS controllable by the program except PortC3. Each pull high MOS is controlled by the value of the corresponding bit in the port pull high control register (PPCR), independently. When the port is selected as an input port (Write 1 to the relevant bit in the port pull high control register (PPCR) could turn on the pull high MOS and write 0 could turn off the pull high MOS). So the pull high MOS can be turned on and off individually. But when the port is selected as output port, the pull high MOS must be turned off automatically, regardless the value of the corresponding bit in the port pull high control register (PPCR). When PORTB and PORTC are selected as the digital input direction, they can active port interrupt by falling edge (if port interrupt is enabled).

PORTA0~PORTA3 can be shared with SEG0~SEG3 signal output for LCD or LED display, KEY_I0~KEY_I3 input for automatic key scan.
PORTB0~PORTB3 can be shared with ADC AN0~3 input channel
PORTC0 can be shared with PLL_C (Code option), if PLL is enabled, a capacitor must be connected with this port.
PORTC1 can be shared with OSCO (if used External clock or RC oscillator, Code option)
PORTC2 can be shared with OSCI (if used Internal RC oscillator, Code option)
PORTC3 can be shared with RESET input (Code option), it with open drain output and without pull high resistor for input
PORTD0~PORTD3 can be shared with COM3~COM0 signal output for LCD or LED display, KEY_O3~0 output for automatic key scan.
PORTE0~PORTE3 can be shared with COM7~COM4 or SEG19~SEG16 signal output for LCD display, COM4~COM5 signal output for LED display
PORTF0~PORTF3 can be shared with SEG4~SEG7 signal output for LCD or LED display, and PORTF0 can be shared with KEY_I4 input for automatic key scan.
PORTG0 can be shared with PWM output
PORTG1 can be shared with TONE output
PORTG2 can be shared with T0 input or external ADC VREF input
PORTG3 can be shared with T2 input
PORTH0~PORTH3 can be shared with SEG12~SEG15 signal output for LCD display
PORTI0~PORTI3 can be shared with SEG8~SEG11 signal output for LCD display
PORTJ0~PORTJ3 can be shared with ADC AN4~7 input channel

Port Data Register (PDR): $08 ~ $0D, $38E ~ $392

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA	0000
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB	0000
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC	0000
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD	0000
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE	0000
$0D	PF.3	PF.2	PF.1	PF.0	R/W	PORTF	0000
$38E	PG.3	PG.2	PG.1	PG.0	R/W	PORTG	0000
$38F	PH.3	PH.2	PH.1	PH.0	R/W	PORTH	0000
$390	PI.3	PI.2	PI.1	PI.0	R/W	PORTI	0000
$391	PJ.3	PJ.2	PJ.1	PJ.0	R/W	PORTJ	0000
$392	-	-	PK.1	PK.0	R/W	PORTK	--00

Port Control Register (PCR): $16 ~ $1B, $393 ~ $397

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$18	PA3OUT	PA2OUT	PA1OUT	PA0OUT	R/W	PORTA input/output control	0000
$19	PB3OUT	PB2OUT	PB1OUT	PB0OUT	R/W	PORTB input/output control	0000
$1A	PC3OUT	PC2OUT	PC1OUT	PC0OUT	R/W	PORTC input/output control	0000
$1B	PD3OUT	PD2OUT	PD1OUT	PD0OUT	R/W	PORTD input/output control	0000
$1C	PE3OUT	PE2OUT	PE1OUT	PE0OUT	R/W	PORTE input/output control	0000
$1D	PF3OUT	PF3OUT	PF1OUT	PF0OUT	R/W	PORTF input/output control	0000
$393	PG3OUT	PG2OUT	PG1OUT	PG0OUT	R/W	PORTG input/output control	0000
$394	PH3OUT	PH2OUT	PH1OUT	PH0OUT	R/W	PORTH input/output control	0000
$395	PI3OUT	PI2OUT	PI1OUT	PI0OUT	R/W	PORTI input/output control	0000
$396	PJ3OUT	PJ3OUT	PJ1OUT	PJ0OUT	R/W	PORTJ input/output control	0000
$397	-	-	PK1OUT	PK0OUT	R/W	PORTK input/output control	--00

I/O control register:

PA(/B/C/D/E/F/G/H/I/J)CR.n, (n = 0, 1, 2, 3), PKCR.n (n=0,1)

0: Set I/O as an input direction. (Default)

1: Set I/O as an output direction.

Port Pull high Control Register (PPCR): $398 ~ $3A2

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks	Power On
$398	PPACR.3	PPACR.2	PPACR.1	PPACR.0	R/W	PORTA pull high control	0000
$399	PPBCR.3	PPBCR.2	PPBCR.1	PPBCR.0	R/W	PORTB pull high control	0000
$39A	-	PPCCR.2	PPCCR.1	PPCCR.0	R/W	PORTC pull high control	-000
$39B	PPDCR.3	PPDCR.2	PPDCR.1	PPDCR.0	R/W	PORTD pull high control	0000
$39C	PPECR.3	PPECR.2	PPECR.1	PPECR.0	R/W	PORTE pull high control	0000
$39D	PPFCR.3	PPFCR.2	PPFCR.1	PPFCR.0	R/W	PORTF pull high control	0000
$39E	PPGCR.3	PPGCR.2	PPGCR.1	PPGCR.0	R/W	PORTG pull high control	0000
$39F	PPHCR.3	PPHCR.2	PPHCR.1	PPHCR.0	R/W	PORTH pull high control	0000
$3A0	PPICR.3	PPICR.2	PPICR.1	PPICR.0	R/W	PORTI pull high control	0000
$3A1	PPJCR.3	PPJCR.2	PPJCR.1	PPJCR.0	R/W	PORTJ pull high control	0-00
$3A2	-	-	PPKCR.1	PPKCR.0	R/W	PORTK pull high control	--00

0: Disable internal pull high MOS. (Default)

1: Enable internal pull high MOS.

In SH69P55, each output port contains a latch, which can hold the output data. Writing the port data register (PDR) under the output mode can directly transfers data to the corresponding pad. All input ports do not have latches, so the external input data should be held externally until the input data is read from outside or reading the port data register (PDR) under the input mode should be performed several times before the available processing. The contents of the port control register (PCR) determine each bi-directional I/O port to be either an input or output, where writing 0 to PCR registers represents the input mode and 1 for the output mode. When a digital I/O port is selected to be an output, the reading of the associated port bit actually represents the value of the output data latch, not the voltage on the pad. When a digital I/O port is selected to be input, the reading of the associated port bit represents the status on the corresponding pad. The output data latch can always be written, regardless of the state of the port control register (PCR). Therefore, when using ports in a mixture of input and output modes, the contents of the output latches for those ports that are selected as inputs may be rewritten by execution of logical instructions. So it is strongly recommended that writing proper data to the port data register (PDR) before changing the corresponding bits in the port control register (PCR) from the input mode to the output mode can avoid glitches on the relevant pads.

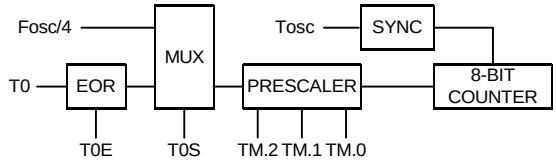
7. Timer

SH69P55 has three timers: two 8-bit timers (Tiemr0, Tiemr1) and one 16-bit timer (Timer2).

The Timer0/Tiemr1 has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified Timer0/Timer1 block diagram.



The Timer0/Timer1 provides the following functions:

- Programmable interval timer function.
- Read counter value.

(a) Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

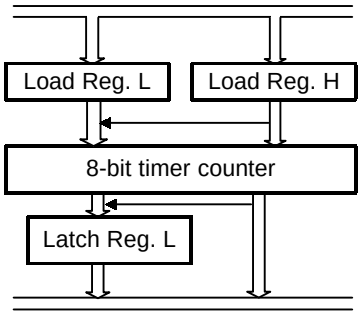
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



(b) Timer0/Timer1 Mode Register

The Timer0/Timer1 can be programmed in several different prescaler by setting Timer Mode register (TM0, TM1).
The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 3-bit registers used for the timer control as shown in Table 1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1 Timer0 Mode Register ($02)

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

Table 2 Timer1 Mode Register ($03)

T1M.2	T1M.1	T1M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

(b) External Clock/Event T0 as Timer0 Source

When external clock/event T0 input (shared with PORTG2) as Timer0 source, it is synchronized with the CPU system clock (OSC clock/4). The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t_{OSC}) and low (at least 2 t_{OSC}). When the prescaler ratio selects /2^0, it is the same as the system clock input.

The requirement is as follows

T0H (T0 high time) $\geq 2 * t_{OSC} + \Delta T$

T0L (T0 low time) $\geq 2 * t_{OSC} + \Delta T$; ΔT= 20ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$T0\,\text{high time} = T0\,\text{low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period

N = prescaler value (2^0, 2^1, 2^2, 2^3, 2^5, 2^7, 2^9, 2^{11})

The requirement is:

$$\frac{N * T0}{2} \geq 2 * tosc + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

Timer0 Mode Register: $02

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02	T0S				R/W	Bit3: T0 signal source
	0	X	X	X	R/W	Shared with PortG2, Timer0 source is system clock
	1	X	X	X	R/W	Shared with T0 input, Timer0 source is T0 input clock

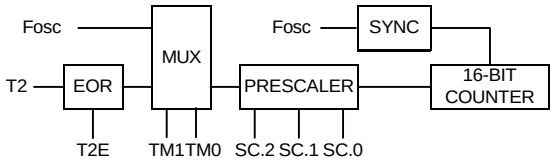
Timer1 Mode Register: $03

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$03	T0E				R/W	Bit3: T0 signal edge
	0	X	X	X	R/W	Falling edge active
	1	X	X	X	R/W	Rising edge active

Timer2 is a 16-bit timer, and it has the following features:

- 16-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FFFF to $0000.

The following is a simplified Timer2 block diagram.



The Timer2 provides the following functions:

- Programmable interval timer function.
- Read counter value.

(a) Timer2 Configuration and Operation

Timer2 consists of a 16-bit write-only timer load register (TL2L, TL2ML, TL2MH, TL2H) and a 16-bit read-only timer counter (TC2L, TC2ML, TC2MH, TC2H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL2L, TL2ML, TL2MH, TL2H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or the counter counts overflow from $FFFF to $0000.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Please follow these steps:

Write Operation:

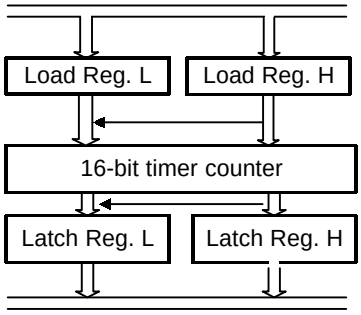
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



(b) Timer2 Control Register

The Timer2 can be programmed in several different modes: timer, external event counter, external trigger timer and pulse width measurement.

Timer2 Control Register: $27

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select Bit2: Select directive edge active enable Bit3: Set Timer2 function start
	X	X	0	0	R/W	Timer with internal system clock
	X	X	0	1	R/W	Event counter with external clock (T2 pin input)
	X	X	1	0	R/W	Timer with external trigger (T2 pin input)
	X	X	1	1	R/W	Pulse width measurement (T2 pin input)
	0	X	X	X	R/W	Timer/counter stops (Read: status; Write: command) (default)
	1	X	X	X	R/W	Timer/counter starts (Read: status; Write: command)

(1) Timer mode

In this mode, Timer2 is performed using the internal clock. The contents of the Timer2 counter register ($384 ~ $387) are loaded into the up-counter while the highest nibble ($387) has been written. The up-counter will start counting if the T2GO (bit3) in the Timer2 control register ($27) is set to 1. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) bit1 (IET2) is set to 1.

After the T2GO (bit3) in the Timer2 control register ($27) has been set to 1, writing the Timer2 counter register ($384 ~ $387) can not affect the up-counter operating anymore. Only when the T2GO (bit3) in the Timer2 control register ($27) has been reset to 0, the revised contents of the Timer2 counter register ($384 ~ $387) will be loaded into the up-counter while the highest nibble ($387) is written.

Timer2 Pre-scaler Register: $15

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	T2E	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 pre-scaler register Bit3: T2 external signal edge select
	X	0	0	0	R/W	Timer clock: OSC clock / 2^{13}
	X	0	0	1	R/W	Timer clock: OSC clock / 2^{11}
	X	0	1	0	R/W	Timer clock: OSC clock / 2^{9}
	X	0	1	1	R/W	Timer clock: OSC clock / 2^{7}
	X	1	0	0	R/W	Timer clock: OSC clock / 2^{5}
	X	1	0	1	R/W	Timer clock: OSC clock / 2^{4}
	X	1	1	0	R/W	Timer clock: OSC clock / 2^{3}
	X	1	1	1	R/W	Timer clock: OSC clock / 2^{2}
	0	X	X	X	R/W	T2 input falling edge active (Default)
	1	X	X	X	R/W	T2 input rising edge active

(2) External event counter mode

In this mode, Timer2 is performed using the external clock via T2 pin (shared with PORTG3). The external events are counted at the edge of the T2 pin. Either the rising or falling edge can be selected with the external trigger controlled by the status of the T2E (bit3) in the Timer1 pre-scaler register ($15). The contents of the Timer2 counter register ($384 ~ $387) are loaded into the up-counter while the highest nibble ($387) has been written. The up-counter will start counting if the T2GO (bit3) in the Timer2 control register ($27) is set to 1. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) bit1 (IET2) is set to 1.

After the T2GO (bit3) in the Timer1 control register ($27) has been set to 1, writing the Timer2 counter register ($384 ~ $387) can not affect the up-counter operating anymore. Only when the T2GO (bit3) in the Timer2 control register ($27) has been reset to 0, the revised contents of the Timer2 counter register ($384 ~ $387) will be loaded into the up-counter while the highest nibble ($387) is written.

The external clock source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 tOSC) and low (at least 2 tOSC). In this mode, the pre-scaler circuit will not affect the external clock input. That means the input clock will bypass the pre-scaler circuit, regardless the real value written by programming. So, the limitation is applied for the T2 period time described as follows:

$$T1 \text{ (period time)} \geq 4 * t_{OSC} + 2 * \Delta T \quad ; \Delta T = 20ns$$

(3) External trigger timer mode

In this mode, the counting is triggered by an external signal. This trigger is the edge of the T2 pin input. Either the rising or falling edge can be selected by setting the T2E (bit3) in the Timer2 pre-scaler register ($25). But the source clock of the up-counter is an internal clock. The contents of the Timer2 counter register ($384 ~ $387) are loaded into the up-counter while the highest nibble ($387) has been written. Only after the T2GO (bit3) in the Timer2 control register ($27) has been set to 1, a proper edge signal on the T2 input pin can start counting. The Timer2 interrupt will issue when the up-counter overflows from $FFFF to $0000 if the Interrupt enable register ($00) bit1 (IET1) is set to 1. When the Timer2 interrupt is generated the up-counter is halted. The up-counter is restarted by the next selected edge of the T2 pin input.

When DEC (bit2) in the Timer2 control register ($27) is 1, inputting the edge to the reverse direction of the trigger edge selected by the former programming to start counting stops the operating and then re-load contents from the Timer2 counter register ($384 ~ $387). Inputting a proper constant pulse width can generate interrupts. When DEC (bit2) in the Timer2 control register ($27) is 0, the reverse directive edge input is ignored. The T2 pin input another active edge before the up-counter overflowing is also ignored.

After the T2GO (bit3) in the Timer2 control register ($27) has been set to 1, writing the Timer2 counter register ($384 ~ $387) can not affect the up-counter operating anymore. Only when the T2GO (bit3) in the Timer2 control register ($27) has been reset to 0, the revised contents of the Timer2 counter register ($384 ~ $387) will be loaded into the up-counter while the highest nibble ($387) is written.

The T2 pin input signal must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 1/2 tTimer clock) and low (at least 1/2 tTimer clock). In this mode, the real value of the Timer clock is selected by the state in the Timer2 pre-scaler register. So, the limitation is applied for the T2 period time described as follows:

$$T1 \text{ (period time)} \geq 1 * t_{Timer\ clock} + 2 * \Delta T \quad ; \Delta T = 20ns$$

$$T1 \text{ (period time)} \geq (M * t_{OSC}) + 2 * \Delta T$$

where M=2^3, 2^4, 2^5, 2^6, 2^8, 2^{10}, 2^{12}or 2^{14}

Timer2 Control Register: $27 (under the external trigger timer mode)

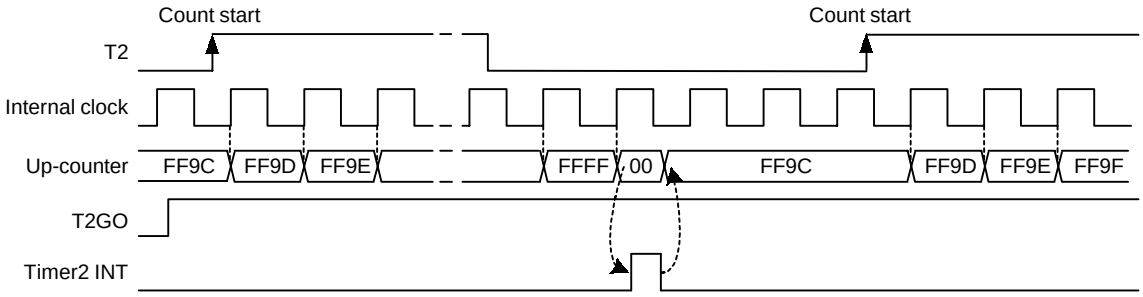
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select
	X	0	1	0	R/W	Bit2: Reverse directive edge input is ignored.
	X	1	1	0	R/W	Bit2: Reverse directive edge input reloads internal up-counter.

Timer2 Pre-scaler Register: $15 (under the external trigger timer mode and pulse width measurement mode)

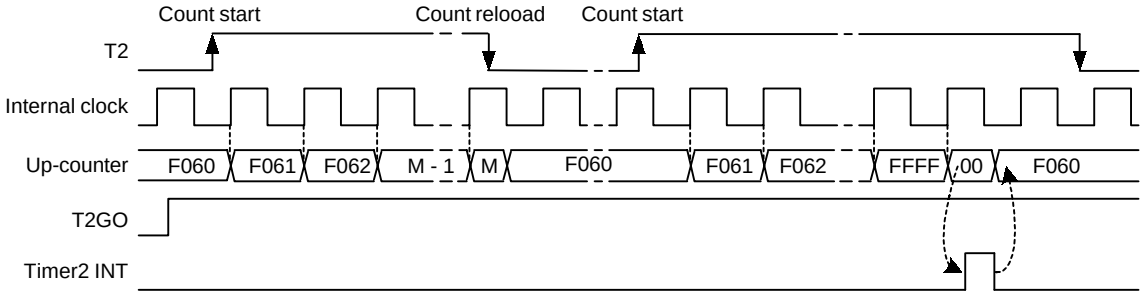
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	T2E	T2SC.2	T2SC.1	T2SC.0	R/W	Bit2-0: Timer2 pre-scaler register
	X	0	0	0	R/W	Timer clock: OSC clock / 2^{14}
	X	0	0	1	R/W	Timer clock: OSC clock / 2^{12}
	X	0	1	0	R/W	Timer clock: OSC clock / 2^{10}
	X	0	1	1	R/W	Timer clock: OSC clock / 2^8
	X	1	0	0	R/W	Timer clock: OSC clock / 2^6
	X	1	0	1	R/W	Timer clock: OSC clock / 2^5
	X	1	1	0	R/W	Timer clock: OSC clock / 2^4
	X	1	1	1	R/W	Timer clock: OSC clock / 2^3
	0	X	X	X	R/W	T2 input falling edge active (Default)
	1	X	X	X	R/W	T2 input rising edge active

Timer2 Counter Register: $384 ~ $387

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$384	T2D.3	T2D.2	T2D.1	T2D.0	R/W	Timer2load / counter register low nibble
$385	T2D.7	T2D.6	T2D.5	T2D.4	R/W	Timer2 load / counter register middle_L nibble
$386	T2D.11	T2D.10	T2D.9	T2D.8	R/W	Timer2 load / counter register middle_H nibble
$387	T2D.15	T2D.14	T2D.13	T2D.12	R/W	Timer2 load / counter register high nibble



Trigger Start (DEC = 0)



Trigger Start and Stop (DEC = 1)

(4) Pulse width measurement mode

In this mode, Timer2 is performed using a special function under the timer mode in which counting is started on an edge of pulse waveform that is input to the T2 pin. It is possible to measure the width of the pulse waveform by reading the up-counter values on state transitions of the input to the T2 pin. The rising or falling edge of the T2 pin input is selected by setting the T2E (bit3) in the Timer2 pre-scaler register ($15). But the source clock of the up-counter is an internal clock selected by proper setting the T2SC (bit2-0) in the Timer2 pre-scaler register ($15). When the T2GO (bit3) in the Timer2 control register ($27) is set to “1”, the contents of the up-counter must reset to “0000H”, automatically. Then a rising (falling) edge signal on the T2 input pin triggers the up-counter to start counting. At the next falling (rising) edge, the counter value is loaded to the Timer2 counter register ($384 ~ $387), individually. Simultaneously, the Timer2 interrupt is generated if the Interrupt enable register ($00) bit1 (IET2) is set to 1.

When DEC (bit2) in the Timer2 control register ($27) is 0, the Timer2 is in the one-edge capture operation. If the rising edge is selected as the counter triggering signal, at the next falling edge, the Timer2 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer2 counter register ($384 ~ $387) at first, then will be cleared again and the counter is halted. When the next rising edge applies to the T2 input pin, the up-counter starts counting for another measurement cycle.

When DEC (bit2) in the Timer2 control register ($27) is 1, the Timer2 is in the double-edge capture operation. If the rising edge is selected as the counter triggering signal, at the next falling edge, the Timer2 interrupt request is generated. At the same time, the contents of the up-counter must be loaded to the Timer2 counter register ($384 ~ $387) at first, then the counter continues counting. When the next rising edge applies to the T2 input pin, the Timer2 interrupt request is also generated. At this time, the contents of the up-counter must be loaded to the Timer2 counter register ($384 ~ $387) again, then the counter must be cleared and can be continued to start counting following measurement cycles.

In this mode, writing the Timer2 counter register ($384 ~ $387) at any time can not affect the up-counter operating anymore.

In this mode, the T2 pin input signal must follow certain constraints as in the external trigger timer mode. So, the limitation is applied for the T2 period time described as follows:

TE (period time) ≥ 1 * tTimer clock + 2 * ΔT ; ΔT = 20ns

TE (period time) ≥ (M * tOSC) + 2 * ΔT

Where M (pre-scaler value for Timer2 internal clock) =23, 24, 25, 26, 28, 210, 212or 214

But, in order to correctly get the pulse measurement value in programming, a sufficient wait period must be needed for the relevant Timer2 interrupt subroutine program.

So, if DEC (bit2) in the Timer2 control register ($27) is 0, the Timer2 is in the one-edge capture operation. The limitation is applied for the external clock period(TE) time described as follows:

TE (period time) ≥ 14 * tTSystem clock

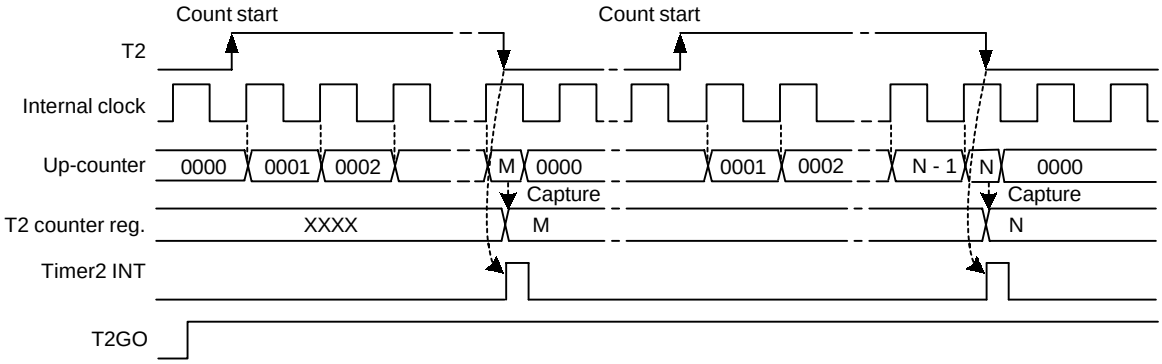
TE (period time) ≥ 14 * 4 * tOSC

The maximum value of these two equations shown above is valid to the proper application.

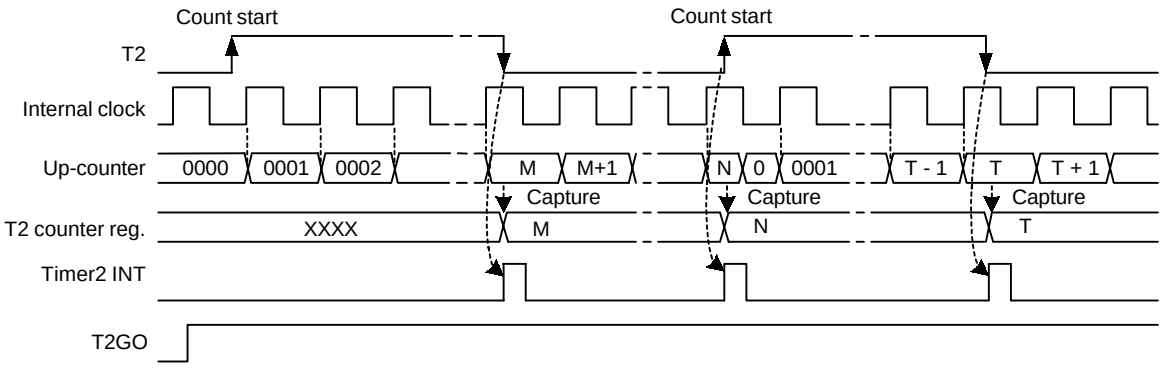
If DEC (bit2) in the Timer2 control register ($27) is 1, the Timer2 is in the double-edge capture operation. The limitation is applied for the ESS input signal high or low level period described as follows:

TE (high or low level period time) ≥ 14 * tTSystem clock

TE (high or low level period time) ≥ 14 * 4 * tOSC



One edge capture (DEC = 0)



Double edge capture (DEC = 1)

Timer2 Control Register: $27 (under the pulse width measurement mode)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	T2GO	DEC	TM2S1	TM2S0	R/W	Bit1-0: Timer2 mode select
	X	0	1	1	R/W	Bit2: One edge capture.
	X	1	1	1	R/W	Bit2: Double edge capture.

8.Key scanner

There is a key scanner built-in the SH69P55, which can automatic detect the key-press. It includes four outputs (KEY_O0~3, shared with COM3~0), five inputs (KEY_I4~0, shared with SEG4~0), and it can detect 20 individual keys.

Key scanner control register $28

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$28	KeyNUM1	KeyNUM0	KeyEND	KeyEN	R/W R R	Bit0: enable key scanner Bit1: one key scan end Bit3~2: key number0, 1
	X	X	X	0	R/W	Disable key scanner
	X	X	X	1	R/W	Enable key scanner
	X	X	0	1	R	Key scan end
	X	X	1	1	R	Key scan processing
	X	0	X	1	R	No key-press
	X	1	X	1	R	Key-press occur
	0	X	X	1	R	One key-press occur, at the same time
	1	X	X	1	R	More than one key-press occur, at the same time

Key scanner data register1 $2C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2C	KeyC3	KeyC2	KeyC1	KeyC0	R	Bit3~0: the result of key scan on KEY_O3~0
	0	0	0	1	R	Key-press occur on KEY_O0
	0	0	1	0	R	Key-press occur on KEY_O1
	0	1	0	0	R	Key-press occur on KEY_O2
	1	0	0	0	R	Key-press occur on KEY_O3

Key scanner data register2 $2D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2D	KeyL3	KeyL2	KeyL1	KeyL0	R	Bit3~0: the result of key scan on KEY_I3~0
	0	0	0	0	R	Key-press occur on KEY_I0
	0	0	0	1	R	Key-press occur on KEY_I1
	0	0	1	0	R	Key-press occur on KEY_I2
	0	1	0	0	R	Key-press occur on KEY_I3
	1	0	0	0	R	Key-press occur on KEY_I4

NOTE:

1.If automatic key scanner is enabled, PORTA0~3, PORTF0 must be shared as SEG signal output for LED or LCD display and PORTD0~3 must be shared as COM signal output for LED or LCD display. Although the LCD or LED is turned off, the automatic key scan is also valid.

2.If and only if one key is pressed at the same time, the result of the key scan is valid.

9.LCD driver:

The LCD driver contains a controller, a voltage generator, 4-8 common and 16-20 segment driver pins. There are three different driving modes programmable: 1/4 duty & 1/3 bias, 1/6 duty & 1/3 bias and 1/8 duty & 1/4 bias. The driving mode is controlled by the system register $29.

All of the segments and coms can be shared as normal I/Os.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the same value after executing the “STOP” instruction.

Before use the LCD driver, LEDEN bit (bit3 in $2B) must be cleared.

LCD control register $29

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$29	LCDON	DUTY2	DUTY1	DUTY0	R/W	Bit2-0: Set duty and com Bit3: Turn on LCD
	0	X	X	X	R/W	Turn off LCD
	1	X	X	X	R/W	Turn on LCD
	X	0	X	X	R/W	PORTD and PORTE are not shared as COM for LCD display
	X	1	0	0	R/W	Set 1/4 duty. PORTD is shared as COM0~3, PORTE is not shared as COM
	X	1	0	1	R/W	Set 1/4 duty. PORTE is shared as COM4~7, PORTD is not shared as COM
	X	1	1	0	R/W	Set 1/6 duty. PORTD is shared as COM0~3, PORTE3~2 is shared as COM4~5 and PORTE1~0 is not shared as COM
	X	1	1	1	R/W	Set 1/8 duty. PORTD is shared as COM0~3 and PORTE is shared as COM4~7

NOTE:

1.LCD clock is divided from OSC, so LCD frame frequency will change in proportion to the variation of OSC frequency in spite of OSC type. The LCD frame frequency is changed from 64Hz to 128Hz.

2. SH69P55 both has LCD driver and LED driver, and just only one is valid at one time. If LEDEN=1, the LCD driver is disabled; if LEDEN=0, the LED driver is disabled.

SEG configuration register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	RLCD	Ps2	Ps1	Ps0	R/W	Bit0~2: Configuration the segment Bit3: set LCD bias resistor
	-	0	0	0	R/W	See the following table

Ps2	Ps1	Ps0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	PE3	PE2	PE1	PE0	PH3	PH2	PH1	PH0	PI3	PI2	PI1	PI0	PF3	PF2	PF1	PF0	PA3	PA2	PA1	PA0
0	0	1	PE3	PE2	PE1	PE0	PH3	PH2	PH1	PH0	PI3	PI2	PI1	PI0	PF3	PF2	PF1	Seg4	Seg3	Seg2	Seg1	Seg0
0	1	0	PE3	PE2	PE1	PE0	PH3	PH2	PH1	PH0	PI3	PI2	PI1	PI0	PF3	PF2	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0
0	1	1	PE3	PE2	PE1	PE0	PH3	PH2	PH1	PH0	PI3	PI2	PI1	PI0	PF3	Seg6	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0
1	0	0	PE3	PE2	PE1	PE0	PH3	PH2	PH1	PH0	PI3	PI2	PI1	PI0	Seg7	Seg6	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0
1	0	1	PE3	PE2	PE1	PE0	PH3	PH2	PH1	PH0	Seg11	Seg10	Seg9	Seg8	Seg7	Seg6	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0
1	1	0	PE3	PE2	PE1	PE0	Seg15	Seg14	Seg13	Seg12	Seg11	Seg10	Seg9	Seg8	Seg7	Seg6	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0
1	1	1	Seg19	Seg18	Seg17	Seg16	Seg15	Seg14	Seg13	Seg12	Seg11	Seg10	Seg9	Seg8	Seg7	Seg6	Seg5	Seg4	Seg3	Seg2	Seg1	Seg0

NOTE:

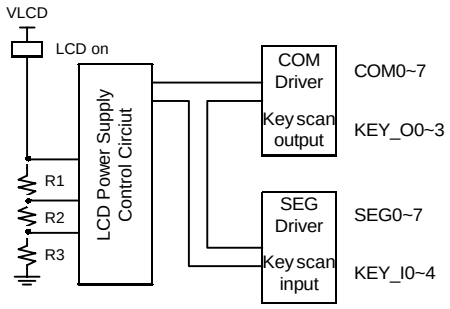
If PORTE0~3 are shared as COM4~7 for LCD display, then PORTE0~3 cannot shared as SEG19~16 for LCD display

SEGs and COMs shall be configed correctly before turn on the LCD

VLCD=VDD

SEG configuration register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	RLCD	-	-	-	R/W	Bit3:Set LCD bias resistor
	0	X	X	X	R/W	R1=R2=R3 =90K
	1	X	X	X	R/W	R1=R2=R3 =10K
	X	X	X	X	R/W	R1=R2=R3 =3K, if KEYEN=1



When large LCD panel is used, user can set the value of $2E to increase the bias current for better LCD performance. But it will cost more power, when smaller divider resistances are used.

When the CPU is in STOP mode, the COMx and SEGx are pulled low. It can easily be woken up by Port interrupt.

Configuration of LCD RAM

LCD 1/4 duty, 1/3 bias (COM0~3, SEG0 ~19)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM3	COM2	COM1	COM0		COM3	COM2	COM1	COM0
$300	SEG0	SEG0	SEG0	SEG0	$30A	SEG10	SEG10	SEG10	SEG10
$301	SEG1	SEG1	SEG1	SEG1	$30B	SEG11	SEG11	SEG11	SEG11
$302	SEG2	SEG2	SEG2	SEG2	$30C	SEG12	SEG12	SEG12	SEG12
$303	SEG3	SEG3	SEG3	SEG3	$30D	SEG13	SEG13	SEG13	SEG13
$304	SEG4	SEG4	SEG4	SEG4	$30E	SEG14	SEG14	SEG14	SEG14
$305	SEG5	SEG5	SEG5	SEG5	$30F	SEG15	SEG15	SEG15	SEG15
$306	SEG6	SEG6	SEG6	SEG6	$310	SEG16	SEG16	SEG16	SEG16
$307	SEG7	SEG7	SEG7	SEG7	$311	SEG17	SEG17	SEG17	SEG17
$308	SEG8	SEG8	SEG8	SEG8	$312	SEG18	SEG18	SEG18	SEG18
$309	SEG9	SEG9	SEG9	SEG9	$313	SEG19	SEG19	SEG19	SEG19

LCD 1/4 duty, 1/3 bias (COM4~7, SEG0~15)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM7	COM6	COM5	COM4		COM7	COM6	COM5	COM4
$320H	SEG0	SEG0	SEG0	SEG0	$328	SEG8	SEG8	SEG8	SEG8
$321H	SEG1	SEG1	SEG1	SEG1	$329	SEG9	SEG9	SEG9	SEG9
$322H	SEG2	SEG2	SEG2	SEG2	$32A	SEG10	SEG10	SEG10	SEG10
$323H	SEG3	SEG3	SEG3	SEG3	$32B	SEG11	SEG11	SEG11	SEG11
$324H	SEG4	SEG4	SEG4	SEG4	$32C	SEG12	SEG12	SEG12	SEG12
$325H	SEG5	SEG5	SEG5	SEG5	$32D	SEG13	SEG13	SEG13	SEG13
$326H	SEG6	SEG6	SEG6	SEG6	$32E	SEG14	SEG14	SEG14	SEG14
$327H	SEG7	SEG7	SEG7	SEG7	$32F	SEG15	SEG15	SEG15	SEG15

LCD 1/8 duty, 1/4 bias (COM0~7, SEG0~15)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0
$320	SEG0	SEG0	SEG0	SEG0	$300	SEG0	SEG0	SEG0	SEG0
$321	SEG1	SEG1	SEG1	SEG1	$301	SEG1	SEG1	SEG1	SEG1
$322	SEG2	SEG2	SEG2	SEG2	$302	SEG2	SEG2	SEG2	SEG2
$323	SEG3	SEG3	SEG3	SEG3	$303	SEG3	SEG3	SEG3	SEG3
$324	SEG4	SEG4	SEG4	SEG4	$304	SEG4	SEG4	SEG4	SEG4
$325	SEG5	SEG5	SEG5	SEG5	$305	SEG5	SEG5	SEG5	SEG5
$326	SEG6	SEG6	SEG6	SEG6	$306	SEG6	SEG6	SEG6	SEG6
$327	SEG7	SEG7	SEG7	SEG7	$307	SEG7	SEG7	SEG7	SEG7
$328	SEG8	SEG8	SEG8	SEG8	$308	SEG8	SEG8	SEG8	SEG8
$329	SEG9	SEG9	SEG9	SEG9	$309	SEG9	SEG9	SEG9	SEG9
$32A	SEG10	SEG10	SEG10	SEG10	$30A	SEG10	SEG10	SEG10	SEG10
$32B	SEG11	SEG11	SEG11	SEG11	$30B	SEG11	SEG11	SEG11	SEG11
$32C	SEG12	SEG12	SEG12	SEG12	$30C	SEG12	SEG12	SEG12	SEG12
$32D	SEG13	SEG13	SEG13	SEG13	$30D	SEG13	SEG13	SEG13	SEG13
$32E	SEG14	SEG14	SEG14	SEG14	$30E	SEG14	SEG14	SEG14	SEG14
$32F	SEG15	SEG15	SEG15	SEG15	$30F	SEG15	SEG15	SEG15	SEG15

LCD 1/6 duty, 1/4 bias (COM0~5, SEG0~17)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	-	-	COM5	COM4		COM3	COM2	COM1	COM0
$320			SEG0	SEG0	$300	SEG0	SEG0	SEG0	SEG0
$321			SEG1	SEG1	$301	SEG1	SEG1	SEG1	SEG1
$322			SEG2	SEG2	$302	SEG2	SEG2	SEG2	SEG2
$323			SEG3	SEG3	$303	SEG3	SEG3	SEG3	SEG3
$324			SEG4	SEG4	$304	SEG4	SEG4	SEG4	SEG4
$325			SEG5	SEG5	$305	SEG5	SEG5	SEG5	SEG5
$326			SEG6	SEG6	$306	SEG6	SEG6	SEG6	SEG6
$327			SEG7	SEG7	$307	SEG7	SEG7	SEG7	SEG7
$328			SEG8	SEG8	$308	SEG8	SEG8	SEG8	SEG8
$329			SEG9	SEG9	$309	SEG9	SEG9	SEG9	SEG9
$32A			SEG10	SEG10	$30A	SEG10	SEG10	SEG10	SEG10
$32B			SEG11	SEG11	$30B	SEG11	SEG11	SEG11	SEG11
$32C			SEG12	SEG12	$30C	SEG12	SEG12	SEG12	SEG12
$32D			SEG13	SEG13	$30D	SEG13	SEG13	SEG13	SEG13
$32E			SEG14	SEG14	$30E	SEG14	SEG14	SEG14	SEG14
$32F			SEG15	SEG15	$30F	SEG15	SEG15	SEG15	SEG15
$330			SEG16	SEG16	$310	SEG16	SEG16	SEG16	SEG16
$331			SEG17	SEG17	$311	SEG17	SEG17	SEG17	SEG17

LCD waveform

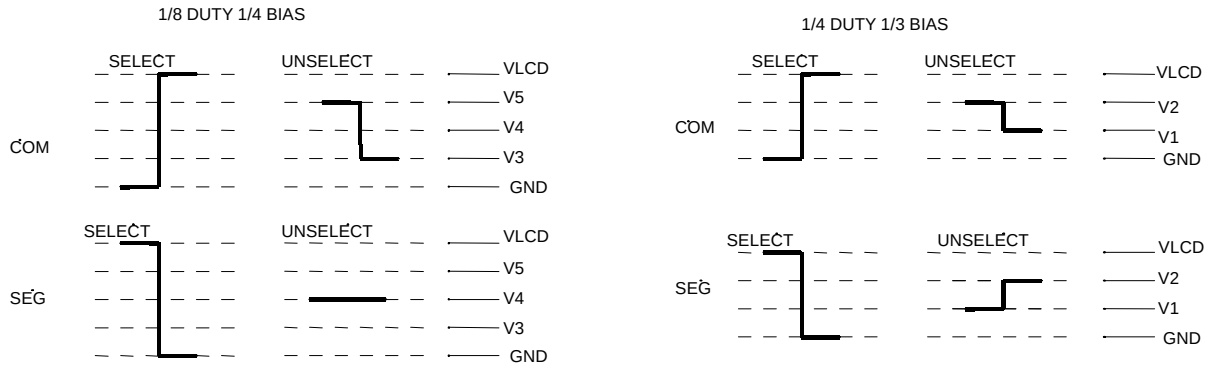
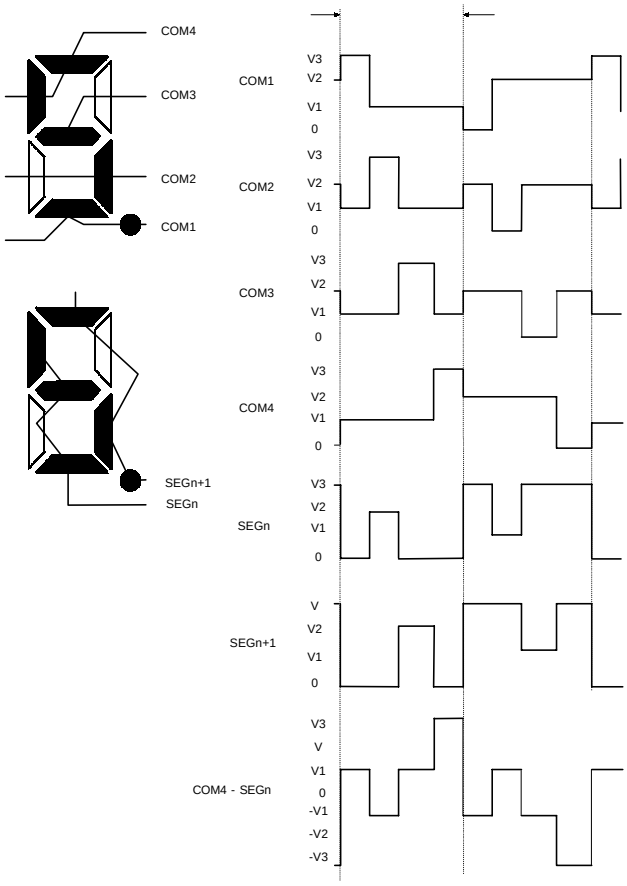


Figure 12: LCD waveform of different duty and bias



10.LED driver:

The LED driver contains a controller, 4-6 common and 8 segment driver pins. The built-in LED driver has so powerful drive ability that it can drive LED directly. COM can source at least 200mA current. For detail information, please reference the application circuit. Before use the LED driver, LEDEN must be set to1.

LED driver duty control register $2B

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2B	LEDEN	LEDON	EDUTY1	EDUTY0	R/W	Bit1-0: Set duty Bit2: Turn on LED driver Bit3: Enable LED driver
	0	X	X	X	R/W	LED disable and LCD enable
	1	X	X	X	R/W	LED enable and LCD disable
	1	0	X	X	R/W	LED driver off
	1	1	X	X	R/W	LED driver on
	1	X	0	0	R/W	PORTD and PORTE3~2 are not shared as COM for LED display
	1	X	0	1	R/W	1/4 duty, PORTD0~3 is shared as COM0~3 for LED display and PORTE3~2 is normal I/O
	1	X	1	0	R/W	1/5 duty, PORTD0~3 and PORTE0 is shared as COM0~4 for LED display and PORTE3 is normal I/O
	1	X	1	1	R/W	1/6 duty, PORTD0~3 and PORTE3~2 is shared as COM0~5 for LED display

NOTE:

SH69P55 both has LCD driver and LED driver, and just only one is valid at one time. If LEDEN=1, the LCD driver is disabled; if LEDEN=0, the LED driver is disabled.

SEG configuration register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	RLCD	Ps2	Ps1	Ps0	R/W	Bit0~3: Configuration the segment
	X	0	0	0	R/W	See the following table

Ps2	Ps1	Ps0	7	6	5	4	3	2	1	0
0	0	0	PF3	PF2	PF1	PF0	PA3	PA2	PA1	PA0
0	0	1	PF3	PF2	PF1	LED_S4	LED_S3	LED_S2	LED_S1	LED_S0
0	1	0	PF3	PF2	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1	LED_S0
0	1	1	PF3	LED_S6	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1	LED_S0
1	0	0	LED_S7	LED_S6	LED_S5	LED_S4	LED_S3	LED_S2	LED_S1	LED_S0

Configuration of LED RAM

LED 1/4 duty (COM0~3,SEG0~7)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	SEG3	SEG2	SEG1	SEG0		SEG7	SEG6	SEG5	SEG4
$314	COM0	COM0	COM0	COM0	$334	COM0	COM0	COM0	COM0
$315	COM1	COM1	COM1	COM1	$335	COM1	COM1	COM1	COM1
$316	COM2	COM2	COM2	COM2	$336	COM2	COM2	COM2	COM2
$317	COM3	COM3	COM3	COM3	$337	COM3	COM3	COM3	COM3

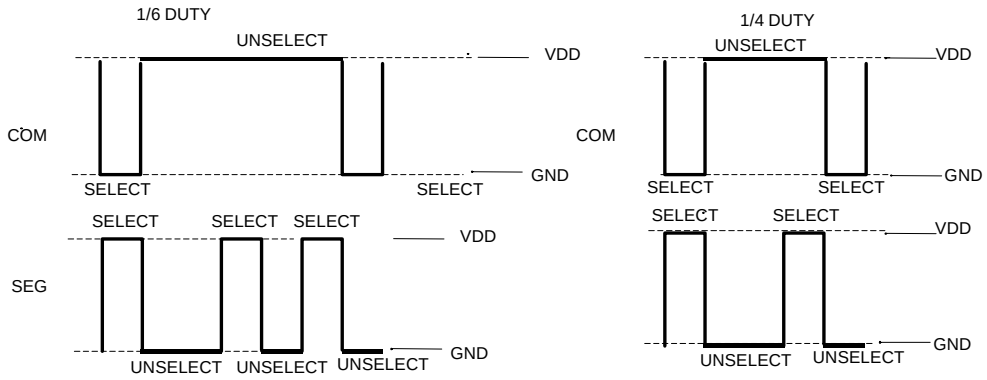
LED 1/5 duty (COM0~4,SEG0~7)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	SEG3	SEG2	SEG1	SEG0		SEG7	SEG6	SEG5	SEG4
$314	COM0	COM0	COM0	COM0	$334	COM0	COM0	COM0	COM0
$315	COM1	COM1	COM1	COM1	$335	COM1	COM1	COM1	COM1
$316	COM2	COM2	COM2	COM2	$336	COM2	COM2	COM2	COM2
$317	COM3	COM3	COM3	COM3	$337	COM3	COM3	COM3	COM3
$318	COM4	COM4	COM4	COM4	$338	COM4	COM4	COM4	COM4

LED 1/6 duty (COM0~5,SEG0~7)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	SEG3	SEG2	SEG1	SEG0		SEG7	SEG6	SEG5	SEG4
$314	COM0	COM0	COM0	COM0	$334	COM0	COM0	COM0	COM0
$315	COM1	COM1	COM1	COM1	$335	COM1	COM1	COM1	COM1
$316	COM2	COM2	COM2	COM2	$336	COM2	COM2	COM2	COM2
$317	COM3	COM3	COM3	COM3	$337	COM3	COM3	COM3	COM3
$318	COM4	COM4	COM4	COM4	$338	COM4	COM4	COM4	COM4
$319	COM5	COM5	COM5	COM5	$339	COM5	COM5	COM5	COM5

LED waveform



11.Analog/Digital Converter (ADC)

The 8 channels and 10-bit resolution A/D converter are implemented in this micro-controller.

The approach for A/D conversion:

- Set analog input channels and select the reference voltage. (When using the external reference voltage, please keep in mind that any analog input voltage can not exceed the V_{REF})
- Enable the A/D converter module with the selected analog channel.
- GO/$\overline{\text{DONE}}$ =1, start the A/D conversion.
- Acquire the converted data

A/D Port Configuration Control Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: A/D port configuration control Bit3: Select Internal/External reference voltage
	X	0	0	0	R/W	See select analog channel Table
	0	X	X	X	R/W	Internal reference voltage (V_{REF}=V_{DD}) (Default)
	1	X	X	X	R/W	External reference voltage

Select analog channels from normal I/O ports

ACR2	ACR1	ACR0	7	6	5	4	3	2	1	0
0	0	0	PJ3	PJ2	PJ1	PJ0	PB3	PB2	PB1	PB0
0	0	1	PJ3	PJ2	PJ1	PJ0	PB3	PB2	PB1	AN0
0	1	0	PJ3	PJ2	PJ1	PJ0	PB3	PB2	AN1	AN0
0	1	1	PJ3	PJ2	PJ1	PJ0	PB3	AN2	AN1	AN0
1	0	0	PJ3	PJ2	PJ1	PJ0	AN3	AN2	AN1	AN0
1	0	1	PJ3	PJ2	PJ1	AN4	AN3	AN2	AN1	AN0
1	1	0	PJ3	PJ2	AN5	AN4	AN3	AN2	AN1	AN0
1	1	1	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

A/D Converter Enable Register $14:

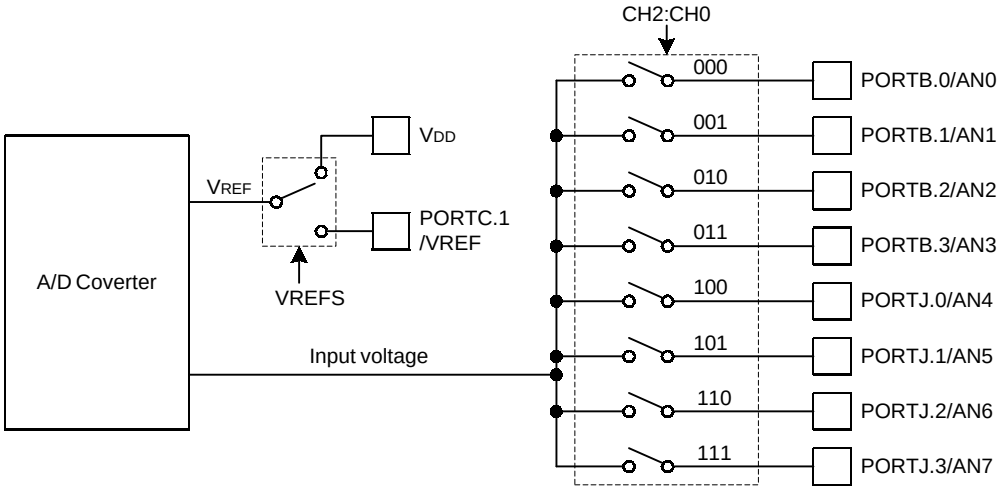
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	ADCON	CH2	CH1	CH0	R/W	Bit2-0: Select ADC channel Bit3: Set ADC module enable
	X	0	0	0	R/W	ADC channel AN0 (Default)
	X	0	0	1	R/W	ADC channel AN1
	X	0	1	0	R/W	ADC channel AN2
	X	0	1	1	R/W	ADC channel AN3
	X	1	0	0	R/W	ADC channel AN4
	X	1	0	1	R/W	ADC channel AN5
	X	1	1	0	R/W	ADC channel AN6
	X	1	1	1	R/W	ADC channel AN7
	0	X	X	X	R/W	Disable the A/D converter module. (Default)
	1	X	X	X	R/W	Enable the A/D converter module.

A/D Result Register: $3AD~$3AF

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3AD	-	-	A1	A0	R	ADC data low nibble (Read only)
$3AE	A5	A4	A3	A2	R	ADC data middle nibble (Read only)
$3AF	A9	A8	A7	A6	R	ADC data high nibble (Read only)

A/D Conversion Control Register $2F:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2F	GO/$\overline{\text{DONE}}$	TADC1	TADC0	-	R/W	Bit2, Bit1: Select A/D Clock Period Bit3: ADC status flag
	X	0	0	X	R/W	A/D Clock Period $t_{AD} = t_{OSC}$
	X	0	1	X	R/W	A/D Clock Period $t_{AD} = 4\ t_{OSC}$
	X	1	0	X	R/W	A/D Clock Period $t_{AD} = 16\ t_{OSC}$
	X	1	1	X	R/W	A/D Clock Period $t_{AD} = 32\ t_{OSC}$
	0	X	X	X	R/W	A/D conversion not in progress
	1	X	X	X	R/W	A/D conversion in progress, when ADCON=1



A/D Converter Block Diagram

Programming Notice:

- Select A/D clock period t_{AD}, make sure that 25μs ≤A/D Conversion Time.
- When the A/D conversion is complete, an A/D converter interrupt occurs (if the A/D converter interrupt is enabled).
- The analog input channels must have their corresponding PXCR (X=B, J) bits selected as inputs.
- If select I/O port as analog input, the I/O functions and pull up resistor are disabled.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the A/D conversion is complete.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion.
- The A/D result register will NOT be updated with the partially completed A/D conversion sample.
- A/D converter could keep on working in HALT mode, and would stop automatic when execute "STOP" instruction.
- A/D converter could wake-up SH69P55 from HALT mode (if the A/D converter interrupt is enabled).

12.Pulse Width Modulation (PWM)

The SH69P55 consists of one 8+2 bit PWM module. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMP is used to control the period cycle of the PWM module output. And the PWMD is used to control the duty in the waveform of the PWM module output.

Systems register$20: (PWMC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	PWMS	TCK1	TCK0	PWM	R/W	Bit0: Select PWM output Bit2, Bit1: Set PWM clock Bit3: Set PWM output mode of duty cycle
	X	X	X	0	R/W	Shared with I/O port
	X	X	X	1	R/W	Shared with PWM
	X	0	0	X	R/W	PWM clock = t_{OSC}
	X	0	1	X	R/W	PWM clock = $2t_{OSC}$
	X	1	0	X	R/W	PWM clock = $4t_{OSC}$
	X	1	1	X	R/W	PWM clock = $8t_{OSC}$
	0	X	X	X	R/W	PWM output normal mode of duty cycle
	1	X	X	X	R/W	PWM output negative mode of duty cycle

Systems register $21 ~ $23: (PWMP)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PP.3	PP.2	PP.1	PP.0	R/W	PWM period low nibble
$22	PP.7	PP.6	PP.5	PP.4	R/W	PWM period high nibble

PWM output period cycle = [PP.7, PP.0] x PWM clock.
When [PP.7, PP.0]= 00H, PWM outputs GND if the PWMS bit is set to 0.
When [PP.7, PP.0]= 00H, PWM outputs high level if the PWMS bit is set to 1.

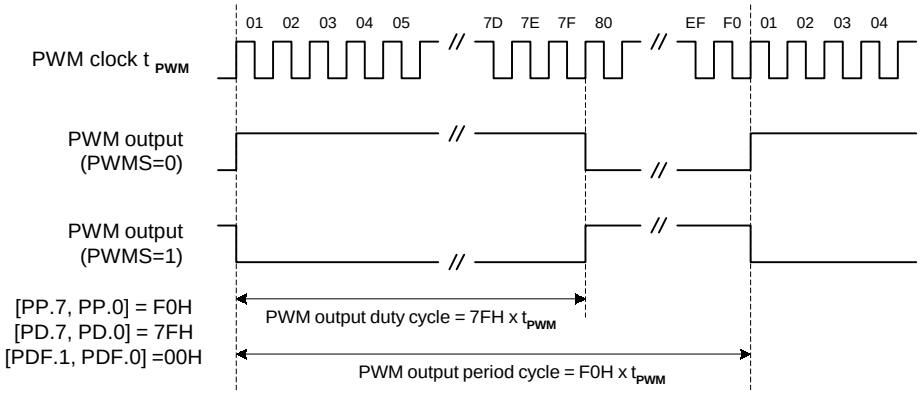
Systems register $24 ~ $26: (PWMD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	-	-	PDF.1	PDF.0	R/W	PWM duty fine tune nibble
$25	PD.5	PD.4	PD.3	PD.2	R/W	PWM duty low nibble
$26	PD.9	PD.8	PD.7	PD.6	R/W	PWM duty high nibble

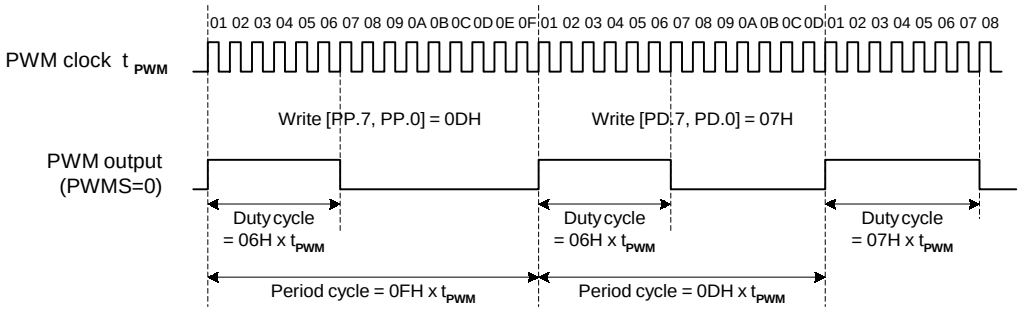
Average PWM output duty cycle =([PD.7, PD.0] + [PDF.1, PDF.0] / 4) x PWM clock.
If [PP.7, PP.0] ≤ [PD.7, PD.0], PWM outputs high when the PWMS bit is set to 0.
If [PP.7, PP.0] ≤ [PD.7, PD.0], PWM outputs GND level when the PWMS bit is set to 1.

Notice:

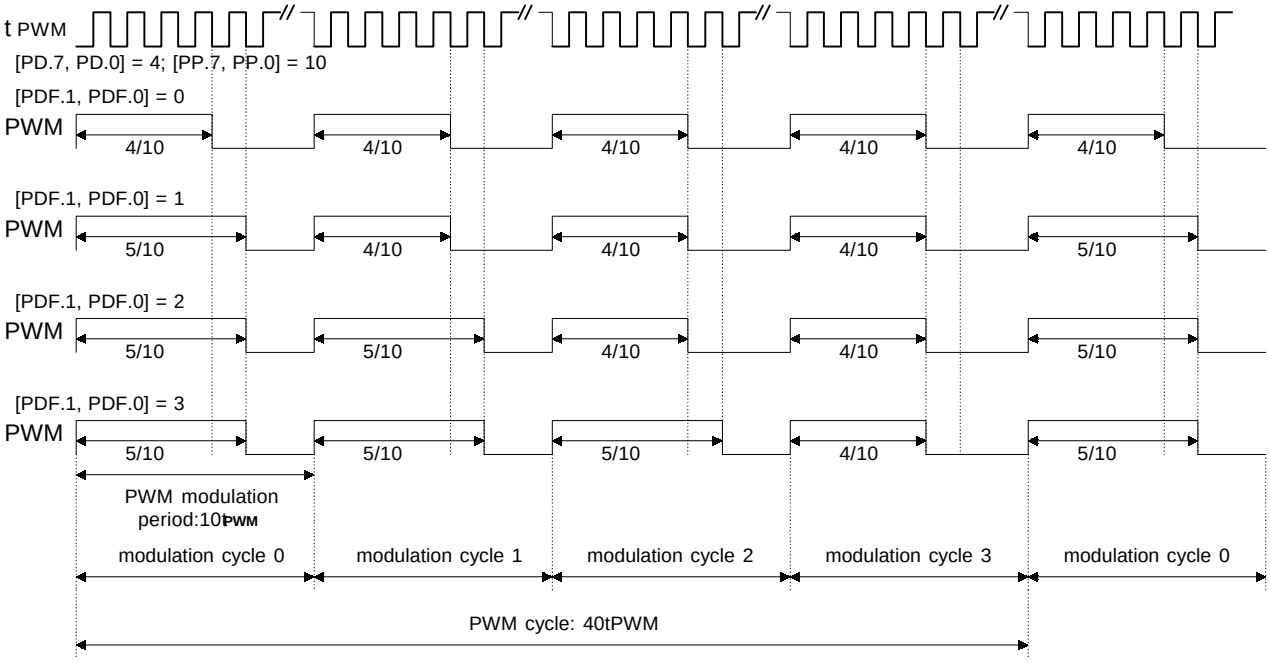
- If the I/O port is selected as the PWM output, the I/O functions and pull up resistor are disabled.
- The writing flow of the PWM duty control register is described as follows. First set the fine tune nibble, then the low nibble and set the high nibble at last.
- The writing flow of the PWM period control register is described as follows. First set the low nibble, then set the high nibble.
- After the high nibble of the PWM period or duty control register is written, the data are loaded into the re-load counter and start counting at next period.
- The reading flow of the PWM period or duty control register is at the reverse direction with that described above. First read the high nibble, then read the low nibble.
- PWM could keep on working in the HALT mode, and would stop automatic when the "STOP" instruction is executed.



PWM output example



PWM output Period or Duty cycle changing example



8+2 bit PWM waveform

In the 8+2 bit PWM waveform, A PWM cycle is divided into 4 modulation cycles(cycle 0 – cycle 3), each modulation cycle has certain period decided by period cycle registers(PWMP). The contents of duty cycle register(PWMD) is divided into two parts. The basic part of PWMD is PD.7 – PD.0. The extended part is PDF.1 – PDF.0. In a PWM cycle, the duty cycle of each modulation cycle is shown in the table.

Parameter	[PDF.1, PDF.0] (0-3)	Duty Cycle
Modulation Cycle I (I=0-3)	I<	([PD.7, PD.0] + 1)/ [PP.7, PP.0]
	I [PDF.1, PDF.0]	[PD.7, PD.0] / [PP.7, PP.0]

The modulation period, cycle period and cycle duty of the PWM output signal are summarized in the following table.

PWM modulation period	PWM cycle period	PWM cycle duty
[PP.7, PP.0] * tpwm	4*[PP.7, PP.0] * tpwm	(4* [PD.7, PD.0] + [PDF.1, PDF.0])/(4*[PP.7, PP.0])

13.Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where heavy loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by the Code option.

The LVR circuit has the following functions when the LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq t_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$ and $t < t_{LVR}$.

System Register: $17

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	LVR	-	-	SCF	R/W	Bit3: Low Voltage Reset flag (Read and Write 0 only) Bit0: System clock fail flag (Read and Write 0 only)
	0	X	X	X	R/W	NO Low Voltage Reset
	1	X	X	X	R/W	Low Voltage Reset

14.ROM Data Table

ROM Data Table Register (RDT): $380 - $383

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$380	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address / data register
$381	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address / data register
$382	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address / data register
$383	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address / data register

The RDT register consists of a 13-bit write-only PC address load register (RDT.12 – RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 – RDT.0).

To read out the ROM table data, users should write the ROM table address to RDT register first (high nibble first then low nibble), then after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into $380 will start the data read-out action)**.**

Programmer can put 16-bit data into one address by data allocation instruction “DW”. (Reference to UASM66 Cross Assembler User’s Guide.)

15.Interrupt

Four interrupt sources are available on SH69P55:

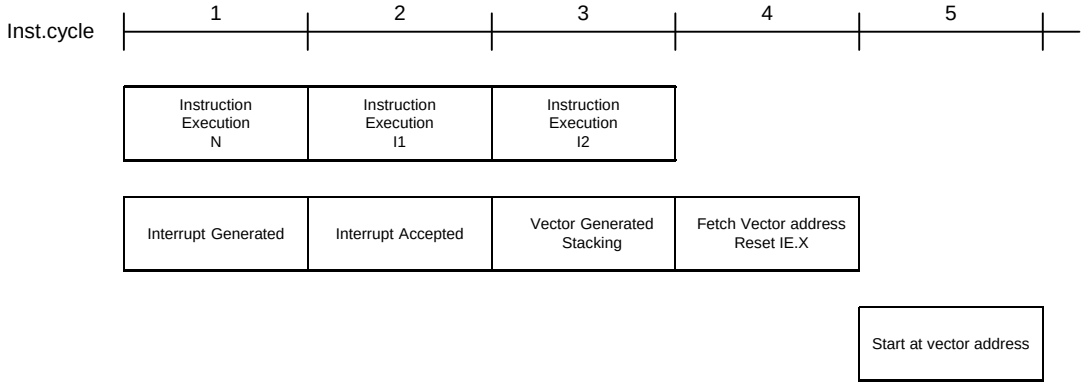
- Timer0 interrupt
- Timer1 interrupt
- Timer2 interrupt
- External interrupts (include PortB, PortC interrupts, AD interrupt, Key scan interrupt)

(a) Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IET0	IET1	IET2	IEEX	R/W	Interrupt enable flags
$01	IRQT0	IRQT1	IRQT2	IRQEX	R/W	Interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into the stack memory and jump to the interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and the vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the SH6610D CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

(b) Timer (Timer0, Timer1, tiemr2) Interrupt

The input clock of Timer0, Timer1 and Timer2 are based on system clocks or external clock/event T0 input as Timer0 source and T2 input as Timer2 source. The timer overflow from $FF to $00 (from $FFFF to $0000 for Timer2) will generate an internal interrupt request (IRQT0, IRQT1=1 or IRQT2=1), If the interrupt enable flag is enabled (IET0, IET1=1 or IET2=1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from the HALT mode.

(c) External interrupts

External interrupts include PORTB, PORTC falling edge interrupt; AD interrupt and Key scan interrupt. Any external interrupt occur, an internal interrupt request (IRQEX) will be generated, if the interrupt enable flag is enabled (IEEX), an external interrupt service routine will start.

The PORTB and PORTC are used as external port interrupt sources. Since PORTB and PORTC are bit programmable I/Os, so only the voltage transition from VDD to GND applying to the digital input port can generate a port interrupt. The analog input can not generate any interrupt request.

The interrupt control flags are mapped on $388, $38A, $38C of the system register. They can be accessed or tested by the read/write operation. Those flags are cleared to 0 at the initialization by the chip reset. Port Interrupts (including other external interrupt sources) can be used to wake up the CPU from the HALT or the STOP mode.

Port Interrupt Enable Flags Register: $388, $38A

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$388	PBIEN.3	PBIEN.2	PBIEN.1	PBIEN.0	R/W	PORTB interrupt enable flags
$38A	PCIEN.3	PCIEN.2	PCIEN.1	PCIEN.0	R/W	PORTC interrupt enable flags

PB/CIEN.n, (n = 0, 1, 2, 3)
0: Disable port interrupt. (Default)
1: Enable port interrupt.

Port Interrupt Request Flags Register: $389, $38B

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$389	PBIF.3	PBIF.2	PBIF.1	PBIF.0	R/W	PORTB interrupt request flags
$38B	PCIF.3	PCIF.2	PCIF.1	PCIF.0	R/W	PORTC interrupt request flags

PB/CIF.n, (n = 0, 1, 2, 3)
0: Port interrupt is not presented. (Default)
1: Port interrupt is presented.
Only writing these bits to 0 is available.
When the A/D conversion is complete, It will generate an interrupt request (ADIF=1), if the ADC interrupt is enabled (ADIE=1), an External interrupt service routine will start. The A/D interrupt can be used to wake the CPU from HALT mode.
When the Key scan is complete, It will generate an interrupt request (KEYIF=1), if the Key scan interrupt is enabled (KEYIE=1), an External interrupt service routine will start. The KEY scan interrupt can be used to wake the CPU from HALT mode.

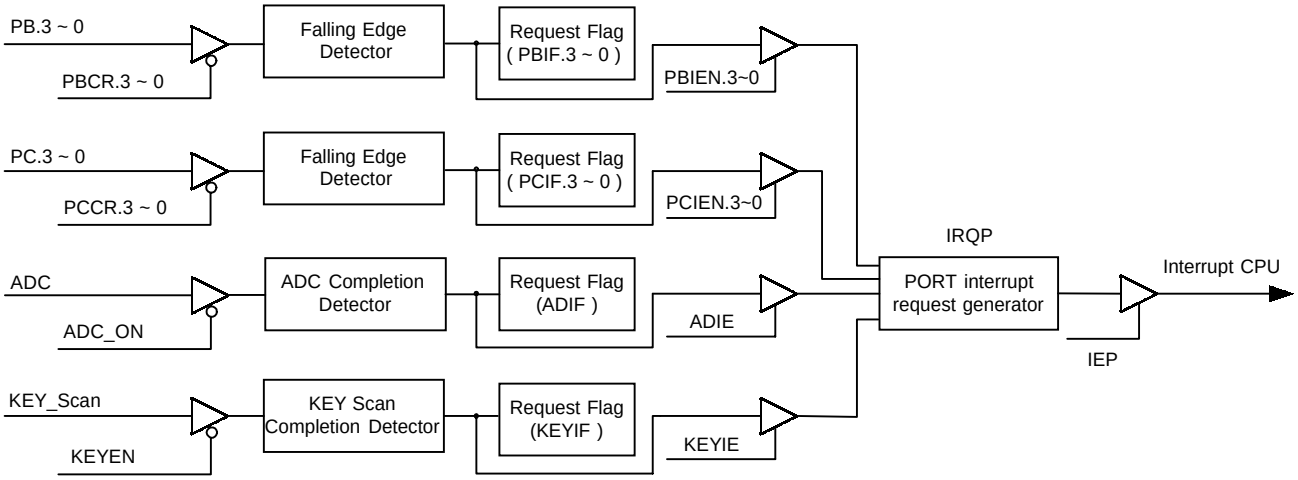
Other external Interrupt Enable Flags Register: $38C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38C	-	-	KEYIE	ADIE	R/W	Bit0: AD interrupt enable flag Bit1: Key scan interrupt enable flag

Other external Interrupt Request Flags Register: $38D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38D	-	-	KEYIF	ADIF	R/W	Bit0: AD interrupt request flag Bit1: Key scan interrupt request flag

Only writing these bits to 0 is available.



Port (including other external sources) Interrupt function block-diagram

16.Dual Tone

(a)Tone Generator Control Register

SH69P55 has two 12-bit tone generators. The tone generators generate the specific frequency of tone with square wave.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3A3	TG1.3	TG1.2	TG1.1	TG1.0	R/W	Tone generator 1 low nibble
$3A4	TG1.7	TG1.6	TG1.5	TG1.4	R/W	Tone generator 1 middle nibble
$3A5	TG1.11	TG1.10	TG1.9	TG1.8	R/W	Tone generator 1 high nibble
$3A6	TG2.3	TG2.2	TG2.1	TG2.0	R/W	Tone generator 2 low nibble
$3A7	TG2.7	TG2.6	TG2.5	TG2.4	R/W	Tone generator 2 middle nibble
$3A8	TG2.11	TG2.10	TG2.9	TG2.8	R/W	Tone generator 2 high nibble

(b) Tone Generator Volume Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$3A9	TV1.3	TV1.2	TV1.1	TV1.0	R/W	Tone generator 1 volume low nibble
$3AA	TG1EN	TV1.6	TV1.5	TV1.4	R/W	Tone generator 1 volume high nibble TG1EN: Tone generator 1 enable
$3AB	TV2.3	TV2.2	TV2.1	TV2.0	R/W	Tone generator 2 volume low nibble
$3AC	TG2EN	TV2.6	TV2.5	TV2.4	R/W	Tone generator 2 volume high nibble TG2EN: Tone generator 2 enable

The volume control register is 7-bit register used to control the output level of the tone generator.

TGxEN: Tone generator X enable

0: Tone generator X disable (default)

1: Tone generator X enable

Note: x = 1 or 2

(c) Programming notice

Never execute the "HALT" or "STOP" instruction while the Tone Generator are playing.

Music Table 1.

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSX = 4MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B2	123.47	4050	02E	123.46	-0.01	#F5	739.99	676	D5C	739.64	-0.05
C3	130.81	3822	112	130.82	0.01	G5	783.99	638	D82	783.70	-0.04
#C3	138.59	3608	1E8	138.58	-0.01	#G5	830.61	602	DA6	830.56	-0.01
D3	146.83	3405	2B3	146.84	0.01	A5	880.00	568	DC8	880.28	0.03
#D3	155.56	3214	372	155.57	0.00	#A5	932.33	536	DE8	932.84	0.06
E3	164.81	3034	426	164.80	-0.01	B5	987.77	506	E06	988.14	0.04
F3	174.61	2863	4D1	174.64	0.02	C6	1046.5	478	E22	1046.0	-0.05
#F3	185.00	2703	571	184.98	-0.01	#C6	1108.7	451	E3D	1108.7	-0.01
G3	196.00	2551	609	196.00	0.00	D6	1174.7	426	E56	1173.7	-0.08
#G3	207.65	2408	698	207.64	-0.01	#D6	1244.5	402	E6E	1243.8	-0.06
A3	220.00	2273	71F	219.97	-0.01	E6	1318.5	379	E85	1319.3	0.06
#A3	233.08	2145	79F	233.10	0.01	F6	1396.9	358	E9A	1396.7	-0.02
B3	246.94	2025	817	246.91	-0.01	#F6	1480.0	338	EAE	1479.3	-0.05
C4	261.63	1911	889	261.64	0.01	G6	1568.0	319	EC1	1567.4	-0.04
#C4	277.18	1804	8F4	277.16	-0.01	#G6	1661.2	301	ED3	1661.1	-0.01
D4	293.66	1703	959	293.60	-0.02	A6	1760.0	284	EE4	1760.6	0.03
#D4	311.13	1607	9B9	311.14	0.00	#A6	1864.7	268	EF4	1865.7	0.05
E4	329.63	1517	A13	329.60	-0.01	B6	1975.5	253	F03	1976.3	0.04
F4	349.23	1432	A68	349.16	-0.02	C7	2093.0	239	F11	2092.1	-0.05
#F4	369.99	1351	AB9	370.10	0.03	#C7	2217.5	225	F1F	2222.2	0.22
G4	392.00	1276	B04	391.85	-0.04	D7	2349.3	213	F2B	2347.4	-0.08
#G4	415.30	1204	B4C	415.28	-0.01	#D7	2489.0	201	F37	2487.6	-0.06
A4	440.00	1136	B90	440.14	0.03	E7	2637.0	190	F42	2631.6	-0.21
#A4	466.16	1073	BCF	465.98	-0.04	F7	2793.8	179	F4D	2793.3	-0.02
B4	493.88	1012	C0C	494.07	0.04	#F7	2960.0	169	F57	2958.6	-0.05
C5	523.25	956	C44	523.01	-0.05	G7	3136.0	159	F61	3144.7	0.28
#C5	554.37	902	C7A	554.32	-0.01	#G7	3322.4	150	F6A	3333.3	0.33
D5	587.33	851	CAD	587.54	0.04	A7	3520.0	142	F72	3521.1	0.03
#D5	622.25	804	CDC	621.89	-0.06	#A7	3729.3	134	F7A	3731.3	0.05
E5	659.26	758	D0A	659.63	0.06	B7	3951.1	127	F81	3937.0	-0.36
F5	698.46	716	D34	698.32	-0.02	C8	4186.0	119	F89	4201.7	0.37

Music Table 2.

Following is the music scale reference table for the Tone Generator channel 1(or channel 2) under OSX =2MHz.

Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%	Note	Ideal freq.	N	TGCR (TGx.11 - TGx.0) (x = 1 or 2)	Real freq.	Error%
B1	61.73	4050	2E	61.73	0.00	C5	523.25	478	E22	523.01	-0.05
C2	65.10	3840	100	65.10	0.00	#C5	554.37	451	E3D	554.32	-0.01
#C2	69.29	3608	1E8	69.29	0.00	D5	587.33	426	E56	586.85	-0.08
D2	73.42	3405	2B3	73.42	0.00	#D5	622.25	402	E6E	621.89	-0.06
#D2	77.78	3214	372	77.78	0.00	E5	659.26	379	E85	659.63	0.06
E2	82.41	3034	426	82.40	-0.01	F5	698.46	358	E9A	698.32	-0.02
F2	87.31	2863	4D1	87.32	0.01	#F5	739.99	338	EAE	739.64	-0.05
#F2	92.50	2703	571	92.49	-0.01	G5	783.99	319	EC1	783.70	-0.04
G2	98.00	2551	609	98.00	0.00	#G5	830.61	301	ED3	830.56	-0.01
#G2	103.82	2408	698	103.82	0.00	A5	880.00	284	EE4	880.28	0.03
A2	110.00	2273	71F	109.99	-0.01	#A5	932.33	268	EF4	932.84	0.06
#A2	116.54	2145	79F	116.55	0.01	B5	987.77	253	F03	988.14	0.04
B2	123.47	2025	817	123.46	-0.01	C6	1046.5	239	F11	1046.0	-0.05
C3	130.81	1911	889	130.82	0.01	#C6	1108.7	225	F1F	1111.1	0.22
#C3	138.59	1804	8F4	138.58	-0.01	D6	1174.7	213	F2B	1173.7	-0.08
D3	146.83	1703	959	146.80	-0.02	#D6	1244.5	201	F37	1243.8	-0.06
#D3	155.56	1607	9B9	155.57	0.00	E6	1318.5	190	F42	1315.8	-0.21
E3	164.81	1517	A13	164.80	-0.01	F6	1396.9	179	F4D	1396.7	-0.02
F3	174.61	1432	A68	174.58	-0.02	#F6	1480.0	169	F57	1479.3	-0.05
#F3	185.00	1351	AB9	185.05	0.03	G6	1568.0	159	F61	1572.3	0.28
G3	196.00	1276	B04	195.92	-0.04	#G6	1661.2	150	F6A	1666.7	0.33
#G3	207.65	1204	B4C	207.64	-0.01	A6	1760.0	142	F72	1760.6	0.03
A3	220.00	1136	B90	220.07	0.03	#A6	1864.7	134	F7A	1865.7	0.05
#A3	233.08	1073	BCF	232.99	-0.04	B6	1975.5	127	F81	1968.5	-0.36
B3	246.94	1012	C0C	247.04	0.04	C7	2093.0	119	F89	2100.8	0.37
C4	261.63	956	C44	261.51	-0.04	#C7	2217.5	113	F8F	2212.4	-0.23
#C4	277.18	902	C7A	277.16	-0.01	D7	2349.3	106	F96	2358.5	0.39
D4	293.66	851	CAD	293.77	0.04	#D7	2489.0	100	F9C	2500.0	0.44
#D4	311.13	804	CDC	310.95	-0.06	E7	2637.0	95	FA1	2631.6	-0.21
E4	329.63	758	D0A	329.82	0.06	F7	2793.8	89	FA7	2809.0	0.54
F4	349.23	716	D34	349.16	-0.02	#F7	2960.0	84	FAC	2976.2	0.55
#F4	369.99	676	D5C	369.82	-0.05	G7	3136.0	80	FB0	3125.0	-0.35
G4	392.00	638	D82	391.85	-0.04	#G7	3322.4	75	FB5	3333.3	0.33
#G4	415.30	602	DA6	415.28	-0.01	A7	3520.0	71	FB9	3521.1	0.03
A4	440.00	568	DC8	440.14	0.03	#A7	3729.3	67	FBD	3731.3	0.05
#A4	466.16	536	DE8	466.42	0.06	B7	3951.1	63	FC1	3968.3	0.44
B4	493.88	506	E06	494.07	0.04	C8	4186.0	60	FC4	4166.7	-0.46

17.Watchdog Timer (WDT)

Watchdog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that the WDT will always run even in the STOP mode (if it is enabled). The watchdog timer automatically generates a device reset when it overflows. Code option can enable and disable this function. The watchdog timer control register (WDT bit2 ~ 0) can be used to select different overflow frequency. WDT bit3 is the watchdog timer overflow flag.

If the watchdog timer is enabled, the CPU will be reset and the WDT bit3 is automatically set to "1" by the relevant circuit when the watchdog timer overflows. Repeat read or write the WDT register ($1F), the watchdog timer should re-count before the overflow happens.

System Register $1F: (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1F	WD	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control Bit3: Watchdog timer overflow flag (Read only)
	X	0	0	0	R/W	Watchdog timer-out period = 4096ms
	X	0	0	1	R/W	Watchdog timer-out period = 1024ms
	X	0	1	0	R/W	Watchdog timer-out period = 256ms
	X	0	1	1	R/W	Watchdog timer-out period = 128ms
	X	1	0	0	R/W	Watchdog timer-out period = 64ms
	X	1	0	1	R/W	Watchdog timer-out period = 16ms
	X	1	1	0	R/W	Watchdog timer-out period = 4ms
	X	1	1	1	R/W	Watchdog timer-out period = 1ms
	0	X	X	X	R	No watchdog timer overflow reset
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer-out period valid for V_{DD} = 5V.

18.HALT and STOP Mode

After the execution of HALT instruction, the device will enter the halt mode. In the halt mode, CPU will stop operating. But peripheral circuits (Timer0, Timer1, Timer2, ADC, PWM and watchdog timer) will keep operating.

After the execution of STOP instruction, the device will enter the stop mode. In the stop mode, the whole chip (including the oscillator) will stop operating without watchdog timer if it is enabled.

In HALT mode, SH69P55 can be waked up if any interrupt occurs.

In STOP mode, SH69P55 can be waked up if any port interrupt (excluding AD interrupt and key scan interrupt) occurs or watchdog timer overflows (WDT is enabled).

19.Warm-up Timer

The device builds in oscillator warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

Power on reset warm-up time interval:

The warm-up counter prescaler is divided by 2^{13} (8192).

Other reset warm-up time interval:

In RC oscillator mode, the warm-up counter prescaler is divided by 2^{7} (128).

In crystal oscillator or ceramic resonator mode, the warm-up counter prescaler is divided by 2^{12} (4096).

NOTE:

In STOP mode, when SH69P55 is waked up, the warn-up time interval:

System clock	32.768kHz in stop	warn-up time interval
PLL	On	2^{7}
	Off	2^{12}
32.768kHz	On	2^{2}
	Off	2^{12}

20.System Clock Monitor (SCM)

SH69P55 has an internal basic RC oscillator, except the main oscillator witch can be selected by the Code option. The main oscillator provides system clock for mcu, if it runs normally. The internal basic RC oscillator provides clock signal for WDT function and SCM function. The internal basic RC oscillator runs all times as soon as mcu is powered on except that WDT function is disabled and mcu is in STOP mode.

The built-in SCM can switch the system clock to the internal basic RC oscillator and set system clock failure flag (SCF bit0 in $17) to 1 when the main oscillator fails. If the main oscillator comes back, SCM switches the system clock to the main oscillator and clears the SCF automatically.

System Register: $17

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	LVR	-	-	SCF	R/W	Bit3: Low Voltage Reset flag (Read and Write 0 only) Bit0: System clock fail flag (Read and Write 0 only)
	X	X	X	0	R/W	System clock is normal
	X	X	X	1	R/W	System clock fails

Note:

If SCF is cleared, the SCM switches the system clock to the original automatically.

21. Code option

(a) Oscillator type:

- **Internal RC Oscillator :** (Select OSCO pin as PORTC1 and OSCI pin as PORTC2 for normal I/O ports.)
- **External RC Oscillator (400kHz ~ 8MHz):** (Select OSCO pin as PORTC1 for a normal I/O port.)
- **Ceramic Resonator (400kHz ~ 8MHz):** The system oscillation is provided by the ceramic resonator connected between OSCI and OSCO pins.
- **Crystal Oscillator (400kHz ~ 8MHz):** The system oscillation is provided by the crystal oscillator connected between OSCI and OSCO pins.
- **32.768kHz Crystal Oscillator:** The system oscillation is provided by the crystal (32.768kHz) oscillator connected between OSCI and OSCO pins.

(b) Watchdog Timer (WDT):

- **Enable:** Enable WDT function.
- **Disable:** Disable WDT function.

(c) Low Voltage Reset:

- **Disable:** Disable LVR function.
- **Enable:** Enable LVR function.

(d) LVR voltage Range:

- **4V:** Generate an internal reset signal when $V_{DD} \leq 4V$ if LVR is enabled.
- **2.5V:** Generate an internal reset signal when $V_{DD} \leq 2.5V$ if LVR is enabled.

(e) Chip pin Reset:

- **Enable:** The pin reset function is enabled.
- **Disable:** The pin reset function is disabled. (Select RESET pin as PORTC3.)

Instructions

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

(a) Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

(b) Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

2. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

3. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

4. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

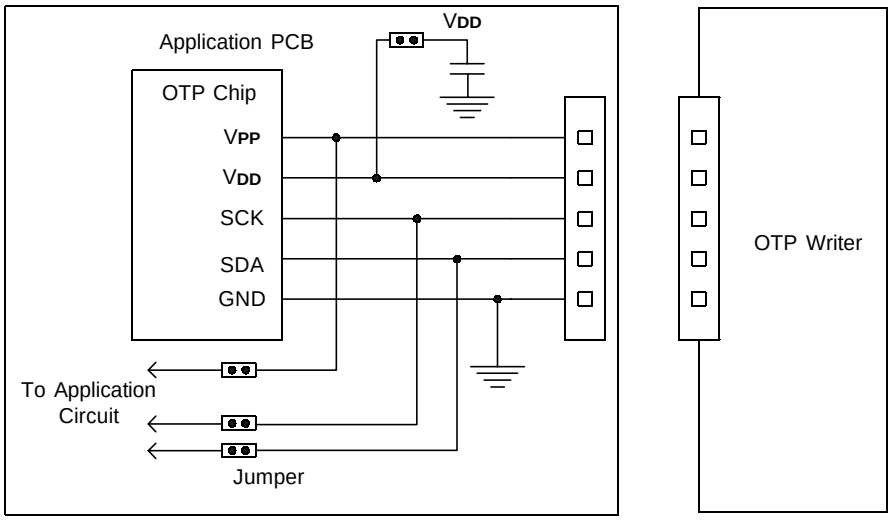
PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

In System Programming Notice for OTP

The In System Programming technology is valid for SinoWealth OTP chip.

The Programming Interface of the OTP chip must be set on the user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended step is as follow for these jumpers:

(1) The jumper is Open to separate the programming pins from the application circuit before programming the code.

(2) Connect the programming interface with OTP Writer and Begin Programming code.

(3) Disconnect OTP writer and short these jumpers when programming is finished.

For more detail information, please refer to the OTP writer user manual.

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input / Output Voltage . . . . . GND-0.3V to VDD+0.3V

Operating Ambient Temperature . . . . . .-40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

1. DC Electrical Characteristics

(a) GND = 0V, T_A = -40℃ to +85℃, F_{OSC} = 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	
Operating Current	I_{OP}	-	1.5	2	mA	All output pins unloaded, WDT off, ADC disable, LVR off, LCD off, Key scan disable (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	-	800	μA	All output pins unload, WDT off, ADC disable LCD off, Key scan disable
Stand by Current (STOP)	I_{SB2}	-	-	10	μA	All output pins unload, WDT off, ADC disable LCD off, Key scan disable, 32.768kHz on, if 32.768kHz is selected
Stand by Current (STOP)	I_{SB3}	-	-	1	μA	All output pins unload, WDT off, ADC disable LCD off, Key scan disable
Input Low Voltage	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input Low Voltage	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger)
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger)
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN}=V_{DD} or GND
Pull-up Resistor	R_{PH}		30		KΩ	V_{DD} =5.0V, V_{IN}=GND
Output High Voltage	V_{OH1}	V_{DD} – 0.7	-	-	V	I/O ports, I_{OH} = -10mA
Output Low Voltage	V_{OL1}	-	-	GND + 0.6	V	I/O ports, IOL = 20mA (exclude PORTD, PORTE [1:0])
Output Low Voltage	V_{OL2}	-	-	GND + 1	V	I/O ports, I_{OL} = 200mA (PORTD, PORTE [1:0])
WDT Current	I_{WDT}	-	-	20	μA	STOP, WDT on, ADC disable, LVR off
LCD Driving on resistor	R_{ON}		5		KΩ	LCD COMx, LCD SEGx, the voltage variation of V1, V2, V3, is less than 0.2V.
LCD voltage divider resistor	R_{LCD}	-	90 10	-	KΩ	RLCD=0 RLCD=1

Note:

Max. Current into V_{DD} =200mA

Max. Current out of Vss=250mA

(b) GND = 0V, T_A = -40℃ to +85℃, F_{OSC} = 4MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	5.0	5.5	V	
Operating Current	I_{OP}	-	1.0	1.5	mA	All output pins unloaded, WDT off, ADC disable, LVR off, LCD off, Key scan disable (Execute NOP instruction)
Stand by Current (HALT)	I_{SB1}	-	-	500	μA	All output pins unload, WDT off, ADC disable LCD off, Key scan disable
Stand by Current (STOP)	I_{SB2}	-	-	10	μA	All output pins unload, WDT off, ADC disable LCD off, Key scan disable, 32.768kHz on, if 32.768kHz is selected
Stand by Current (STOP)	I_{SB3}	-	-	1	μA	All output pins unload, WDT off, ADC disable LCD off, Key scan disable
Input Low Voltage	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports, pins tri-state
Input Low Voltage	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger)
Input High Voltage	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports, pins tri-state
Input High Voltage	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T2, OSCI (Schmitt trigger)

*: Data in “Typ.” column is at 5.0V, 25℃,unless otherwise specified.

2. AC Electrical Characteristics

(a) VDD = 2.4V ~ 5.5V, GND = 0V, TA = 25°C, FOSC = 30KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	T_{CY}	0.5	-	133.4	μs	
T0/T2 input width	t_{IW}	$(T_{CY} + 40)/N$	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	$t_{IW}/2$	-	-	ns	

(b) VDD = 2.4V ~ 5.5V, GND = 0V, TA = 25°C, FOSC = 30KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width	t_{RESET}	10	-	-	μs	Low active
WDT Period	T_{WDT}	1	-	-	ms	
Frequency Variation	|ΔF|/F	-	-	15	%	External R_{OSC} Oscillator, Include chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)
Frequency Variation	|ΔF|/F	-	-	20	%	Internal R_{OSC} Oscillator, F_{OSC} = 2MHz, 4MHz, 6MHz. Include chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)

3. A/D Converter Electrical Characteristics

(a) V_{DD} = 2.4V ~ 5.5V, GND = 0V, T_A = 25℃, F_{OSC} = 30KHz ~ 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	NR	-	10	-	bit	$GND \le V_{AIN} \le V_{REF}$
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor	R_{AIN}	2	1000	-	MΩ	V_{IN}=5.0V
A/D conversion current	I_{AD}	-	1	3	mA	A/D converter module operating, V_{DD}=5.0V
A/D Input current	IADIN			10	μA	V_{DD} = 5.0V
Differential linearity error	DLE	-	-	±1	LSB	V_{REF} = V_{DD} = 5.12V, F_{OSC}=8MHz
Integral linearity error	ILE			±2	LSB	V_{REF} = V_{DD} = 5.12V, F_{OSC}=8MHz
Full scale error	E_F	-	±1	±3	LSB	V_{REF} = V_{DD} = 5.12V, F_{OSC}=8MHz
Offset error	E_Z	-	±0.5	±2	LSB	V_{REF} = V_{DD} = 5.12V, F_{OSC}=8MHz
Total Absolute error	E_{AD}	-	-	±3	LSB	V_{REF} = V_{DD} = 5.12V, F_{OSC}=8MHz
Conversion time	T_{CON}	25	-	-	μs	10 bit resolution and F_{OSC}=8MHz

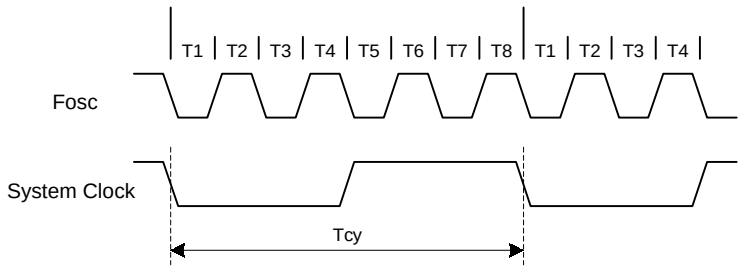
Low Voltage Reset Electrical Characteristics

(a) VDD = 3.0V ~ 5.5V, GND = 0V, TA = 25°C, FOSC = 32.768KHz ~ 8MHz, unless otherwise specified.

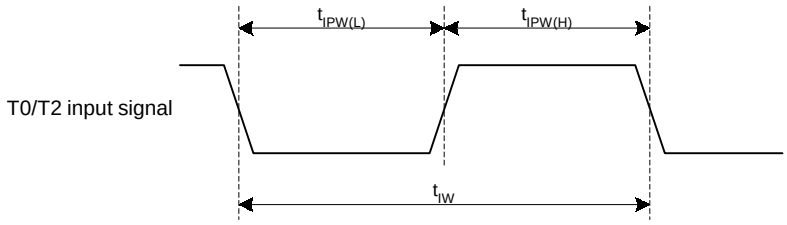
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage (High)	V_{LVR1}	3.8	-	4.2	V	LVR enable
LVR Voltage (Low)	V_{LVR2}	2.3	-	2.7	V	LVR enable
LVR Voltage Pulse Width	t_{LVR}	500	-	-	μs	$V_{DD} \le V_{LVR}$

Timing Waveform

(a) System Clock Timing Waveform



(b) T0/T2 Input Waveform

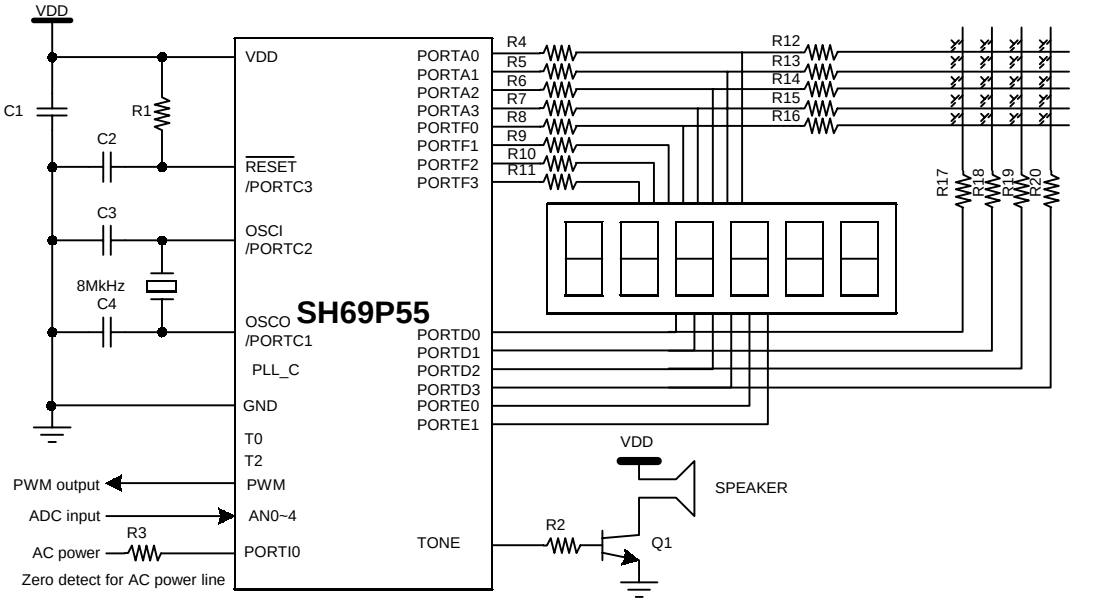


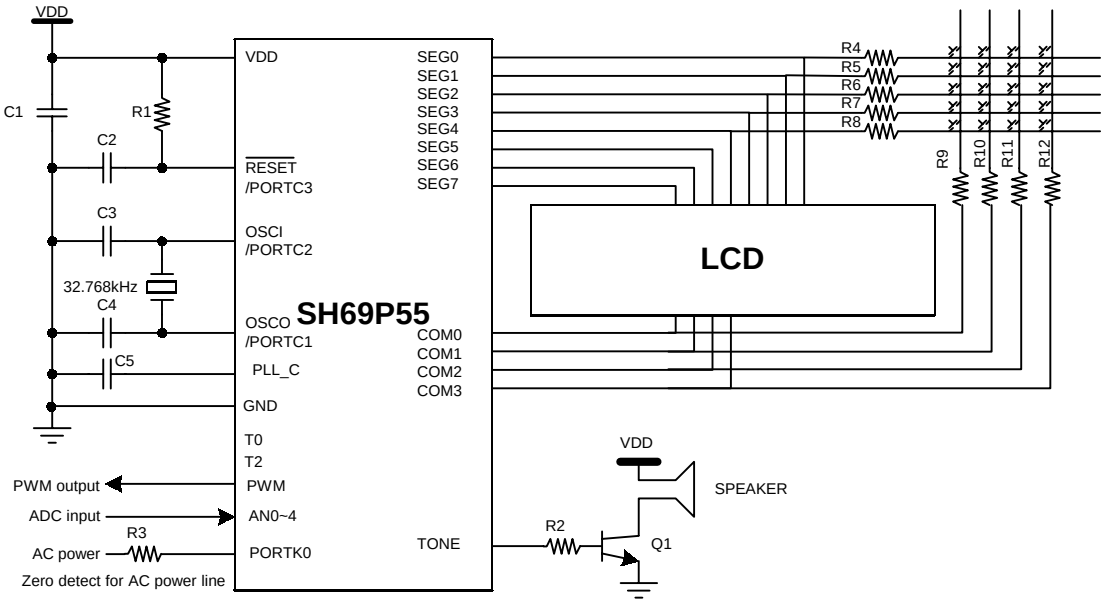
Application Circuit (for reference only)

AP1:

Function:

LED driver, automatic key scan, Zero Cross Detect function for AC Power line, Tone output, ADC,





Product SPEC. Change Notice

SH69P44 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	July. 2004