SH69P561/K561

OTP/MASK 4K 4-bit Micro-controller With LCD Driver & 8-bit SAR ADC

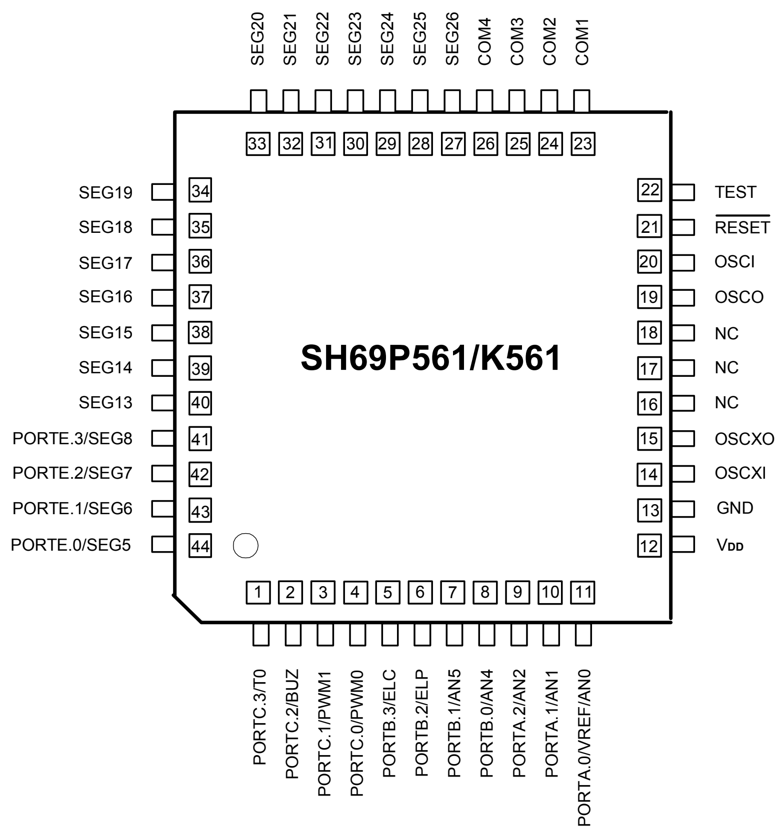
Features

- SH6610D-Based Single-Chip 4-bit Micro-Controller With LCD Driver & 8-bit SAR ADC
- OTP ROM: 4K X 16 bits (SH69P561)
- MASK ROM: 4K X 16 bits (SH69K561)
- RAM: 274 X 4bits
  - 58 System control register
  - 216 Data memory
  - 72 bits LCD RAM
- Operation Voltage:
  - f_{OSC} = 32.768kHz - 4MHz, V_{DD} = 2.4V - 5.5V
  - f_{OSC} = 4MHz - 8MHz, V_{DD} = 4.5V - 5.5V
- 15 CMOS Bi-directional I/O Pins
- 8-Level Stack (Including Interrupts)
- Two 8-bit Auto Re-Loaded Timer/Counter
- Warm-Up Timer
- Powerful Interrupt Sources:
  - A/D Interrupt
  - Timer0 Interrupt
  - Timer1 Interrupt
  - External Interrupts: PORTB (Rising/Falling Edge)
- 2 Clock Oscillator
  OSC:
  - Crystal Oscillator: 32.768kHz
  - RC Oscillator: 262kHz
  OSCX:
  - Ceramic/Crystal Oscillator: 400kHz - 8MHz
  - RC Oscillator: 400kHz - 8MHz
- Instruction Cycle Time (4/f_{OSC})
- Two Low Power Operation Modes: HALT And STOP
- Reset
  - Built-in Watchdog Timer (WDT) (Code Option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR) (Code Option)
- LCD Driver:
  18SEG X 4COM (1/4 duty, 1/3 bias)
- 2 Channels 10-bit PWM output
- 5 Channels 8-bit Resolution Analog/Digital Converter (ADC)
- Built-in Pull-high/Pull-low Resistor for PORTA - PORTE
- Built-in Alarm Generator
- Built-in Electroluminescent Light (EL-light) Driver
- ROM Data Read Table function
- Zero Cross Detect function for AC Power Line
- LCD shared as LED matrix (Code Option)
- LCD SEG 9-28 shared with scan output
- OTP type & Code Protect (SH69P561)
- MASK type (SH69K561)
- 44-pin QFP package

General Description

SH69P561/69K561 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, RAM, ROM, timer, LCD driver, I/O ports, EL-light driver, watchdog timer, 5 channels 8-bit ADC, alarm generator, low voltage reset, 2 channels 10-bit high speed PWM output, zero cross detect function. This chip builds in a dual-oscillator to enhance the total chip performance. SH69P561/69K561 is suitable for the home appliance application.

Pin Configuration (44 QFP Package)



Pin Description (44 QFP Package)

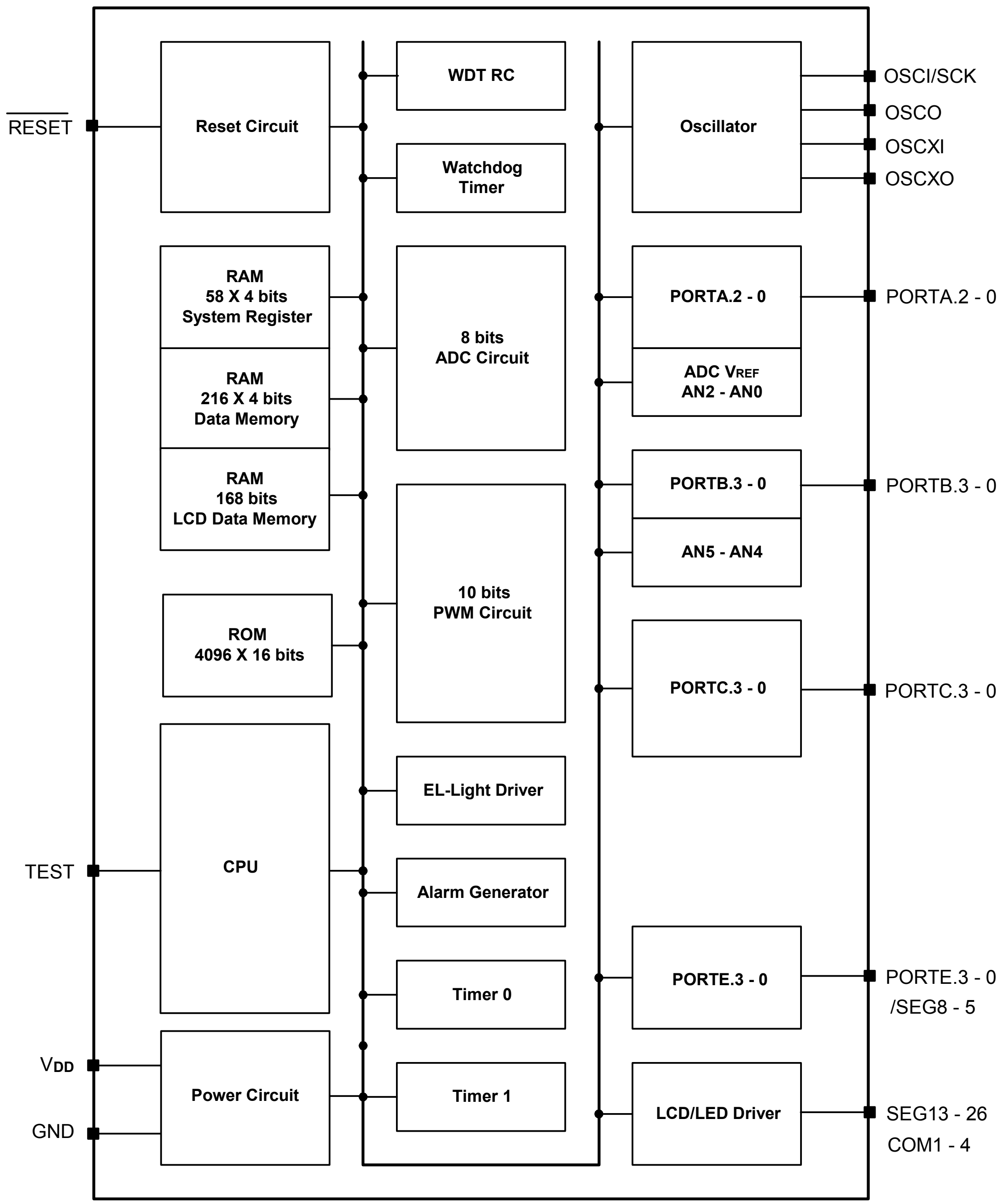
Pin No.	Pin Name	I/O	Description
1	PORTC.3 /T0	I/O I	Bit programmable I/O Shared with T0 input
2	PORTC.2 /BUZ	I/O O	Bit programmable I/O Shared with BUZ output
3	PORTC.1 /PWM1	I/O O	Bit programmable I/O Shared with PWM1 output
4	PORTC.0 /PWM0	I/O O	Bit programmable I/O Shared with PWM0 output
5 - 6	PORTB.3 - 2 /ELC-ELP	I/O I O	Bit programmable I/O Vector interrupt (active falling/rising edge) Shared with EL-light driving circuit output
7 - 8	PORTB.1 - 0 /AN5 - AN4	I/O I I	Bit programmable I/O Vector interrupt (active falling/rising edge) Shared with ADC input channel AN5 - AN4
9 - 10	PORTA.2 - 1 /AN2 - AN1	I/O I	Bit programmable I/O Shared with ADC input channel AN2 - AN1
11	PORTA.0 /VREF /AN0	I/O I I	Bit programmable I/O Shared with external ADC V_{REF} input Shared with ADC input channel AN0
12	V_{DD}	P	Power supply pin
13	GND	P	Ground pin
14	OSCXI	I	OSCX input connected to high-frequency ceramic/crystal oscillator or external resistor
15	OSCXO	O	OSCX output connected to high-frequency ceramic/crystal oscillator
19	OSCO	O	OSC output connected to low-frequency crystal oscillator
20	OSCI	I	OSC input connected to low-frequency crystal or external resistor
21	$\overline{RESET}$	I	Reset input (active low, Schmitt trigger input)
22	TEST	I	Test pin pull-low internally (No connection for users)
23 - 26	COM1 - 4	O	Common signal output for LCD display
27 - 40	SEG26 - 13	O	Segment signal output for LCD display shared with output port
41 - 44	PORTE.3 - 0 /SEG8 - 5	I/O O	Bit programmable I/O Shared with SEG8 - 5
16 - 18	NC		No connection for users

OTP Programming Pin Description* (44 QFP Package)

Pin No.	Symbol	I/O	Sharing Pin	Description
12	V_{DD}	P	V_{DD}, AV_{DD}	Programming Power supply (+5.5V)
21	V_{PP}	P	$\overline{RESET}$	Programming high voltage Power supply (+11.0V)
13	GND	P	AGND, GND	Ground
20	SCK	I	OSCI	Programming Clock input Pin/Pad
11	SDA	I/O	PORTA.0	Programming Data Pin/Pad

*: Only SH69P561 has the OTP Program Mode, SH69K561 has not the OTP Program Mode

Block Diagram



Functional Descriptions

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H--3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - Bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O: $000 - $027, $380 - $391
Data memory: $028 - $0FF
LCD RAM space: $304 - $319, $35C - $369

RAM Bank Table:

Bank 0 B = 0	**Bank 1** B = 1	**Bank 6** B = 6	**Bank 7** B = 7
$028 - $07F	$080 - $0FF	$300 - $37F	$380 - $3FF

Where, B: RAM bank bit use in instructions

2.2. Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEPB	R/W	Interrupt enable flags register
$01	IRQAD	IRQT0	IRQT1	IRQPB	R/W	Interrupt request flags register
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter high nibble register
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter low nibble register
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter high nibble register
$08	0	PA.2	PA.1	PA.0	R/W	Bit2-0: PORTA data register **Bit3 must be cleared to "0" by the User's program and always be kept up.** **Refer to I/O note**
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	0	0	0	0	R/W	**All bits of this register must be cleared to "0" by the User's program and always be kept up.** **Refer to I/O note**
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PULLEN	PH/PL	OXS	OXON	R/W	Bit0: Turn on OSCX oscillator control register Bit1: System clock control register Bit2: Port pull-high and falling edge interrupt or pull-low and rising edge interrupt control register Bit3: Port pull-high/low enable control register
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	T0S1	T0E1	T0S0	T0E0	R/W	Bit0: T0 clock edge in Timer0 control register Bit1: Timer0 clock source control register Bit2: T0 clock edge in Timer1 control register Bit3: Timer1 clock source control register
$14	PIEN.3	PIEN.2	PIEN.1	PIEN.0	R/W	Bit3-0: PORTB interrupt enable flags register
$15	PIF.3	PIF.2	PIF.1	PIF.0	R/W	Bit3-0: PORTB interrupt request flags register
$16	-	ALMF1	ALMF0	PAM0	R/W	Bit0: Alarm output enable control register Bit2-1: Alarm carrier frequency control register
$17	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
$18	1	PACR.2	PACR.1	PACR.0	R/W	Bit2-0: PORTA input/output control register **Bit3 must be set to "1" by the User's program and always be kept up.** **Refer to I/O note**
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	1	1	1	1	R/W	**All bits of this register must be set to "1" by the User's program and always be kept up.** **Refer to I/O note**
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register

Configuration of System Register (Continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1D	-	ELF	ELPF	ELON	R/W	Bit0: EL-light on/off control register Bit1: EL-light driver charge frequency control register Bit2: EL-light driver discharge frequency control register
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: WDT overflow flag register
$1F	-	-	-	-	-	Reserved
$20	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: ADC port configuration control register Bit3: Internal/External reference voltage control register
$21	ADCON	CH2	CH1	CH0	R/W	Bit2-0: ADC channel control register Bit3: ADC module operate control register
$22	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: A/D Conversion Time control register Bit2-1: A/D Clock Period control register Bit3: ADC status flag register
$23	A3	A2	A1	A0	R	ADC data low nibble register
$24	A7	A6	A5	A4	R	ADC data high nibble register
$25	-	LCDON	RLCD1	RLCD0	R/W	Bit1-0: Set LCD bias resistor register Bit2: LCD display on control register
$26	LPS1	LPS0	0	1	R/W	**Bit0 must be set to "1" by the User's program and always be kept up.** **Bit1 must be cleared to "0" by the User's program and always be kept up.** Bit3-2: Different LCD frame frequency control register
$27	LVD	O/S2	O/S1	0	R/W	**Bit0 must be cleared to "0" by the User's program and always be kept up.** **Refer to LCD note** Bit1: PORTE as LCD SEG5-8 control register Bit2: LCD SEG13-26 as output control register Bit3: LCD Voltage degrade control register
$380	PWM0S	T0CK1	T0CK0	PWM0	R/W	Bit0: PWM0 output enabled control register Bit2-1: PWM0 clock control register Bit3: PWM0 output mode of duty cycle control register
$381	PWM1S	T1CK1	T1CK0	PWM1	R/W	Bit0: PWM1 output enabled control register Bit2-1: PWM1 clock control register Bit3: PWM1 output mode of duty cycle control register
$382	PP0.3	PP0.2	PP0.1	PP0.0	R/W	PWM0 period low nibble register
$383	PP0.7	PP0.6	PP0.5	PP0.4	R/W	PWM0 period middle nibble register
$384	-	-	PP0.9	PP0.8	R/W	Bit1-0: PWM0 period high register
$385	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble register
$386	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty middle nibble register
$387	-	-	PD0.9	PD0.8	R/W	Bit1-0: PWM0 duty high register
$388	PP1.3	PP1.2	PP1.1	PP1.0	R/W	PWM1 period low nibble register
$389	PP1.7	PP1.6	PP1.5	PP1.4	R/W	PWM1 period middle nibble register
$38A	-	-	PP1.9	PP1.8	R/W	Bit1-0: PWM1 period high register
$38B	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble register
$38C	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty middle nibble register
$38D	-	-	PD1.9	PD1.8	R/W	Bit1-0: PWM1 duty high register
$38E	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$38F	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$390	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$391	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

3. ROM

The ROM can address 4096 X 16 bits of program area from $000 to $FFF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to ADC interrupt service routine
$002	JMP*	Jump to TIMER0 interrupt service routine
$003	JMP*	Jump to TIMER1 interrupt service routine
$004	JMP*	Jump to PORTB interrupt service routine

*JMP instruction can be replaced by any instruction.

3.2. ROM Data Read Table (RDT)

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$38E	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$38F	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$390	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$391	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 12-bit write-only PC address load register (RDT.11 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should fill 0 to higher 4 bits (RDT.15 - 12) first, then write the ROM table address to RDT register (high nibble first then low nibble), after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into $38E will start the data read-out action).

4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset /LVR	WDT Reset
$00	IEAD	IET0	IET1	IEPB	0000	0000
$01	IRQAD	IRQT0	IRQT1	IRQPB	0000	0000
$02	-	T0M.2	T0M.1	T0M.0	-000	-uuu
$03	-	T1M.2	T1M.1	T1M.0	-000	-uuu
$04	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	xxxx
$05	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	xxxx
$06	T1L.3	T1L.2	T1L.1	T1L.0	xxxx	xxxx
$07	T1H.3	T1H.2	T1H.1	T1H.0	xxxx	xxxx
$08	-	PA.2	PA.1	PA.0	x000	x000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	-	-	-	-	xxxx	xxxx
$0C	PE.3	PE.2	PE.1	PE.0	0000	0000
$0D	PULLEN	PH/PL	OXS	OXON	0100	01uu
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	T0S1	T0E1	T0S0	T0E0	0000	uuuu
$14	PIEN.3	PIEN.2	PIEN.1	PIEN.0	0000	uuuu
$15	PIF.3	PIF.2	PIF.1	PIF.0	0000	0000
$16	-	ALMF1	ALMF0	PAM0	-000	-uu0
$17	AEC3	AEC2	AEC1	AEC0	0000	uuuu
$18	-	PACR.2	PACR.1	PACR.0	x000	x000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	-	-	-	-	xxxx	xxxx
$1C	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1D	-	ELF	ELPF	ELON	-000	-uu0
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	1000
$1F	-	-	-	-	----	----
$20	VREFS	ACR2	ACR1	ACR0	0000	uuuu
$21	ADCON	CH2	CH1	CH0	0000	0uuu
$22	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	0000	0uuu

System Register States (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset /LVR	WDT Reset
$23	A3	A2	A1	A0	xxxx	uuuu
$24	A7	A6	A5	A4	xxxx	uuuu
$25	-	LCDON	RLCD1	RLCD0	-000	-uuu
$26	LPS1	LPS0	-	-	00xx	uuxx
$27	LVD	O/S2	O/S1	-	000x	u00x
$380	PWM0S	T0CK1	T0CK0	PWM0	0000	uuu0
$381	PWM1S	T1CK1	T1CK0	PWM1	0000	uuu0
$382	PP0.3	PP0.2	PP0.1	PP0.0	xxxx	uuuu
$383	PP0.7	PP0.6	PP0.5	PP0.4	xxxx	uuuu
$384	-	-	PP0.9	PP0.8	--xx	--uu
$385	PD0.3	PD0.2	PD0.1	PD0.0	xxxx	uuuu
$386	PD0.7	PD0.6	PD0.5	PD0.4	xxxx	uuuu
$387	-	-	PD0.9	PD0.8	--xx	--uu
$388	PP1.3	PP1.2	PP1.1	PP1.0	xxxx	uuuu
$389	PP1.7	PP1.6	PP1.5	PP1.4	xxxx	uuuu
$38A	-	-	PP1.9	PP1.8	--xx	--uu
$38B	PD1.3	PD1.2	PD1.1	PD1.0	xxxx	uuuu
$38C	PD1.7	PD1.6	PD1.5	PD1.4	xxxx	uuuu
$38D	-	-	PD1.9	PD1.8	--xx	--uu
$38E	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$38F	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$390	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$391	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as ‘0’.

4.2. Others Initial States:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4

5.1. Instruction Cycle Time

(1) 4/32.768kHz (≈ 122μs) for 32.768kHz oscillator.
(2) 4/262kHz (≈ 15.27μs) for 262kHz oscillator.
(3) 4/455kHz (≈ 8.79μs) for 455kHz oscillator.
(4) 4/4MHz (= 1μs) for 4MHz oscillator.
(5) 4/8MHz (= 0.5μs) for 8MHz oscillator.

5.2. Circuit Configuration

SH69P561/69K561 has two on-chip oscillation circuits: the OSC and the OSCX.

The OSC is a low frequency crystal (Typ. 32.768kHz) or RC (Typ.262kHz) determined by the code option. This is designed for low frequency operation. The OSCX also has two types: ceramic/crystal (400k to 8MHz) or RC (400k to 8MHz) to be determined by the code option. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At the start of Power on reset, Pin reset and low power reset initialization, the OSC starts oscillation and OSCX is turned off. But at the start of WDT reset initialization, the OSC starts oscillation and the OSCX remains the original state. Immediatly after reset initialization, the OSC clock is automatically selected as the system clock input source.

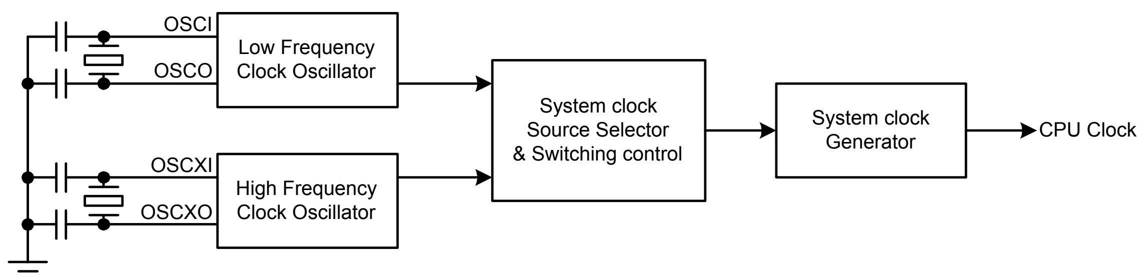


Figure 1. Oscillator Block Diagram

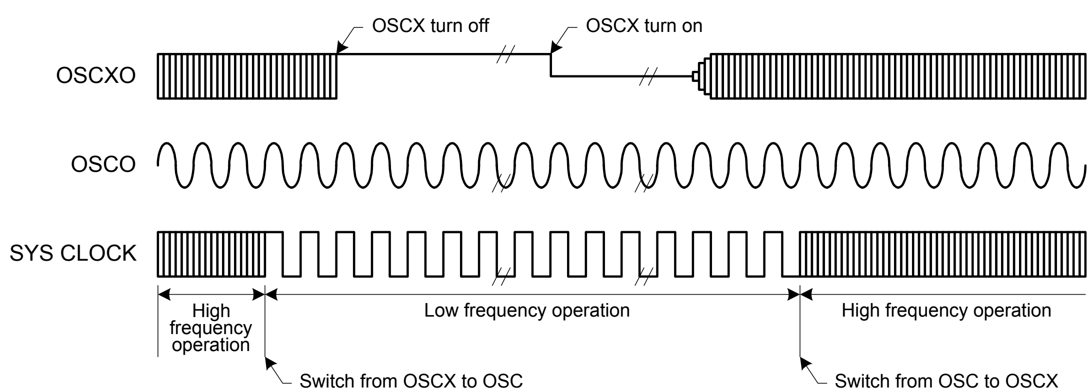
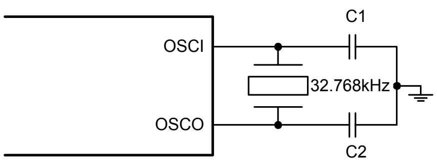


Figure 2. Timing of System Clock Switching

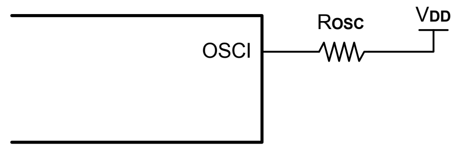
5.3. OSC Oscillator

The OSC generates the basic clock pulses that provide the CPU and peripherals (Timer0, Timer1) with an operating clock.

(1) OSC Crystal Oscillator



(2) OSC RC Oscillator

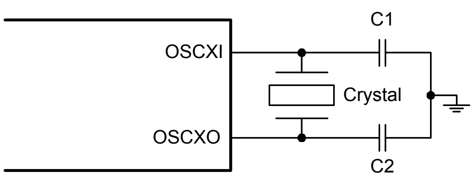


External Rosc RC

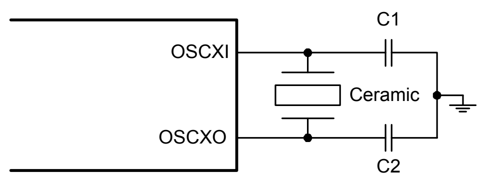
5.4. OSCX Oscillator

OSCX has two clock oscillators. The code options select the ceramic or RC as the CPU's clock.
If the OSCX is not used, it must be masked to be Ceramic resonator and the OSCXI must be connected to GND.

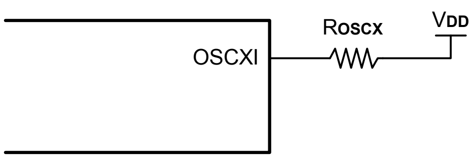
(1) OSCX Crystal oscillator: 400kHz - 8MHz



(2) OSCX Ceramic resonator: 400kHz - 8MHz



(3) OSCX RC Oscillator: 400kHz - 8MHz



External Roscx RC

5.5. Control of Oscillator

The oscillator control register configuration is shown as blow.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0D	PULLEN	PH/PL	OXS	OXON	R/W	Bit0: Turn on OSCX oscillator control register Bit1: System clock control register Bit2: Port pull-high and falling edge interrupt or pull-low and rising edge interrupt control register Bit3: Port pull-high/low enable control register

OXON: OSCX oscillation on/off.
0: Turn off OSCX oscillation
1: Turn on OSCX oscillation

OXS: switching system clock.
0: select OSC as system clock
1: select OSCX as system clock

Programming Notes:

It takes at least 5ms for the OSCX oscillation circuit to go on until the oscillation stabilizes. When the CPU system clock switching from OSC to OSCX, the user has to wait at least 5ms till the OSCX oscillation is activated. In addition, the start time varies a lot with respect to oscillator characteristics and operational conditions. Therefore the waiting time depends on applications. When switching from OSCX to OSC, and turning off OSCX in one instruction, the OSCX turns off control would be delayed for one instruction cycle automatically to prevent CPU operation error.

If the OSCX is selected as system clock (OXS = 1,OXON = 1), but the OXON bit is cleared to 0 by an unexpected factor such as noise, the OSCX will stop and the system clock will switch to the OSC automatically.

5.6. Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	C1	C2		
455kHz	47 - 100pF	47 - 100pF	ZTB 455KHz	Vectron International
			ZT 455E	Shenzhen DGJB Electronic Co., Ltd.
3.58MHz	-	-	ZTT 3.580M	Vectron International
			ZT 3.58M*	Shenzhen DGJB Electronic Co., Ltd.
4MHz	-	-	ZTT 4.000M	Vectron International
			ZT 4M*	Shenzhen DGJB Electronic Co., Ltd.

* The specified ceramic resonator has internal built-in load capaciyies.

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS
			φ 3x8 - 32.768KHz	Vectron International
4MHz	8 - 15pF	8 - 15pF	HC-49U/S 4.000MHz	Vectron International
			49S-4.000M-F16E	Shenzhen DGJB Electronic Co., Ltd.
8MHz	8 - 15pF	8 - 15pF	HC-49U/S 8.000MHz	Vectron International
			49S-8.000M-F16E	Shenzhen DGJB Electronic Co., Ltd.

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Ports

The MCU provides 15 bi-directional I/O ports. The PORT data is put in register $08 - $0C The PORT control register ($18 - $1C) controls the PORT as input or output. Each I/O port has an internal pull-high/pull-low resistor, which is controlled by PULLEN, PH/PL of $0D and the data of the port, when the PORT is used as input.

Port I/O Address Map

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	0	PA.2	PA.1	PA.0	R/W	PORTA data register **Bit3 must be cleared to "0" by the User's program and always be kept up**
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	0	0	0	0	R/W	**All bits of this register must be cleared to "0" by the User's program and always be kept up.**
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$18	1	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register **Bit3 must be set to "1" by the User's program and always be kept up.**
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	1	1	1	1	R/W	**All bits of this register must be set to "1" by the User's program and always be kept up.**
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register

PA (/B/C/E) CR, n (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin

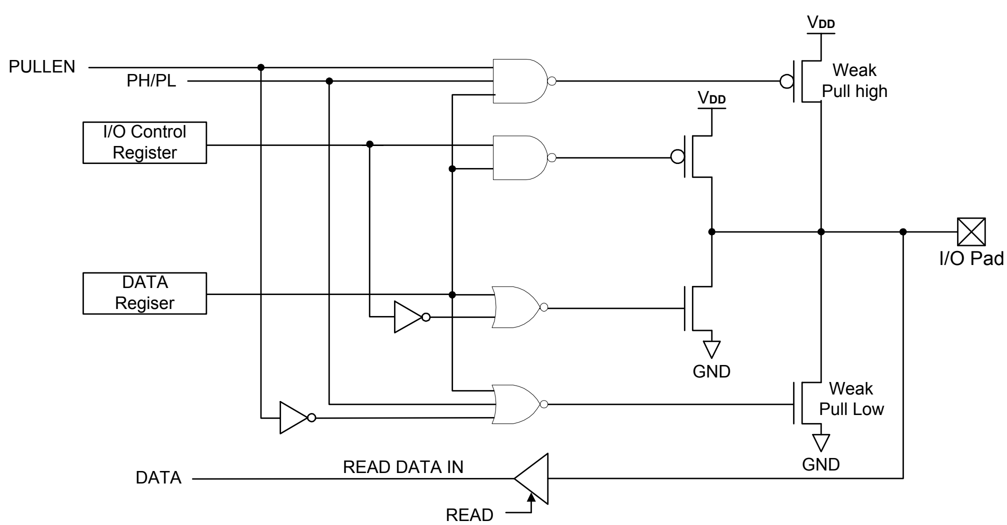


Figure 3

System Register $0D

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0D	PULLEN	PH/PL	OXS	OXON	R/W	Bit0: Turn on OSCX oscillator control register Bit1: System clock control register Bit2: Port pull-high and falling edge interrupt or pull-low and rising edge interrupt control register Bit3: Port pull-high/low enable control register
	1	X	X	X	R/W	Port Pull-high/Pull-low enable
	0	X	X	X	R/W	Port Pull-high/Pull-low disable (Power on initial)
	1	1	X	X	R/W	Port Pull-high resister ON, set falling edge interrupt (Power on initial)
	1	0	X	X	R/W	Port Pull-low resister ON, set rising edge interrupt

I/O Note:

- In user' program, it is necessary to always keep the Bit3 of system register $08 as 0, also all the bits of system register $0B.
- In user' program, it is necessary to always keep the Bit3 of system register $18 as 1, also all the bits of system register $1B.

After the chip Power on, LVR, Pin or WDT Reset, User's program must be set as the follow step:

```
LDI 18H, 1xxxB          ; x = 0 or 1
LDI 1BH, 1111B
LDI 08H, 0xxxB
LDI 0BH, 0000B
```

7. PORTB Interrupt

The PORTB is used as port interrupt sources. Since PORTB I/O is bit programmable I/O, so only the digital input port can generate a port interrupt. The analog input can't generate an interrupt request (when PORTB0, PORTB1 used as AN4, AN5). The PORTB interrupt control flags are mapped on $14, $15 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

System Register $14

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	PIEN.3	PIEN.2	PIEN.1	PIEN.0	R/W	Bit3-0: PORTB interrupt enable flags register

PIEN.n, (n = 0, 1, 2, 3)
0: Disable port interrupt. (Power on initial)
1: Enable port interrupt.

System Register $15

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PIF.3	PIF.2	PIF.1	PIF.0	R/W	Bit3-0: PORTB interrupt request flags register

PIF.n, (n = 0, 1, 2, 3)
0: Port interrupt is not presented. (Power on initial)
1: Port interrupt is presented.
Only writing these bits to 0 is available.

Following is the port interrupt function block-diagram for reference.

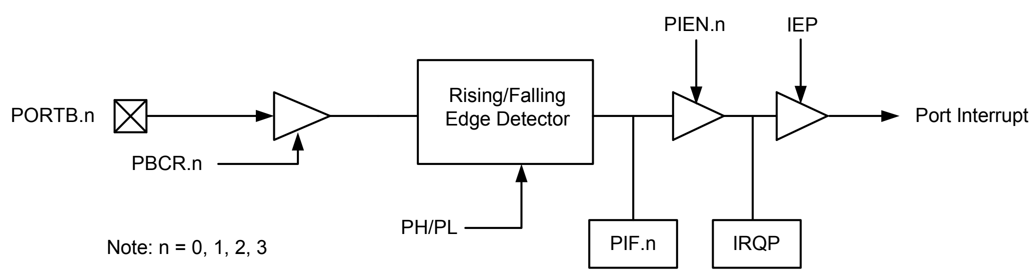


Figure 4. Port Interrupt Block Diagram

Port Interrupt Programming Notes:

When PH/PL (Bit2 of $0D) is set to 1, any one of PORTB input pin transitions from V_{DD} to GND would set PIF.x to 1, in spite of level of the other pin of PORTB.

If PIEN.x = 1and IEPB = 1, the x of PORTB input pin transitions from V_{DD} to GND would generate an interrupt request (IRQPB = 1) and interrupt the CPU, in spite of any level of the other pin of PORTB.

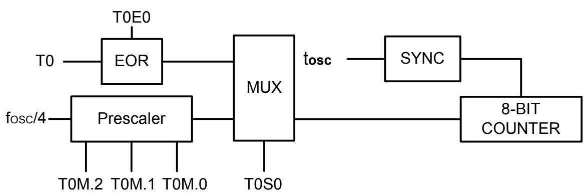
When PH/PL (Bit2 of $0D) is cleared to 0, any one of PORTB input pin transitions from GND to V_{DD} would set PIF.x to "1", in spite of level of the other pin of PORTB.

If PIEN.x = 1and IEPB = 1, the x of PortB input pin transitions from GND to V_{DD} would generate an interrupt request (IRQPB = 1) and interrupt the CPU, in spite of any level of the other pin of PORTB.

8. Timer

SH69P561/69K561 has two 8-bit timers. The timer/counter has the following features:
- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:
- Programmable interval timer function.
- Read counter value.

8.1. Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has both low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

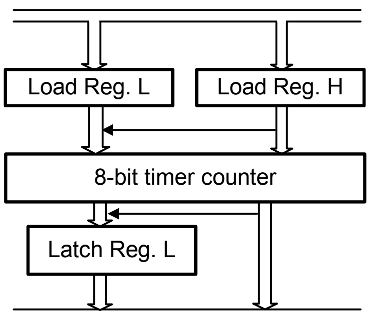
The low-order digit should be written first, and then the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high-order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: The register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:
 Low nibble first
 High nibble to update the counter

Read Operation:
 High nibble first
 Low nibble followed.



8.2. Timer0 Mode Register

The Timer0 can be programmed in several different prescalers by setting Timer0 Mode register (T0M).

The clock source pre-scale by the 8-level counter first, then generate the output plus to timer counter. The Timer0 Mode registers (T0M) are 3-bit registers used for the timer control as shown below.

System Register $13: Timer0/Timer1 Clock Source and Edge Configuration Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T0S1	T0E1	T0S0	T0E0	R/W	Bit0: T0 clock edge in Timer0 control register Bit1: Timer0 clock source control register Bit2: T0 clock edge in Timer1 control register Bit3: Timer1 clock source control register
	X	X	0	X	R/W	fosc/4 is selected as Timer0 clock source (Power on initial)
	X	X	1	X	R/W	T0 is selected as Timer0 clock source
	X	X	1	0	R/W	Increment on low-to-high transition when T0S0 = 1 (Power on initial)
	X	X	1	1	R/W	Increment on high-to-low transition when T0S0 = 1

System Register $02: Timer0 Mode Register, when T0S0 = 1

T0M.2	T0M.1	T0M.0	Prescaler	Clock Source
X	X	X	/1	T0

System Register $02: Timer0 Mode Register, when T0S0 = 0

T0M.2	T0M.1	T0M.0	Prescaler	Clock Source
0	0	0	$/2^{11}$	fosc/4
0	0	1	$/2^{9}$	fosc/4
0	1	0	$/2^{7}$	fosc/4
0	1	1	$/2^{5}$	fosc/4
1	0	0	$/2^{3}$	fosc/4
1	0	1	$/2^{2}$	fosc/4
1	1	0	$/2^{1}$	fosc/4
1	1	1	$/2^{0}$	fosc/4

External Clock/Event T0 as Timer0 Source

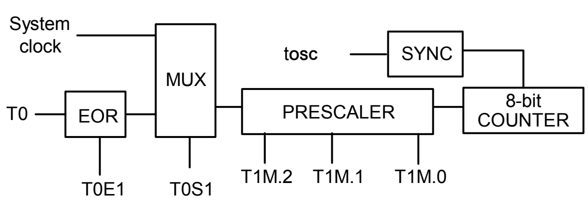
When external clock/event T0 input as Timer0 source, PORTC.3 is shared as T0 input and it is synchronized with OSC clock. The external source must follow certain constraints. The OSC clock samples T0 input. Therefore it is necessary to be high (at least 2 tosc) and low (at least 2 tosc). The requirement is as follows:

T0H (T0 high time) ≥ 2 tosc + ΔT

T0L (T0 low time) ≥ 2 tosc + ΔT; ΔT = 20ns

8.3. Timer1 Mode Register

The following is a simplified Timer1 block diagram.



Timer1

When OSC is selected as system clock, System clock = fosc/4;
When OSCX is selected as system clock, System clock = foscx/4.

System Register $13: Timer0/Timer1 Clock Source and Edge Configuration Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	T0S1	T0E1	T0S0	T0E0	R/W	Bit0: T0 clock edge in Timer0 control register Bit1: Timer0 clock source control register Bit2: T0 clock edge in Timer1 control register Bit3: Timer1 clock source control register
	0	X	X	X	R/W	System clock is selected as Timer1 clock source (Power on initial)
	1	X	X	X	R/W	T0 is selected as Timer1 clock source
	1	0	X	X	R/W	Increment on low-to-high transition when T0S1 = 1 (Power on initial)
	1	1	X	X	R/W	Increment on high-to-low transition when T0S1 = 1

System Register $03: Timer1 Mode Register

T1M.2	T1M.1	T1M.0	Prescaler	Clock Source
0	0	0	$/2^{11}$	System clock /T0
0	0	1	$/2^{9}$	System clock /T0
0	1	0	$/2^{7}$	System clock /T0
0	1	1	$/2^{5}$	System clock /T0
1	0	0	$/2^{3}$	System clock /T0
1	0	1	$/2^{2}$	System clock /T0
1	1	0	$/2^{1}$	System clock /T0
1	1	1	$/2^{0}$	System clock /T0

External Clock/Event T0 as Timer1 Source

When external clock/event T0 input as Timer1 source, PORTC.3 is shared as T0 input and it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t_{SYSCLK}) and low (at least 2 t_{SYSCLK}). When the prescaler ratio selects $/2^0$, it is the same as the system clock input.

The requirement is as follows:

T0H (T0 high time) $\geq 2 \times t_{SYSCLK} + \Delta T$

T0L (T0 low time) $\geq 2 \times t_{SYSCLK} + \Delta T$; $\Delta T = 20ns$

When another prescaler ratio is selected, the Timer1 is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$\text{T0 high time} = \text{T0 low time} = \frac{T0}{2} \geq \frac{2 \times t_{SYSCLK} + \Delta T}{N}$$

Where: T0 = Timer0 input period

N = prescaler value

The requirement is:

$$\frac{N \times T0}{2} \geq 2 \times t_{SYSCLK} + \Delta T$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$\text{T0 period} \geq \frac{4 \times t_{SYSCLK} + 2 \times \Delta T}{N} \quad ; \Delta T = 20ns$$

Notes:

When OSC is selected as system clock, $t_{SYSCLK} = 4 \times t_{OSC}$;

When OSCX is selected as system clock, $t_{SYSCLK} = 4 \times t_{OSCX}$.

9. Watchdog Timer (WDT)

The watchdog timer is a count-down counter, and its clock source is an independent built-in RC oscillator, so that it will always run even in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E Bit2 - 0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E Bit3) will be automatically set to "1" by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag
	X	0	0	0	R/W	Watchdog timer overflow period is 4096ms. (Power on initial)
	X	0	0	1	R/W	Watchdog timer overflow period is 1024ms.
	X	0	1	0	R/W	Watchdog timer overflow period is 256ms.
	X	0	1	1	R/W	Watchdog timer overflow period is 128ms.
	X	1	0	0	R/W	Watchdog timer overflow period is 64ms.
	X	1	0	1	R/W	Watchdog timer overflow period is 16ms.
	X	1	1	0	R/W	Watchdog timer overflow period is 4ms.
	X	1	1	1	R/W	Watchdog timer overflow period is 1ms.
	0	X	X	X	R	No watchdog timer overflow resets. (Power on initial)
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens (Cleared after Power on Reset, Pin Reset or Low Voltage Reset)

Note: Watchdog timer overflow period is valid for V_{DD} = 5V.

10. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

A. Power-on Reset and Pin Reset:

(1) In RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^7$ (128).

(2) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

B. Wake up from stop mode, WDT Reset, LVR Reset:

(1) In RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^7$ (128).

(2) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).

11. HALT and STOP Mode

After the execution of HALT instruction, SH69P561/69K561 will enter the HALT mode. In the HALT mode, CPU will stop operating. But peripheral circuit (Timer0, Timer1, ADC) will keep status.

After the execution of STOP instruction, SH69P561/69K561 will enter the STOP mode. The whole chip (including oscillator) will stop operating. But watchdog is still enabled.

In the HALT mode, SH69P561/69K561 can be waked up if any interrupt occurs.

In the STOP mode, SH69P561/69K561 can be waked up if port interrupt occurs.

When CPU is waked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

12. Pulse Width Modulation (PWM)

The SH69P561/69K561 consists of two 10-bit PWM modules. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMP is used to control the period cycle of the PWM module output. And the PWMD is used to control the duty in the waveform of the PWM module output.

Systems Register $380, $381: PWM Control Register (PWMC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$380, $381	PWMnS	TnCK1	TnCK0	PWMn	R/W	Bit0: PWMn output enabled control register Bit2-1: PWMn clock control register Bit3: PWMn output mode of duty cycle control register
	0	X	X	X	R/W	PWMn output normal mode of duty cycle (Power on initial)
	1	X	X	X	R/W	PWMn output negative mode of duty cycle
	X	X	X	0	R/W	Shared with I/O port (Power on initial)
	X	X	X	1	R/W	Shared with PWMn, n = 0 or 1
	X	0	0	X	R/W	PWMn clock = T_{CLK} (Power on initial)
	X	0	1	X	R/W	PWMn clock = 2 T_{CLK}
	X	1	0	X	R/W	PWMn clock = 4 T_{CLK}
	X	1	1	X	R/W	PWMn clock = 8 T_{CLK}

n = 0 or 1
The PWM0 output pin is shared with PORTC.0
The PWM1 output pin is shared with PORTC.1
T_{CLK} means one period time of system oscillator. When OSC is selected as system clock, T_{CLK} = t_{OSC};
When OSCX is selected as system clock, T_{CLK} = t_{OSCX}. Referring to setting of system register of $0D for system oscillator switch.

Systems Register $382 - $384, $388 - $38A: PWM Period Control Register (PWMP)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$382, $388	PPn.3	PPn.2	PPn.1	PPn.0	R/W	PWMn period low nibble register
$383, $389	PPn.7	PPn.6	PPn.5	PPn.4	R/W	PWMn period middle nibble register
$384, $38A	-	-	PPn.9	PPn.8	R/W	Bit1-0: PWMn period high nibble register

n = 0 or 1
PWM output period cycle = [PPn.9, PPn.0] X PWMn clock.
When [PPn.9, PPn.0] = 000H, PWM output GND if the PWMnS bit is cleared to “0”.
When [PPn.9, PPn.0] = 000H, PWM output the high level if the PWMnS bit is set to “1”.

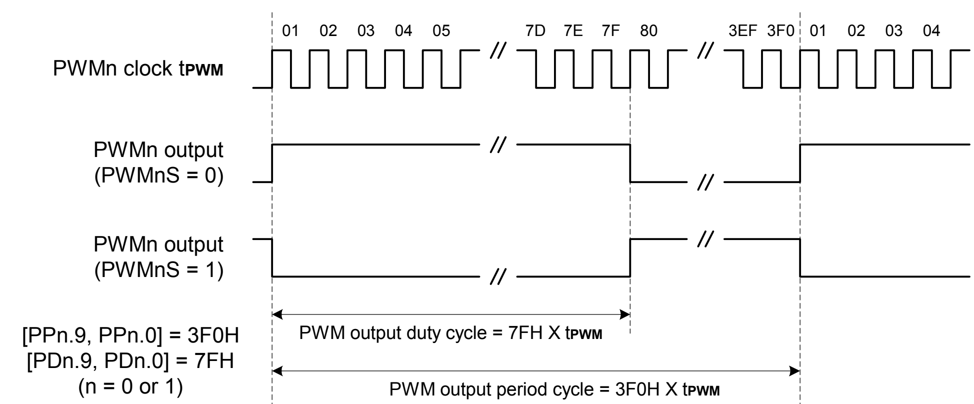
Systems Register $385 - $387, $38B - $38D: PWM Duty Control Register (PWMD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$385, $38B	PDn.3	PDn.2	PDn.1	PDn.0	R/W	PWMn duty low nibble register
$386, $38C	PDn.7	PDn.6	PDn.5	PDn.4	R/W	PWMn duty middle nibble register
$387, $38D	-	-	PDn.9	PDn.8	R/W	Bit1-0: PWMn duty high nibble register

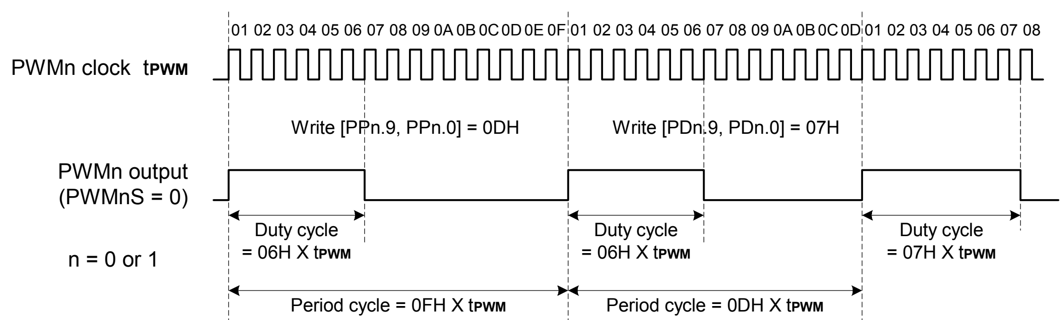
n = 0 or 1
PWM output duty cycle = [PDn.9, PDn.0] X PWMn clock.
If [PPn.9, PPn.0] ≤ [PDn.9, PDn.0], PWM outputs high level when the PWMnS bit is cleared to “0”.
If [PPn.9, PPn.0] ≤ [PDn.9, PDn.0], PWM outputs GND level when the PWMnS bit is set to “1”.

Programming Notes:

a. Select the PWM module system clock.
b. Set the PWM period cycle by writing proper value to the PWM period control register (PWMP). First set the high nibble, then the middle nibble and the last set the low nibble.
c. Set the PWM duty cycle by writing proper value to the PWM duty control register (PWMD). First set the high nibble, , then the middle nibble and the last set the low nibble.
d. Select the PWM output mode of the duty cycle by writing the PWMnS bit in the PWM control register (PWMC).
e. To output the desired PWM waveform, enable the PWM module by writing "1" to the PWMn bit in the PWM control register (PWMC).
f. If select the I/O port as the PWM output, the I/O function and the pull-high resistor are disabled.
g. If the PWM period cycle or the duty cycle need to be changed, the writing flow should be followed as described in step b or step c. Then the revised data are loaded into the re-load counter and the PWM module starts counting at next period.
h. The PWM could keep on working in the HALT mode, and would stop automatically when execute a "STOP" instruction.



PWM Output Example



PWM Output Period or Duty Cycle Changing Example

13. Analog/Digital Converter (ADC)

The 5 channels and 8-bit resolution ADC are implemented in this micro-controller.

The ADC control registers can be used to define the A/D channel number, select analog channel, reference voltage and conversion clock, start A/D conversion, and set the end of A/D conversion flag. The A/D conversion result register byte is read-only.

The approach for A/D conversion:

- Set analog channels and select reference voltage. (When using the external reference voltage, keep in mind that any analog input voltage must not exceed V_{REF})
- Operating ADC module and select the converted analog channel.
- Set A/D conversion clock source.
- GO/$\overline{DONE}$ = 1, start A/D conversion.

Systems Register $20:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	VREFS	ACR2	ACR1	ACR0	R/W	Bit2-0: ADC port configuration control register Bit3: Internal/External reference voltage control register
	X	0	0	0	R/W	Set Analog Channels
	0	X	X	X	R/W	Internal reference voltage (V_{REF} = V_{DD}) (Power on initial)
	1	X	X	X	R/W	External reference voltage

Set Analog Channels

ACR2	ACR1	ACR0	PB.1	PB.0	PA.2	PA.1	PA.0
0	0	0	PB1	PB0	PA2	PA1	PA0
0	0	1	PB1	PB0	PA2	PA1	AN0
0	1	0	PB1	PB0	PA2	AN1	AN0
0	1	1	PB1	PB0	AN2	AN1	AN0
1	0	0	PB1	PB0	AN2	AN1	AN0
1	0	1	PB1	AN4	AN2	AN1	AN0
1	1	X	AN5	AN4	AN2	AN1	AN0

Systems Register $21:

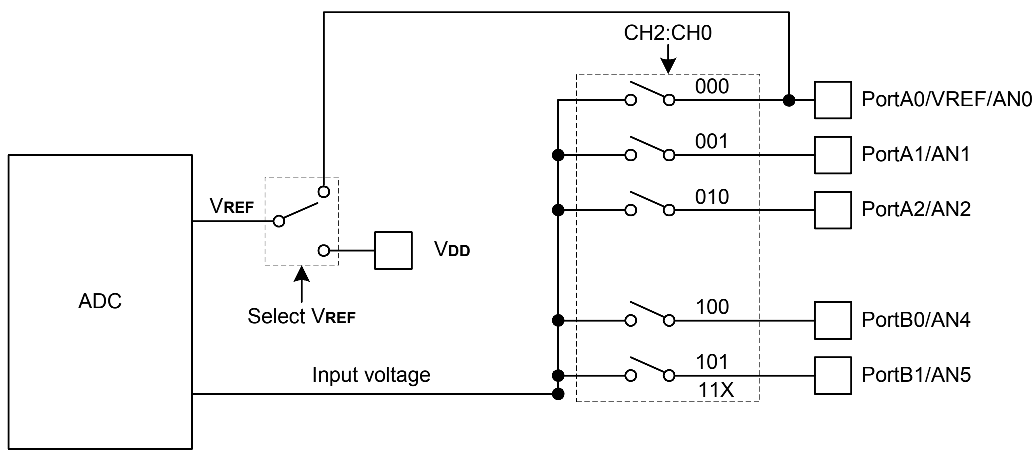
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	ADCON	CH2	CH1	CH0	R/W	Bit2-0: ADC channel control register Bit3: ADC module operate control register
	X	0	0	0	R/W	ADC channel AN0 (Power on initial)
	X	0	0	1	R/W	ADC channel AN1
	X	0	1	0	R/W	ADC channel AN2
	X	1	0	0	R/W	ADC channel AN4
	X	1	0	1	R/W	ADC channel AN5
	X	1	1	X	R/W	ADC channel AN5
	0	X	X	X	R/W	Disable ADC module
	1	X	X	X	R/W	Enable ADC module

Systems Register $23 - $24 for ADC Data:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$23	A3	A2	A1	A0	R	ADC data low nibble register
$24	A7	A6	A5	A4	R	ADC data high nibble register

Systems Register $22:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$22	GO/$\overline{\text{DONE}}$	TADC1	TADC0	ADCS	R/W	Bit0: A/D Conversion Time control register Bit2-1: A/D Clock Period control register Bit3: ADC status flag register
	X	X	X	0	R/W	A/D Conversion Time = 50 t_{AD} (Power on initial)
	X	X	X	1	R/W	A/D Conversion Time = 330 t_{AD}
	X	0	0	X	R/W	A/D Clock Period t_{AD} = t_{OSC}
	X	0	1	X	R/W	A/D Clock Period t_{AD} = 2 t_{OSC}
	X	1	0	X	R/W	A/D Clock Period t_{AD} = 4 t_{OSC}
	X	1	1	X	R/W	A/D Clock Period t_{AD} = 8 t_{OSC}
	0	X	X	X	R/W	A/D conversion is completed or not in processing
	1	X	X	X	R/W	Set 1 to start A/D conversion, keep GO/$\overline{\text{DONE}}$ = 1, when A/D conversion is in processing



ADC Block Diagram

Notes:

- Select A/D clock period t_{AD}, make sure that 1μs ≤ t_{AD} ≤ 33.4 μs.
- When the A/D conversion is complete, an ADC interrupt occurs (if the ADC interrupt is enabled).
- The analog input channels must have their corresponding PXCR (X = A, B) bits selected as inputs.
- If select I/O ports as analog input, the I/O functions and Pull-high/low resistor are disabled.
- Bit GO/$\overline{\text{DONE}}$ is automatically cleared by hardware when the A/D conversion is complete.
- Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion.
- The A/D result register will NOT be updated with the partially completed A/D conversion sample.
- 4-t_{OSC} waits is required before the next acquisition is started.
- ADC could keep on working in the HALT mode, and would stop automatic when execute “STOP” instruction.
- ADC could wake-up SH69P561/69K561 from the HALT mode (if the ADC interrupt is enabled).

14. Alarm Output

Alarm Output Configuration:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	-	ALMF1	ALMF0	PAM0	R/W	Bit0: Alarm output enable control register Bit2-1: Alarm carrier frequency control register
	-	X	X	0	R/W	PORTC.2 is shared as I/O port (Power on initial)
	-	X	X	1	R/W	PORTC.2 is shared as Alarm output

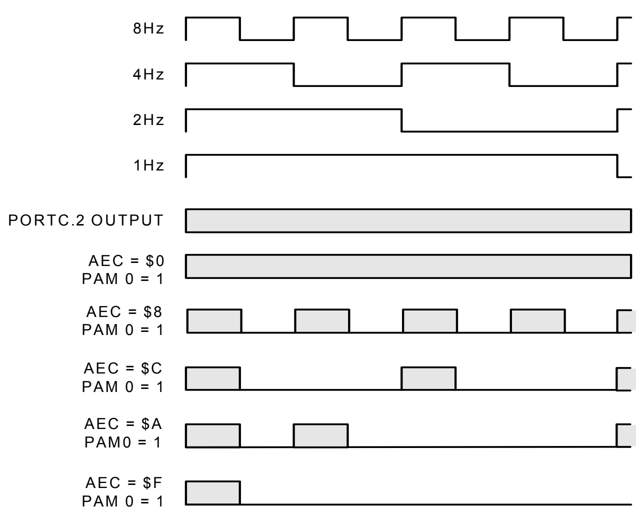
Alarm Carrier Frequency Setting:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	-	ALMF1	ALMF0	PAM0	R/W	Bit0: Alarm output enable control register Bit2-1: Alarm carrier frequency control register
	-	0	0	X	R/W	Alarm carrier frequency is 4kHz (Power on initial)
	-	0	1	X	R/W	Alarm carrier frequency is 2kHz
	-	1	0	X	R/W	Alarm carrier frequency is 1kHz
	-	1	1	X	R/W	Alarm carrier frequency is 0.5kHz

Envelope Setting:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$17	AEC3	AEC2	AEC1	AEC0	R/W	Alarm envelope control register
	0	0	0	0	R/W	DC envelope (Power on initial)
	X	X	X	1	R/W	1Hz envelope AND other envelope choice logically
	X	X	1	X	R/W	2Hz envelope AND other envelope choice logically
	X	1	X	X	R/W	4Hz envelope AND other envelope choice logically
	1	X	X	X	R/W	8Hz envelope AND other envelope choice logically

The programming alarm waveform is shown as below:



Alarm Output Waveform

To activate the Alarm function, first switch the PAM0 to the Alarm output mode. After setting PAM0 equal to 1, then set the proper envelope. When the data have been written into AEC, the envelope counter will be synchronized at the same time. The ALARM will output GND in the STOP mode.

Notes: The Alarm block clock is fetched from 32.768kHz Crystal Oscillator or 262kHz/8 @262kHz RC Oscillator by code option, so the Alarm carrier frequency and the alarm envelope will change in different OSC frequency and different OSC type.

15. EL-LIGHT

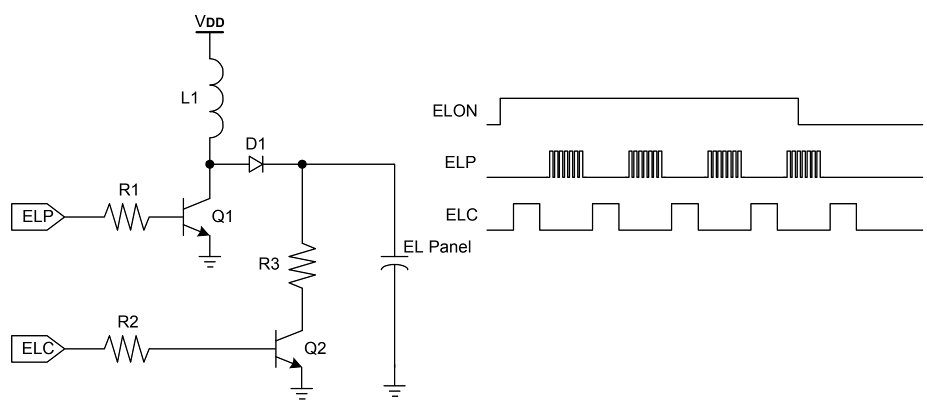
System Register $1D:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1D	-	ELF	ELPF	ELON	R/W	Bit0: EL-light on/off control register Bit1: EL-light driver charge frequency control register Bit2: EL-light driver discharge frequency control register
	-	X	X	0	R/W	EL-light driver turn off (Power on initial)
	-	X	X	1	R/W	EL-light driver turn on
	-	X	0	X	R/W	ELP pad output frequency = ELCLK (Power on initial)
	-	X	1	X	R/W	ELP pad output frequency = ELCLK/2
	-	0	X	X	R/W	ELC pad output frequency = ELCLK/64 (Power on initial)
	-	1	X	X	R/W	ELC pad output frequency = ELCLK/32

ELCLK = 32.768kHz @32.768kHz Crystal Oscillator or 262kHz/8 @262kHz RC Oscillator by code option.

When EL-light driver turn off, the ELP and ELC output low.

Setup system register to select the EL-light driver waveform. Set ELON = 1 will turn on EL-light driver. ELC and ELP will output driver waveform automatic as diagram blew. With externally transistor, diode, inductance and resistor, we can pump the EL panel to AC 100 - 250V



EL-light Driving Circuit for Reference

While EL-light is turned on, the ELC will be turned on before ELP being turned on. When EL-light is turned off, the ELP will be turned off first, then ELC will still work for one cycle to make sure no voltage left on EL panel.

The EL-light driver would keep on working in the HALT mode. But it would be turned off after executing a “STOP” instruction (ELC & ELP keep low).

For Design Notes:

- ELP negative pulse width is about 2 - 12μs.
- Please turn off EL-light before executing a “STOP” instruction.

16. LCD Driver

The LCD driver contains a controller, a voltage generator, 4 common and 18 segment driver pins. The driving mode is controlled by the system register $26.

The LCD SEG13 - SEG26 can also be used as output port which is selected by the Bit2 of the system register $27. When SEG13 - SEG26 are selected to be output ports, the user should write data to bit x at the same addresses (35CH-369H). The LCD RAM could be used as data memory if needed. When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the same value after executing the "STOP" instruction. When LCD off, both common and segment output low.

LCD Note:

- **In user' program, it is necessary to always keep the Bit0 of the system register $27 being cleared to 0. And the Bit1 of the system register $26 must be cleared to 0 as well as Bit0 set to 1.**

After the chip Power on, LVR, Pin or WDT Reset, User's program must be set as the follow step:

```
LDI 27H, XXX0B        ; x = 0 or 1
LDI 26H, XX01B
```

16.1. LCD Control Registers

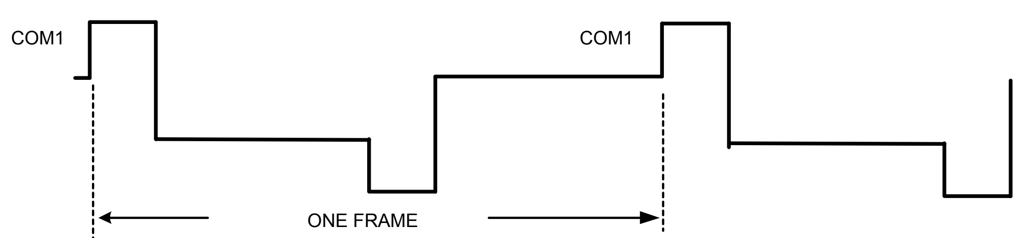
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$25	-	LCDON	RLCD1	RLCD0	R/W	Bit1-0: Set LCD bias resistor register Bit2: Turn on LCD control register
$26	LPS1	LPS0	0	1	R/W	**Bit0 must be set to "1" by the User's program and always be kept up** **Bit1 must be cleared to "0" by the User's program and always be kept up** Bit3-2: Different LCD frame frequency control register
$27	LVD	O/S2	O/S1	0	R/W	**Bit0 must be cleared to "0" by the User's program and always be kept up.** Bit1: PORTE as LCD SEG5 - 8 control register Bit2: LCD SEG13 - 26 as output control register Bit3: LCD Voltage degrade control register

LPS1, LPS0: LCD frame frequency control

LCD clock is divided from OSC, so LCD frame frequency will change in proportion to the variation of OSC frequency in spite of OSC type.

Frame Frequency (When fosc = 32768Hz)	LPS1, LPS0			
	0, 0	**0, 1**	**1, 0**	**1, 1**
In 1/4 DUTY mode	32Hz	16Hz	8Hz	4Hz

Frame Frequency (When fosc = 262kHz)	LPS1, LPS0			
	0, 0	**0, 1**	**1, 0**	**1, 1**
In 1/4 DUTY mode	256Hz	128Hz	64Hz	32Hz



LCD Output Frame

16.2. Configuration of LCD RAM

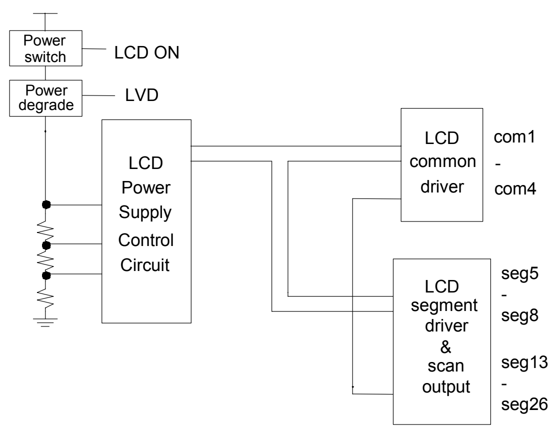
LCD 1/4 duty, 1/3 bias (COM1 - COM4, SEG5 - SEG8, SEG13 - SEG26)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$304	SEG5	SEG5	SEG5	SEG5	$311	SEG18	SEG18	SEG18	SEG18
$305	SEG6	SEG6	SEG6	SEG6	$312	SEG19	SEG19	SEG19	SEG19
$306	SEG7	SEG7	SEG7	SEG7	$313	SEG20	SEG20	SEG20	SEG20
$307	SEG8	SEG8	SEG8	SEG8	$314	SEG21	SEG21	SEG21	SEG21
$30C	SEG13	SEG13	SEG13	SEG13	$315	SEG22	SEG22	SEG22	SEG22
$30D	SEG14	SEG14	SEG14	SEG14	$316	SEG23	SEG23	SEG23	SEG23
$30E	SEG15	SEG15	SEG15	SEG15	$317	SEG24	SEG24	SEG24	SEG24
$30F	SEG16	SEG16	SEG16	SEG16	$318	SEG25	SEG25	SEG25	SEG25
$310	SEG17	SEG17	SEG17	SEG17	$319	SEG26	SEG26	SEG26	SEG26

SEG13 - 26 is used as scan output port.

Address	Bit0	Address	Bit0	Address	Bit0	Address	Bit0
$35C	SEG13	$360	SEG17	$364	SEG21	$368	SEG25
$35D	SEG14	$361	SEG18	$365	SEG22	$369	SEG26
$35E	SEG15	$362	SEG19	$366	SEG23		
$35F	SEG16	$363	SEG20	$367	SEG24		

16.3. LCD Power



LCD Block Diagram

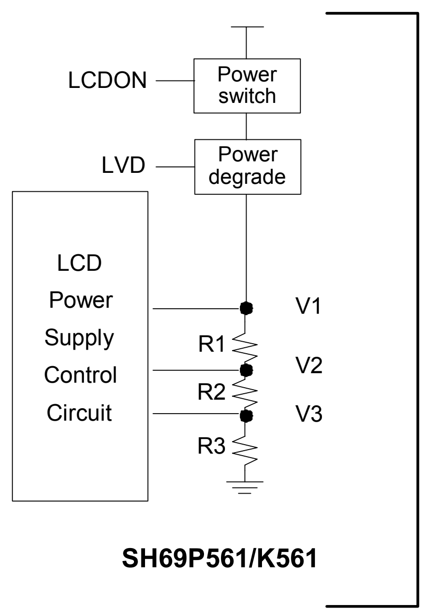
Built-in special LCD power control for LCD power modulation.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	LVD	O/S2	O/S1	0	R/W	Bit1: PORTE as LCD SEG5 - 8 control register Bit2: LCD SEG13 - 26 as output control register Bit3: LCD Voltage degrade control register
	X	X	X	0	R/W	**Bit0 must be cleared to “0” by the User’s program and always be kept up.**
	X	X	0	0	R/W	PORTE as I/O ports
	X	X	1	0	R/W	PORTE as LCD SEG5 - 8
	X	0	X	0	R/W	SEG13 - 26 as LCD segment outputs
	X	1	X	0	R/W	SEG13 - 26 as output ports

When LVD is set to 1 and the divider resistance is 270k, LCD voltage power will be degraded to about 90% of V_{DD}. It is designed to reduce extra LCD contrast control output pins. Then the LCD can be fitted automatically for different voltage levels by the software.

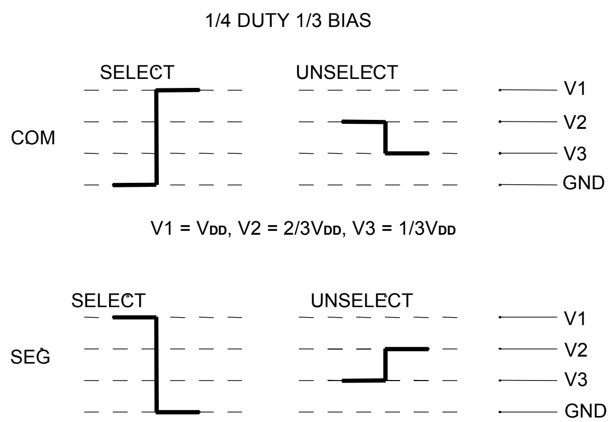
16.4. Select Different Divider Resistance

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$25	-	LCDON	RLCD1	RLCD0	R/W	Bit1-0: Set LCD bias resistor register Bit2: Turn on LCD control register
	-	X	0	0	R/W	R1 = R2 = R3 = 270k (Power on initial)
	-	X	0	1	R/W	R1 = R2 = R3 = 90k
	-	X	1	0	R/W	R1 = R2 = R3 = 30k
	-	X	1	1	R/W	R1 = R2 = R3 = 10k
	-	0	X	X	R/W	LCD OFF (Power on initial)
	-	1	X	X	R/W	LCD ON

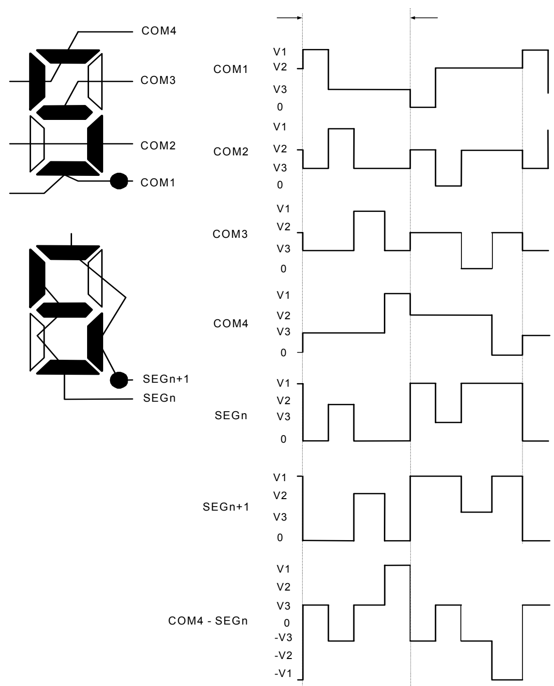


LCD Bias Resistor Diagram

16.5. LCD Waveform



LCD Waveform of Different Duty and Bias



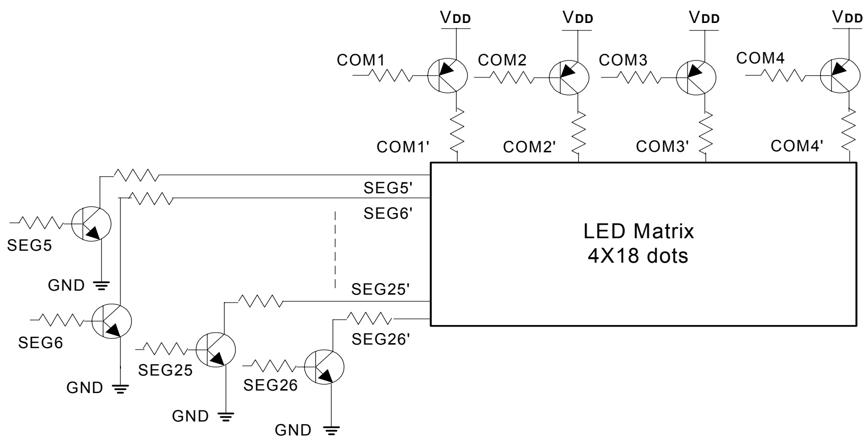
Example of 1/4 Duty 1/3 Bias

16.6. LCD shared to LED Application

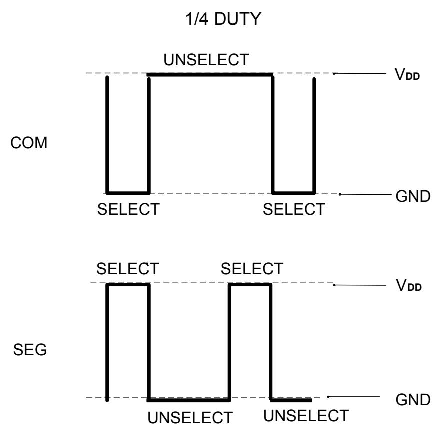
User can use SEG & COM in the application of LED matrix by code option and configuration of LED RAM is the same as LCD RAM. If LCD is off and LCD is shared to LED application, COM output V_{DD} and SEG output GND.

Notes:

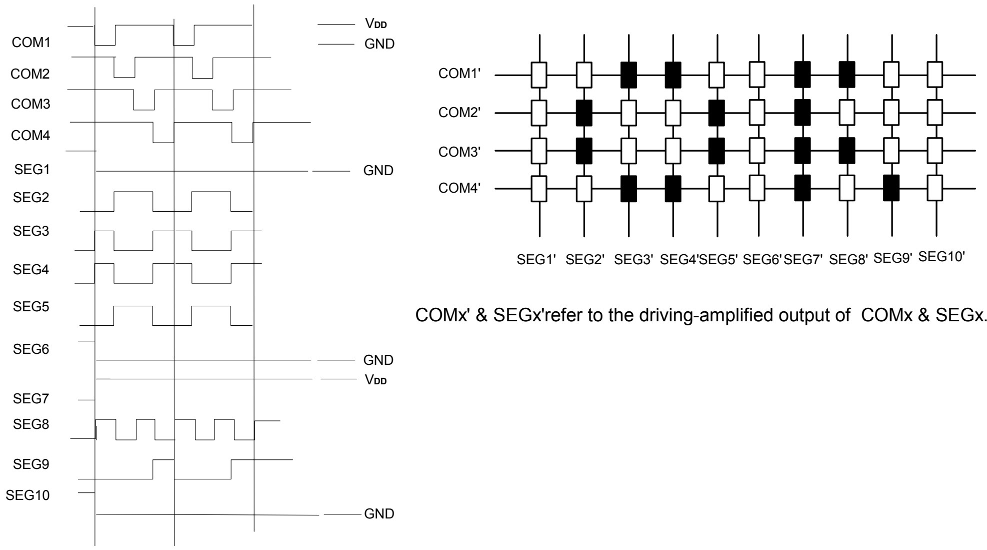
The SEG & COM cann't be used to drive the LED matrix directly as the weak driving ability. So in the LED Matrix application the driving-transistor circuit will be used such as following.



Example of 1/4 Duty LED Matrix Application Circuit



LED Driving Output Waveform



Example of 1/4 Duty 4 X 10 Dots

17. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by code option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$.

Here, V_{LVR} which is LVR detect voltage has two level select by code option.

18. Interrupt

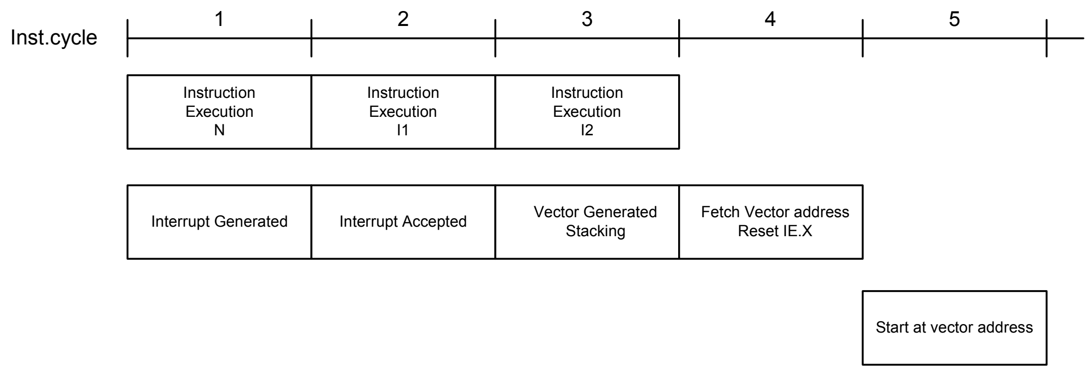
Four interrupt sources are available on SH69P561/69K561:
- A/D interrupt
- Timer0 interrupt
- Timer1 interrupt
- PORTB interrupt

Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00, $01, $14 and $15 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEAD	IET0	IET1	IEPB	R/W	Interrupt enable flags register
$01	IRQAD	IRQT0	IRQT1	IRQPB	R/W	Interrupt request flags register

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the SH6610D CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

A/D Interrupt

Bit3 (IEAD) of system register $00 is the A/D interrupt enable flag. When the A/D conversion is complete, it will generate an interrupt request (IRQAD), if the A/D interrupt is enabled (IEAD), an A/D interrupt service routine will start. The A/D interrupt can be used to wake the CPU from the HALT mode.

Timer (Timer0, Timer1) Interrupt

The input clock of Timer0 and Timer1 are based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1 = 1), If the interrupt enable flag is enabled (IET0 or IET1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from the HALT mode.

Port Interrupt

Each bits of PORTB is used as port interrupt sources. Since PORTB I/O is bit programmable I/O, so only the digital input port can generate a port interrupt. The analog input can’t generate an interrupt request (when PORTB0, PORTB1 are used as AN4, AN5).

Port Interrupt can be used to wake the CPU from the HALT or the STOP mode. See “PORTB edge detector and interrupt” for detailed description.

19. Code Option

(a) OSC Type:
0 = 32.768kHz Crystal oscillator (Default)
1 = 262kHz RC oscillator

(b) OSCX Type:
0 = Ceramic/Crystal oscillator (Default)
1 = RC oscillator

(c) OSCX Range Select:
0 = 400kHz - 2MHz (Default)
1 = 2MHz - 8MHz

(d) Watchdog Timer:
0 = Disable
1 = Enable (Default)

(e) LVR Reset:
0 = Disable
1 = Enable (Default)

(f) LVR Level:
0 = High level: 4.0V (Default)
1 = Low level: 2.5V

(g) LCD/LED Matrix Share:
0 = LCD application (Default)
1 = LED matrix application

Instructions

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh; AC ← llll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Rating*

DC Supply Voltage . . . .-0.3V to +7.0V

Input Voltage . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . .-40 ℃ to +85℃

Storage Temperature . . . .-55 ℃ to +125℃

*Comments

Stresses exceed those listed under **"Absolute Maximum Ratings"** may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 2.4 - 5.5V GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	30kHz ≤ f_{OSC} ≤ 8MHz
		2.4	3.0	3.6	V	30kHz ≤ f_{OSC} ≤ 4MHz
Low Voltage Reset Voltage	V_{LVR1}	3.8	-	4.2	V	V_{DD} = 2.4V - 5.5V, 30kHz ≤ f_{OSC} ≤ 8MHz,LVR enable
	V_{LVR2}	2.4	-	2.6	V	V_{DD} = 2.4V - 5.5V, 30kHz ≤ f_{OSC} ≤ 8MHz,LVR enable
Operating Current1	I_{OP}	-	12	20	μA	All output pins unload execute NOP instruction f_{OSC} = 32.768kHz (excluding LCD bias current, WDT off, ADC disable) V_{DD} = 5.0V
			4	10	μA	All output pins unload execute NOP instruction f_{OSC} = 32.768kHz (excluding LCD bias current, WDT off, ADC disable) V_{DD} = 3.0V
		-	1.5	2	mA	All output pins unloaded, OSCX as system clock, f_{OSCX} = 8MHz (Execute NOP instruction) V_{DD} = 5.0V
			0.3	0.5	mA	All output pins unloaded, OSCX as system clock, f_{OSCX} = 4MHz (Execute NOP instruction) V_{DD} = 3.0V
Standby Current1 (HALT)	I_{SB1}	-	8	15	μA	All output pins unload (HALT mode) f_{OSC} = 32.768kHz (excluding LCD bias current, WDT off, LVR off, ADC disable) V_{DD} = 5.0V
			2	5	μA	All output pins unload (HALT mode) f_{OSC} = 32.768kHz (excluding LCD bias current, WDT off, LVR off, ADC disable) V_{DD} = 3.0V
		-	600	800	μA	All output pins unload, (HALT mode), OSCX as system clock, f_{OSCX} = 8MHz (WDT off, ADC disable) V_{DD} = 5.0V
			200	300	μA	All output pins unload, (HALT mode), OSCX as system clock, f_{OSCX} = 4MHz (WDT off, ADC disable) V_{DD} = 3.0V
Standby Current2 (STOP)	I_{SB2}	-	-	1	μA	All output pins unload (STOP mode), (LCD off, LVR off, WDT off ADC disable) V_{DD} = 5.0V
		-	-	1	μA	All output pins unload (STOP mode), (LCD off, LVR off, WDT off ADC disable) V_{DD} = 3.0V
WDT Current	I_{WDT}	-	10	20	μA	V_{DD} = 5.0V
		-	5	10	μA	V_{DD} = 3.0V

DC Electrical Characteristics (continued) (V_{DD} = 2.4 - 5.5V GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	V_{IL}	GND	-	V_{DD} X 0.3	V	PORTA - PORTE, V_{DD} = 2.4V - 5.5V
		GND	-	V_{DD} X 0.2	V	T0, $\overline{RESET}$, (Schmitt trigger input) V_{DD} =2.4V - 5.5V
Input High Voltage	V_{IH}	V_{DD} X 0.7	-	V_{DD}	V	PORTA - PORTE, V_{DD} =2.4V - 5.5V
		V_{DD} X 0.8	-	V_{DD}	V	T0, $\overline{RESET}$, (Schmitt trigger input) V_{DD} =2.4V - 5.5V
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pin, without pull-high resistor, V_{IN} = V_{DD} or GND V_{DD} = 5.0V
		-1	-	1	μA	Input pin, without pull-high resistor, V_{IN} = V_{DD} or GND V_{DD} = 3.0V
Pull-high Resistor	R_{PH}	-	100	-	kΩ	PORTA - PORTE, V_{IN} = GND, V_{DD} = 5.0V
		-	200	-	kΩ	PORTA - PORTE, V_{IN} = GND, V_{DD} = 3.0V
Pull-low Resistor	R_{PL}	-	100	-	kΩ	PORTA - PORTE, V_{IN} = V_{DD}, V_{DD} = 5.0V
		-	200	-	kΩ	PORTA - PORTE, V_{IN} = V_{DD}, V_{DD} = 3.0V
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	PORTA - PORTE, I_{OH} = -5mA, V_{DD} = 5.0V
		V_{DD} - 0.7	-	-	V	PORTA - PORTE, I_{OH} = -3mA, V_{DD} = 3.0V
		V_{DD} - 0.6	-	-	V	SEGx to be output port or LED SEGx I_{OH} = -1.5mA, V_{DD} = 5.0V
		V_{DD} - 0.6	-	-	V	SEGx to be output port or LED SEGx I_{OH} = -1mA V_{DD} = 3.0V
		V_{DD} - 0.6	-	-	V	LED COMx, I_{OH} = -150μA, V_{DD} = 5.0V
		V_{DD} - 0.6	-	-	V	LED COMx, I_{OH} = -100μA, V_{DD} = 3.0V
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	PORTA - PORTE, I_{OL} = 10mA, V_{DD} = 5.0V
		-	-	GND + 0.6	V	PORTA - PORTE, I_{OL} = 4mA, V_{DD} = 3.0V
		-	-	GND + 0.6	V	SEGx to be output port or LED SEGx, I_{OL} = 1.5mA, V_{DD} = 5.0V
		-	-	GND + 0.6	V	SEGx to be output port or LED SEGx, I_{OL} = 1mA, V_{DD} = 3.0V
		-	-	GND + 0.6	V	LED COMx, I_{OL} = 4mA, V_{DD} = 5.0V
		-	-	GND + 0.6	V	LED COMx, I_{OL} = 2.5mA, V_{DD} = 3.0V
LCD Driving on Resistor	R_{ON}	-	5	-	kΩ	LCD COMx, LCD SEGx, the voltage variation of V1, V2, V3 is less than 0.2V. V_{DD} = 3.0V - 5.0V
LCD Voltage Divider Resistor	R_{LCD}	-	270	-	kΩ	RLCD1, RLCD0 = 0, 0
		-	90	-	kΩ	RLCD1, RLCD0 = 0, 1
		-	30	-	kΩ	RLCD1, RLCD0 = 1, 0
		-	10	-	kΩ	RLCD1, RLCD0 = 1, 1

AC Electrical Characteristics

V_{DD} = 5.0V, GND = 0V, T_A = +25°C, f_{OSC} = 30kHz - 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction cycle time	t_{CY}	0.5	-	133.4	μs	
T0 input width	t_{IW}	(t_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	

V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = +25°C, f_{OSC} = 30kHz - 8MHz, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width	t_{RESET}	10	-	-	μs	Low active, V_{DD} = 5.0V
WDT Period	T_{WDT}	1	-	-	ms	V_{DD} = 5.0V
Frequency Stability (RC)	|Δf|/f	-	-	20	%	External R_{OSC} Oscillator, Include supply voltage, temperature and chip-to-chip variation T_A = -40°C to +85°C |f(5.0V)-f(4.5V)|/f(5.0V), |f(3.0V)-f(2.7V)|/f(3.0V)

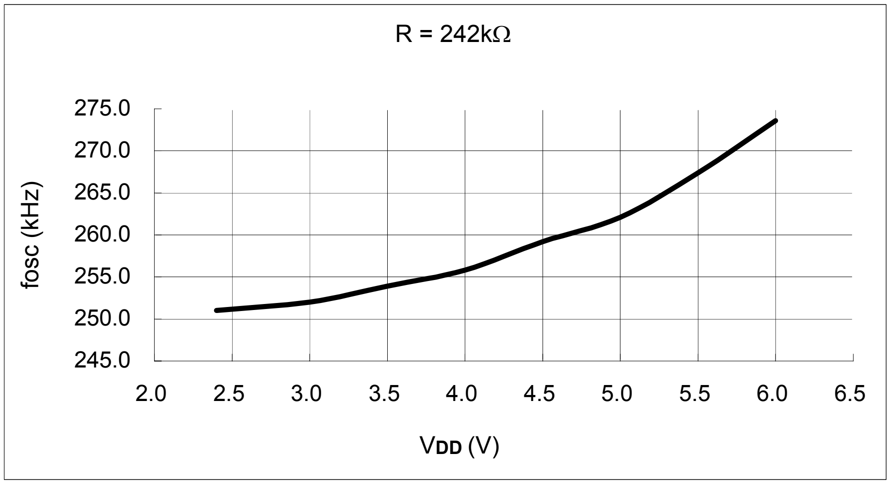
ADC Electrical Characteristics

V_{DD} = 2.4V - 5.5V, GND = 0V, T_A = +25°C, f_{OSC} = 30kHz - 8MHz, unless otherwise specified.

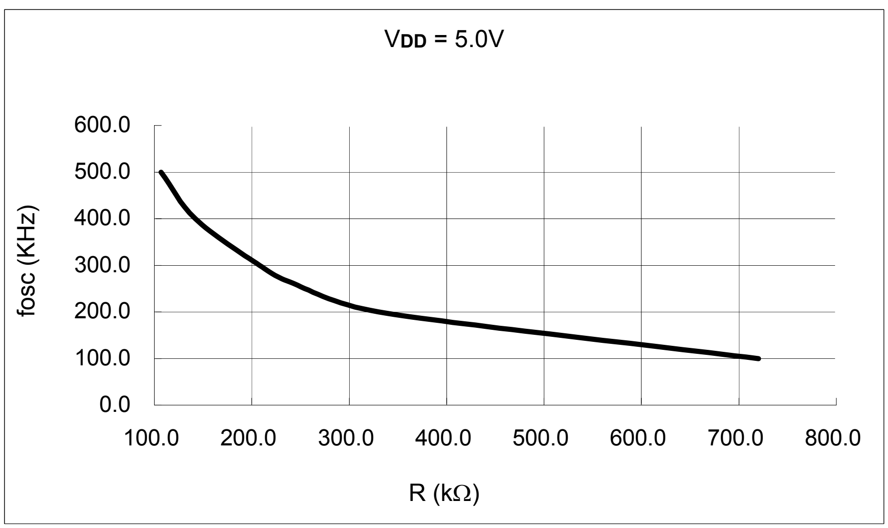
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	NR	-	-	8	bit	GND ≤ V_{AIN} ≤ V_{REF}
Reference Voltage	V_{REF}	2.4	-	V_{DD}	V	
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor	R_{AIN}	1000	-	-	kΩ	V_{IN} = 5.0V
A/D conversion current	I_{AD}	-	100	300	μA	ADC module operating, V_{DD} = 5.0V
Nonlinear Error	E_{NL}	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Full scale error	E_F	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Offset error	E_Z	-	-	±1	LSB	V_{REF} = V_{DD} = 5.0V
Total Absolute error	E_{AD}	-	±0.5	±1	LSB	V_{REF} = V_{DD} = 5.0V
A/D Clock Period	t_{AD}	1	-	33.4	μs	f_{OSC} = 30kHz - 8MHz
A/D Conversion Time	t_{CNV1}	-	50	-	t_{AD}	Set ADCS = 0
A/D Conversion Time	t_{CNV2}	-	330	-	t_{AD}	Set ADCS = 1

RC Oscillator Characteristics Graphs

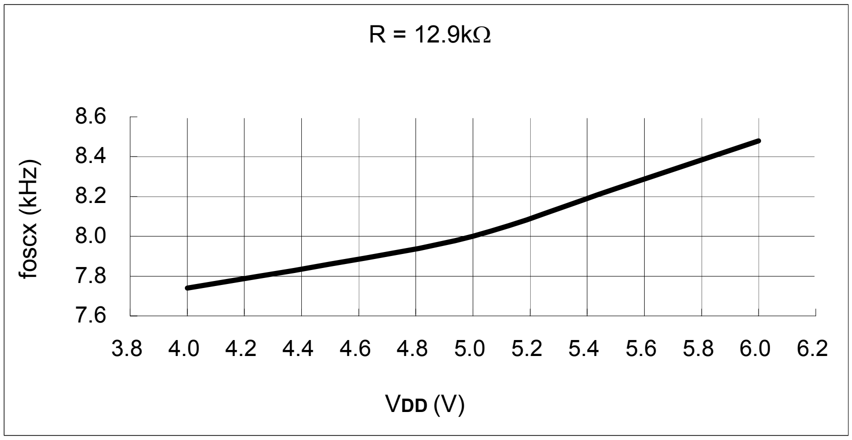
Typical External Oscillator (OSC) Frequency vs. Operating Voltage: (for reference only)
(R = 242 KΩ)



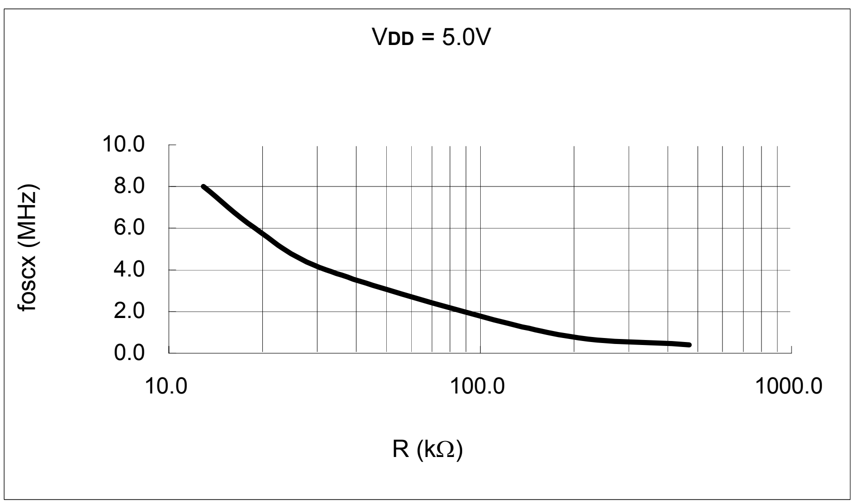
Typical External RC Oscillator (OSC) Resistor vs. Frequency: (for reference only)



Typical External RC oscillator (OSCX) Frequency vs. Operating Voltage: (for reference only)
(R = 12.9 KΩ)

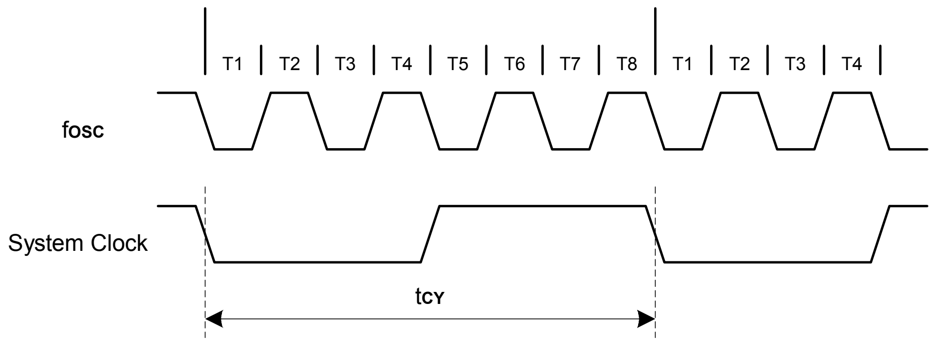


Typical External RC Oscillator (OSCX) Resistor vs. Frequency: (for reference only)

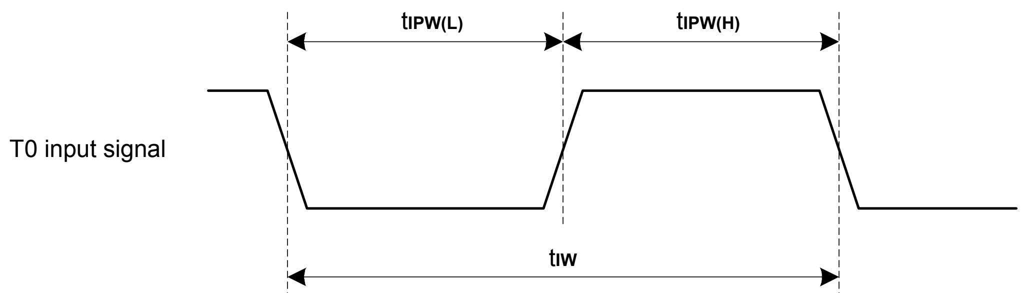


Timing Waveform

(a) System Clock Timing Waveform:



(b) T0 Input Waveform:

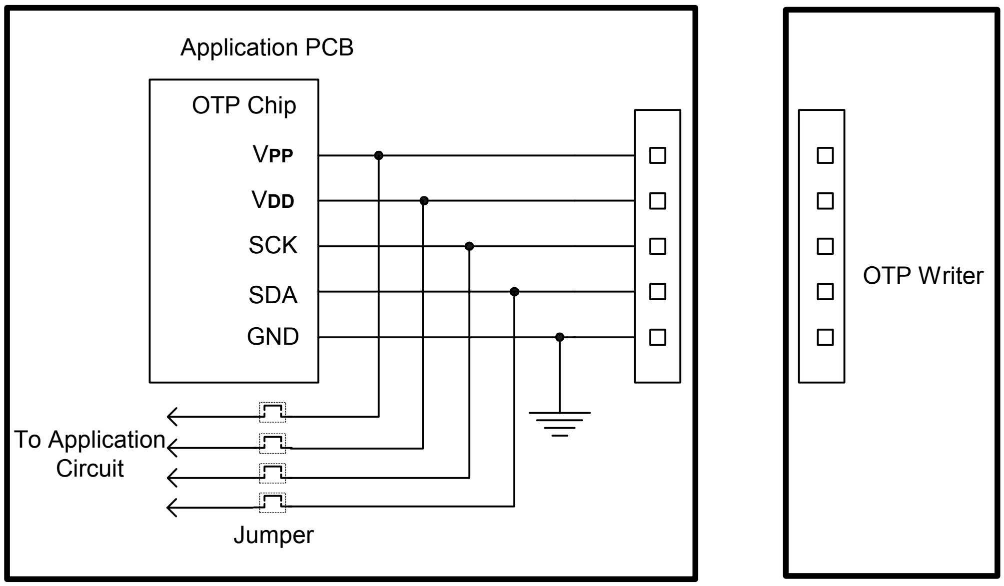


In System Programming Notes for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are the followings:

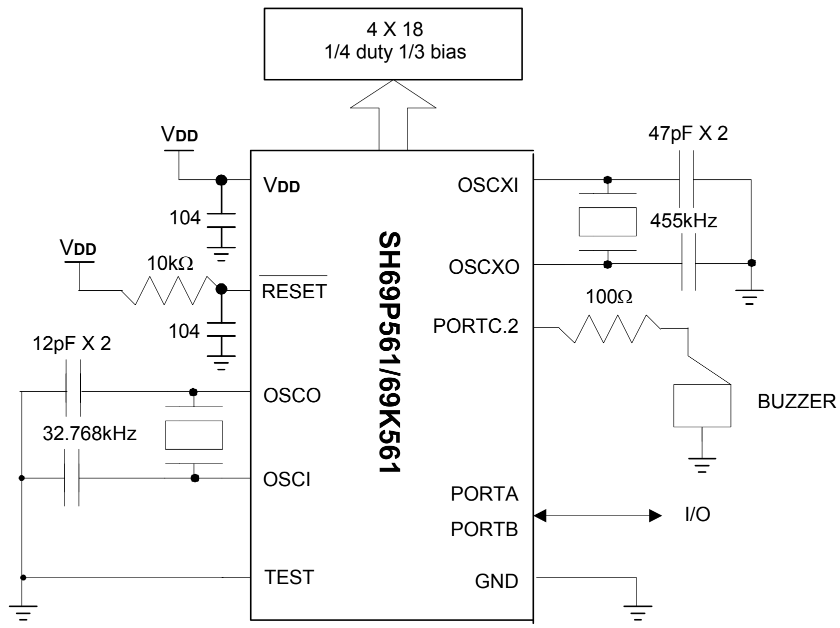
(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.
(2) Connect the programming interface with OTP writer and begin programming.
(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Application Circuit (for reference only)

Ap1:

(1) Operating voltage:	5.0V
(2) OSC:	Crystal oscillator 32.768kHz (code option)
OSCX:	Ceramic oscillator 455kHz (code option)
(3) PORTA - PORTB:	I/O
PORTC.2:	Alarm ouput
(4) LCD:	1/4 duty, 1/3 bias

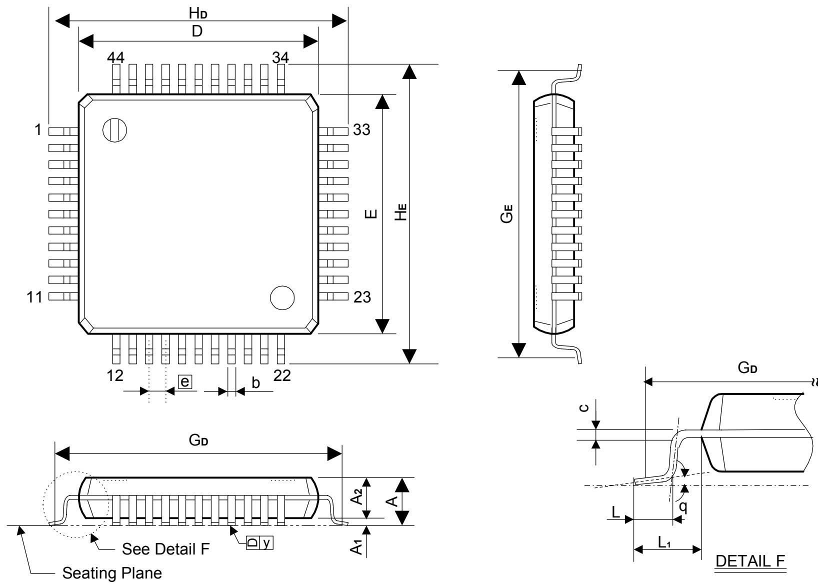


Ordering Information

Part No.	Package
SH69P561F	44 QFP
SH69K561F	44 QFP

Package Information

QFP 44 Outline Dimensions unit: inch/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.70 Max.
A_1	0.01 Min. 0.02Max.	0.25 Min. 0.50Max.
A_2	0.079+0.008 -0.004	2.00+0.2 -0.1
b	0.012 Typ.	0.30 Typ.
c	0.006 ± 0.002	0.15 ± 0.05
D	0.394 ± 0.004	10.00 ± 0.10
E	0.394 ± 0.004	10.00 ± 0.10
e	0.031 Typ.	0.80 Typ.
G_D	0.488 NOM.	12.40 NOM.
G_E	0.488 NOM.	12.40 NOM.
H_D	0.519 ± 0.008	13.20 ± 0.20
H_E	0.519 ± 0.008	13.20 ± 0.20
L	0.035+0.002 -0.006	0.88+0.05 -0.15
L_1	0.063 Typ.	1.60 Typ.
y	0.004 Max.	0.10 Max.
θ	0° - 7°	0° - 7°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

Data Sheet Revision History

Version	Content	Date
2.1	Package information update	Dec.2008
2.0	Revise the Timer0 clock source from “System clock” to “fosc/4”	Jul. 2006
1.0	Original	Mar. 2006