SH77P1651/1652

Enhanced 8051 Microcontroller with 10bit ADC

1. Features

- 8bits micro-controller with Pipe-line structured 8051 compatible instruction set
- OTP ROM:
  - 4K X 8bit, program four times
  - 8K X 8bit, program two times
  - 16K X 8bit, program one time
- RAM: internal 256 Bytes, external 286 Bytes
- Operation Voltage: 1.8V - 3.6V
- Oscillator (code option)
  - Crystal oscillator: 32.768kHz
  - Internal RC: 32kHz
  - Internal RC: 4MHz
- 46 CMOS bi-directional I/O pins
- One open-drain I/O pin
- Built-in pull-up resistor for input pins
- Two 16-bit timer/counters: T2, T3
- One 8-bit PWM
- One remote control carrier wave generator
- Three I/O with 20mA sink current, act as LCD backlight driver
- One I/O with 500mA sink current, act as remote control
- 7channels 10-bits Analog Digital Converter (ADC), with comparator function built-in (no ADC in SH77P1651)
- One EUART
- Interrupt sources:
  - INT41 - INT47
  - Timer2, 3
  - PWM1, REM
  - ADC, EUART, SCM
- LCD driver(Resistor and Capacitor Mode):
  - 4 X 30 dots (1/4 duty, 1/3 bias)
  - 5 X 29 dots (1/5 duty, 1/3 bias)
- Low Voltage Reset (LVR) function
- CPU Machine cycle: 1 oscillator clock
- Watch Dog Timer (WDT)
- Warm-up Counter
- Support Low power operation modes:
  - Idle Mode
  - Power-Down Mode
- Package:
  - TQFP48 (SH77P1651)
  - TQFP48 and chip form (SH77P1652)

2. General Description

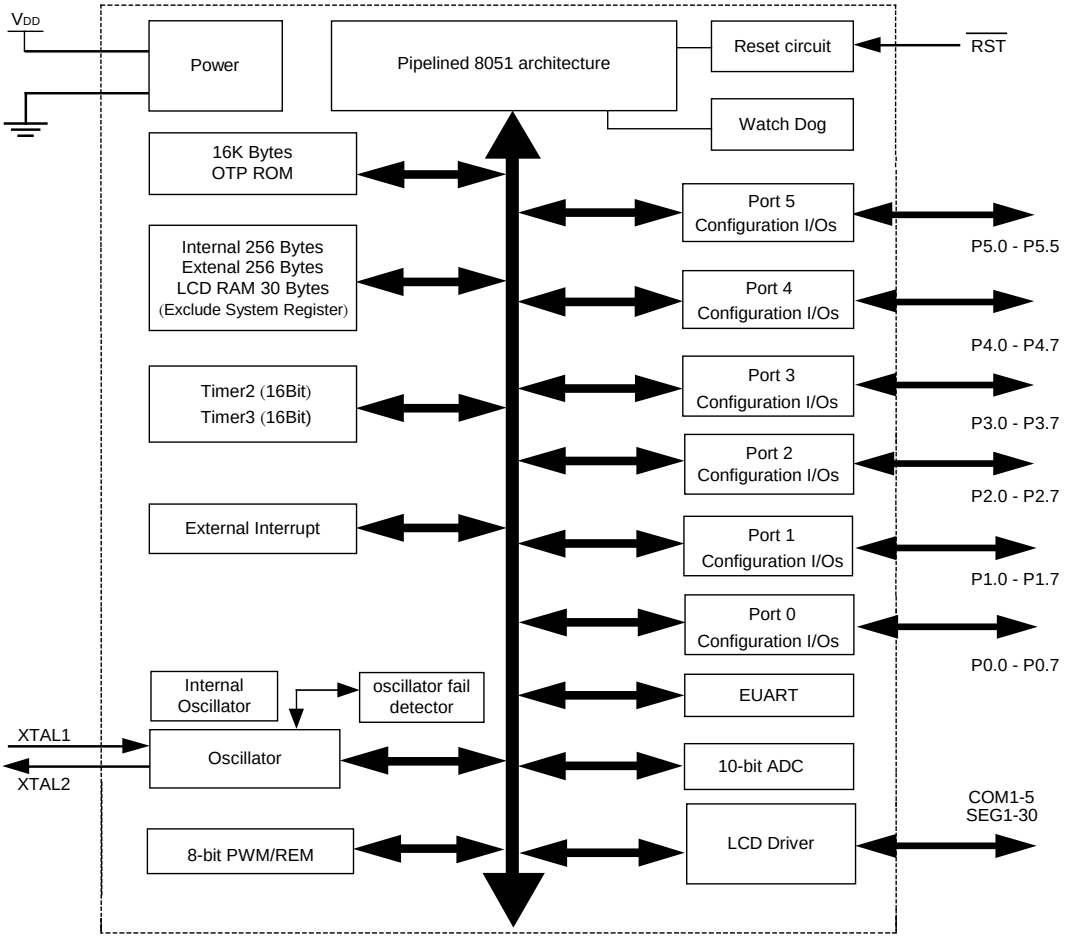
The SH77P1651/SH77P1652 is a high performance 8051 compatible micro-controller, compare with standard 8051 at the same clock frequency, the SH77P1651/SH77P1652 performs more fast operation speed and higher calculation performance.

The SH77P1651/SH77P1652 retains most features of the standard 8051. These features include internal 256 bytes RAM, 1 UART and 1 external interrupt (8 Multiplexed Input Channels).

In addition, the SH77P1651/SH77P1652 builds in UART standard communication module, LCD voltage regulator circuit, capacitor bias circuit, resistor bias circuit and 1 PWM, etc.

For high reliability and low cost issues, the SH77P1651/SH77P1652 builds in Watchdog Timer, Low Voltage Reset function and system clock monitor function, in addition, SH77P1651/SH77P1652 supports two power saving modes to reduce power consumption.

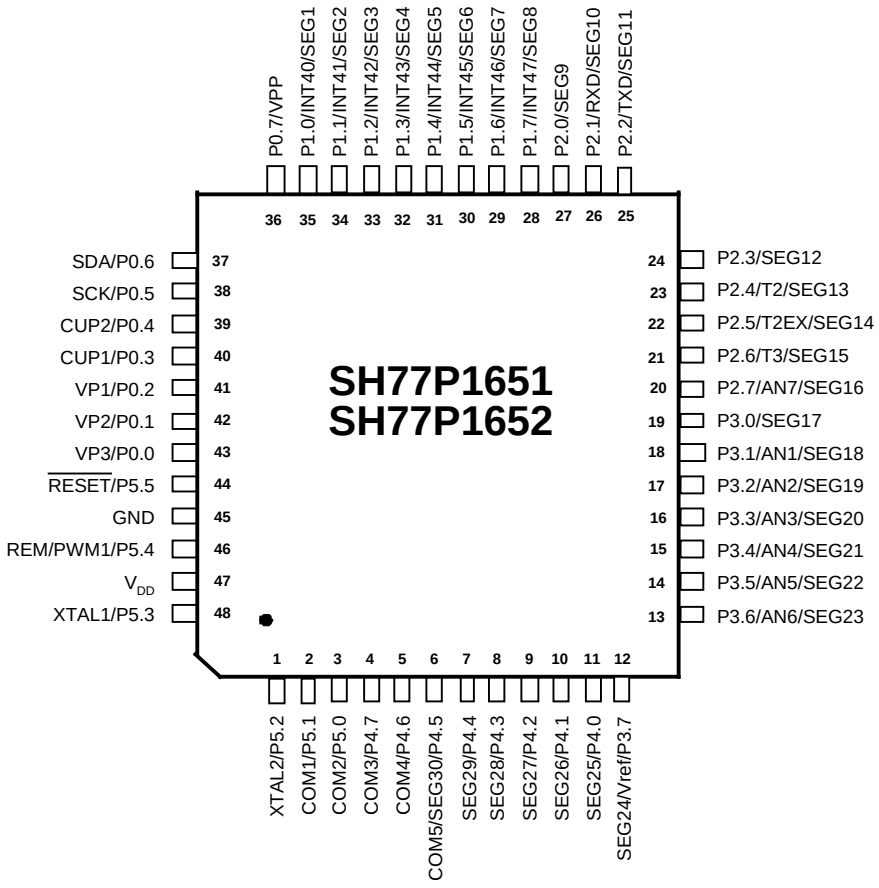
3. Block Diagram



Note: *no ADC in SH77P1651*

4. Pin Configuration

TQFP48



Pin Configuration Diagram

Total: 48 PIN

Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram. This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function use.

No ADC in SH77P1651.

Table 4.1 TQFP48 Pin Function

Pin No.	Pin Name	Default Function	Pin No.	Pin Name	Default Function
1	XTAL2/P5.2	P5.2	25	SEG11/TXD/P2.2	P2.2
2	COM1/P5.1	P5.1	26	SEG10/RXD/P2.1	P2.1
3	COM2/P5.0	P5.0	27	SEG9/P2.0	P2.0
4	COM3/P4.7	P4.7	28	SEG8/INT47/P1.7	P1.7
5	COM4/P4.6	P4.6	29	SEG7/INT46/P1.6	P1.6
6	COM5/SEG30/P4.5	P4.5	30	SEG6/INT45/P1.5	P1.5
7	SEG29/P4.4	P4.4	31	SEG5/INT44/P1.4	P1.4
8	SEG28/P4.3	P4.3	32	SEG4/INT43/P1.3	P1.3
9	SEG27/P4.2	P4.2	33	SEG3/INT42/P1.2	P1.2
10	SEG26/P4.1	P4.1	34	SEG2/INT41/P1.1	P1.1
11	SEG25/P4.0	P4.0	35	SEG1/INT40/P1.0	P1.0
12	SEG24/V_{REF}/P3.7	P3.7	36	VPP/P0.7	P0.7
13	SEG23/AN6/P3.6	P3.6	37	SDA/P0.6	P0.6
14	SEG22/AN5/P3.5	P3.5	38	SCK/P0.5	P0.5
15	SEG21/AN4/P3.4	P3.4	39	CUP2/P0.4	P0.4
16	SEG20/AN3/P3.3	P3.3	40	CUP1/P0.3	P0.3
17	SEG19/AN2/P3.2	P3.2	41	VP1/P0.2	P0.2
18	SEG18/AN1/P3.1	P3.1	42	VP2/P0.1	P0.1
19	SEG17/P3.0	P3.0	43	VP3/P0.0	P0.0
20	SEG16/AN7/P2.7	P2.7	44	$\overline{\text{RESET}}$/P5.5	$\overline{\text{RESET}}$
21	SEG15/T3/P2.6	P2.6	45	GND	GND
22	SEG14/T2EX/P2.5	P2.5	46	REM/PWM1/P5.4	P5.4
23	SEG13/T2/P2.4	P2.4	47	V_{DD}	V_{DD}
24	SEG12/P2.3	P2.3	48	XTAL1/P5.3	P5.3

**: These ports are configured as N-channel open drain I/O*

Table 4.2 Pin Description

Pin	Type	Description
PORT		
P0.0 - P0.7	I/O	8 bit General purpose CMOS I/O
P1.0 - P1.7	I/O	8 bit General purpose CMOS I/O
P2.0 - P2.7	I/O	8 bit General purpose CMOS I/O
P3.0 - P3.7	I/O	8 bit General purpose CMOS I/O
P4.0 - P4.7	I/O	8 bit General purpose CMOS I/O
P5.0 - P5.5	I/O	8 bit General purpose CMOS I/O
Timer		
T2	I/O	Timer2 external input
T2EX	I	Timer2 Reload/Capture/Direction Control
T3	I/O	Timer3 external input
EUART		
RXD	I/O	EUART data input
TXD	O	EUART data output
ADC		
AN1 - AN7	I	ADC input channel (*No ADC in SH77P1651*)
V_{REF}	I	External ADC reference voltage input (*No ADC in SH77P1651)*
PWM		
PWM1	O	PWM1 Output pin
REM		
REM	O	Carrier synthesizer for infrared output pin
LCD		
COM1 - COM4/5	O	Common signal output for LCD display
SEG1 - SEG30/29	O	Segment signal output for LCD display
LCD Capacitance Driver		
CUP1	P	Connection for LCD bias capacitor
CUP2	P	Connection for LCD bias capacitor
VP3	P	LCD Power
VP2	P	LCD Power
VP1	P	LCD Power
Interrupt & Reset & Clock & Power		
INT40 - INT47	I	External interrupt 40-47 input source
$\overline{\text{RESET}}$	I	The device will be reset by A low voltage on this pin longer than 10us, an internal resistor about 30kΩ to V_{DD}, So using only an external capacitor to GND can cause a power-on reset
XTAL1	I	Oscillator input
XTAL2	O	Oscillator output
GND	P	Ground
V_{DD}	P	Power supply

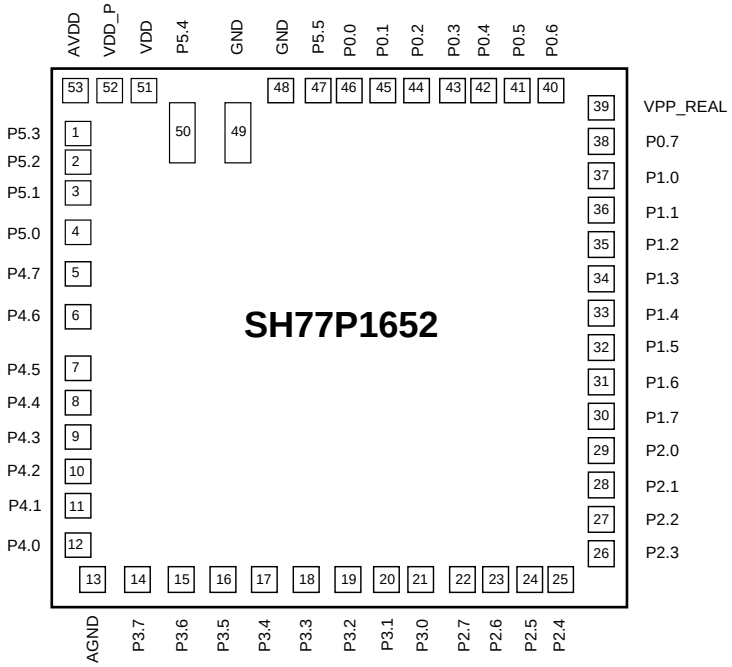
(to be continued)

(continue)

Pin	Type	Description
Programming Port		
V_{DD}	P	Programming Power (+3.3V)
VPP	P	Programming High Voltage Power (+7.5V)
GND	P	Ground
SCK	I	Programming Clock input Pin
SDA	I/O	Programming Data Pin

Note:
When P0.5, P0.6 and P0.7 are used as test ports, I/O function is forbidden.

5. Pad Configuration



PAD No.	PAD Name	Default Function	PAD No.	PAD Name	Default Function
1	P5.3	P5.3	28	P2.1	P2.1
2	P5.2	P5.2	29	P2.0	P2.0
3	P5.1	P5.1	30	P1.7	P1.7
4	P5.0	P5.0	31	P1.6	P1.6
5	P4.7	P4.7	32	P1.5	P1.5
6	P4.6	P4.6	33	P1.4	P1.4
7	P4.5	P4.5	34	P1.3	P1.3
8	P4.4	P4.4	35	P1.2	P1.2
9	P4.3	P4.3	36	P1.1	P1.1
10	P4.2	P4.2	37	P1.0	P1.0
11	P4.1	P4.1	38	P0.7	P0.7
12	P4.0	P4.0	39	VPP_REAL	VPP_REAL
13	AGND	AGND	40	P0.6	P0.6
14	P3.7	P3.7	41	P0.5	P0.5
15	P3.6	P3.6	42	P0.4	P0.4
16	P3.5	P3.5	43	P0.3	P0.3
17	P3.4	P3.4	*44	P0.2	P0.2
18	P3.3	P3.3	45	P0.1	P0.1
19	P3.2	P3.2	46	P0.0	P0.0
20	P3.1	P3.1	47	P5.5	P5.5
21	P3.0	P3.0	48	GND	GND
22	P2.7	P2.7	49	GND	GND
23	P2.6	P2.6	50	P5.4	P5.4
24	P2.5	P2.5	51	V_{DD}	V_{DD}
25	P2.4	P2.4	52	VDD_P	VDD_P
26	P2.3	P2.3	53	AV_{DD}	AV_{DD}
27	P2.2	P2.2			

**: unused PAD*

6. Product Information

Part Num	RAM (byte)	Flash (byte)	EUART	ADC (10bit)	PWM (8bit)	Timer	ExINT	Internal RC	IO	Package
SH77P1651	512+30	16K	1	-	1	2	8	±2%	46	TQFP48
SH77P1652	512+30	16K	1	7	1	2	8	±2%	46	TQFP48/ chip form

7. SFR Mapping

The SH77P1651/SH77P1652 provides 256 bytes of internal RAM which contain general-purpose data memory and Special Function Register (SFR). The SFRs of the SH77P1651/SH77P1652 are categoried as below:

CPU Core Registers:	ACC, B, PSW, SP, DPL, DPH
Enhanced CPU Core Registers:	AUXC, DPL1, DPH1, INSCON, XPAGE
Power and Clock Control Registers:	PCON, SUSLO
Data Memory Register:	XPAGE
OTP Access Control Register:	OTPCON
Hardware Watchdog Timer Registers:	RSTSTAT
System Clock Control Register:	CLKCON
Interrupt System Registers:	IEN0, IEN1, EXF0, EXF1, IPH0, IPL0, IPH1, IPL1, IENC
I/O Port Registers:	P0, P1, P2, P3, P4, P5, P0CR, P1CR, P2CR, P3CR, P4CR, P5CR, P0PCR, P1PCR, P2PCR, P3PCR, P4PCR, P5PCR
Timer Registers:	T2CON, T2MOD, TL2, TH2, RCAP2L, RCAP2H, T3CON, TL3, TH3
EUART Registers:	SCON, SBUF, SADEN, SADDR, PCON, SBRTH, SBRTL, SFINE
ADC Registers:	ADCON, ADCON1, ADT, ADCH, ADDL, ADDH
LCD Registers:	LCDCON, P1SS, P2SS, P3SS, P4SS, P5SS, LCDCON1
PWM Registers:	PWM1CON, PWM1P, PWM1D
REM Registers:	REMCON, REMNUMH, REMNUML

Table 7.1 CPU Core SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	C	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	----00-0	-	-	-	-	DIV	MUL	-	DPS

Table 7.2 Data Memory SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	F7H	Data Memory	-------0	-	-	-	-	-	-	-	XPAGE.0

Table 7.3 Power and Clock control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 7.4 OTP Access Control SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTPCON	B7H	OTP Access Control	-------0	-	-	-	-	-	-	-	FAC

Table 7.5 WDT SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H	Watchdog Timer Control	0-000000	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

Table 7.6 CLKCON SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	B2H	System Clock Control	111000--	32k_ SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	-	-

Table 7.7 Interrupt SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H	Interrupt Enable Control 0	0000----	EA	EADC	ET2	ES	-	-	-	-
IEN1	A9H	Interrupt Enable Control 1	00-00-0-	ESCM	EPWM1	-	ET3	EX4	-	EREM	-
IPL0	B8H	Interrupt Priority Control Low 0	-000----	-	PADCL	PT2L	PS0L	-	-	-	-
IPH0	B4H	Interrupt Priority Control High 0	-000----	-	PADCH	PT2H	PS0H	-	-	-	-
IPL1	B9H	Interrupt Priority Control Low 1	00-00-0-	PSCML	PPWM1L	-	PT3L	PX4L	-	PREML	-
IPH1	B5H	Interrupt Priority Control High 1	00-00-0-	PSCMH	PPWM1L	-	PT3H	PX4L	-	PREMH	-
EXF0	E8H	External interrupt Control 0	00------	IT4.1	IT4.0	-	-	-	-	-	-
IENC	BAH	Interrupt 4 channel enable control	00000000	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
EXF1	D8H	External interrupt Control 1	00000000	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40

Table 7.8 Port SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	80H	8-bit Port 0	00000000	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1	90H	8-bit Port 1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2	A0H	8-bit Port 2	00000000	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3	B0H	8-bit Port 3	00000000	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4	C0H	8-bit Port 4	00000000	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5	F8H	6-bit Port 5	--000000	-	-	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
P0CR	E1H	Port0 input/output direction control	00000000	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR	E2H	Port1 input/output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR	E3H	Port2 input/output direction control	00000000	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR	E4H	Port3 input/output direction control	00000000	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR	E5H	Port4 input/output direction control	00000000	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR	E6H	Port5 input/output direction control	--000000	-	-	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P0PCR	E9H	Internal pull-high enable for Port0	-0000000	-	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR	EAH	Internal pull-high enable for Port1	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR	EBH	Internal pull-high enable for Port2	00000000	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR	ECH	Internal pull-high enable for Port3	00000000	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR	EDH	Internal pull-high enable for Port4	00000000	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR	EEH	Internal pull-high enable for Port5	--000000	-	-	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0

Table 7.9 Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	C8H	Timer/Counter 2 Control	00--0000	TF2	EXF2	-	-	EXEN2	TR2	$\overline{C/T2}$	$\overline{CP/RL2}$
T2MOD	C9H	Timer/Counter 2 Mode	0-----00	TCLKP2	-	-	-	-	-	T2OE	DCEN
RCAP2L	CAH	Timer/Counter 2 Reload /Caprure Low Byte	00000000	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	CBH	Timer/Counter 2 Reload /Caprure High Byte	00000000	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH	Timer/Counter 2 Low Byte	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH	Timer/Counter 2 High Byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
T3CON	CEH	Timer/Counter 2 Control	0-00-000	TF3	-	T3PS1	T3PS0	-	TR3	T3CLKS1	T3CLKS0
TL3	F2H	Timer/Counter 3 Low Byte	00000000	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	F3H	Timer/Counter 3 High Byte	00000000	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0

Table 7.10 EUART SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	98H	Serial Control	00000000	SM0/FE	SM1/RXOV	SM2/TXCOL	REN	TB8	RB8	TI	RI
SBUF	99H	Serial Data Buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADDR	9AH	Slave Address	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN	9BH	Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
PCON	87H	Power & Serial Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SBRTH	9CH	Baud Rate Generator High Byte	00000000	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL	9DH	Baud Rate Generator Low Byte	00000000	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
SFINE	9EH	Baud Rate Generator (Fine tuning)	----0000	-	-	-	-	SFINE.3	SFINE.2	SFINE.1	SFINE.0

Table 7.11 ADC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	93H	ADC Control	00000000	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	GO/DONE
ADCON1	8FH	ADC Control 1	0-------	RGON	-	-	-	-	-	-	-
ADT	94H	ADC Time Configuration	000-0000	TADC2	TADC1	TADC0	-	TS3	TS2	TS1	TS0
ADCH	95H	ADC Channel Configuration	0000000-	CH7	CH6	CH5	CH4	CH3	CH2	CH1	-
ADDL	96H	ADC Data Low Byte	------00	-	-	-	-	-	-	A1	A0
ADDH	97H	ADC Data High Byte	00000000	A9	A8	A7	A6	A5	A4	A3	A2

Table 7.12 LCD SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON1	AAH	LCD Control 1	0-00-000	PUMPON	-	FCCTL1	FCCTL0	-	RLCD	MOD1	MOD0
LCDCON	ABH	LCD Control	00-0-000	LCDON	LCDSEL	-	DUTY	-	VOL2	VOL1	VOL0
P1SS	ADH	P1 mode Select	00000000	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
P2SS	BBH	P2 mode Select	00000000	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
P3SS	BCH	P3 mode Select	00000000	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0
P4SS	BDH	P4 mode Select	00000000	P4S7	P4S6	P4S5	P4S4	P4S3	P4S2	P4S1	P4S0
P5SS	BEH	P5 mode Select	------00	-	-	-	-	-	-	P5S1	P5S0

Table 7.13 PWM SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMCON	D9H	REM Control	------00	-	-	-	-	-	-	REMIF	REMSW
REMNUMH	DAH	REM Envelope Carrier Number High Byte	0-000000	REMHLSIGN	-	REMNUM.13	REMNUM.12	REMNUM.11	REMNUM.10	REMNUM.9	REMNUM.8
REMNUML	DBH	REM Envelope Carrier Number Low Byte	00000000	REMNUM.7	REMNUM.6	REMNUM.5	REMNUM.4	REMNUM.3	REMNUM.2	REMNUM.1	REMNUM.0
PWM1CON	DCH	PWM1 Control	0000--00	PWM1EN	PWM1S	PWM1CK1	PWM1CK0	-	-	PWM1IF	PWM1SS
PWM1P	DDH	PWM1 Period Control	00000000	PWM1P.7	PWM1P.6	PWM1P.5	PWM1P.4	PWM1P.3	PWM1P.2	PWM1P.1	PWM1P.0
PWM1D	DEH	PWM1 Duty Control	00000000	PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0

Note: *- :Reserved bit*

SFR Map

	Bit addressable	Non Bit addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H	P5	-	-	-	-	-	-	(Reserved)	FFH
F0H	B	AUXC	TL3	TH3	-	-	-	XPAGE	F7H
E8H	EXF0	P0PCR	P1PCR	P2PCR	P3PCR	P4PCR	P5PCR	-	EFH
E0H	ACC	P0CR	P1CR	P2CR	P3CR	P4CR	P5CR	-	E7H
D8H	EXF1	REMCON	REMNUMH	REMNUML	PWM1CON	PWM1P	PWM1D		DFH
D0H	PSW	-	-	-	-	-	-	-	D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T3CON	-	CFH
C0H	P4	-	-	-	-	-	-	-	C7H
B8H	IPL0	IPL1	IENC	P2SS	P3SS	P4SS	P5SS	-	BFH
B0H	P3	RSTSTAT	CLKCON	-	IPH0	IPH1	-	OTPCON	B7H
A8H	IEN0	IEN1	LCDCON1	LCDCON	-	P1SS	-	-	AFH
A0H	P2	-	-	-	-	-	-	-	A7H
98H	SCON	SBUF	SADDR	SADEN	SBRTH	SBRTL	SFINE	-	9FH
90H	P1	-	-	ADCON	ADT	ADCH	ADDL	ADDH	97H
88H	-	-	-	-	-	-	SUSLO	ADCON1	8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

Note: *The unused addresses of SFR are not available.*

8. Normal Function

8.1 CPU

8.1.1 Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. The Names for accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Table 8.1 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	C	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**C**	**Carry flag bit** 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	**AC**	**Auxiliary Carry flag bit** 0: an auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	**F0**	**F0 flag bit** Available to the user for general purposes
4-3	**RS[1:0]**	**R0-R7 Register bank select bits** 00: Bank0 (Address to 00H-07H) 01: Bank1 (Address to 08H-0FH) 10: Bank2 (Address to 10H-17H) 11: Bank3 (Address to 18H-1FH)
2	**OV**	**Overflow flag bit** 0: no overflow happen 1: an overflow happen
1	**F1**	**F1 flag bit** Available to the user for general purposes
0	**P**	**Parity flag bit** 0: an even number of “one” bits in the Accumulator 1: an odd number of “one” bits in the Accumulator

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

8.1.2 Enhanced CPU core SFRs

- Extended 'MUL' and 'DIV' instructions: 16bit*8bit, 16bit/8bit
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH77P1651/SH77P1652 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8 bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16 bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8 bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16 bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is the same with DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

8.1.3 Register

Table 8.2 Data Pointer Select Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	-	-	-	-	DIV	MUL	-	DPS
R/W	-	-	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	-	0

Bit Number	Bit Name	Description
3	DIV	**16 bit/8 bit Divide Selection Bit** 0: 8 bit Divide 1: 16 bit Divide
2	MUL	**16 bit/8 bit Multiply Selection Bit** 0: 8 bit Multiply 1: 16 bit Multiply
0	DPS	**Data Pointer Selection Bit** 0: Data pointer 1: Data pointer1

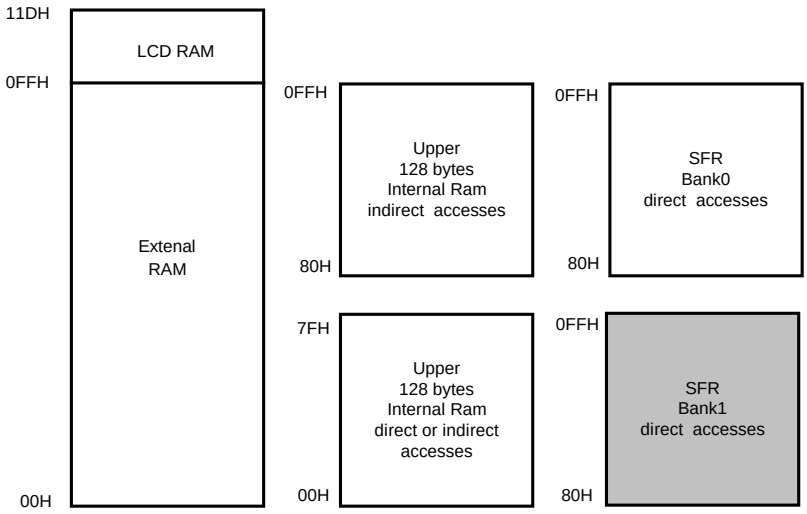
8.2 RAM

8.2.1 Features

SH77P1651/SH77P1652 provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:

- The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.
- The external RAM are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separated from SFR space. When an instruction accesses an internal location above address 7FH, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.



The SH77P1651/SH77P1652 provides traditional method for accessing of external RAM. Use *MOVX A, @Ri* or *MOVX @Ri, A* to access external low 256 bytes RAM, use *MOVX A, @DPTR, MOVX @DPTR, A* to access external 256 bytes RAM.

Users can also use XPAGE register to access external RAM only with *MOVX A, @Ri* or *MOVX @Ri, A* instructions. Users can use XPAGE to represent the high byte address of RAM above 256 Bytes.

8.2.2 Register

Table 8.3 Data Memory Page Register

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	-	-	-	-	-	-	XPAGE.0
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Name	Description
0	**XPAGE.0**	RAM page control-bit

8.3 OTP Program Memory

8.3.1 Features

- The SH77P1651/SH77P1652 built-in 16KB OTP program memory
- Built-in 128 bytes information area
- Minimum years data retention: 10
- Low Power Consumption

Accessing to the 128 bytes information area is similar to accessing OTP area, The difference is that FAC bit of OTPCON is set to 1 before accessing the information memory.

Note:

(1) When the 128 bytes information area is no need to be accessed, FAC bit should be cleared.
(2) Aboat the way to program OTP ROM please refer to help of ProWriter (《Pro03A烧写器使用说明》)

8.3.2 Register

Table 8.4 Access Control Register

B7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OTPCON	-	-	-	-	-	-	-	FAC
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Name	Description
0	**FAC**	**Access Control** 0: MOVC instruction access Main Block 1: MOVC instruction access the128 bytes information

8.4 System Clock and Oscillator

8.4.1 Features

- 32.768kHz crystal, Built-in 4MHz RC & 32kHz RC
- 2 Oscillator pins (XTAL1, XTAL2) are used to connect 32.768kHz crystal
- Built-in 32kHz WDT RC, is also available to SCM Clock
- Built-in 32.768kHz speed up circuit
- Built-in system clock prescaler

8.4.2 General Description

SH77P1651/SH77P1652 has three oscillator types: 32.768kHz crystal oscillator, internal RC (4MHz) and internal RC (32kHz), which is selected by code option OP_OSC (Refer to code option section for details). SH77P1651/SH77P1652 has two Oscillator pins (XTAL1, XTAL2), it can select one or two clock sources from three clock source that is selected by code option OP_OSC (Refer to code option section for details). The clock source provides the system clock to supply CPU and on-chip peripheral devices.

8.4.3 Clock Definition

The SH77P1651/SH77P1652 has several internal clocks defined as below:

OSCCLK: the oscillator clock from one of the three oscillator types (32.768kHz crystal oscillator, internal 4MHz RC and internal 32kHz RC). f_{OSC} is defined as the OSCCLK frequency, t_{OSC} is defined as the OSCCLK period.

32KCRYCLK: 32.768kHz crystal from external XTAL input, f_{32KCRY} is defined as the 32KCRYCLK frequency, t_{32KCRY} is defined as the 32KCRYCLK period.

LRCCLK: Internal 32kHz oscillator clock. f_{LRC} is defined as the LRCCLK frequency, t_{LRC} is defined as the LRCCLK period.

HRCCLK: Internal 4MHz oscillator clock. f_{HRC} is defined as the HRCCLK frequency, t_{HRC} is defined as the HRCCLK period.

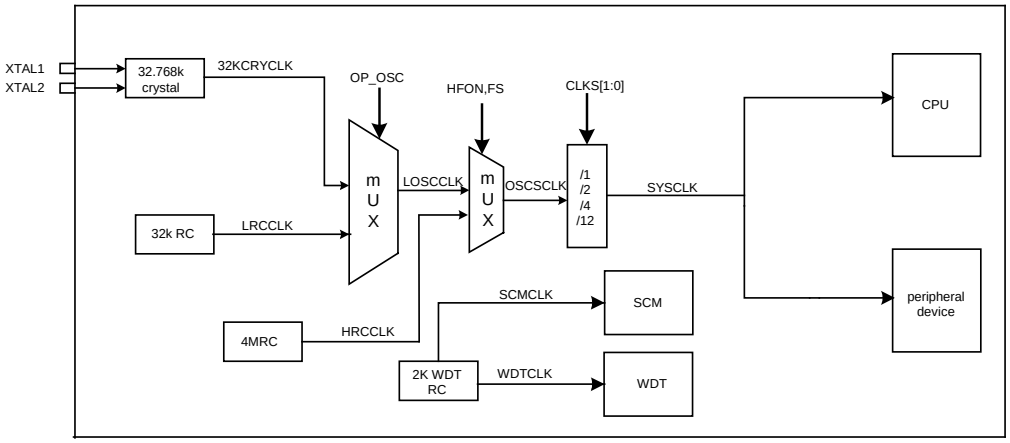
LOSCCLK: LOSCCLK is selected from three oscillator types defined by OP_OSC. f_{LOSC} is defined as the LOSCCLK frequency, t_{LOSC} is defined as the LOSCCLK period.

WDTCLK: the internal WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK period.

SCMCLK: Shared with the internal WDT RC clock.

OSCSCLK: the input of system clock prescaler. It can be LOSCCLK or HRCCLK, is selected by FS. f_{OSCS} is defined as the OSCSCLK frequency, t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output of system clock prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency, t_{SYS} is defined as the SYSCLK period.



8.4.4 Power Consumption Control

SH77P1651/SH77P1652 can select LOSCCLK or HRCCLK as OSCSCLK, No useful clock soure can be shut down after OSCSCLK is selected to reduce power consumption. After the clock source is shut down, if it is turned on again, you must wait for the oscillator warm-up time. It appears slow because of the clock source is not turned off throughout the clock switching process.

8.4.5 System Clock Monitor (SCM)

In order to enhance the system reliability, SH77P1651/SH77P1652 contains a system clock monitor (SCM) module. If the system clock fails (such as the oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal 32k WDTCLK and set system clock monitor bit (SCMIF) to 1.The SCM interrupt only occurs when EA and ESCM are 1. If the OSCCLK restores, SCM will switch the OSCCLK back to the oscillator and clears the SCMIF automatically.

Notes:

The SCMIF is a read only bit; it can only be clear or set by hardware.
If SCMIF is cleared, the SCM switches the system clock to the previous state automatically.
*If Internal RC is selected as OSCCLK by code option (Refer to **code option** section for detail), the SCM does not work.*

8.4.6 Register

Table 8.5 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	32k_SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	-	-
R/W	R/W	R/W	R/W	R	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	1	1	1	0	0	0	-	-

Bit Number	Bit Name	Description
7	**32k_SPDUP**	**32.768kHz oscillator speed up mode control bit** 0: 32.768kHz oscillator normal mode, cleared by software. 1: 32.768kHz oscillator speed up mode, set by hardware or software. This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. This bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when exit Power-down mode. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption. Only when code option OP_OSC is 1010 or 1101, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)
6-5	**CLKS[1:0]**	**SYSCLK Prescaler Register** 00: $f_{SYS} = f_{OSCS}$ 01: $f_{SYS} = f_{OSCS}/2$ 10: $f_{SYS} = f_{OSCS}/4$ 11: $f_{SYS} = f_{OSCS}/12$ If 32.768kHz oscillator is selected as OSCSCLK, these control bits is invalid.
3	**HFON**	**Internal 4MHz RC Switch Control Register** 0: turn off Internal 4MHz RC 1: turn on Internal 4MHz RC
2	**FS**	**Frequency Select Register** 0: LOSCCLK is selected as OSCSCLK 1: Internal 4MHz RC is selected as OSCSCLK

Note:

1. If code option OP_OSC is 1, OSCXCLK is the external 32.768kHz oscillator*.*
2. If code option OP_OSC is 0, OSCXCLK is the internal 32kHz RC oscillator*.*
3. When OSCSCLK changed from 32.768kHz/32kHz to 4MHz RC *and HRCCLK is turned off, the steps below must be done in sequence:*
   a. Set HFON = 1 to turn on the HRCCLK
   *b. Wait at least Oscillator Warm-up time (Refer to **Warm-up Timer** section for details)*
   c. Set FS = 1 to select 4MHz *as OSCSCLK*
4. When OSCSCLK changed from 4MHz RC *to 32.768kHz/32kHz, the steps below must be done in sequence:*
   a. Clear FS to select 32.768kHz/32kHz as OSCSCLK
   b. Add one nop
   c. Clear HFON

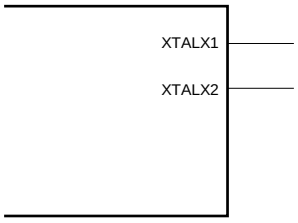
Table 8.6 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	-	-	-	SCMIF	-	-	-	-
R/W	-	-	-	R	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	-	-	-	-

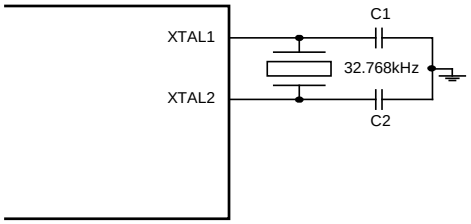
Bit Number	Bit Name	Description
4	**SCMIF**	**System Clock Monitor bit** 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails

8.4.7 Oscillator Type

(1) OP_OSC = 0: internal RC, XTAL1 and XTAL2 are shared as IO



(2) OP_OSC = 1: 32.768kHz Crystal Oscillator at XTAL, Internal *32kHz* RC is turned off



Crystal Oscillator			Recommended Type
Frequency	**C1**	**C2**	
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (ϕ 3x8)
			ϕ 3x8 - 32.768kHz

Notes:

(1) ***Capacitor values are used for design guidance only!***

(2) These capacitors were tested with the crystals listed above for basic start-up and operation. They are ***not optimized.***

(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit *http://www.sinowealth.com*for more recommended manufactures.

8.5 I/O Port

8.5.1 Features

- 46 bi-directional I/O ports, all support bit operation
- 1 open drain I/O port (P0.7)
- 3 I/O ports with 20mA sink current, can be used to drive LCD backlight (P0.6, P2.2, P2.3)
- 1 I/O ports with 500mA sink current, can be used to drive Remote Carrier (P5.4)
- Share with alternative functions

The SH77P1651/SH77P1652 has 46 bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x = 0-5, y = 0-7).

For SH77P1651/SH77P1652, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions be conflict when all the functions are enabled. (Refer to **Port Share** Section for details).

8.5.2 Register

Table 8.7 Port Control Register

E1H - E6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CR (E1H)	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR (E2H)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR (E3H)	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR (E4H)	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR (E5H)	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR (E6H)	-	-	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**PxCRy x = 0-5, y = 0-7**	**Port input/output direction control Register** 0: input mode 1: output mode

Table 8.8 Port Pull up Resistor Control Register

E9H - EEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PCR (E9H)	-	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR (EAH)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR (EBH)	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR (ECH)	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR (EDH)	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR (EEH)	-	-	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**PxPCRy x = 0-5, y = 0-7**	**Input Port internal pull-high resistor control** 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled

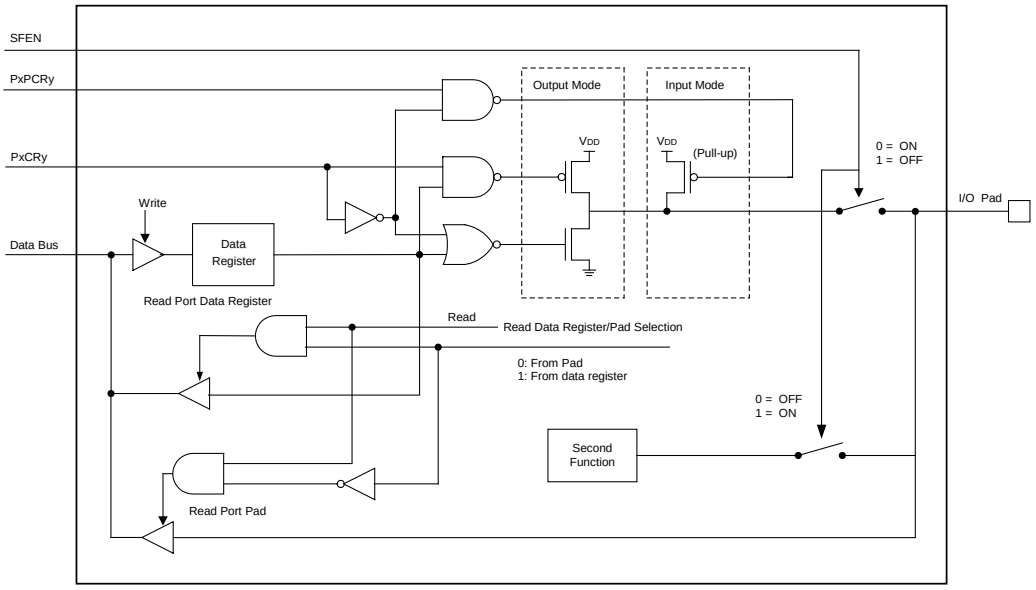
Table 8.9 Port Data Register

80H - F8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0 (80H)	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1 (90H)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2 (A0H)	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3 (B0H)	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4 (C0H)	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5 (F8H)	-	-	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**Px.y** **x = 0-5, y = 0-7**	Port Data Register

Note: *P0.7 is configured as N-channel open drain I/O, but voltage provided for this pin can't exceed V_{DD}+0.3V.*

8.5.3 Port Diagram



Note:

(1) The input source of reading input port operation is from the input pin directly.
(2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly.
(3) The read Instruction distinguishes which path is selected:The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.The destination of writing port operation is the data register regardless the port shared as the second function or not.

8.5.4 Port Share

The 46 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Highest Inner Lowest** rule:

The outmost pin function in **Pin Configuration** has the highest priority, and the innermost pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin, even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 0-5), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register while the port pin keeps unchanged until all the share functions are disabled.

PORT0:

- VP3: Power supply pin for LCD (P0.0)
- VP2: Power supply pin for LCD (P0.1)
- VP1: Power supply pin for LCD (P0.2)
- CUP1: Connect to capacitance pin for LCD pump circuit (P0.3)
- CUP2: Connect to capacitance pin for LCD pump circuit (P0.4)
- SCK: Programming data clock (P0.5)
- SDA: Programming data input port (P0.6)
- VPP: Programming voltage input (P0.7)

Table 8.10 PORT0 Share Table

Pin No.	SPriority	Function	Enable bit
43	1	VP3	**OP_LCDSEL** select capacitor LCD driver in **option code**
	2	P0.0	**OP_LCDSEL** select resistor LCD driver in **option code**
42	1	VP2	**OP_LCDSEL** select capacitor LCD driver in **option code**
	2	P0.1	**OP_LCDSEL** select resistor LCD driver in **option code**
41	1	VP1	**OP_LCDSEL** select capacitor LCD driver in **option code**
	2	P0.2	**OP_LCDSEL** select resistor LCD driver in **option code**
40	1	CUP1	**OP_LCDSEL** select capacitor LCD driver in **option code**
	2	P0.3	**OP_LCDSEL** select resistor LCD driver in **option code**
39	1	CUP2	**OP_LCDSEL** select capacitor LCD driver in **option code**
	2	P0.4	**OP_LCDSEL** select resistor LCD driver in **option code**
38	1	SCK	-
	2	P0.5	Above condition is not met
37	1	SDA	-
	2	P0.6	Above condition is not met
36	1	VPP	-
	2	P0.7	Above condition is not met

PORT1:
- SEG1/INT40: LCD Segment1/external inturrupt40 (P1.0)
- SEG2/INT41: LCD Segment2/external inturrupt41 (P1.1)
- SEG3/INT42: LCD Segment3/external inturrupt42 (P1.2)
- SEG4/INT43: LCD Segment4/external inturrupt43 (P1.3)
- SEG5/INT44: LCD Segment5/external inturrupt44 (P1.4)
- SEG6/INT45: LCD Segment6/external inturrupt45 (P1.5)
- SEG7/INT46: LCD Segment7/external inturrupt46 (P1.6)
- SEG8/INT47: LCD Segment8/external inturrupt47 (P1.7)

Table 8.11 PORT1 Share Table

Pin No.	SPriority	Function	Enable bit
35	1	SEG1	Set **P1S0** bit in **P1SS** register
	2	INT40	Set EX4 bit in IEN1 Register, Set EXS40 bit in IENC Register and Port1.0 is in input mode (pull up by software)
	3	P1.0	Above condition is not met
34	1	SEG2	Set **P1S1** bit in **P1SS** register
	2	INT41	Set EX4 bit in IEN1 Register, Set EXS41 bit in IENC Register and Port1.1 is in input mode (pull up by software)
	3	P1.1	Above condition is not met
33	1	SEG3	Set **P1S2** bit in **P1SS** register
	2	INT42	Set EX4 bit in IEN1 Register, Set EXS42 bit in IENC Register and Port1.2 is in input mode (pull up by software)
	3	P1.2	Above condition is not met
32	1	SEG4	Set **P1S3** bit in **P1SS** register
	2	INT43	Set EX4 bit in IEN1 Register, Set EXS43 bit in IENC Register and Port1.3 is in input mode (pull up by software)
	3	P1.3	Above condition is not met
31	1	SEG5	Set **P1S4** bit in **P1SS** register
	2	INT44	Set EX4 bit in IEN1 Register, Set EXS44 bit in IENC Register and Port1.4 is in input mode (pull up by software)
	3	P1.4	Above condition is not met
30	1	SEG6	Set **P1S5** bit in **P1SS** register
	2	INT45	Set EX4 bit in IEN1 Register, Set EXS45 bit in IENC Register and Port1.5 is in input mode (pull up by software)
	3	P1.5	Above condition is not met
29	1	SEG7	Set **P1S6** bit in **P1SS** register
	2	INT46	Set EX4 bit in IEN1 Register, Set EXS46 bit in IENC Register and Port1.6 is in input mode (pull up by software)
	3	P1.6	Above condition is not met
28	1	SEG8	Set **P1S7** bit in **P1SS** register
	2	INT47	Set EX4 bit in IEN1 Register, Set EXS47 bit in IENC Register and Port1.7 is in input mode (pull up by software)
	3	P1.7	Above condition is not met

PORT2:

- SEG9: LCD Segment 9 (P2.0)
- SEG10/RXD: LCD Segment10/Serial receive (P2.1)
- SEG11/TXD: LCD Segment11/Serial transmit (P2.2)
- SEG12: LCD Segment12 (P2.3)
- SEG13/T2: LCD Segment13/Timer2 external input (P2.4)
- SEG14/T2EX: LCD Segment14/Timer2 reload, capture, direction control (P2.5)
- SEG15/T3: LCD Segment15/Timer3 external input (P2.6)
- SEG16/AN7: LCD Segment16/ADC input channel (P2.7)

Table 8.12 PORT2 Share Table

Pin No.	SPriority	Function	Enable bit
27	1	SEG9	Set **P2S0** bit in **P2SS** register
	2	P2.0	Above condition is not met
26	1	SEG10	Set **P2S1** bit in **P2SS** register
	2	RXD	Set **REN** bit in **SCON** register
	3	P2.1	Above condition is not met
25	1	SEG11	Set **P2S2** bit in **P2SS** register
	2	TXD	Write to **SBUF** register
	3	P2.2	Above condition is not met
24	1	SEG12	Set **P2S3** bit in **P2SS** register
	2	P2.3	Above condition is not met
23	1	SEG13	Set **P2S4** bit in **P2SS** register
	2	T2	Set **TR2** bit and **C/$\overline{T2}$** bit in **T2CON** register (Auto Pull up) or clear **C/$\overline{T2}$** bit and set **T2OE** bit in **T2MOD** register
	3	P2.4	Above condition is not met
22	1	SEG14	Set **P2S5** bit in **P2SS** register
	2	T2EX	In mode 0 or 2, set **EXEN2 bit in T2CON** register, or in mode 1, set **DCEN bit in T2CON** register or in mode1, clear **DCEN** bit and set **EXEN2** bit (Auto Pull up)
	3	P2.5	Above condition is not met
21	1	SEG15	Set **P2S6** bit in **P2SS** register
	2	T3	Set **TR3** bit in **T3CON** register **and T3CLKS[1:0] = 01** (Auto Pull up)
	3	P2.6	Above condition is not met
20	1	SEG16	Set **P2S7** bit in **P2SS** register
	2	AN7	Set **CH7** bit in **ADCH** Register and set **SCH [2:0]**
	3	P2.7	Above condition is not met

PORT3:

- SEG17 - SEG23: LCD Segment 17 - LCD Segment 23 (P3.0 - P3.6)
- AN1 - AN6: ADC input channel (P3.1 - P3.6) (No ADC in SH77P1651)
- SEG24/V_{REF}: LCD Segment24/ADC reference voltage (P3.7)

Table 8.13 PORT3 Share Table

Pin No.	SPriority	Function	Enable bit
12	1	SEG24	Set **P3S7** bit in **P3SS** register
	2	V_{REF}	Set **ADON** bit and **REFC** bit in **ADCON** register
	3	P3.7	Above condition is not met
18-13	1	SEG23-SEG18	Set **P3S1 - P3S6** bit in **P3SS** register
	2	AN1-AN6	Set **CH6-CH1** bit and **SCH[2:0]** bit in **ADCH** register (No ADC in SH77P1651)
	3	P3.1-P3.6	Above condition is not met
19	1	SEG17	Set **P3S0** bit in **P3SS** register
	2	P3.0	Above condition is not met

PORT4:

- SEG25: LCD Segment25 (P4.0)
- SEG26: LCD Segment26 (P4.1)
- SEG27: LCD Segment27 (P4.2)
- SEG28: LCD Segment28 (P4.3)
- SEG29: LCD Segment29 (P4.4)
- SEG30: LCD Segment30 (P4.5)
- COM4: LCD COM4 (P4.6)
- COM3: LCD COM3 (P4.7)

Table 8.14 PORT4 Share Table

Pin No.	SPriority	Function	Enable bit
11	1	SEG25	Set **P4S0** bit in **P4SS** register
	2	P4.0	Above condition is not met
10	1	SEG26	Set **P4S1** bit in **P4SS** register
	2	P4.1	Above condition is not met
9	1	SEG27	Set **P4S2** bit in **P4SS** register
	2	P4.2	Above condition is not met
8	1	SEG28	Set **P4S3** bit in **P4SS** register
	2	P4.3	Above condition is not met
7	1	SEG29	Set **P4S4** bit in **P4SS** register
	2	P4.4	Above condition is not met
6	1	COM5	Set **DUTY** bit in **LCDCON**register
	2	SEG30	Set **P4S5** bit in **P4SS** register
	3	P4.5	Above condition is not met
5	1	COM4	Set **P4S6** bit in **P4SS** register
	2	P4.6	Above condition is not met
4	1	COM3	Set **P4S7** bit in **P4SS** register
	2	P4.7	Above condition is not met

PORT5:
- COM2 : LCD COM2 (P5.0)
- COM1 : LCD COM1 (P5.1)
- XTAL2 : External crystal output (P5.2)
- XTAL1 : External crystal input (P5.3)
- PWM1 : PWM1/REM output (P5.4)
- $\overline{\text{RESET}}$: PIN reset (P5.5)

Table 8.15 PORT5 Share Table

Pin No.	SPriority	Function	Enable bit
3	1	COM2	Set **P5S0** bit in **P5SS** register
	2	P5.0	Above condition is not met
2	1	COM1	Set **P5S1** bit in **P5SS** register
	2	P5.1	Above condition is not met
1	1	XTAL2	Option code select external 32.768kHz crystal as oscillator1
	2	P5.2	Option code select internal 32kHz RC as oscillator1
48	1	XTAL1	Option code select external 32.768kHz crystal as oscillator1
	2	P5.3	Option code select internal 32kHz RC as oscillator1
46	1	REM	Set **PWM1SS** bit and **REMSW** bit
	2	PWM1	Set **PWM1SS** bit and clear **REMSW** bit
	3	P5.4	Above condition is not met
44	1	$\overline{\text{RESET}}$	Option code **OP_RST** select P5.5 as reset pin
	2	P5.5	Option code **OP_RST** select P5.5 as I/O

8.6 Timer

8.6.1 Features

- The SH77P1651/SH77P1652 has two timers (Timer2, 3)
- Timer2 is compatible with the standard 8052 and has up or down counting and programmable clock output function
- Timer3 is a 16-bit auto-reload timer and can operate even in Power-Down mode

8.6.2 Timer2

The Timer 2 is implemented as a 16-bit register accessed as two cascaded data registers: TH2 and TL2. It is controlled by the register T2CON and T2MOD. The Timer2 interrupt can be enabled by setting the ET2 bit in the IEN0 register. (Refer to Interrupt Section for details)

C/$\overline{T2}$selects system clock (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows Timer 2/Counter 2 Data Register to increment by the selected input.

TCLKP2 bit in T2MOD register is used to select system clock or (system clock)/12 as the clock source of Timer2.

Timer2 Modes

Timer2 has 3 operating modes: Capture/Reload, Auto-reload mode with up or down counter and Programmable clock-output.

Table 8.16 Timer2 Mode select

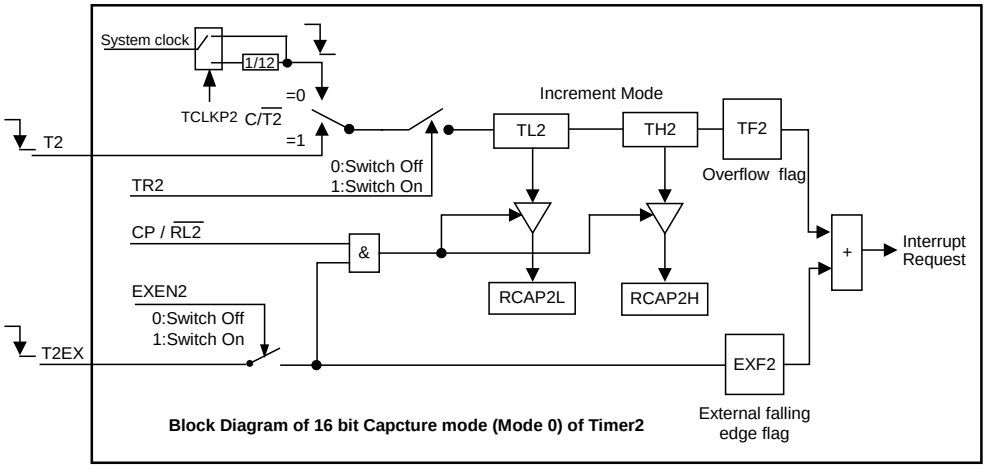
C/$\overline{T2}$	T2OE	DCEN	TR2	CP/RL2	Mode	
X	0	X	1	1	0	16 bit capture
X	0	0	1	0	1	16 bit auto-reload timer
X	0	1	1	0		
0	1	X	1	X	2	Programmable clock-output only
1	1	X	1	X		Not recommending
X	X	X	0	X	X	Timer2 stop, the T2EX path still enable

Mode0: 16 bit Capture

In the capture mode, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 is a 16-bit timer or counter which will set TF2 on overflow to generate an interrupt if ET2 is enabled.

If EXEN2 = 1, Timer2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L respectively, In addition, a 1-to-0 transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can also generate an interrupt if ET2 is enabled.



Block Diagram of 16 bit Capcture mode (Mode 0) of Timer2

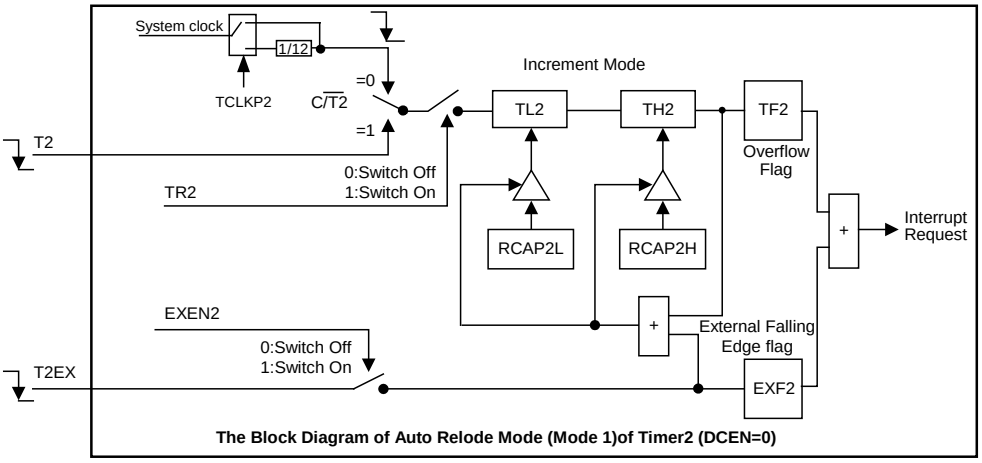
Mode1: 16 bit auto-reload Timer

Timer2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit in T2MOD. After reset, the DCEN bit is set to 0 so that Timer2 will default to count up. When DCEN is set, Timer2 can count up or down, depending on the value of the T2EX pin.

When DCEN = 0, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software.

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if ET2 is enabled.



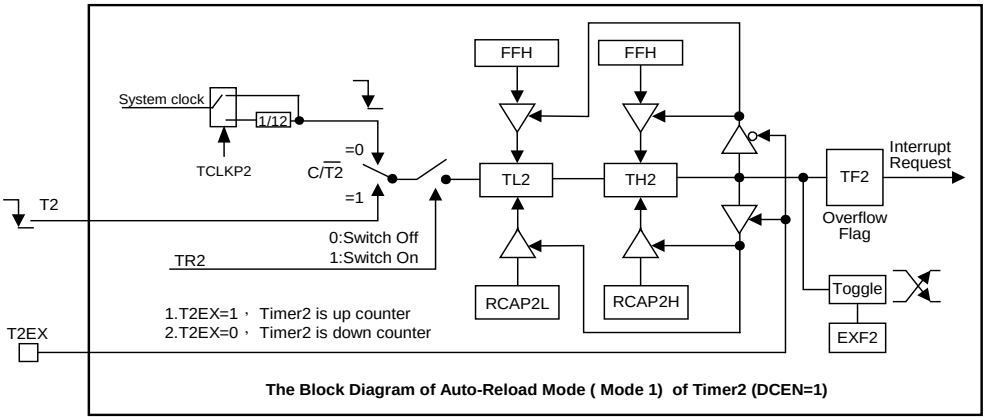
The Block Diagram of Auto Relode Mode (Mode 1)of Timer2 (DCEN=0)

Setting the DCEN bit enables Timer2 to count up or down. When DCEN = 1, the T2EX pin controls the direction of the count, and EXEN2's control is invalid.

A logical "1" at T2EX makes Timer2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logical "0" at T2EX makes Timer2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.



The Block Diagram of Auto-Reload Mode (Mode 1) of Timer2 (DCEN=1)

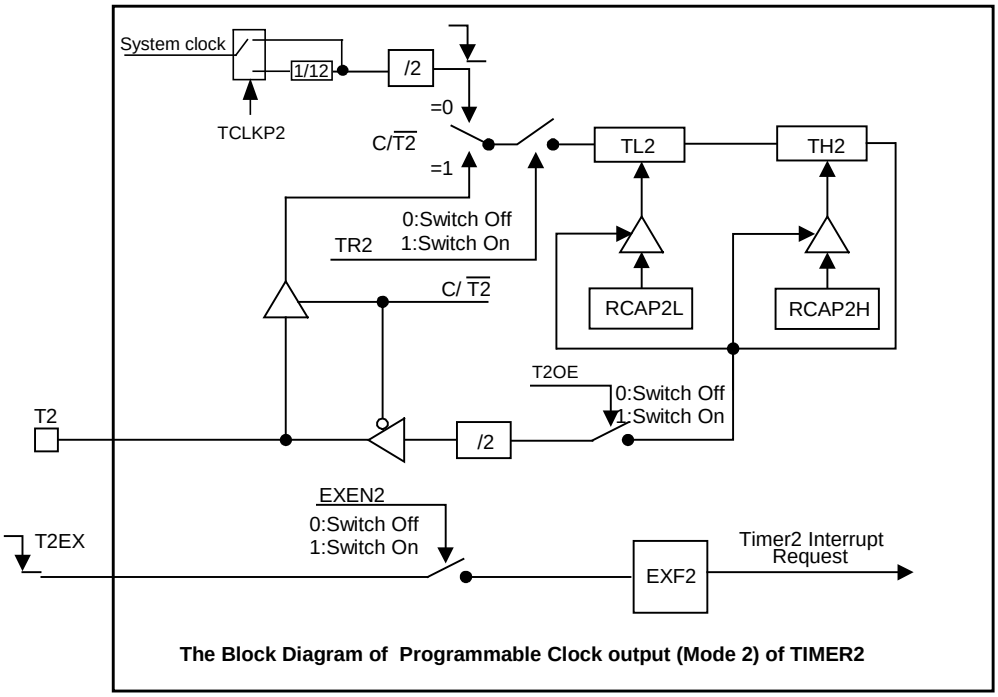
Mode2: Programmable Clock Output

A 50% duty cycle clock can be programmed to come out on T2 port. To configure the Timer2 as a clock generator, bit C/$\overline{T2}$ must be cleared and bit T2OE must be set. Bit TR2 starts and stops the timer.

In this mode T2 will output a 50% duty cycle clock:

$$\text{Clock Out Frequency} = \frac{1}{2 \times 2} \times \frac{f_{SYS}}{65536 - [\text{RCAP2H}, \text{RCAP2L}]}$$

Timer2 overflow will not generate an interrupt, so it is possible to use Timer2 as a baud-rate generator and a clock output simultaneously with the same frequency.



The Block Diagram of Programmable Clock output (Mode 2) of TIMER2

Note:

(1) Both TF2 and EXF2 can cause timer2 interrupt request, and they have the same vector address.

(2) TF2 and EXF2 are set as 1 by hardware while event occurs. But they can also be set by software at any time. Only the software will be able to clear TF2 & EXF2 to 0.

(3) When EA = 1 & ET2 = 1, setting TF2 or EXF2 as 1 will cause a timer2 interrupt.

Register

Table 8.17 Timer2 Control Register

C8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2	-	-	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Name	Description
7	**TF2**	**Timer2 overflow flag bit** 0: No overflow 1: Overflow (Set by hardware)
6	**EXF2**	**External event input (falling edge) from T2EX pin detected flag bit** 0: No external event input (Must be cleared by software) 1: Detected external event input (Set by hardware if EXEN2 = 1)
3	**EXEN2**	**External event input (falling edge) from T2EX pin used as Reload/Capture trigger enable/disable control bit** 0: Ignore events on T2EX pin 1: Cause a capture or reload when a negative edge on T2EX pin is detected
2	**TR2**	**Timer2 start/stop control bit** 0: Stop Timer2 1: Start Timer2
1	**C/$\overline{T2}$**	**Timer2 Timer/Counter mode selected bit** 0: Timer Mode, T2 pin is used as I/O port 1: Counter Mode, the internal pull-up resister is turned on
0	**CP/$\overline{RL2}$**	**Capture/Reload mode selected bit** 0: 16 bits timer/counter with reload function 1: 16 bits timer/counter with capture function

Table 8.18 Timer2 Mode Control Register

C9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	TCLKP2	-	-	-	-	-	T2OE	DCEN
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
7	**TCLKP2**	**Divide Select Control bit** 0: Select (system clock)/12 as the clock source of Timer2 1: Select system clock as the clock source of Timer2
1	**T2OE**	**Timer2 Output Enable bit** 0: Set P2.4/T2 as clock input or I/O port 1: Set P2.4/T2 as clock output (Baud-Rate generator mode)
0	**DCEN**	**Down Counter Enable bit** 0: Disable Timer2 as up/down counter, Timer2 is an up counter 1: Enable Timer2 as up/down counter

Table 8.19 Timer2 Reload/Capture & Data Registers

CAH-CDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCAP2L	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**RCAP2L[7:0]**	**Timer2 Reload/Capturer Data**
	RCAP2H[7:0]	
7-0	**TL2[7:0]**	**Timer2 High & Low byte counter**
	TH2[7:0]	

8.6.3 Timer3

Timer3 is a 16-bit auto-reload timer. It is implemented as a 16-bit register accessed as two cascaded Data Registers: TH3 and TL3. It is controlled by the T3CON register. The Timer3 interrupt can be enabled by setting ET3 bit in IEN1 register (Refer to **Interrupt** Section for details).

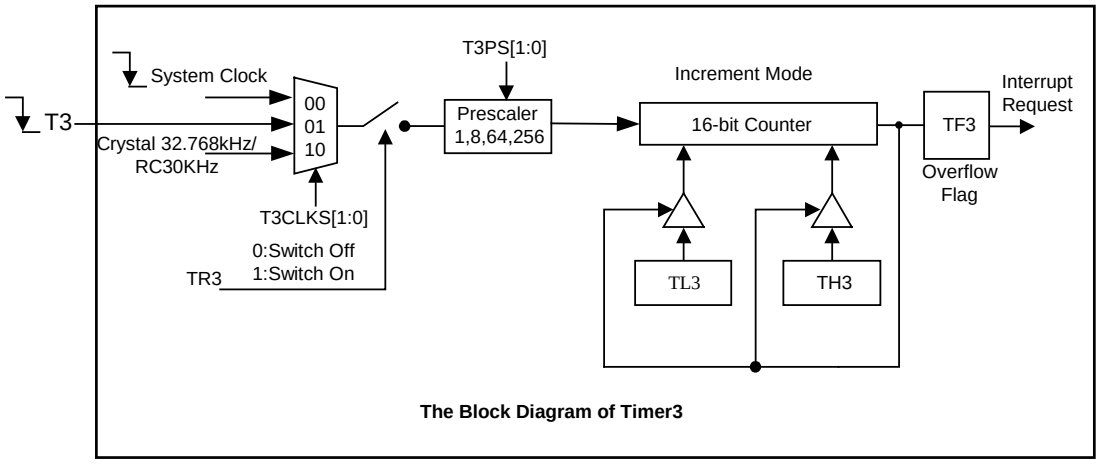
Timer3 has only one operating mode: 16-bit Counter/Timer with auto-reload. Timer3 also supports the following features: selectable pre-scaler setting and Operation during CPU Power-Down mode.

Timer3 consists of a 16-bit counter/reload register (TH3, TL3). When writing to TH3 and TL3, they are used as timer load register. When reading from TH3 and TL3, they are used as timer counter register. Setting the TR3 bit enables Timer 3 to count up. The Timer will overflow from 0xFFFF to 0x0000 and set the TF3 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH3 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH3 and TL3 should follow these steps:

Write operation: Low nibble first, High nibble to update the counter

Read operation: High nibble first, Low nibble followed.



The Block Diagram of Timer3

When T3CLKS [1:0] is 00, Timer3 can't work in Power Down mode.

When T3CLKS [1:0] is 01, Timer3 can work in Power Down mode. Even if all the oscillators are all turned off, Timer3 still can count the pulse on T3.

When T3CLKS [1:0] is10, Timer3 can work in Power Down mode. If LOSCCLK are all turned off in Power Down mode, Timer3 can't work.

It can be described in the following table:

T3CLKS[1:0]	Osillator status	Can work in normal mode	Can work in Power Down mode
00	Any	Work	Don't work
01	Any	Work	Don't work
10	Turn on LOSCCLK and turn off LOSCCLK in Power Down mode	Work	Don't work
	Turn on LOSCCLK and still turn on LOSCCLK in Power Down mode	Work	Don't work

Note:

(1) When TH3 and TL3 read or written, must make sure TR3 = 0.

(2) When T3 is selected as Timer3 clock source and after TR3 is set 0 to 1, T3 falling will be ignored during 1.5 system clock period

Register

Table 8.20 Timer3 Control Register

CEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T3CON	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
R/W	R/W	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	-	0	0	0

Bit Number	Bit Name	Description
7	**TF3**	**Timer3 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T3PS[1:0]**	**Timer3 input clock Prescaler Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
2	**TR3**	**Timer3 start/stop control bit** 0: Stop Timer3 1: Start Timer3
1-0	**T3CLKS[1:0]**	**Timer3 Clock Source select bits** 00: System clock, T3 pin is used as I/O port 01: External clock from pin T3, auto pull-up 10: 32.768kHz from external Crystal or 32kHz RC(Refer to code option section) 11: reserved

Table 8.21 Timer3 Reload/Counter Data Registers

F2H-F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL3	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**TL3.x**	Timer3 Low & High byte counter, x = 0 - 7
	TH3.x	

8.7 Interrupt

8.7.1 Features

- 8 interrupt sources
- 4 interrupt priority levels

The SH77P1651/SH77P1652 provides total 8 interrupt sources: 1 external interrupts INT4 including INT40-47, which share the same vector address, 2 timer interrupts (Timer2, 3), one EUART interrupt, PWM interrupts, REM Interrupt, ADC interrupt(No ADC in SH77P1651) and SCM interrupt.

8.7.2 Interrupt Enable

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

8.7.3 Register

Table 8.22 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC*	ET2	ES	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	-	-

Bit Number	Bit Name	Description
7	**EA**	**All interrupt enable bit** 0: Disable all interrupt 1: Enable all interrupt
6	**EADC***	**ADC interrupt enable bit** 0: Disable ADC interrupt 1: Enable ADC interrupt
5	**ET2**	**Timer2 overflow interrupt enable bit** 0: Disable Timer2 overflow interrupt 1: Enable Timer2 overflow interrupt
4	**ES**	**EUART interrupt enable bit** 0: Disable EUART interrupt 1: Enable EUART interrupt

Note: *signed by * not available in SH77P1651.*

Table 8.23 Secondary Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	ESCM	EPWM1	-	ET3	EX4	-	EREM	-
R/W	R/W	R/W	-	R/W	R/W	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	0	-	0	0	-	0	-

Bit Number	Bit Name	Description
7	**ESCM**	**SCM interrupt enable bit** 0: Disable SCM interrupt 1: Enable SCM interrupt
6	**EPWM1**	**PWM1 interrupt enable bit** 0: Disable PWM1 interrupt 1: Enable PWM1 interrupt
4	**ET3**	**Timer3 overflow interrupt enable bit** 0: Disable Timer3 overflow interrupt 1: Enable Timer3 overflow interrupt
3	**EX4**	**External interrupt enable bit** 0: Disable external interrupt4 1: Enable external interrupt4
1	**EREM**	**REM interrupt enable bit** 0: Disable REM interrupt 1: Enable REM interrupt

Note: *To enable External interrupt4, the corresponding port must be set to input mode before using it.*

Table 8.24 Interrupt channel4 Enable Register

BAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IENC	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**EXS4x (x = 7-0)**	**External interrupt4 channel select bit (x = 7-0)** 0: Disable external interrupt 4x 1: Enable external interrupt 4x

8.7.4 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in Table bellow.

When an **external interrupt4** is generated, the flag (IF4x (x = 0-7) in EXF1 register) that generated this interrupt should be cleared by user's program because the same vector entrance was used in INT4. But if INT4 is setup as level trigged, the flag can't be cleared by user's program, it only be controlled by peripheral signal level that connect to INT source pin.

The **timer 2 interrupt** is generated by the logical OR of flag TF2 and bit EXF2 in T2CON register, which is set by hardware. None of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, so the flag must be cleared by software.

The **timer 3 interrupt** is generated when they overflow, the flag TF3 in T3CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **EUART interrupt** is generated by the logical OR of flag RI and TI in SCON register, which is set by hardware. Neither of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the receive interrupt flag or the transmission interrupt flag that generated the interrupt, so the flag must be cleared by software.

The **ADC interrupt** is generated by ADCIF bit in ADCON. If an interrupt is generated, the converted result in ADCDH/ADCDL will be valid. If continuous compare function in ADC module is Enable, ADCIF will not be set at each conversion, but set if converted result is larger than compare value. The flag must be cleared by software.

The **SCM interrupt** is generated by SCMIF in SCM register, which is set by hardware. And the flag can only be cleared by hardware.

The **PWM interrupt** is generated by PWM1IF in PWMCON. And the flag can only be cleared by hardware.

The **REM interrupt** is generated by REMIF in REMCON. And the flag can only be cleared by hardware.

Table 8.25 External Interrupt Flag Register

E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF0	IT4.1	IT4.0	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	-	-	-	-

Bit Number	Bit Name	Description
7-6	**IT4[1:0]**	**External interrupt4 trigger mode selection bit** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge IT4 [1:0] is effect on external interrupt 4x at the same mode

Table 8.26 External Interrupt4 Flag Register1

D8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF1	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**IF4x (x = 7-0)**	**External interrupt4 request flag bit** 0: No interrupt pending 1: Interrupt is pending IF4x is cleared by software

8.7.5 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in **Interrupt Summary table**.

8.7.6 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. But the OVL NMI interrupt has the highest Priority Level (except RESET) of all the interrupt sources, with no IPH/IPL control. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction cycle, an internal polling sequence determines which request is serviced.

Interrupt Priority		
Priority bits		**Interrupt Lever Priority**
IPHx	IPLx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 8.27 Interrupt Priority Control Registers

B8H, B4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL0	-	PADCL*	PT2L	PSL	-	-	-	-
IPH0	-	PADCH*	PT2H	PSH	-	-	-	-
R/W	-	R/W	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	-	-	-	-
B9H, B5H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL1	PSCML	PPWML	-	PT3L	PX4L	-	PREML	-
IPH1	PSCMH	PPWMH	-	PT3H	PX4H	-	PREMH	-
R/W	R/W	R/W	-	R/W	R/W	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	0	-	0	0	-	0	-

Bit Number	Bit Name	Description
7-0	**PxxxL/H**	Corresponding interrupt source xxx's priority level selection bits

Note: *signed by * not available in SH77P1651.*

8.7.7 Interrupt Handling

The interrupt flags are sampled and polled at the fetch cycle of each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current cycle is not in the final cycle of the instruction in progress. This ensures that the instruction in progress is completed before vectoring to any service routine.

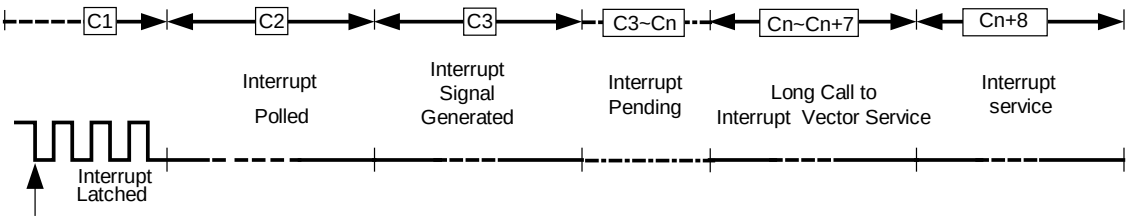
The instruction in progress is RETI. This ensures that if the instruction in progress is RETI then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Note:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.

The polling cycle/LCALL sequence is illustrated below:



Interrupt Response Timing

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with corresponding address that depends on the source of the interrupt being vectored too, as shown in Interrupt Summary table.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt service. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt with this priority was still in progress. In this case, no interrupt of the same or lower priority level would be acknowledged.

8.7.8 Interrupt Response Time

If an interrupt is recognized, its request flag is set in every machine cycle after recognize. The value will be polled by the circuitry until the next machine cycle; the CPU will generate an interrupt at the third machine cycle. If the request is active and conditions are right for it to be acknowledged, hardware LCALL to the requested service routine will be the next instruction to be executed. Else the interrupt will pending. The call itself takes 7 machine cycles. Thus a minimum of 3+7 complete machine cycles will elapse between activation and external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine.

If the instruction in progress is not in its final cycle and the instruction in progress is RETI, the additional wait time is 8 machine cycles. For a single interrupt system, if the next instruction is 20 machine cycles long (the longest instructions DIV & MUL are 20 machine cycles long for 16 bit operation), adding the LCALL instruction 7 machine cycles the total response time is 2+8+20+7 machine cycles.

Thus interrupt response time is always more than 10 machine cycles and less than 37 machine cycles.

8.7.9 External Interrupt Inputs

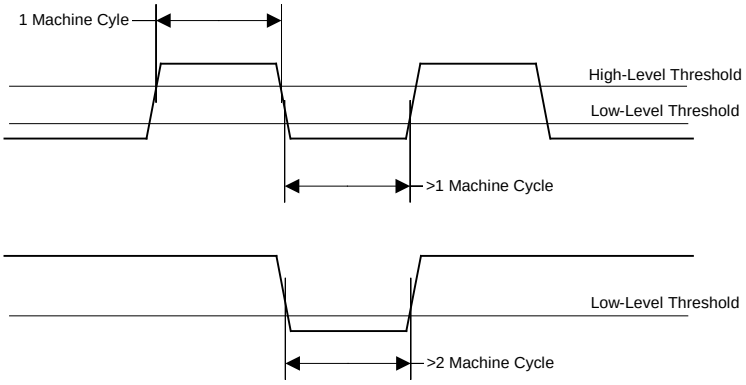
The SH77P1651/SH77P1652 has 1 external interrupt vector address. External interrupt 4 has 8 inputs; all of them share one vector address. These external interrupts can be programmed to be level-triggered or edge-triggered by clearing or setting IT4.0 bit or IT4.1bit in EXF0. If IT4[1:0] = 0, external interrupt 4 is triggered by a low level detected at the INT4 pin. If IT4[1:0] = 1, external interrupt 4 is edge triggered. In this mode if consecutive samples of the INT4 pin show a high level in one cycle and a low level in the next cycle, interrupt request flag in register r EXF1 is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

If the external interrupt is edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag IF40-IF47 is set. Notice that IF40-IF47 is automatically cleared by CPU when the service routine is called.

If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag IE0 when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the SH77P1651/SH77P1652 is put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation.

***Note**: IF40-43 should be cleared by software.*



Detect External Interrupt

8.7.10 Interrupt Summary

Source	Vector Address	Enable bits	Flag bits	Polling Priority	Interrupt number (c language)
$\overline{\text{RESET}}$	0000H	-	-	0 (higest)	-
EUART	0023H	ES	RI+TI	1	4
Timer2	002BH	ET2	TF2+EXF2	2	5
ADC*	0033H	EADC	ADCIF	3	6
REM	0043H	EREM	REMIF	4	8
INT4	0053H	EX4+IENC	IF47-40	5	10
Timer3	005BH	ET3	TF3	6	11
PWM1	006BH	EPWM1	PWM1IF	7	13
SCM	0073H	ESCM	SCMIF	8 (Lowest)	14

***Note:** Signed by * not available in SH77P1651.*

9. Enhanced Function

9.1 LCD Driver

9.1.1 Feature

- LCD driver support: 4 X 30 dots or 5 X 29 dots
- Support resistor and capacitor bias voltage generating circuit
- Resistor LCD driver support software contrast adjustment and fast charge mode to reduce power consumption
- Capacitor LCD driver contain capacitor bias voltage and buit-in voltage regulator

SH77P1651/SH77P1652 provides two different ways of LCD driver: resistor LCD driver and capacitor LCD driver, which is selected by OP_LCDSEL (Refer to **code option** section for details). The capacitor LCD driver also contain capacitor bias voltage and built-in voltage regulator, which is selected thr ough TYPESEL bit in LCDCON register, in addition, only when the LCDON bit is set , the LCD function will be effective.

The LCD driver has two driving modes: 1/4duty - 1/3 bias or 1/5 duty - 1/3 bias, Driving mode is selected by DUTY bit in LCDCON register

When MCU enter idle or Power-Down mode in HRCCLK, LCD still work, RAM still hold data, otherwise LCD dirve will be turned off.

LCD dirver will be turned off in POR/PIN/LVR/WDT.

When LCD turn to close (OFF), Common and segment output low level.

When 32kHz RC or 32.768kHz is as the LCD clock source, LCD frame is fixed to 64Hz.

9.1.2 Resistor LCD Driver Mode

The resistor LCD driver contains a controller, a duty cycle generator, 4/5 Common signal pins and 30/29 Segment driver pins. Segment 1-30 and COM1-COM5 can also be used as I/O port, which is controlled by the P1SS, P2SS, P3SS, P4SS & P5SS register. The 30 bytes display data RAM is addressed to 100H-11DH, which can be used as data memory if needed.

LCD bias resistor (R_{LCD}) can be configured to 60K, 450k or 990k by MOD[1:0] bits in the LCDCON register. 60K bias resistor can get better effect, but the current will be relatively large, not suitable for low power consumption application. when the MOD[1:0] bits in LCDON register is set to 990K bias resistor, the LCD display will become worse, although it can achieve lower power consumption.

Therefore, SH77P1651 provides both the low power consumption and display effect of the display mode: fast charge mode.

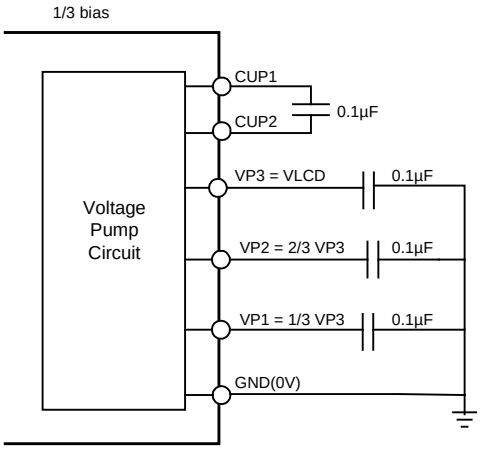
Set MOD[1:0] = 10-1x to select this mode. When refresh the display data 60k bias resistors are selected to provide larger current. When keep the display data 450/990K bias resistors are selected to save drive current.

Charging time is selected as 1/4,1/8,1/16 or 1/32 of LCD com period by FCCTL[1:0] in LCDCON1 register.

9.1.3 Capacitor LCD Driver Mode

Capacitor bias voltage LCD Driver

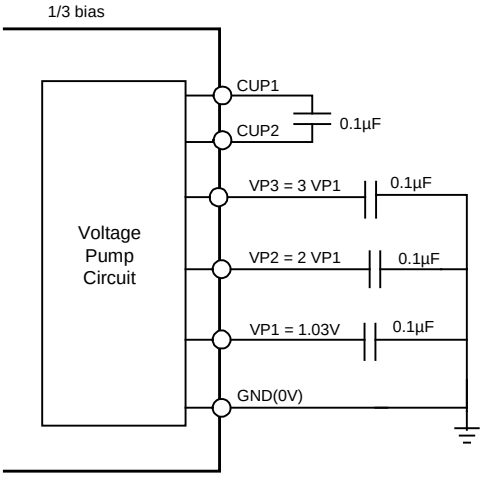
The LCD drive voltage (V_{LCD}) of Capacitor bias voltage mode is V_{DD}.



The capacitor bias voltage LCD driver contains a controller, a duty cycle generator, 4/5 Common signal pins and 30/29 Segment driver pins. Segment 1-30 and COM1-COM5 can also be shared as I/O port, it is controlled by the P1SS, P2SS, P3SS, P4SS & P5SS register. The 30 bytes display data RAM is addressed to 100H-11DH, which could be used as data memory if needed.

Built-in voltage regulator LCD Driver

Buit-in voltage regulator, It's V_{DD} is between 1.8V and 3.6V, It can generate a stable voltage.

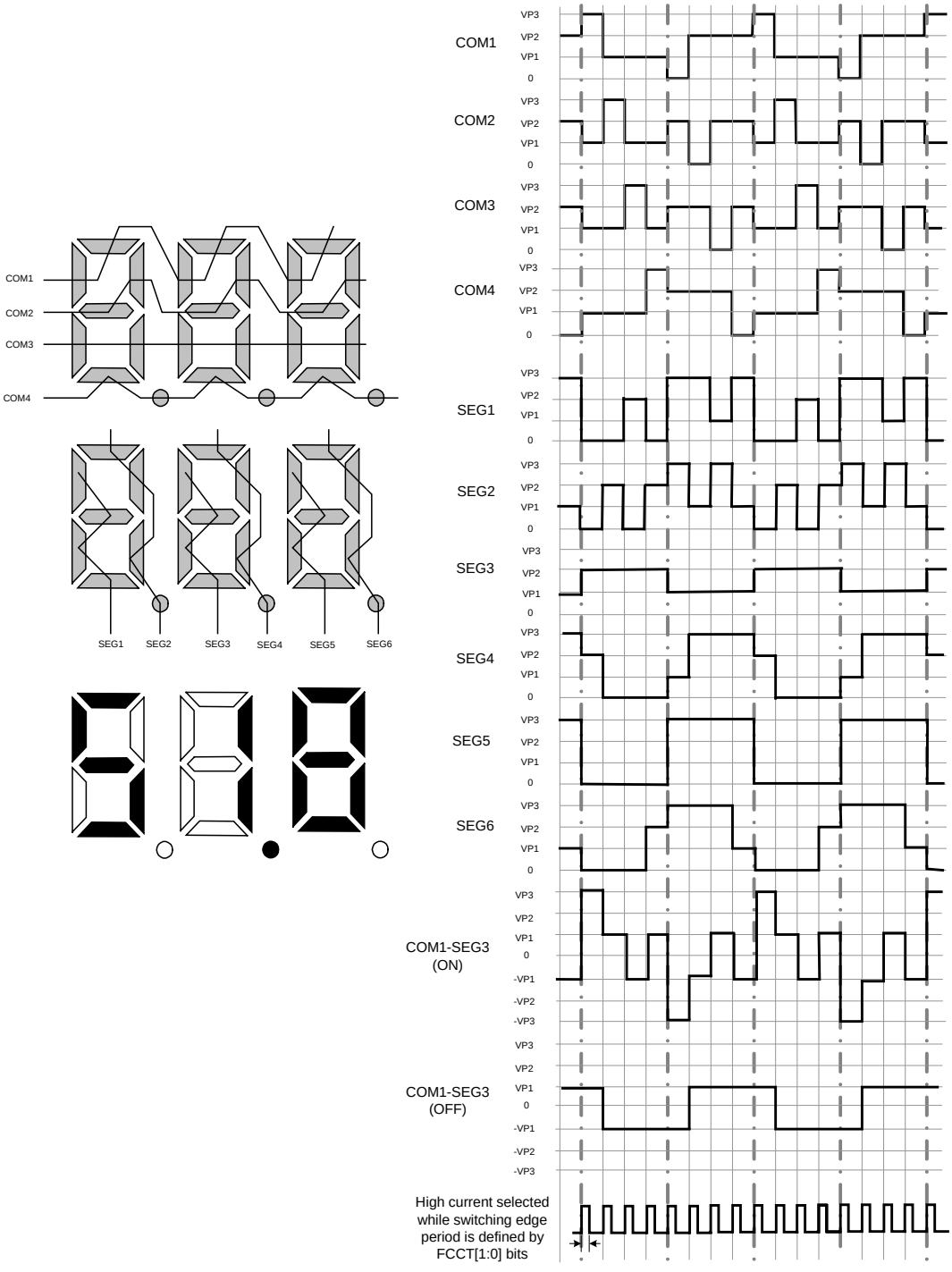


The capacitor LCD driver contains a controller, a duty cycle generator, 4/5 Common signal pins and 30/29 Segment driver pins. Segment 1-30 and COM1-COM5 can also be used as I/O port, it is controlled by the P1SS, P2SS, P3SS, P4SS & P5SS register. The 30 bytes display data RAM is addressed to 100H-11DH, which could be used as data memory if needed.

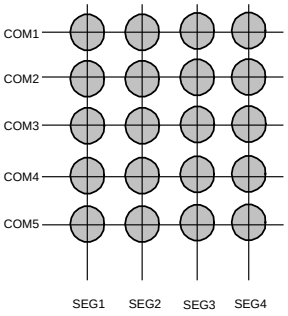
Note:

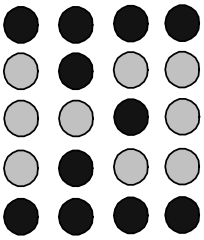
For more efficient use of the capacitor LCD dirver, user must firstly set all control bit except PUMPON bit and LCDON bit, then set PUMPON bit, after delay of at least 25 ms, open LCD is that LCDON bit is set, light LCD panel.

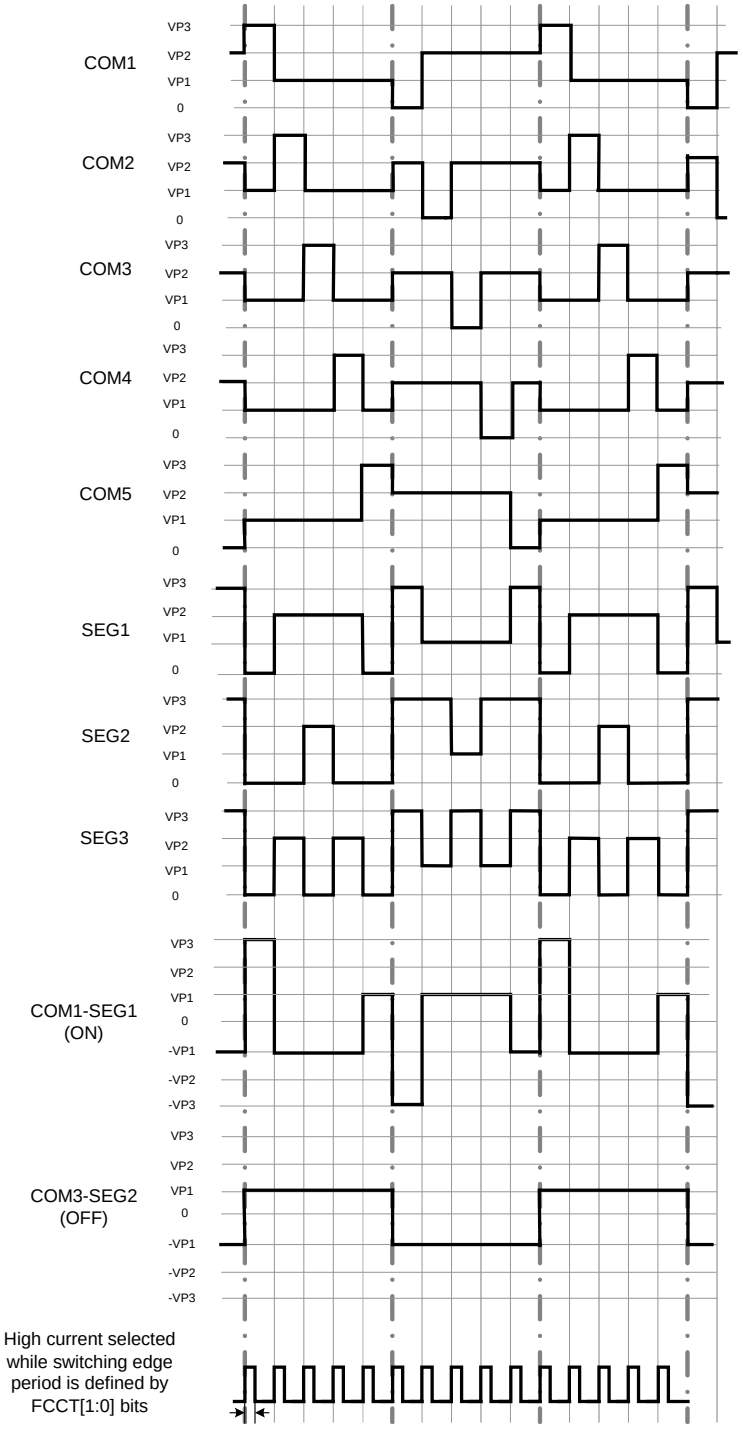
9.1.4 LCD Waveform



LCD diplay 51.8 (1/4 duty, 1/3 bias)







LCD diplay ∑ (1/5 duty, 1/3 bias)

9.1.5 Register

Table 9.1 LCD Control Register

ABH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON	LCDON	PUMPON	-	DUTY	TYPESEL	VOL2	VOL1	VOL0
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	0	0	0	0	0

Bit Number	Bit Name	Description
7	**LCDON**	**LCD enable bit** 0: Disable LCD driver 1: Enable LCD driver
6	**PUMPON**	**PUMP on/off enable bit** 0: Disable LCD PUMP 1: Enable LCD PUMP ***Note:*** *capacitor bias and voltage regulator work when PUMPON = 1*
4	**DUTY**	**LCD duty selection bit** 0: 1/4 duty, 1/3 bias, P4.5 as segment or I/O 1: 1/5 duty, 1/3 bias, P4.5 as common
3	**TYPESEL**	**LCD capacitor drive mode selection bit** 0: capacitor bias voltage LCD drive mode 1: buit-in voltage regulator LCD drive mode
2-0	**VOL[2:0]**	**LCD contrast control bits** 000: V_{LCD} = 0.650 V_{DD} 001: V_{LCD} = 0.700 V_{DD} 010: V_{LCD} = 0.750 V_{DD} 011: V_{LCD} = 0.800 V_{DD} 100: V_{LCD} = 0.850 V_{DD} 101: V_{LCD} = 0.900 V_{DD} 110: V_{LCD} = 0.950 V_{DD} 111: V_{LCD} = 1.000 V_{DD} ***Note:*** *When capacitor LCD drive mode is selected, this three bits are invalid*

Table 9.2 LCD Control Register 1

AAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON1	-	-	FCCTL1	FCCTL0	-	RLCD	MOD1	MOD0
R/W	-	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	0	0	-	0	0	0

Bit Number	Bit Name	Description
5-4	**FCCTL[1:0]**	**Fast charge time control bit** 00: 1/4 LCD com period 01: 1/8 LCD com period 10: 1/16 LCD com period 11: 1/32 LCD com period
2	**RLCD**	**LCD bias resistor control bit** 0: LCD bias resistor sum is 450K 1: LCD bias resistor sum is 990K
1-0	**MOD[1:0]**	**LCD Drive mode control bit** 00: traditional mode, bias resistor sum is 450K/990K 01: traditional mode, bias resistor sum is 60K 1x: fast charge mode, bias resistor sum switch between 60K and 450K/990K

Note: *When the capacitor LCD drive mode is selected, all bits in this register will be invalid.*

Table 9.3 P1 Mode Select Register

ADH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1SS	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P1S[7:0]**	**P1 mode select** 0: P1.7-P1.0 is I/O 1: P1.7-P1.0 is Segment (SEG8 - SEG1)

Table 9.4 P2 Mode Select Register

BBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2SS	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P2S[7:0]**	**P2 mode select** 0: P2.7-P2.0 is I/O 1: P2.7-P2.0 is Segment (SEG16 - SEG9)

Table 9.5 P3 Mode Select Register

BCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P3SS	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P3S[7:0]**	**P3 mode select** 0: P3.7-P3.0 is I/O 1: P3.7-P3.0 is Segment (SEG24 - SEG17)

Table 9.6 P4 Mode Select Register

BDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P4SS	P4S7	P4S6	P4S5	P4S4	P4S3	P4S2	P4S1	P4S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P4S[7:0]**	**P4 mode select** 0: P4.7-P4.0 is I/O 1: P4.7-P4.6 is Common (COM3 - COM4), P4.5-P4.0 is Segment (SEG30 - SEG25)

Note: *COM5 is selected through the DUTY bit in LCD Control Register.*

Table 9.7 P5 Mode Select Register

BEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5SS	-	-	-	-	-	-	P5S1	P5S0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
1-0	**P5S[1:0]**	**P5.x mode select (x = 1, 0)** 0: P5.1-P5.0 is I/O 1: P5.1-P5.0 is Common (COM1 - COM2)

9.1.6 Configuration of LCD RAM

LCD 1/4 duty, 1/3 bias (COM1 - 4, SEG1 - 30)

Address	7	6	5	4	3	2	1	0
	-	-	-	-	COM4	COM3	COM2	COM1
100H	-	-	-	-	SEG1	SEG1	SEG1	SEG1
101H	-	-	-	-	SEG2	SEG2	SEG2	SEG2
102H	-	-	-	-	SEG3	SEG3	SEG3	SEG3
103H	-	-	-	-	SEG4	SEG4	SEG4	SEG4
104H	-	-	-	-	SEG5	SEG5	SEG5	SEG5
105H	-	-	-	-	SEG6	SEG6	SEG6	SEG6
106H	-	-	-	-	SEG7	SEG7	SEG7	SEG7
107H	-	-	-	-	SEG8	SEG8	SEG8	SEG8
108H	-	-	-	-	SEG9	SEG9	SEG9	SEG9
109H	-	-	-	-	SEG10	SEG10	SEG10	SEG10
10AH	-	-	-	-	SEG11	SEG11	SEG11	SEG11
10BH	-	-	-	-	SEG12	SEG12	SEG12	SEG12
10CH	-	-	-	-	SEG13	SEG13	SEG13	SEG13
10DH	-	-	-	-	SEG14	SEG14	SEG14	SEG14
10EH	-	-	-	-	SEG15	SEG15	SEG15	SEG15
10FH	-	-	-	-	SEG16	SEG16	SEG16	SEG16
110H	-	-	-	-	SEG17	SEG17	SEG17	SEG17
111H	-	-	-	-	SEG18	SEG18	SEG18	SEG18
112H	-	-	-	-	SEG19	SEG19	SEG19	SEG19
113H	-	-	-	-	SEG20	SEG20	SEG20	SEG20
114H	-	-	-	-	SEG21	SEG21	SEG21	SEG21
115H	-	-	-	-	SEG22	SEG22	SEG22	SEG22
116H	-	-	-	-	SEG23	SEG23	SEG23	SEG23
117H	-	-	-	-	SEG24	SEG24	SEG24	SEG24
118H	-	-	-	-	SEG25	SEG25	SEG25	SEG25
119H	-	-	-	-	SEG26	SEG26	SEG26	SEG26
11AH	-	-	-	-	SEG27	SEG27	SEG27	SEG27
11BH	-	-	-	-	SEG28	SEG28	SEG28	SEG28
11CH	-	-	-	-	SEG29	SEG29	SEG29	SEG29
11DH	-	-	-	-	SEG30	SEG30	SEG30	SEG30

LCD 1/5 duty, 1/3 bias (COM1 - 5, SEG1 - 29)

Address				4	3	2	1	0
				COM5	COM4	COM3	COM2	COM1
100H	-	-	-	SEG1	SEG1	SEG1	SEG1	SEG1
101H	-	-	-	SEG2	SEG2	SEG2	SEG2	SEG2
102H	-	-	-	SEG3	SEG3	SEG3	SEG3	SEG3
103H	-	-	-	SEG4	SEG4	SEG4	SEG4	SEG4
104H	-	-	-	SEG5	SEG5	SEG5	SEG5	SEG5
105H	-	-	-	SEG6	SEG6	SEG6	SEG6	SEG6
106H	-	-	-	SEG7	SEG7	SEG7	SEG7	SEG7
107H	-	-	-	SEG8	SEG8	SEG8	SEG8	SEG8
108H	-	-	-	SEG9	SEG9	SEG9	SEG9	SEG9
109H	-	-	-	SEG10	SEG10	SEG10	SEG10	SEG10
10AH	-	-	-	SEG11	SEG11	SEG11	SEG11	SEG11
10BH	-	-	-	SEG12	SEG12	SEG12	SEG12	SEG12
10CH	-	-	-	SEG13	SEG13	SEG13	SEG13	SEG13
10DH	-	-	-	SEG14	SEG14	SEG14	SEG14	SEG14
10EH	-	-	-	SEG15	SEG15	SEG15	SEG15	SEG15
10FH	-	-	-	SEG16	SEG16	SEG16	SEG16	SEG16
110H	-	-	-	SEG17	SEG17	SEG17	SEG17	SEG17
111H	-	-	-	SEG18	SEG18	SEG18	SEG18	SEG18
112H	-	-	-	SEG19	SEG19	SEG19	SEG19	SEG19
113H	-	-	-	SEG20	SEG20	SEG20	SEG20	SEG20
114H	-	-	-	SEG21	SEG21	SEG21	SEG21	SEG21
115H	-	-	-	SEG22	SEG22	SEG22	SEG22	SEG22
116H	-	-	-	SEG23	SEG23	SEG23	SEG23	SEG23
117H	-	-	-	SEG24	SEG24	SEG24	SEG24	SEG24
118H	-	-	-	SEG25	SEG25	SEG25	SEG25	SEG25
119H	-	-	-	SEG26	SEG26	SEG26	SEG26	SEG26
11AH	-	-	-	SEG27	SEG27	SEG27	SEG27	SEG27
11BH	-	-	-	SEG28	SEG28	SEG28	SEG28	SEG28
11CH	-	-	-	SEG29	SEG29	SEG29	SEG29	SEG29

9.2 Analog Digital Converter (ADC) (no ADC in SH77P1651)

9.2.1 Feature

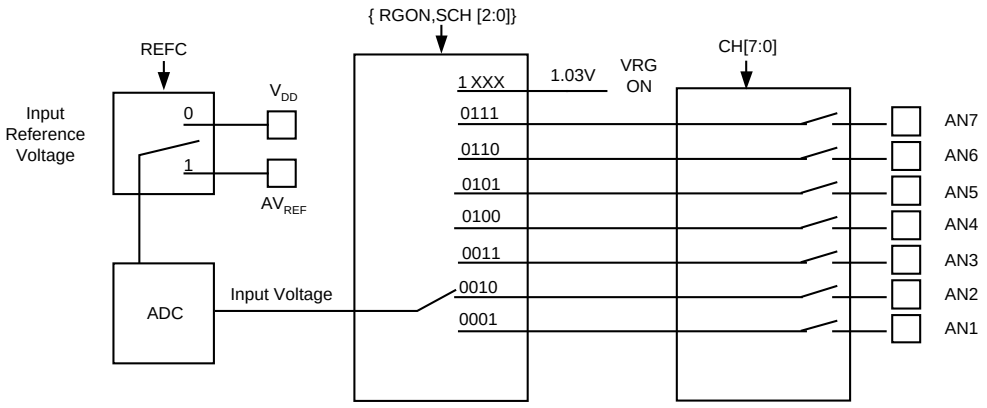
- 10-bit Resolution
- Selectable external or built-in V_{REF}
- 7 Multiplexed Input Channels, and one channel connected to the internal reference voltage (1.03V) to detect battery voltage

The SH77P1652 include a single ended, 10-bit SAR Analog to Digital Converter (ADC) with build in reference voltage connected to the V_{DD}, users also can select the V_{REF} pin input reference voltage. The 7 ADC channels are shared with 1 ADC module; each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. There is one channel connected to the internal refence voltage through RGON bit. GO/$\overline{\text{DONE}}$ signal is available to start convert, and indicate end of convert. When the conversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCON register will be set. If ADC Interrupt is enabled, the ADC interrupt will generate.

The ADC integrates a digital compare function to compare the value of analog input with the digital value in the AD converter. If this function is enabled (set EC bit in ADCON register) and ADC module is enabled (set ADON bit in ADCON register). When the corresponding digital value of analog input is larger than the value in compare value register (ADDH/L), the ADC interrupt will occur, otherwise no interrupt will be generated. The digital comparator can work continuously when GO/$\overline{\text{DONE}}$ bit is set until software clear, which behaviors different with the AD converter operation mode.

The ADC module including digital compare module can wok in Idle mode which can be waken up by the ADC interrupt. In Power-Down mode and the ADC interrupt will wake up the Idle mode, ADC module is disabled.

9.2.2 ADC Diagram



ADC Diagram

9.2.3 ADC Register

Table 9.8 ADC Control Register

93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	$\overline{\text{GO/DONE}}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**ADON**	**ADC Enable bit** 0: Disable the ADC module 1: Enable the ADC module
6	**ADCIF**	**ADC Interrupt Flag bit** 0: No ADC interrupt, cleared by software. 1: Set by hardware to indicate that the AD Convert has been completed, or analog input is larger than ADDH/ADDL if compare is enabled
5	**EC**	**Compare Function Enable bit** 0: Compare function disabled 1: Compare function enabled
4	**REFC**	**Reference Voltage Select bit** 0: the reference voltage connected to V_{DD} 1: the reference voltage input from V_{REF} pin
3-1	**SCH[2:0]**	**ADC Channel Select bits** 000: no channel selected 001: ADC channel AN1 010: ADC channel AN2 011: ADC channel AN3 100: ADC channel AN4 101: ADC channel AN5 110: ADC channel AN6 111: ADC channel AN7 ***Notes:*** *In use of AN1-AN7, the RGON bit in ADCON1 register must be cleared.*
0	**$\overline{\text{GO/DONE}}$**	**ADC status flag bit** 0: Automatically cleared by hardware when AD conversion is completed. Clearing this bit during converting time will stop current conversion. If Compare function is enabled, this bit will not be cleared by hardware until software clear. 1: Set to start AD convert or digital compare.

Notes:

When select the reference voltage input from V_{REF} pin (REFC = 1), the P3.7 is shared as V_{REF} input rather than AN3 input.

Table 9.9 ADC Control Register 1

8FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	RGON	-	-	-	-	-	-	-
R/W	R/W	-	-	-	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	-	-

Bit Number	Bit Name	Description
7	**RGON**	**RGON Enable bit** 0: not select 1.03V,the ADC external channel (AN1-AN7) can be selected. 1: select 1.03V, the ADC external channel (AN1-AN7) can not be selected.

Note: *When enable RGON bit, the ADC can be used as voltage detector.*

Table 9.10 ADC Timer Control Register

94H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	TADC2	TADC1	TADC0	-	TS3	TS2	TS1	TS0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Name	Description
7-5	**TADC[2:0]**	**ADC Clock Period Select bits** 000: ADC Clock Period t_{AD} = 2 t_{SYS} 001: ADC Clock Period t_{AD} = 4 t_{SYS} 010: ADC Clock Period t_{AD} = 6 t_{SYS} 011: ADC Clock Period t_{AD} = 8 t_{SYS} 100: ADC Clock Period t_{AD} = 12 t_{SYS} 101: ADC Clock Period t_{AD} = 16 t_{SYS} 110: ADC Clock Period t_{AD} = 24 t_{SYS} 111: ADC Clock Period t_{AD} = 32 t_{SYS}
3-0	**TS[3:0]**	**Sample time select bits** 2 t_{AD} ≤ Sample time = (TS [3:0]+1) * t_{AD} ≤ 15 t_{AD}

Note:

(1) Make sure that t_{AD} ≧ 1μs;
(2) The minimum sample time is 2 t_{AD}, even TS[3:0] = 0000; The maximum sample time is 15 t_{AD} , even TS[3:0] = 1111;
(3) Evaluate the series resistance connected with ADC input pin before set TS[3:0];
(4) Be sure that the series resistance connected with ADC input pin is no more than 10kΩ when 2 t_{AD} sample time is selected;
(5) Total conversion time is: 12 t_{AD} + sample time.

For Example

System Clock (SYSCLK)	TADC[2:0]	t_{AD}	TS[3:0]	Sample Time	Conversion Time
32.768kHz	000	30.5*2=61μs	0000	2*61=122μs	12*61+122=854μs
	000	30.5*2=61μs	0111	8*61=488μs	12*61+488=1220μs
	000	30.5*2=61μs	1111	15*61=915μs	12*61+915=1647μs
	111	30.5*32=976μs	0000	2*976=1952μs	12*976+1952=13664μs
	111	30.5*32=976μs	0111	8*976=7808μs	12*976+7808=19520μs
	111	30.5*32=976μs	1111	15*976=14640μs	12*976+14640=26352μs
4MHz	000	0.25*2=0.5μs	-	-	(t_{AD} < 1μs, not recommended)
	001	0.25*4=1μs	0000	2*1=2μs	12*1+2=14μs
	001	0.25*4=1μs	0111	8*1=8μs	12*1+8=20μs
	001	0.25*4=1μs	1111	15*1=15μs	12*1+15=27μs
	111	0.25*32=8μs	0000	2*8=16μs	12*8+16=112μs
	111	0.25*32=8μs	0111	8*8=64μs	12*8+64=160μs
	111	0.25*32=8μs	1111	15*8=120μs	12*8+120=216μs

Table 9.11 ADC Channel Configure Register

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH	CH7	CH6	CH5	CH4	CH3	CH2	CH1	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	-

Bit Number	Bit Name	Description
7-1	**CH[7:1]**	**Channel Configuration bits** 0: P2.7, P3.6-P3.1 are I/O port 1: P2.7, P3.6-P3.1 are ADC input port

Table 9.12 ADConverter Data Register (Compare Value Register)

96H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDL	-	-	-	-	-	-	A1	A0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0
97H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDH	A9	A8	A7	A6	A5	A4	A3	A2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
1-0 **7-0**	**A9-A0**	**ADC Data register** Digital Value of sampled analog voltage, updated when conversion is completed If ADC Compare function is enabled (EC = 1), this is the value to be compared with the analog input

The Approach for AD Conversion:

(1) Select the analog input channels and reference voltage.
(2) Enable the ADC module with the selected analog channel.
(3) Set GO/$\overline{DONE}$ = 1 to start the AD conversion.
(4) Wait until GO/$\overline{DONE}$ = 0 or ADCIF = 1, if the ADC interrupt is enabled, the ADC interrupt will occur.
(5) Acquire the converted data from ADDH/ADDL.
(6) Repeat step 3-5 if another conversion is required.

The Approach for Digital Compare Function:

(1) Select the analog input channels and reference voltage.
(2) Set ADDH/ADDL to the compare value.
(3) Set EC = 1 to enable compare function.
(4) Enable the ADC module with the selected analog channel.
(5) Set GO/$\overline{DONE}$ = 1 to start the compare function.
(6) If the analog input is lager than compare value set in ADDH/ADDL, the ADCIF will be set to 1. if the ADC interrupt is enabled, the ADC interrupt will occur.
(7) The compare function will continue work until the GO/$\overline{DONE}$ bit is cleared to 0.

9.3 PWM (Pulse Width Modulation)

9.3.1 Feature

- Support one 8-bit PWM1 output, can also be used as 8-bit timer or remote carrier generator
- Selectable output polarity

9.3.2 PWM1 (8-bit Pulse Width Modulation)

Feature

- 8-bit PWM
- Provided interrupt function on period, can also be used as 8-bit timer
- Selectable output polarity

The SH77P1651/SH77P1652 has one bult-in 8-bit PWM1 module, which can generate pulse width modulation waveform with an adjustable period or duty cycle. PWM1CON controls the clock source of PWM1of which period is controlled by PWM1P and the duty cycle is controlled by PWM1D.

Register

Table 9.13 PWM1 Control Register

DCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1CON	PWM1EN	PWM1S	PWM1CK1	PWM1CK0	-	-	PWM1IF	PWM1SS
R/W	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	0	0

Bit Number	Bit Name	Description
7	**PWM1EN**	**PWM1 Control bit** 0: Disable PWM1 1: Enable PWM1
6	**PWM1S**	**PWM1 Output Mode** 0: high active, PWM1 output high during duty time, output low during remain period time 1: low active, PWM1 output low during duty time, output high during remain period time
5-4	**PWM1CK[1:0]**	**PWM clock selection bits** 00: System clock/1 01: System clock /2 10: System clock /4 11: System clock /8
1	**PWM1IF**	**PWM1 interrupt flag** 0: the PWM0 period counter no overflow 1: the PWM0 period counter overflow, Set by hardware, cleared by hardware
0	**PWM1SS**	**PWM1 Output Control bit** 0: Disable PWM1 output, as I/O 1: Enable PWM1PWM1 output

Table 9.14 PWM1 Period Control Register

DDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1P	PWM1P.7	PWM1P.6	PWM1P.5	PWM1P.4	PWM1P.3	PWM1P.2	PWM1P.1	PWM1P.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**PWM1P[7:0]**	**PWM1 output period = PWM1P X PWM clock** ***Note:*** *(1) When PWM1P Is 00, and PWM1S is 0, PWM1 output low.* *(2) When PWM1P Is 00, and PWM1S is 1, PWM1 output high.*

Table 9.15 PWM Duty Control Register

DEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1D	PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

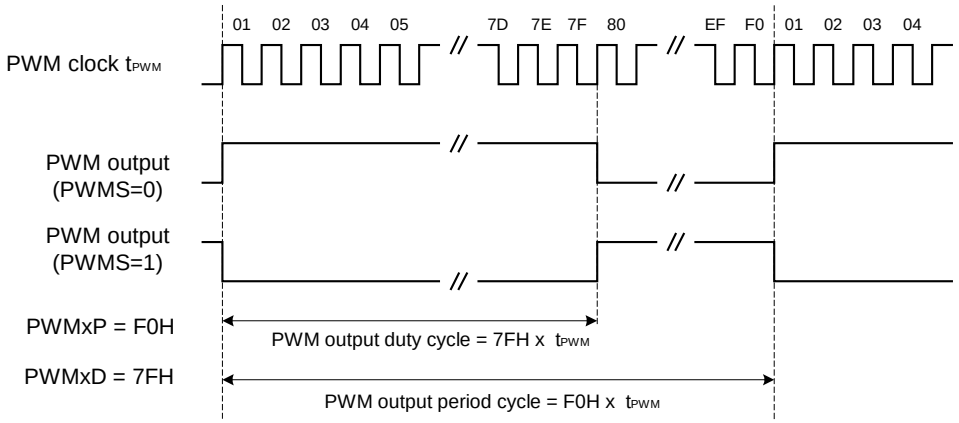
Bit Number	Bit Name	Description
7-0	**PWM1D[7:0]**	**PWM1 Duty Control bits, Control duty output time of PWM1 waveform** ***Note:*** ***(1) When PWM1P ≤ PWM1D*** *If PWM1S is 0, PWM1 output high level* *If PWM1S is 1, PWM1 output low level* ***(2) When PWM1D = 00H*** *If PWM1S is 0, PWM1 output high level* *If PWM1S is 1, PWM1 output low level*

Note:

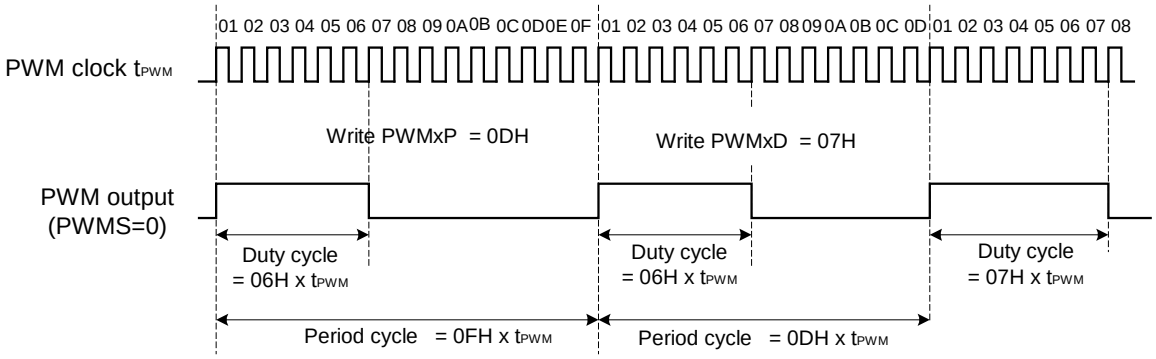
(1) PWM1EN bit: Control PWM1 on/off.

(2) PWM1SS bit: Select P5.4 as I/O or PWM1 output port.

(3) In IEN1register EPWM1bit: Enable/disable PWM1 interrupt.



PWM Output



PWM Output Period or Change Duty

9.4 The infrared module based on 8-bit PWM1 (REM)

REM port sink current is up to 500mA, can directly drive the remote carrier.

The infrared emission principle:

(1) Transmit envelope time of the infrared emission to carrier number (REMNUMH: REMNUML), set thecarrier number in the envelope register and start sending by software.

(2) Number of carriers in envelope will be sent by hardware, so MCU can do other tasks during the infrared emission.

(3) Hardware automatically load carrier number in the next envelope (REMNUMH: REMNUML) after transmission of carriers in this envelope.

(4) When hardware load REMNUMH[5:0]&REMNUML[7:0] which are 0, infrared diode can't generate REM wave, REM ports are in high-impedance state

Table 9.16 Infrared Emission Control Register

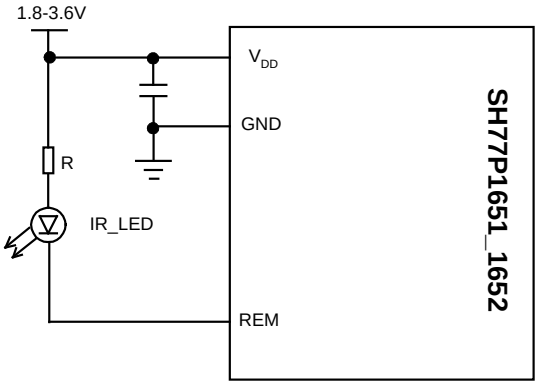
D9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMCON	-	-	-	-	-	-	REMIF	REMSW
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
1	**REMIF**	**Infrared Interrupt Flag** 0: REM envelope timer no overflow 1: REM envelope timer overflow, set by hardware, cleared by hardware
0	**REMSW**	**Infrared Enable bit (when PWM1SS is set to 1, this configuration bit will be valid)** 0: P5.4 as PWM1 output 1: P5.4 as infrared application (the port is high-impedance or low level)

Table 9.17 Infrared Emission Envelope Carrier Number Register

DAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMNUMH	REMHLSIGN	-	REMNUMH.5	REMNUMH.4	REMNUMH.3	REMNUMH.2	REMNUMH.1	REMNUMH.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	0	0	0	0
DBH	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
REMNUML	REMNUML.7	REMNUML.6	REMNUML.5	REMNUML.4	REMNUML.3	REMNUML.2	REMNUML.1	REMNUML.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**REMHLSIGN**	**Infrared Diode Envelope Level Flag** 0: Low envelope (infrared diode is closed, time: carrier number X Tpwm1) 1: High envelope (infrared diode transmit, time: carrier number X Tpwm1, carrier number is up to RMMNUM, RENMNUL)
6	**-**	**-**
5-0	**REMNUMH.x**	**High byte of Infrared Diode Envelope Carrier Number Control, y = 0 - 5**
7-0	**REMNUML.x**	**Low byte of Infrared Diode Envelope Carrier Number Control, x = 0 - 7**



Typical Application Circuit

(R selection: please selecte according to infrared diode parameters and REM drive current configuration in code option)

Reference program to generate 38KHZ carrier

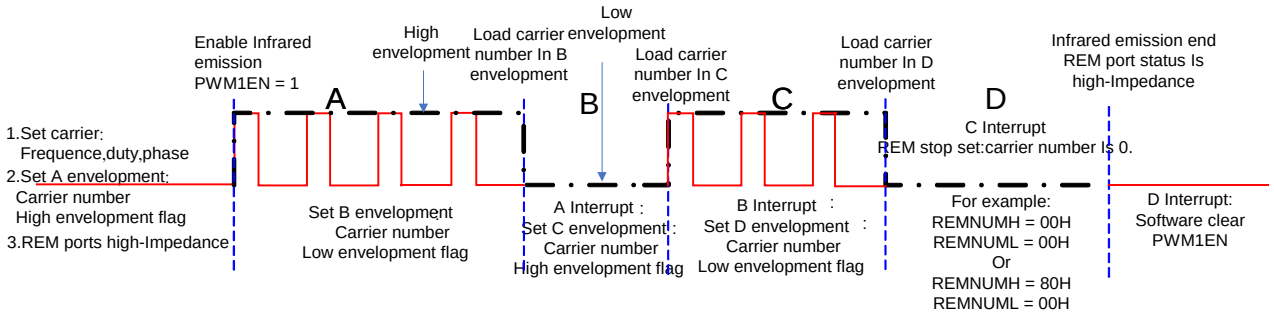
REM ports transmit A B C D carrier (AS shown in **Infrared Diode Emission Voltage Waveform**)

```
/*Envelope carrier number in auiRemCod code:
High 8-bit: high 6-bit data and high/low envelope flag
Low 8-bit: low 8-bit data
*/
char g_auiRemCode[5][2] = {{0x80,0x04},{0x00,0x02},{0x80,0x03},{0x00,0x03},{0x00,0x00}};
                  /*   A            B            C              D              end */

void REM_InitCarrier(void)
{
        PWM1CON    = 0x44;              //Low level drive, select REM function, select 4MHz system clock
        PWM1P      = 0x69;              //Set carrier frequence to 38kHz
        PWM1D      = 0x23;              // Set carrier duty to 33%
        REMNUMH    = g_auiRemCode[0][0];    //Set 38kHz carrier number in A envelope, high envelope flag
        REMNUML    = g_auiRemCode[0][1];
        IEN1       |= 0x02;             //Enable REM interrupt
        PWM1CON    |= 0x80;             //PWM output
        REMNUMH    = g_auiRemCode[1][0];    // Set 38kHz carrier number in B envelope, low envelope flag
        REMNUML    = g_auiRemCode[1][1];
}

void REM_IntSetInfrared(void)  interrupt  8
{
    static unsigned  int i = 1;
        unsigned  int j = 0;
        i = i + 1;

        /*If REMNUMH and REMNUML are all 0, The infrared emission will end */
        if((REMNUML == 0)&&(REMNUMH == 0x40))
        {
                /*Software close PWM wave*/
                PWM1CON &= 0x7F ;
                i = 1;
        }
        else
        {
                /*Set carrier number in the next envelope and high envelope flag*/
                REMNUMH = g_auiRemCode[i][j];
                REMNUML = g_auiRemCode[i][j+1];
        }
}
```



Infrared Diode Emission Voltage Waveform

9.5 EUART

9.5.1 Feature

- The SH77P1651/SH77P1652 has one enhanced EUART which are compatible with the conventional 8051
- 15-bit up counter withthe baud rate generator
- Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
- The EUART can be operated in four modes

Note: *when EUART is used, system must switch to 4MHz.*

9.5.2 EUART Mode Description

The EUART can be operated in 4 modes. Users must initialize the SCON before any communication can take place. This involves selection of the Mode and the baud rate.

In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if RI = 0 and REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

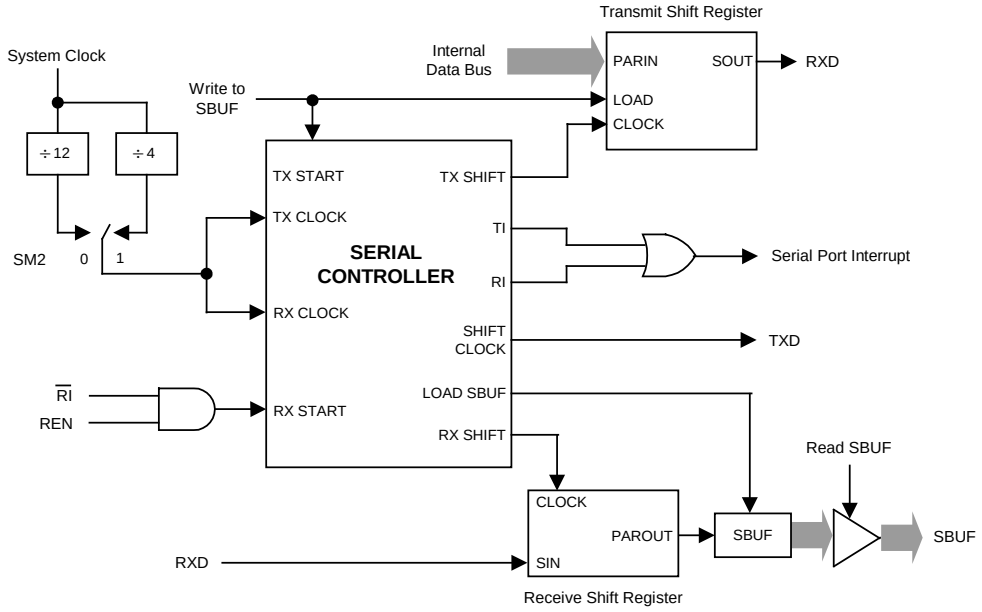
SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit
0	0	0	Sych	f_{SYS}/(4 or 12)	8 bits	NO	NO	None
0	1	1	Ansych	overflow rate of baud rate generator /16	10 bits	1	1	None
1	0	2	Ansych	f_{SYS}/(32 or 64)	11 bits	1	1	0, 1
1	1	3	Ansych	overflow rate of baud rate generator /16	11 bits	1	1	0, 1

Mode0: Synchronous Mode, Half duplex

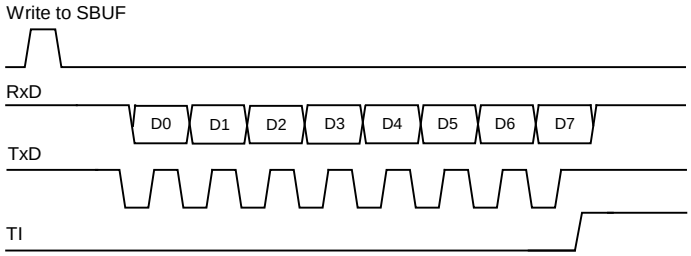
This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RxD line. TxD is used to output the shift clock. The TxD clock is provided by the SH77P1651/SH77P1652 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first.

The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

The functional block diagram is shown below. Data enters and exits the serial port on the RxD line. The TxD line is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the SH77P1651/SH77P1652.

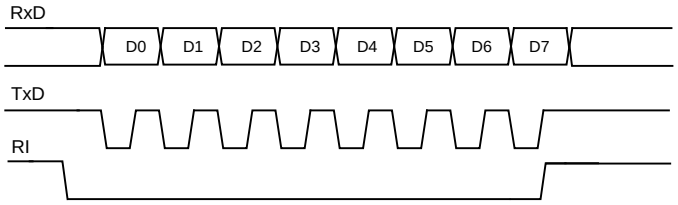


Any instruction that uses SBUF as a destination register (“write to SBUF” signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivates SEND and sets TI (SCON.1) at the rising edge of the next system clock.



Send Timing of Mode 0

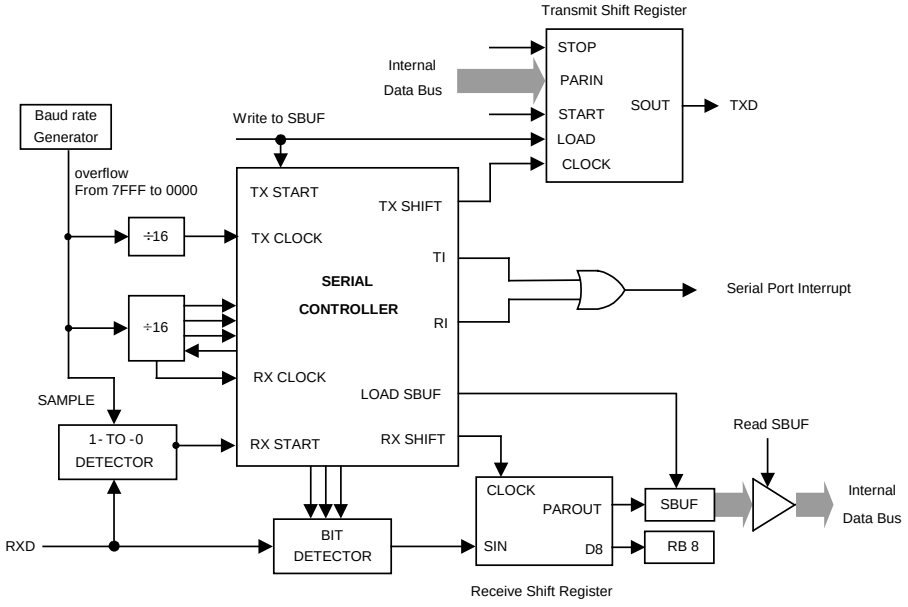
Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivates RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.



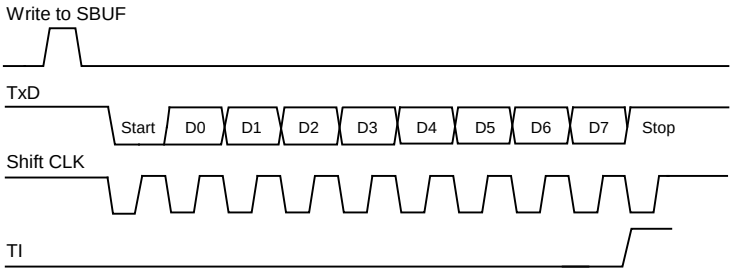
Receive Timing of Mode 0

Mode1: 8-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The baud rate in mode1 is its own baud rate generator overflow rate/16. The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal. The start bit is firstly put out on TxD pin, then are the 8 bits of data. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time that the stop is send.



Send Timing of Mode 1

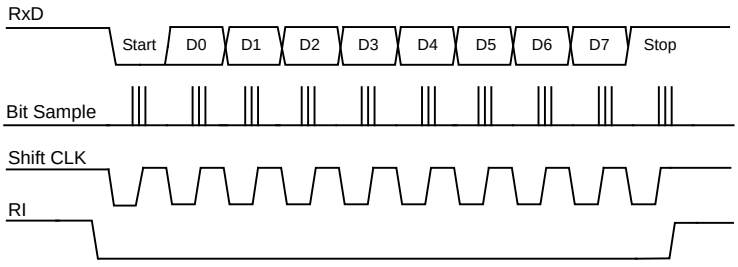
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7^{th}, 8^{th} and 9^{th} counter states of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI are set if the following conditions are met:

1. RI must be 0

2. Either SM2 = 0, or the received stop bit = 1

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

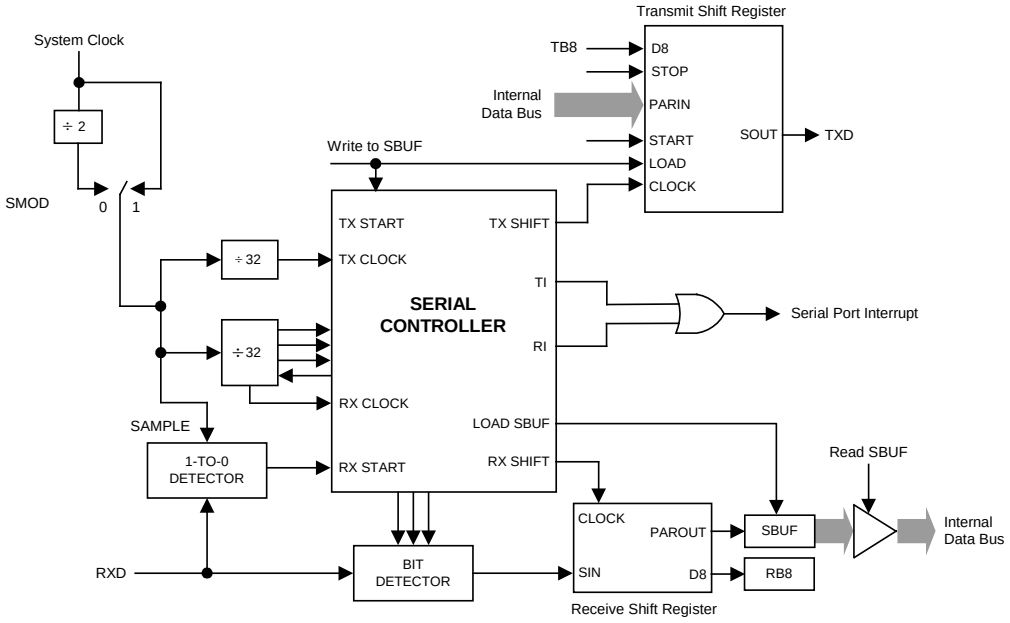
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



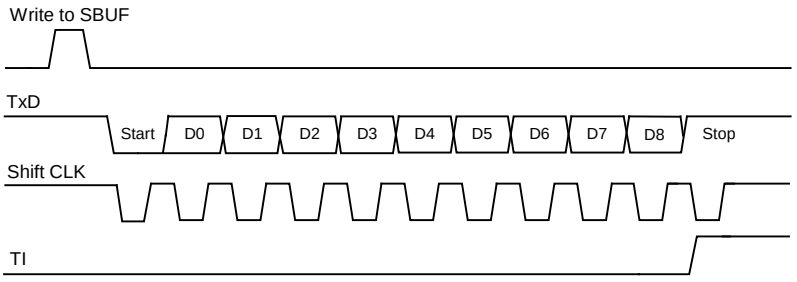
Receive Timing of Mode 1

Mode2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

This mode provides the 11 bits full duplex asynchronous communication. The 11 bit consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition (Refer to Multiprocessor Communication Section for details). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, the “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal). The start bit is firstly put out on TxD pin, then are the 9 bits of data. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time, this will be at the 11th rollover of the divide-by-16 counter after a write to SBUF.



Send Timing of Mode 2

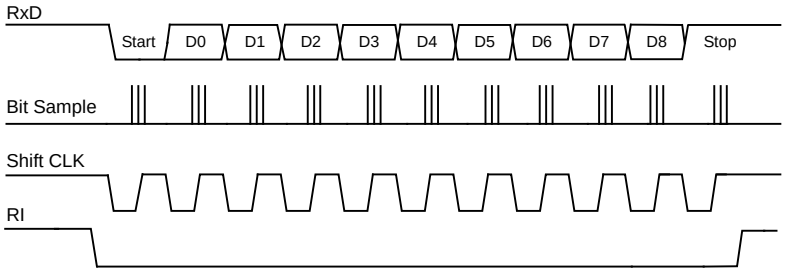
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter. The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7th, 8th and 9th counter state of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit detected after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set if the following conditions are met:

1. RI must be 0

2. Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

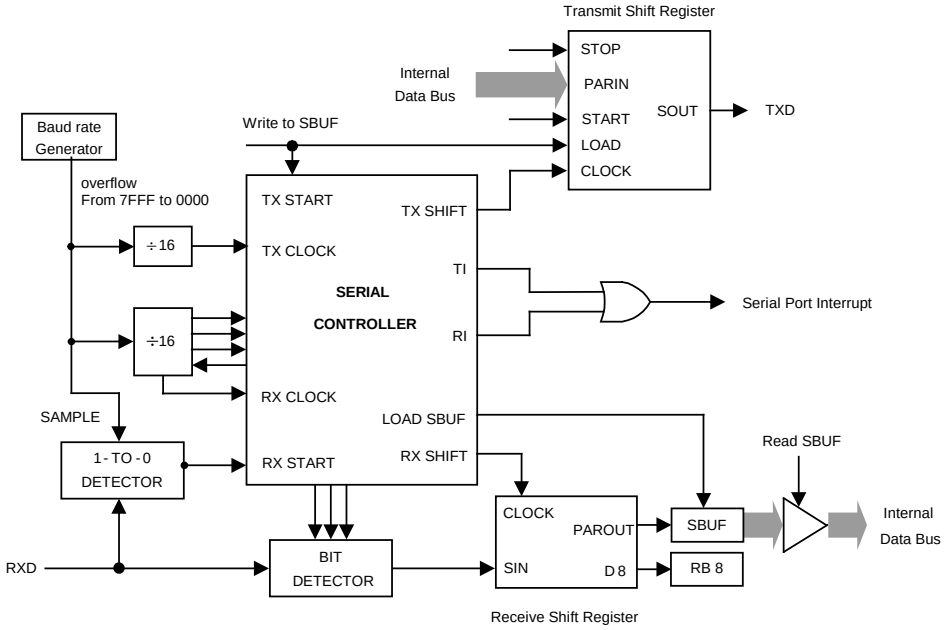
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

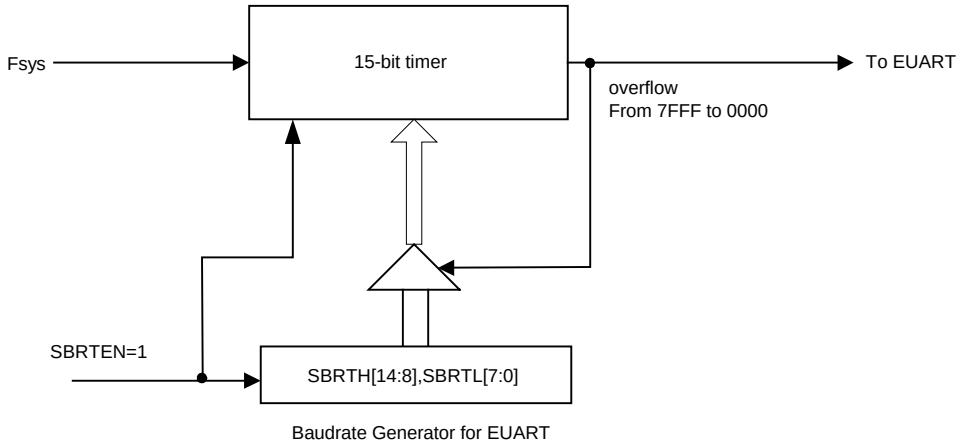
Mode3: 9-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

Mode3 uses transmission protocol of the Mode2 and baud rate generation of the Mode1.



9.5.3 Adjustable Baud Rate

EUART has its own baud rate generator, which is actually a 15-bit up counter.



Baudrate Generator for EUART

From the figure, the baud rate generator overflow rate: $\text{SBRToverflowrate} = \frac{\text{Fsys}}{32768 - \text{SBRT}}$,

$\text{SBRT} = [\text{SBRTH}, \text{SBRTL}]$.

Therefore, EUART baud rate calculation formula in each mode is as follows:

In Mode0, the baud rate is programmable to be either 1/12 or 1/4 of the system frequency. This baud rate is determined by SM2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

The baud rate can be adjust at a accuracy of one system clock period in Mode1 & Mode3, the formula is as follows:

$$\text{BaudRate} = \frac{\text{Fsys}}{16 \times (32768 - \text{SBRT}) + \text{BFINE}}$$

For example: If you want to get the baud rate of 19200Hz in condition of Fsys = 4MHz, SBRT and SFINE value is calculated as follows:

4000000/16/19200 = 13.02

SBRT = 32768 - 13 = 32755

19200 = 4000000/(16 X 13 + BFINE)

BFINE = 0.33 ≈ 0

The actual baud calculated according to this fine-tuning mode is 19230 with 0.16% error which will be 8.5% in the past.

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, the serial port runs at 1/64 of the clock. When set to 1, the serial port runs at 1/32 of the clock.

9.5.4 Multi-Processor Communication

Software Address Recognition

Modes 2 and 3 of the EUART have a special provision for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the EUART interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte.

With SM2 = 1, no other slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed leave their SM2 set, ignoring the incoming data bytes.

Note: *In Mode0, SM2 is used to select baud rate doubling. In Mode1, SM2 can be used to check the validity of the stop bit. If SM2 = 1 in Mode1, the receive interrupt will not be activated unless a valid stop bit is received.*

Automatic (Hardware) Address Recognition

In Mode2 & 3, setting the SM2 bit will configure EUART act as following: when a stop bit is received, EUART will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts on the reception of the following data byte(s).

The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the addressed slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the addressed slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, as they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all transmissions until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. The slave address is an 8-bit value specified in the SADDR register. The SADEN register is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

	Slave 1	Slave 2
SADDR	10100100	10100111
SADEN (0 mask)	11111010	11111001
Given Address	10100x0x	10100xx1
Broadcast Address (OR)	1111111x	11111111

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it doesn't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as don't cares. In most cases, the Broadcast Address is FFh, this address will be acknowledged by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXXXXXX (all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUART 0 will reply to any address, which it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor by software address recognition mentioned above.

9.5.5 Error Detection

Error detection is available when the SSTAT bit in register PCON is set to logic 1.The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).All the 3 bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Transmit Collision

The Transmit Collision bit (TXCOL bit in register SCON) reads '1' if RI is set 0 and user software writes data to the SBUF register while a transmission is still in progress. If this occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overrun

The Receive Overrun bit (RXOV in register SCON) reads '1' if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happen.

Frame Error

The Frame Error bit (FE in register SCON) reads '1' if an invalid (low) STOP bit is detected.

9.5.6 Register

Table 9.18 EUART Control & Status Register

98H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0 /FE	SM1 /RXOV	SM2 /TXCOL	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-6	**SM[0:1]**	**EUART Serial mode control bit, when SSTAT = 0** 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8 bit Asynchronous Mode, variable baud rate 10: mode 2, 9 bit Asynchronous Mode, fixed baud rate 11: mode 3, 9 bit Asynchronous Mode, variable baud rate
7	**FE**	**EUART Frame Error flag, when FE bit is read, SSTAT bit must be set 1** 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware
6	**RXOV**	**EUART Receive Over flag, when RXOV bit is read, SSTAT bit must be set 1** 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware
5	**SM2**	**EUART Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0** 0: In Mode0, baud-rate is 1/12 of system clock In Mode1, disable stop bit validation check, any stop bit will set RI to generate interrupt In Mode2 & 3, any byte will set RI to generate interrupt 1: In Mode0, baud-rate is 1/4 of system clock In Mode1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In Mode2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	**TXCOL**	**EUART Transmit Collision flag, when TXCOL bit is read, SSTAT bit must be set 1** 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware
4	**REN**	**EUART Receiver enable bit** 0: Receive Disable 1: Receive Enable
3	**TB8**	**The 9th bit to be transmitted in Mode2 & 3 of EUART, set or clear by software**
2	**RB8**	**The 9th bit to be received in Mode1, 2 & 3 of EUART** In Mode0, RB8 is not used In Mode1, if receive interrupt occurs, RB8 is the stop bit that was received In Modes2 & 3 it is the 9th bit that was received
1	**TI**	**Transmit interrupt flag of EUART** 0: cleared by software 1: Set by hardware
0	**RI**	**Receive interrupt flag of EUART** 0: cleared by software 1: Set by hardware

Table 9.19 EUART Data Buffer Register

99H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**SBUF[7:0]**	This SFR accesses two registers; a transmit shift register and a receive latch register A write of SBUF will send the byte to the transmit shift register and then initiate a transmission A read of SBUF returns the contents of the receive latch

Table 9.20 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Name	Description
7	**SMOD**	**Baud rate doubler** 0: In mode 2, the baud rate is system clock1/64 1: In mode 2, the baud rate is system clock1/32
6	**SSTAT**	**SCON[7:5] function select bit** 0: SCON[7:5] operates as SM0, SM1, SM2 1: SCON[7:5] operates as FE, RXOV, TXCOL
3-2	**GF[1:0]**	Software General Flag
1	**PD**	Power Down Mode Control bit
0	**IDL**	Idle Mode Control bit

Table 9.21 EUART Slave Address & Address Mask Register

9AH-9BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR (9AH)	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN (9BH)	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**SADDR[7:0]**	**SFR SADDR defines the EUART's slave address**
7-0	**SADEN[7:0]**	**SFR SADEN is a bit mask to determine which bits of SADDR are checked against a received address** 0: Corresponding bit in SADDR is a "don't care" 1: Corresponding bit in SADDR is checked against a received address

Table 9.22 EUART Baud Rate Generator Register

9CH-9DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRTH (9CH)	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL (9DH)	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**SBRTEN**	**EUART Baud Rate Generator Enable bit** 0: Off (default) 1: On
6-0 **7-0**	**SBRT[14:0]**	**EUART Baud Rate Generator Counter High 7-bit & Low 8-bit Register**

Table 9.23 EUART Baud Rate Generator Fine-Tune Register

9EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SFINE	-	-	-	-	SFINE.3	SFINE.2	SFINE.1	SFINE.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Name	Description
3-0	**SFINE[3:0]**	**EUART Baud Rate Generator Fine Tune Data Register**

9.6 Low Voltage Reset (LVR)

9.6.1 Feature

- Enabled by the code option and V_{LVR} is 1.95V
- LVR de-bounce timer T_{LVR} is about 30μs
- An internal reset flag indicates low voltage reset generates

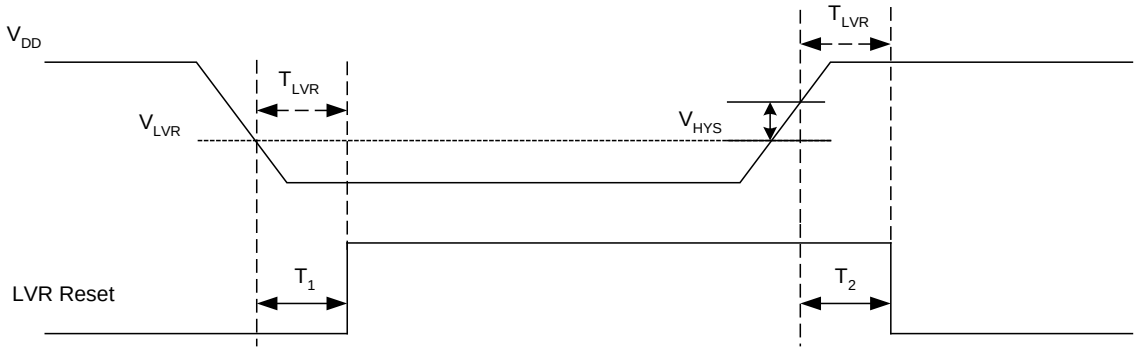
The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage below the specified value V_{LVR}. The LVR de-bounce time T_{LVR} is about 30μs.

The LVR circuit has the following functions when the LVR function is enabled: (T_1 means the time of the supply voltage below VLVR, T_2 means the time of the supply voltage above $V_{LVR} + V_{HYS}$)

Generates the system reset when $V_{DD} \leq V_{LVR}$ and $T_1 \geq T_{LVR}$

Cancels the system reset when $V_{DD} > V_{LVR} + V_{HY}$ and $T_2 \geq T_{LVR}$

No system reset occurs when $V_{DD} < V_{LVR}$ and $T_1 < T_{LVR}$, $0.09V \leq V_{HYS} \leq 0.11V$



V_{DD} as power voltage, V_{LVR} as LVR detection voltage, V_{HYS} as low voltage reset sluggish voltage.

The LVR function is enabled by the code option.

It is typically used in AC line or large battery supplier applications, where heavy loads switched can cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage. This feature can protect system from working under bad power supply environment.

9.7 Watchdog Timer (WDT) and Reset State

9.7.1 Feature

- Auto detect Program Counter (PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH77P1651/SH77P1652 built in Program Counter (PC) over range detect circuit, if program counter value is larger than flash romsize, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash rom with A5H.

Watchdog Timer

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled permanently by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow frequency. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

There are also some reset flags in this register as below:

9.7.2 Register

Table 9.24 Reset Control Register

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Name	Description
7	**WDOF**	**Watch Dog Timer Overflow or OVL Reset Flag** Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows and no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	**PORF**	**Power On Reset Flag** Set only by Power On Reset, cleared only by software 0: No Power On Reset. 1: Power On Reset occurred.
4	**LVRF**	**Low Voltage Reset Flag** Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	**LVRF**	**Pin Reset Flag** Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred
2-0	**WDT[2:0]**	**WDT Overflow period control bit** 000: Overflow period minimal value= 4096 ms 001: Overflow period minimal value= 1024 ms 010: Overflow period minimal value = 256 ms 011: Overflow period minimal value = 128 ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms ***Notes:*** *If WDT_opt is enable in application, you must clear WatchDog periodically, and the interval must be less than the value list above.*

9.8 Power Management

9.8.1 Feature

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH77P1651/SH77P1652 supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

9.8.2 Idle Mode

In this mode, the clock to CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH77P1651/SH77P1652 enter Idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter Idle mode. The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

(1) An interrupt generated. CPU clock will be restored, and the hardware will clear IDL bit in CON register and SUSLO register. Then the program will execute the interrupt service routine, and then jumps to the instruction following the instruction that activated Idle mode.

(2) After reset signal (logic low on the RESET pin, WDT RESET, LVR REST) happen, CPU clock will be restored, the hardware will clear IDL bit in CON register and SUSLO register. SH77P1651/SH77P1652 will finally be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

9.8.3 Power-Down Mode

The Power-Down mode places the SH77P1651/SH77P1652 in a very low power consumption state.

If system clock selects 32.768kHz crystal or the internal 32kHz RC, power-Down mode will stop all the clocks including CPU and peripherals.

If system clock selects internal 4MHz RC, power-Down mode will stop all the clocks including CPU and peripherals (except 32kHz/32.768KHz used to LCD and Timer3).

If WDT is enabled by code option, WDT module will keep on working in Power-Down mode. All the CPU status will be preserved before entering Power-Down mode. Such as: PSW, PC, SFR & RAM.

Two consecutive instructions: first setting SUSLO register as 0x55, then setting the PD bit of PCON register immediately, make SH77P1651/SH77P1652 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. Otherwise CPU will not enter Power-Down mode.

Note: *If IDL bit and PD bit are set simultaneously, the SH77P1651/SH77P1652 enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit form Power-Down mode.*

1. If SH77P1651/SH77P1652 enter Power-Down mode in high frequence status, there are three ways to exit the Power-Down mode:

(1) An effective external Interrupt INT4 makes SH77P1651/SH77P1652 exit Power-Down mode. The high frequence oscillator restarts after interrupt occurs. After warm-up time, the clocks of the CPU and peripheral are restored, and the SUSLO register and PD bit are cleared by hardware. Then the CPU executes the corresponding interrupt service program. After that, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) Timer3 interrupt makes SH77P1651/SH77P1652 exit Power-Down mode. The high frequence oscillator restarts after the interrupt ocurrs, After warm-up time, the clocks of the CPU and peripheral are restored, and the SUSLO register and PD bit are cleared by hardware. Then the CPU executes the corresponding interrupt service program. After that, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(3) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled). The low frequence oscillator restarts after reset signal occurs. After warm-up time, the clocks of the CPU and peripheral are restored, and the SUSLO register and PD bit are cleared by hardware. Then the SH77P1651/SH77P1652 is reset. And the program executes from 0000H address. The RAM keeps their values and the SFR values might be changed according to different modules.

2. If SH77P1651/SH77P1652 enter Power-Down mode in low frequence status, there are three ways to exit the Power-Down mode:

(1) An active external Interrupt INT4 will make SH77P1651/SH77P1652 exit Power-Down mode. The low frequence oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) Timer3 interrupt will make SH77P1651/SH77P1652 exit Power-Down mode. The low frequence oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(3) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled). The low frequence oscillator will start after reset signal t happens, after warm-up time, the clocks to the CPU will be restored, the SUSLO register and the PD bit in PCON register will be cleared by hardware, SH77P1651/SH77P1652 will finally be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note: *In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.*

9.8.4 Register

Table 9.25 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Name	Description
7	**SMOD**	**Baud rate double bit**
6	**SSTAT**	**SCON[7:5] function selection bit**
3-2	**GF[1:0]**	**General purpose flags for software use**
1	**PD**	**Power-Down mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode
0	**IDL**	**Idle mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode

Table 9.26 Suspend Mode Control Register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**SUSLO[7:0]**	This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise the either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle.

Example:

```
IDLE_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #01H
        NOP
        NOP
        NOP

POWERDOWN_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #02H
        NOP
        NOP
        NOP
```

9.9 Warm-up Timer

9.9.1 Feature

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation startup

SH77P1651/SH77P1652 has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read customer option etc.

SH77P1651/SH77P1652 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from Power-down mode.

After power-on, SH77P1651/SH77P1652 will start power warm-up procedure first, and then oscillator warm-up procedure.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		**WDT Reset (Not in Power-Down Mode)**		**WDT Reset (Wakeup from Power-Down Mode)**		**Wakeup from Power-Down Mode (Only for interrupt)**	
TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*
12ms	YES	12ms	NO	12ms	YES	NO	YES

OSC Warm-up Time

Oscillator Type	**OSC Warm-up Time**
Internal RC 32K	2^7 X T_{OSC}
Internal RC 4M	2^7 X T_{OSC}
32kHz Crystal	2^{13} X T_{OSC}

9.10 Code Option

OP_WDT:
0: Enable WDT function (default)
1: Disable WDT function

OP_WDTPD:
0: Disable WDT function in Power-Down mode (default)
1: Enable WDT function in Power-Down mode
Note: *This code option is valid, only when OP_WDT[7] is 0.*

OP_SCMEN:
0: Disable SCM function (default)
1: Enable SCM function

OP_OSC:
0: Internal 32kHz RC as oscillator 1, internal 4MHz RC as oscillator 2, XTAL1 and XTAL2 as I/O (default)
1: External 32.768kHz as oscillator 1, internal 4MHz RC as oscillator 2

OP_LVREN:
0: Disable LVR function (default)
1: Enable LVR function

OP_SCM:
0: SCM is off during warm-up time (default)
1: SCM is on during warm-up time

OP_RST:
0: P5.5 as reset pin (default)
1: P5.5 as I/O

OP_LCDSEL:
0: Select resistor LCD driver (default)
1: Select capacitor LCD driver

OP_REM_CURRENT: (REM drive current selection)
00: 125mA (default)
01: 250mA
10: 375mA
11: 500mA

10. Instruction Set

ARITHMETIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ADD A, Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A, direct	Add direct byte to accumulator	0x25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data	Add immediate data to accumulator	0x24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data	Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	2	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	1	3
INC DPTR	Increment data pointer	0xA3	1	4
MUL AB 8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB 8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A	Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES					
Opcode		**Description**	**Code**	**Byte**	**Cycle**
ACALL addr11		Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16		Long subroutine call	0x12	3	7
RET		Return from subroutine	0x22	1	8
RETI		Return from interrupt	0x32	1	8
AJMP addr11		Absolute jump	0x01-0xE1	2	4
LJMP addr16		Long jump	0x02	3	5
SJMP rel		Short jump (relative address)	0x80	2	4
JMP @A+DPTR		Jump indirect relative to the DPTR	0x73	1	6
JZ rel	(not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel	(not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel	(not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel	(not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit, rel	(not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit, rel	(not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel	(not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A, direct, rel	(not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A, #data, rel	(not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn, #data, rel	(not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel	(not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn, rel	(not taken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel	(not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP		No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

11. Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage. . . . . -0.3V to +3.6V

Input/Output Voltage. . . . . GND-0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . . . -10℃ to +70℃

Storage Temperature. . . . . -55℃ to +125℃

***Comments**

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	3.0	3.6	V	30kHz ≤ f_{OSC} ≤ 4MHz
Operating Current	I_{OP1}	-	1.2	2	mA	f_{OSC} = 4MHz, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, all other function block off
Stand by Current (IDLE)	I_{SB1}	-	11	16.5	μA	f_{OSC} = RC 32kHz, V_{DD} = 3.0V, OSCX off, all output pins unload, CPU off (IDLE); all digital input pins unfloating; LVR on, WDT off, SCM off, LCD resistance circuit (V_{LCD} = V_{DD}), bias resistance sum 990K, LCD on (not include LCD panel), all other function block off
	I_{SB2}	-	10	15	μA	f_{OSC} = RC 32kHz, V_{DD} = 3.0V, OSCX off, all output pins unload, CPU off (IDLE); all digital input pins unfloating; LVR on, WDT off, SCM off, LCD buit-in voltage regulator (PUMP on), bias resistance sum 990K, LCD on (not include LCD panel), all other function block off
	I_{SB3}	-	9	13.5	μA	f_{OSC} = RC 32kHz, V_{DD} = 3.0V, OSCX off; all output pins unload, CPU off (IDLE); all digital input pins unfloating; LVR on, WDT off, SCM off, LCD bias capacitance mode (PUMP off, V_{LCD} = V_{DD}), LCD on (not include LCD panel), all other function block off
	I_{SB4}	-	9	13.5	μA	f_{OSC} = 32.768kHz, V_{DD} = 3.0V, OSCX off; all output pins unload, CPU off (IDLE); all digital input pins unfloating; LVR on, WDT off, SCM off, LCD bias resistance mode (V_{LCD} = V_{DD}), bias resistance sum 990K, LCD on (not include LCD panel), all other function block off
Stand by Current (Power-Down)	I_{SB5}	-	4	6	μA	f_{OSC} = 32.768kHz, V_{DD} = 3.0V, OSCX off; all output pins unload, CPU off (Power-Down); all digital input pins unfloating; LVR off, WDT off, SCM off, LCD bias capacitance mode, LCD on (not include LCD panel), all other function block off
	I_{SB6}	-	-	1.5	μA	Osc off, V_{DD} = 3.0V; all output pins unload (including all digital input pins unfloating), CPU off (Power-Down), LCD off, WDT off, SCM off, LVR on, all other function block off

(to be continued)

(continue)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
LCD Current 1	I_{LCD1}	-	2	3	μA	V_{DD} = 3.0V, buit-in voltage regulator (not include LCD panel)
LCD Current 2	I_{LCD2}	-	3	4	μA	V_{DD} = 3.0V, bias resistance mode, bias resistance sum 990K, LCD on (not include LCD panel) VOL[2:0] = 000
LCD Current 3	I_{LCD3}	-	1	1.5	μA	V_{DD} = 3.0V, bias capacitance mode (not include LCD panel).
WDT Current	I_{WDT}	-	-	1	μA	All output pins unload, WDT on, V_{DD} = 3.0V
Input Low Voltage 1	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input High Voltage 1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input Low Voltage 2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T2, T3, INT4, T2EX, RXD, TXD (Schmitt trigger input)
Input High Voltage 2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T2, T3, INT4, T2EX, RXD, TXD (Schmitt trigger input)
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN} = V_{DD} or GND
Output Leakage Current	I_{OL}	-1	-	1	μA	Open-drain output, V_{DD} = 3.0V, V_{OUT} = V_{DD} or GND
Rest pin Pull-up Resistor	R_{RPH}	-	30	-	kΩ	V_{DD} = 3.0V, V_{IN} = GND
Pull-up Resistor	R_{PH}	-	150	-	kΩ	V_{DD} = 3.0V, V_{IN} = GND
Output High Voltage 1	V_{OH1}	V_{DD} - 0.7	-	-	V	I/O Ports, I_{OH} = -5mA, V_{DD} = 3.0V
Output Low Voltage 1	V_{OL1}	-	-	GND +0.6	V	I/O Ports, I_{OL} = 10mA, V_{DD} = 3.0V (except P2.3, P2.2 and P0.6)
Output Low Voltage 2	V_{OL2}	-	-	GND +0.6	V	I_{OL} = 20mA, V_{DD} = 3.0V, P2.3, P2.2 and P0.6
Output Low Voltage 3	V_{OL3}	-	-	GND +0.6	V	Only P0.7, I_{OL} = 0.5mA, V_{DD} = 3.0V
REM Sink Current	I_{REML}	-	500	-	mA	V_{DD} = 3.0V, V_{OL} = GND + 1.2V REM (PWM1/P5.4)
V_{P1}	V_{P1}	0.965	1.03	1.095	V	SEG1 - 30, COM1 - 5, V_{DD} = 1.8V - 3.6V The voltage variation of VP3 is less than 0.2V
LCD Resistor	R_{ON}	-	5	-	kΩ	SEG1 - 30, COM1 - 5, V_{DD} = 1.8V - 3.6V The voltage variation of VP3 is less than 0.2V

Note:

(1) "" Data in "Typ." Column is at 3.0V, 25°C, unless otherwise specified.*
(2) Maximum value of the supply current to V_{DD} is 80mA.
(3) Maximum value of the output current from GND is 700mA.

A/D Converter Electrical Characteristics (V_{DD} = 3V, GND = 0V, T_A = 25°C, Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{AD}	1.8	3.0	3.6	V	
A/D Referance Voltage	V_{REF}	1.8	-	V_{DD}	V	
Resolution	N_R	-	10	-	bit	$GND \le V_{AIN} \le V_{REF}$
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor*	R_{AIN}	2	-	-	MΩ	V_{IN} = 3.0V
Recommended impedance of analog voltage source	Z_{AIN}	-	-	10	kΩ	
A/D conversion current	I_{AD}	-	1	3	mA	ADC work, V_{DD} = 3.0V
A/D Input current	I_{ADIN}	-	-	10	μA	V_{DD} = 3.0V
Differential linearity error	D_{LE}	-	-	±1	LSB	f_{OSC} = 4MHz, V_{DD} = 3.0V
Integral linearity error	I_{LE}	-	-	±2	LSB	f_{OSC} = 4MHz, V_{DD} = 3.0V
Full scale error	E_F	-	±1	±3	LSB	f_{OSC} = 4MHz, V_{DD} = 3.0V
Offset error	E_Z	-	±0.5	±3	LSB	f_{OSC} = 4MHz, V_{DD} = 3.0V
Total Absolute error	E_{AD}	-	-	±3	LSB	f_{OSC} = 4MHz, V_{DD} = 3.0V
Total Conversion time	T_{CON}	14	-	-	t_{AD}	10 bit, V_{DD} = 3.0V, t_{AD} = 1μs

Note:

(1) "" Here the A/D input Resistor is the DC input-resistance of A/D itself.*

(2) Suggest that the sigal source resistance connected with ADC is less than 10 kΩ.

AC Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = 25°C, f_{OSC} = 4MHz, unless otherwise specified)

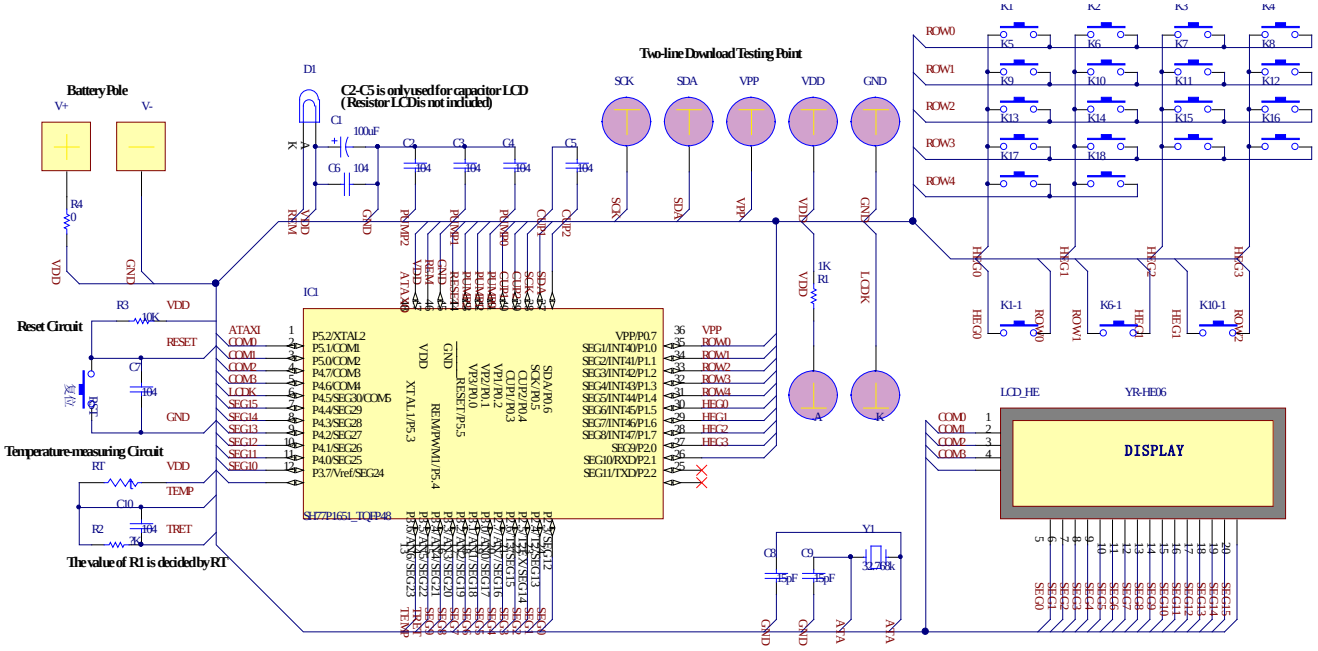
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	T_{OSC}	-	-	1	s	f_{OSC} = 32.768kHz
RESET pulse width	t_{RESET}	10	-	-	μs	
WDT RC Frequency	f_{WDT}	-	-	2	kHz	
32K RC Frequency	f_{32K}	28.8	32	35.2	kHz	
Built-in 4MHZ RC Frequency Stability	$\lvert \Delta F \rvert / F$	3.92	4.0	4.08	MHz	Built-in RC oscillator, V_{DD} = 2.0V - 3.6V, T_A = -10℃ ~ +70℃

Note: *Typically (T_A = 25°C), the precision of internal 4M RC is less than 5‰.*

Low Voltage Reset Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = 25°C, f_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage	V_{LVR}	1.85	1.95	2.05	V	Enable LVR 30kHZ ≤ f_{OSC} ≤ 4MHZ, V_{DD} = 1.8V - 3.6V
LVR low reset pulse width	T_{LVR}	-	30	-	μs	

12. Application

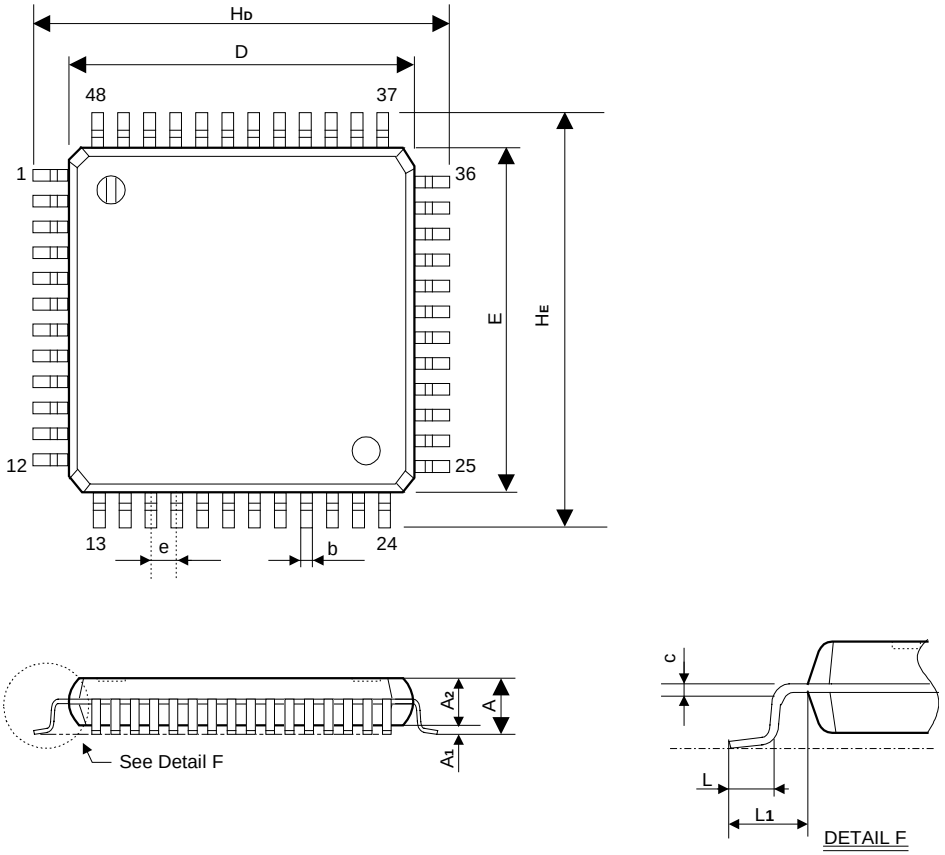


13. Ordering Information

Part No.	Package
SH77P1651U/048UR	TQFP48
SH77P1652U/048UR	TQFP48
SH77P1652U/048UA	TQFP48
SH77P1652H	Chip form

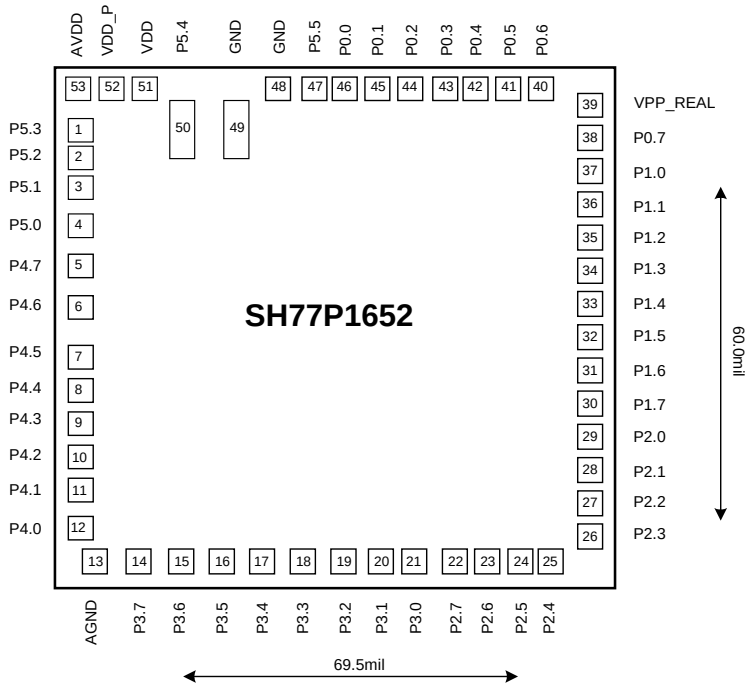
14. Package Information

TQFP48 Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	---	0.047	---	1.2
A1	0.002	0.006	0.05	0.15
A2	0.035	0.041	0.9	1.05
D	0.270	0.281	6.85	7.15
E	0.270	0.281	6.85	7.15
H_D	0.346	0.362	8.8	9.2
H_E	0.346	0.362	8.8	9.2
b	0.007	0.010	0.19	0.26
e	0.020 TYP		0.500 TYP	
c	0.004	0.008	0.090	0.200
L	0.018	0.030	0.45	0.75
L1	0.033	0.045	0.85	1.15
θ	0°	10°	0°	10°

Bonding Diagram



Pad Location **Unit: mil**

Pad No	Pad Name	X	Y	TQFP48	Pad No	Pad Name	X	Y	TQFP48
1	P5.3	-795.72	580.42	48	28	P2.1	795.72	-396.36	26
2	P5.2	-795.72	490.42	1	29	P2.0	795.72	-306.36	27
3	P5.1	-795.72	367.64	2	30	P1.7	795.72	-216.36	28
4	P5.0	-795.72	247.64	3	31	P1.6	795.72	-126.36	29
5	P4.7	-795.72	127.64	4	32	P1.5	795.72	-36.36	30
6	P4.6	-795.72	7.64	5	33	P1.4	795.72	53.64	31
7	P4.5	-795.72	-136.72	6	34	P1.3	795.72	143.64	32
8	P4.4	-795.72	-226.72	7	35	P1.2	795.72	233.64	33
9	P4.3	-795.72	-316.72	8	36	P1.1	795.72	323.64	34
10	P4.2	-795.72	-406.72	9	37	P1.0	795.72	413.64	35
11	P4.1	-795.72	-496.72	10	38	P0.7	795.72	504.64	36
12	P4.0	-795.72	-586.72	11	39	VPP_REAL	795.72	653.78	
13	AGND	-758.95	-675.72	FRAME	40	P0.6	700.72	675.72	37
14	P3.7	-570.11	-675.72	12	41	P0.5	605.72	675.72	38
15	P3.6	-444.11	-675.72	13	42	P0.4	515.72	675.72	39
16	P3.5	-318.11	-675.72	14	43	P0.3	425.72	675.72	40
17	P3.4	-192.11	-675.72	15	44	P0.2	335.72	675.72	41
18	P3.3	-66.11	-675.72	16	45	P0.1	245.72	675.72	42
19	P3.2	59.89	-675.72	17	46	P0.0	146.72	675.72	43
20	P3.1	185.89	-675.72	18	47	P5.5	56.72	675.72	44
21	P3.0	311.89	-675.72	19	48	GND	-33.28	675.72	45 & FRAME
22	P2.7	437.89	-675.72	20	49	GND	-151.32	574.1	45
23	P2.6	527.89	-675.72	21	50	P5.4	-367.48	574.1	46
24	P2.5	617.89	-675.72	22	51	VDD	-567.53	675.72	47
25	P2.4	707.89	-675.72	23	52	VDD_P	-657.53	675.72	47
26	P2.3	795.72	-576.36	24	53	AVDD	-747.53	675.72	47
27	P2.2	795.72	-486.36	25					

15. Product SPEC. Change Notice

Version	Content	Date
2.0	Change the package informationand I/O port feature	July. 2015
1.0	Original	Apr. 2014

Content