SINO WEALTH

SH79E02

8051 Microcontroller with 10-bit ADC & 128 Bytes EEPROM

1. Features

- 8051 compatible Pipe-lined instruction based on the single-chip 8-bit micro-controller
- Flash ROM: 2K Bytes
- RAM: internal 128 Bytes
- EEPROM: 128 Bytes
- High Endurance FLASH/EEPROM Cell
  - 10,000 write FLASH endurance
  - 100,000 write EEPROM endurance
- Operating Voltage:
  - f_{OSC} = 30kHz - 4MHz，V_{DD} = 2.7V - 5.5V
  - f_{OSC} = 30kHz - 8MHz，V_{DD} = 4.5V - 5.5V
- Oscillator (code option):
  - Crystal oscillator: 32.768kHz
  - Crystal oscillator: 400kHz - 8MHz
  - Ceramic resonator: 400kHz - 8MHz
  - Internal RC oscillator: 8MHz
  - External clock: 400kHz - 8MHz
- 14 CMOS bi-directional I/O pins
- Built in pull-up resistor for input pin
- Two 16-bit timer/counters: Timer0, Timer1

Powerful Interrupt sources:
- Timer0, Timer1
- $\overline{INT0}$, $\overline{INT1}$
- ADC, EEPROM, CMP, SCM

- 10-bit 8-channel Analog Digital Converter (ADC)
- Analog Comparator module (CMP)
- Two High-performance Operational Amplifiers (selected by code option)
- Low voltage Reset (LVR) function (enabled by code option)
  - LVR voltage level 1: 4.0V
  - LVR voltage level 2: 2.6V
- CPU machine cycle: 1 oscillator clock
- Watchdog Timer (WDT)
- Warm-up Timer
- Oscillator Failure Detect function
- Support Low power operation modes:
  - Idle mode
  - Power-down mode
- Low power consumption
- Packages: DIP16, SOP16, TSSOP20

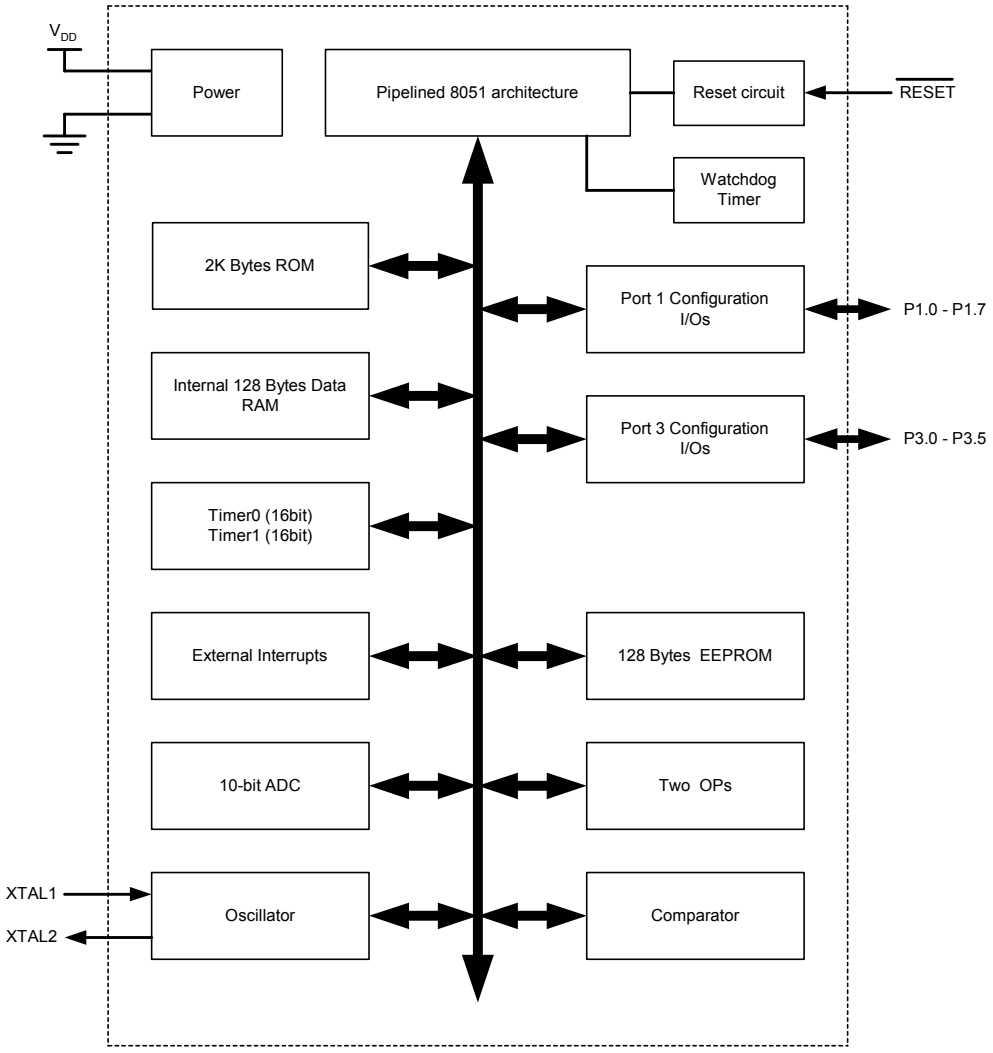
2. General Description

The SH79E02 is a fast 8051 compatible micro-controller with a redesigned CPU of no wasted clock and memory cycles. Typically, it will be faster and exhibit better performance than the traditional 8051 at the same oscillator frequency.

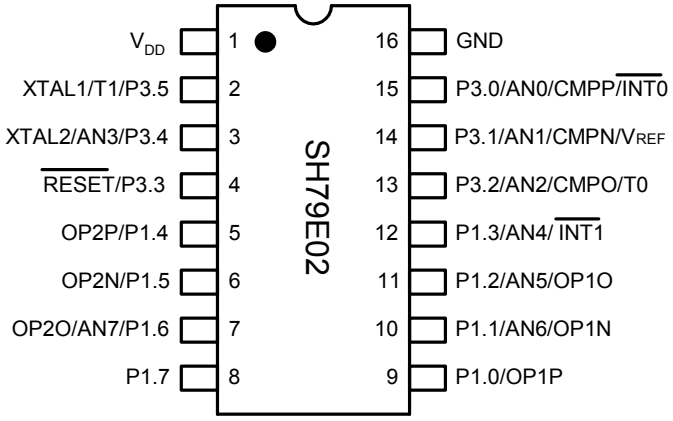
The SH79E02 retains most features of the standard 8051. These features include internal 128 bytes RAM and two 16-bit timer/counters, and external interrupts $\overline{INT0}$ & $\overline{INT1}$. It also contains 10-bit 8-channel ADC, an analog Comparator module (CMP), two high-performance Operational Amplifiers, 128 bytes EEPROM, and 2K bytes Flash memory block for program.

For high reliability and low cost issues, the SH79E02 builds in a Watchdog timer, a Warm-up timer, a Low-voltage Reset module, and a system clock monitoring module. And the SH79E02 also supports two power saving modes to reduce power consumption.

3. Block Diagram



4. Pin Configuration



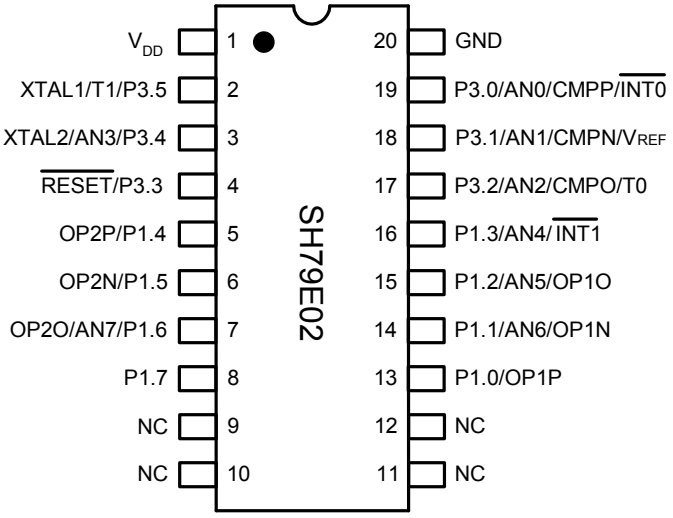


Table 4.1 Pin Functions

Pin No		Pin Name	Default Function
Pin 16	Pin 20		
1	1	V_{DD}	------
2	2	XTAL1/T1/P3.5	XTAL1 or P3.5, selected by code option
3	3	XTAL2/AN3/P3.4	XTAL2 or P3.4, selected by code option
4	4	$\overline{\text{RESET}}$/P3.3	$\overline{\text{RESET}}$ or P3.3, selected by code option
5	5	OP2P/P1.4	OP2P or P1.4, selected by code option
6	6	OP2N/P1.5	OP2N or P1.5, selected by code option
7	7	OP2O/AN7/P1.6	OP2O or P1.6, selected by code option
8	8	P1.7	P1.7
-	9	NC	NC
-	10	NC	NC
-	11	NC	NC
-	12	NC	NC
9	13	OP1P/P1.0	OP1P or P1.0, selected by code option
10	14	OP1N/AN6/P1.1	OP1N or P1.1, selected by code option
11	15	OP1O/AN5/P1.2	OP1O or P1.2, selected by code option
12	16	$\overline{\text{INT1}}$/AN4/P1.3	P1.3
13	17	T0/CMPO/AN2/P3.2	P3.2
14	18	V_{REF} /CMPN/AN1/P3.1	P3.1
15	19	$\overline{\text{INT0}}$/CMPP/AN0/P3.0	P3.0
16	20	GND	------

Note:

*The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to **Pin Configuration Diagram**). This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function use.*

5. Pin Description

Table 5.1 Pin Description

Pin	Type	Description
PORT		
P3.0 - P3.5	I/O	Bi-directional I/O port
P1.0 - P1.7	I/O	Bi-directional I/O port
Timer		
T0, T1	I	Timer0, Timer1 external input
ADC		
AN0 - AN7	I	ADC input channel
V_{REF}	I	ADC reference voltage
Comparator		
CMPP	I	Comparator positive input
CMPN	I	Comparator negative input
CMPO	O	Comparator output
OP		
OP1P, OP2P	I	Operational Amplifier positive input
OP1N, OP2N	I	Operational Amplifier negative input
OP1O, OP2O	O	Operational Amplifier output
Interrupt & Reset & Clock & Power		
$\overline{INT0}$, $\overline{INT1}$	I	External interrupt 0, 1
$\overline{RESET}$	I	A low level on this pin for 10μs or longer would reset the device
XTAL1	I	Oscillator input
XTAL2	O	Oscillator output
GND	P	Ground
V_{DD}	P	Power supply

Table 5.2 Programming Pin Description (Program Mode)

Pin No.		Symbol	I/O	Shared by	Description
16 Pin	20 Pin				
1	1	V_{DD}	P	V_{DD}	Programming power supply
16	20	GND	P	GND	Ground
14	18	TCK	I	V_{REF}/CMPN/AN1/P3.1	Programming clock input pin
15	19	TDI	I	$\overline{INT0}$/CMPP/AN0/P3.0	Programming data input pin
2	2	TDO	O	XTAL1/T1/P3.5	Programming data output pin
3	3	TMS	I	XTAL2/AN3/P3.4	Programming mode selecting pin

6. SFR Mapping

The SH79E02 provides 256 bytes of internal RAM to contain general-purpose data memory and Special Function Registers (SFRs). The SFRs of the SH79E02 fall into the following categories:

C51 Core Registers:	ACC, B, PSW, SP, DPL, DPH
Enhanced C51 Core Registers:	AUXC, DPL1, DPH1, INSCON
Power and Clock Control Registers:	PCON, SUSLO
Flash Registers:	IB_OFFSET, IB_DATA, IB_CON1, IB_CON2, IB_CON3, IB_CON4, IB_CON5
Data Memory Register:	XPAGE
Hardware Watchdog Timer Register:	RSTSTAT
System Clock Monitor Register:	CLKCON
Interrupt System Registers:	IEN0, IEN1, IPH0, IPL0, IPH1, IPL1
I/O Port Registers:	P1, P3, P1CR, P3CR, P1PCR, P3PCR
Timer Registers:	TCON, TH0, TH1, TMOD, TL0, TL1, TCON1
ADC Registers:	ADCON, ADT, ADCH, ADDL, ADDH
EEPROM Register:	EECON
Comparator Register:	CMPCON
OP Register:	OPCON

Table 6.1 C51 Core SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	----00-0	-	-	-	-	DIV	MUL	-	DPS

Table 6.2 Power and clock control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	----0000	-	-	-	-	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 6.3 Flash control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFF SET	FBH	Low offset address of the Flash programming byte	---00000	-	-	-	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
IB_DATA	FCH	Data Register for Programming Flash Memory	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1	F2H	Flash Memory Control Register 1	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2	F3H	Flash Memory Control Register 2	----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3	F4H	Flash Memory Control Register 3	----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4	F5H	Flash Memory Control Register 4	----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5	F6H	Flash Memory Control Register 5	----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0

Table 6.4 Data MPAGE SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	F7H	Memory Page	--000000	-	-	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0

Table 6.5 WDT SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H	Watchdog Timer Control	*-***000	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

Note: ** RSTSTAT initial value is determined by different RESET.*

Table 6.6 CLKCON SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	B2H	System Clock Control Register	01100000	RCPS	CLKPS1	CLKPS0	SCMIF	RCON	OXS	LPCON	32K_SPDUP

Table 6.7 Interrupt SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H	Interrupt Enable Control 0	00--0000	EA	EADC	-	-	ET1	EX1	ET0	EX0
IEN1	A9H	Interrupt Enable Control 1	---0-00-	-	-	-	ESCM	-	EEIE	CMPIE	-
IPL0	B8H	Interrupt Priority Control Low 0	-0--0000	-	PADCL	-	-	PT1L	PX1L	PT0L	PX0L
IPH0	B4H	Interrupt Priority Control High 0	-0--0000	-	PADCH	-	-	PT1H	PX1H	PT0H	PX0H
IPL1	B9H	Interrupt Priority Control Low 1	---000--	-	-	-	PSCML	PCMPL	PEEL	-	-
IPH1	B5H	Interrupt Priority Control High 1	---000--	-	-	-	PSCMH	PCMPH	PEEH	-	-

Table 6.8 Port SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1	90H	8-bit Port 1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P3	B0H	8-bit Port 3	--000000	-	-	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P1CR	E2H	Port1 input/output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P3CR	E4H	Port3 input/output direction control	--000000	-	-	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P1PCR	EAH	Internal pull-high enable for Port1	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P3PCR	ECH	Internal pull-high enable for Port3	--000000	-	-	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0

Table 6.9 Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	88H	Timer/Counter 0 and 1 Control	00000000	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89H	Timer/Counter 0 and 1 Modes	00000000	GATE1	C/$\overline{T1}$	M11	M10	GATE0	C/$\overline{T0}$	M01	M00
TL0	8AH	Timer/Counter 0 Low Byte	00000000	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
TH0	8CH	Timer/Counter 0 High Byte	00000000	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
TL1	8BH	Timer/Counter 1 Low Byte	00000000	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.1
TH1	8DH	Timer/Counter 1 High Byte	00000000	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.1
TCON1	CEH	Timer0 and Timer1 Clock Source	-00-----	-	TCLKS1	TCLKS0	-	-	-	-	-

Table 6.10 ADC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	93H	ADC Control	00000000	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	GO/$\overline{DONE}$
ADT	94H	ADC Time Configuration	000-0000	TADC2	TADC1	TADC0	-	TS3	TS2	TS1	TS0
ADCH	95H	ADC Channel Configuration	00000000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
ADDL	96H	ADC Data Low Byte	------00	-	-	-	-	-	-	A1	A0
ADDH	97H	ADC Data High Byte	00000000	A9	A8	A7	A6	A5	A4	A3	A2

Table 6.11 OP SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPCON	91H	OP Control	------00	-	-	-	-	-	-	OP2PC	OP1PC

Table 6.12 CMPCON SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON	92H	Comparator Control	0---0000	CMPIF	-	-	-	CMPEN	CMPOC	CINV	COUT

Table 6.13 EEPROM SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON	C0H	EEPROM Control	00000000	EEPC	EEIF	EWSC	EEPM	WRERR	EEWE	EEWR	EERD

Note: *-: unimplemented, keep the value of the latest read operation result*

SFR Map

	Bit addressable	Non Bit addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8h				IB_OFFSET	IB_DATA				FFh
F0h	B	C	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7h
E8h			P1PCR		P3PCR				EFh
E0h	ACC		P1CR		P3CR				E7h
D8h									DFh
D0h	PSW								D7h
C8h							TCON1		CFh
C0h	EECON								C7h
B8h	IPL0	IPL1							BFh
B0h	P3	RSTSTAT	CLKCON		IPH0	IPH1			B7h
A8h	IEN0	IEN1							AFh
A0h									A7h
98h									9Fh
90h	P1	OPCON	CMPCON	ADCON	ADT	ADCH	ADDL	ADDH	97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1	SUSLO		8Fh
80h		SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87h
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

Note: *The unused addresses of SFR are not available.*

7. Normal Function

7.1 CPU

7.1.1 CPU Core SFRs

Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET,RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Table 7.1 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	C	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	C	**Carry flag bit** 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	AC	**Auxiliary Carry flag bit** 0: an auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	F0	**F0 flag bit** Available to the user for general purposes
4-3	RS[1:0]	**R0-R7 Register bank select bits** 00: Bank 0 (Address to 00H-07H) 01: Bank 1 (Address to 08H-0FH) 10: Bank 2 (Address to 10H-17H) 11: Bank 3 (Address to 18H-1FH)
2	OV	**Overflow flag bit** 0: no overflow happen 1: an overflow happen
1	F1	**F1 flag bit** Available to the user for general purposes
0	P	**Parity flag bit** 0: an even number of “one" bits in the Accumulator 1: an odd number of “one" bits in the Accumulator

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

7.1.2 Enhanced CPU core SFRs

Feature

- Extended 'MUL' and 'DIV' instructions: 16bit*8bit, 16bit/8bit
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH79E02 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8 bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16 bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8 bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16 bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is the same with DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

Register

Table 7.2 Data Pointer Select Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	-	-	-	-	DIV	MUL	-	DPS
R/W	-	-	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	-	0

Bit Number	Bit Mnemonic	Description
3	DIV	**16 bit/8 bit Divide Selection Bit** 0: 8 bit Divide 1: 16 bit Divide
2	MUL	**16 bit/8 bit Multiply Selection Bit** 0: 8 bit Multiply 1: 16 bit Multiply
0	DPS	**Data Pointer Selection Bit** 0: Data pointer 1: Data pointer 1

7.2 RAM

The SH79E02 provides internal RAM for random data storage. The 128 bytes of RAM (addresses 00h to 7Fh) are directly and indirectly addressable. The Special Function Registers (SFR, addresses 80h to FFh) are directly addressable only.

Note: *The unused address is unavailable in SFR.*

7.3 Flash Program Memory

7.3.1 Feature

- The program memory consists 4 X 512B sectors, total 2KB
- Programming and erase can be done over the full operation voltage range
- Write, read and erase operation are all supported by In-Circuit Programming (ICP)
- Fast mass/sector erase and programming
- Minimum program/erase cycles: 10000
- Minimum years data retention: 10
- Low power consumption

The SH79E02 embeds 2K flash program memory for program code. The flash program memory provides electrical erasure and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode.

Note*: The last 64bytes (0x7FC0-0x7FFF) are reserved, can't be used as program memory.*

In ICP mode, the programmer can do all the operations to flash memory, such as erase or write. The read or write operation of flash memory is done by byte, but the erase operation is done by sectors or whole chip.

In ICP mode, the sector erase operation can erase any flash sector except the sector 3. In SSP mode, the sector erase function can erase any flash sector except the sector 3 and the sector that contains SSP code.

The mass-erase operation only support in ICP mode and this operation will erase the entire program memory including sector 3.

7.3.2 Flash Operation in ICP Mode

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 wires (VDD, GND, TCK, TDI, TMS, TDO).

At first the 4 JTAG pins (TDO, TDI, TCK, TMS) are used to enter the programming mode. Only after the 4 pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the **FLASH Programmer's user guide**.

The ICP mode supports the following operations:

(1) Code-Protect Control mode Programming

SH79E02 implements code-protect function to offer high safeguard for customer code. Two modes are available for each sector.

Code-protect control mode 0: Used to enable/disable the write/read operation (except mass erase) from any programmer.

Code-protect control mode 1: Used to enable/disable the read operation through MOVC instruction from other sectors; or the sector erase/write operation through **SSP** Function

To enable the wanted protect mode, the user must use the **Flash Programmer** to set the corresponding protect bit.

(2) Mass Erase

The mass erase operation will erase all the contents of program code, code option, code protect bit and customer code ID, regardless the status of code-protect control mode. (The Flash Programmer supplies customer code ID setting function for customer to distinguish their product.)

Mass erase is only available in Flash Programmer.

(3) Sector Erase

The sector erase operation will erase the contents of program code of selected sector. This operation can be done by Flash Programmer or by the user's program.

If done by the user's program, the code-protect control mode 1 of the selected sector must be disabled.

If done by the Flash Programmer, the code-protect control mode 0 of the selected sector must be disabled.

Note: *The last sector (Sector 3) cannot be erased by sector erase. The sector itself in which SSP program located cannot be erased by user's program sector erase.*

(4) Write/Read Code

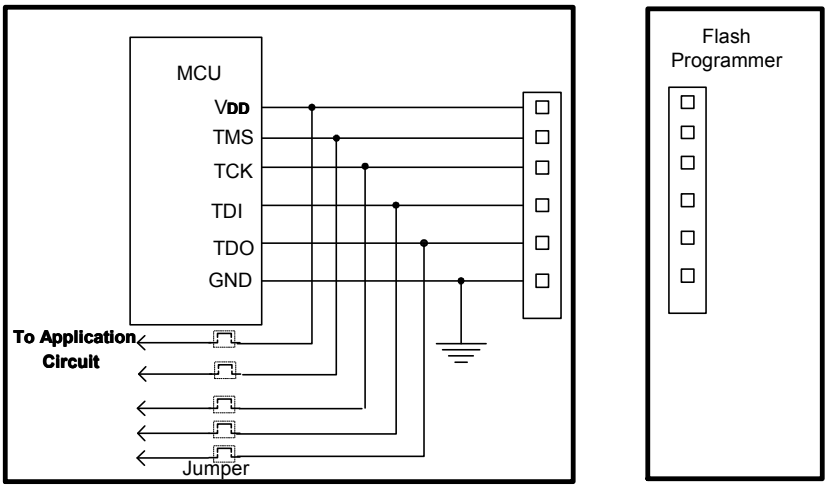
The Write/Read Code operation will write the customer code into the Flash Programming Memory or read the customer code from the Flash Programming Memory. This operation can be done by Flash Programmer or the user's program.

If done by the user's program, the code-protect control mode 1 of the selected sector must be disabled. But the program can read/write its own sector regardless of its security bit.

If done by the Flash Programmer, the code-protect control mode 0 of the selected sector must be disabled.

Operation	ICP	SSP
Code Protection	Yes	No
Sector Erase	Yes (without security bit)	Yes (without security bit)
Mass Erase	Yes	No
Write/Read	Yes (without security bit)	Yes (without security bit or its own sector)

In ICP mode，all the flash operations are completed by the programmer through 6-wire interface. Since the program timing is very sensitive, 6 jumpers are needed (V_{DD}, GND, TCK, TDI, TMS, TDO) to separate the program pins from the application circuit as the following diagram.



The recommended steps are as following:

(1) The jumpers must be open to separate the programming pins from the application circuit before programming;
(2) Connect the programming interface with programmer and begin programming;
(3) Disconnect programmer and short these jumpers after programming is complete.

7.4 SSP Function

The SH79E02 provides SSP (Self Sector Programming) function, each sector can be sector erased or programmed by the user's code if the selected sector is not being protected.

The SH79E02 build in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON2-5), the SSP will be terminated.

See **Flash control flow** for more information.

7.4.1 Register

Table 7.3 Offset Register for Programming

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	-	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
5-4	**XPAGE[5:4]**	Sector of the flash memory to be programmed, 00---means sector 0, and so on
3-0	**XPAGE[3:0]**	High Address of Offset of the flash memory sector to be programmed

Table 7.4 Offset of Flash Memory for Programming

FBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	-	-	-	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
4-0	**IB_OFFSET[4:0]**	Low Address of Offset of the flash memory sector to be programmed

Table 7.5 Data Register for Programming

FCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_DATA[7:0]**	Data to be programmed

Table 7.6 SSP Type Select Register

F2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_CON1[7:0]**	**SSP Type select** 0xE6: Sector Erase 0x6E: Sector Programming

Table 7.7 SSP Flow Control Register 1

F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON2[3:0]**	Must be 05H, or else Flash Programming will terminate

Table 7.8 SSP Flow Control Register 2

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON3[3:0]**	Must be 0AH, or else Flash Programming will terminate

Table 7.9 SSP Flow Control Register 3

F5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

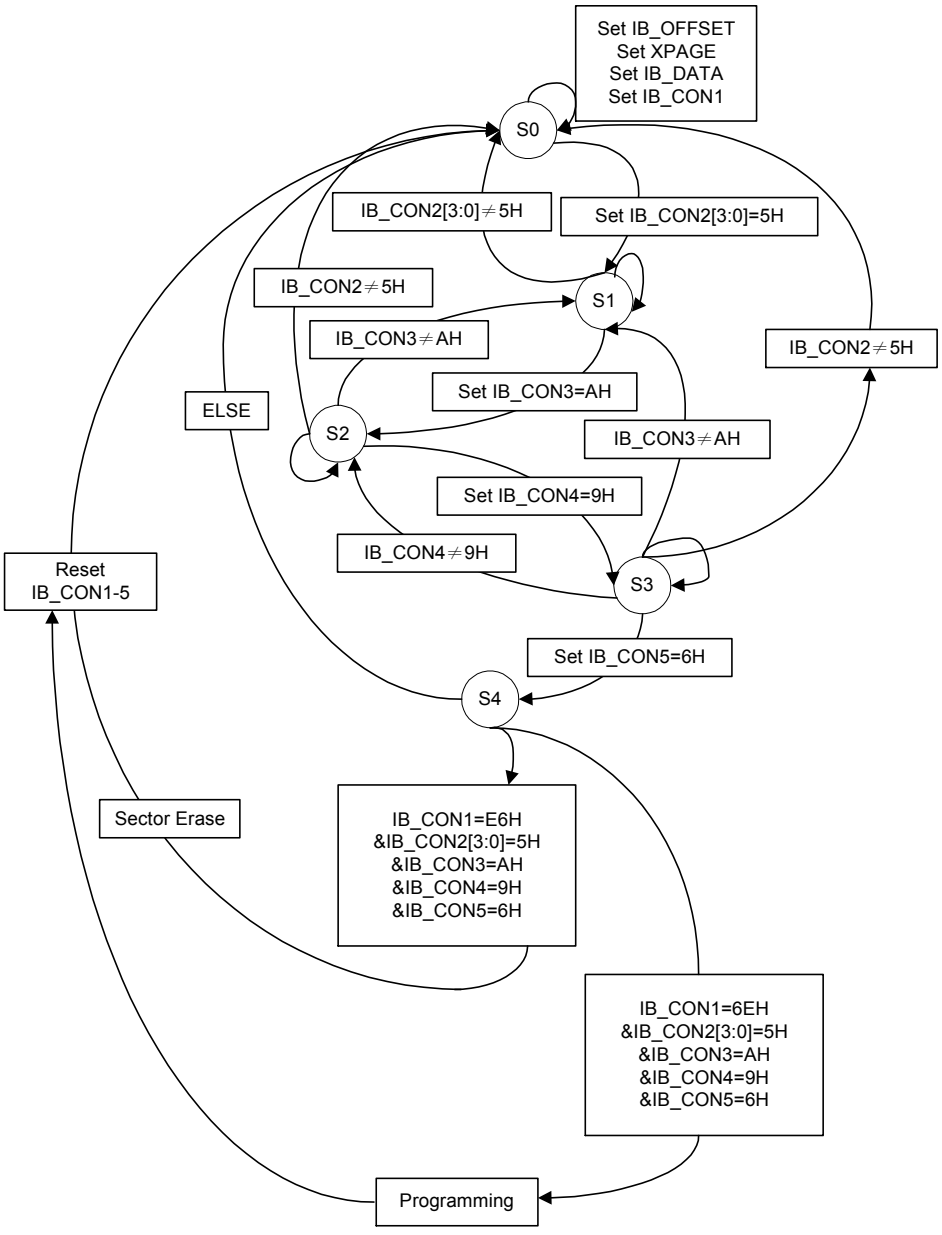
Bit Number	Bit Mnemonic	Description
3-0	**IB_CON4[3:0]**	Must be 09H, or else Flash Programming will terminate

Table 7.10 SSP Flow Control Register 4

F6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON5[3:0]**	Must be 06H, or else Flash Programming will terminate

7.4.2 Flash Control Flow



7.4.3 SSP Programming Notice

To successfully complete SSP programming, the user's software must follow the steps below:

(1) For Code/Data Programming:

1. Disable interrupt;
2. EWSC = 0;
3. Fill in the XPAGE, IB_OFFSET for the corresponding sector;
4. Fill in IB_DATA if programming is wanted;
5. Fill in IB_CON1-5 sequentially;
6. Add 4 nops for more stable operation;
7. Code/Data programming: CPU will be in IDLE mode;
8. Go to Step 3 if more data are to be programmed in the successive address of same sector;
9. Clear XPAGE and enable interrupt.

(2) Sector Erase:

1. Disable interrupt;
2. EWSC = 0;
3. Fill in the XPAGE for the corresponding sector;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Sector Erase, CPU will be in IDLE mode;
7. Go to step 3 for more sectors;
8. Clear XPAGE and enable interrupt.

(3) For Code Reading:

Just Use "MOVC A, @A+DPTR" or "MOVC A, @A+PC".

7.5 System Clock and Oscillator

7.5.1 Feature

- Five oscillator types: 32.768kHz crystal, crystal oscillator, ceramic resonator, external clock and Internal 8M RC
- Built-in 8MHz RC
- Built-in 32.768kHz speed up circuit
- Built-in system clock prescaler

7.5.2 Clock Definition

The SH79E02 has several internal clocks defined as below:

OSCCLK: the oscillator clock from one of the five oscillator types (32.768kHz crystal, crystal oscillator, ceramic resonator, external clock at XTAL1 pin or Internal 8M RC). f_{OSC} is defined as the OSCCLK frequency. t_{OSC} is defined as the OSCCLK period.

RCCLK: Internal 8M RC clock. f_{RC} is defined as the RCCLK frequency. t_{RC} is defined as the RCCLK period.

WDTCLK: the internal 32kHz WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK period.

OSCSCLK: the input of system clock prescaler. It can be OSCCLK. f_{OSCS} is defined as the OSCSCLK frequency. t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output of system clock prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency. t_{SYS} is defined as the SYSCLK period.

The SH79E02 has two clock sources. One is crystal oscillator or ceramic resonator; the other is built-in RC. Clock source is determined by code option. The oscillator generates the basic clock pulses that provide the system clock for the CPU and on-chip peripherals.

7.5.3 Register

Table 7.11 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	RCPS	CLKPS1	CLKPS0	SCMIF	RCON*	OXS*	LPCON	32K_SPDUP
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	1	1	0	0	0	0	1

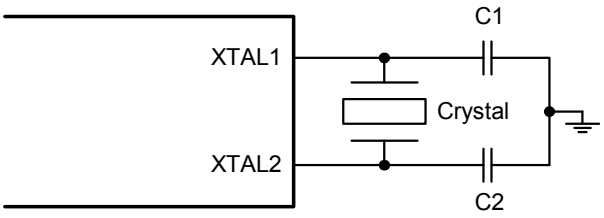
Bit Number	Bit Mnemonic	Description
7	**RCPS**	**Prescaler from internal RC** 0: $f_{OSCS} = f_{RC}$ 1: $f_{OSCS} = f_{RC}/2$
6-5	**CLKPS[1:0]**	**SYSCLK Prescaler Register** 00: $f_{SYS} = f_{OSCS}$ 01: $f_{SYS} = f_{OSCS}/2$ 10: $f_{SYS} = f_{OSCS}/4$ 11: $f_{SYS} = f_{OSCS}/12$ If 32.768kHz oscillator is selected as OSCSCLK, these control bits are invalid.
4	**SCMIF**	**System Clock Monitor**
3	**RCON**	**Internal RC turn on/off** 0: Turn off internal RC (default) 1: Turn on internal RC Only when code option OP_OSC is 011, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)
2	**OXS**	**Switching system clock** 0: Select 32.768kHz crystal oscillator as **OSCSCLK** (determined by code option) 1: Select internal RC as **OSCSCLK** Only when code option OP_OSC is 011, this bit is valid. (32.768kHz oscillator is selected. Refer to **code option** section for details)
1	**LPCON**	**Low power mode control bit** 0: turn off Low power mode 1: turn on Low power mode This bit is available when 32.768kHz Oscillator or 455kHz ceramic is selected as system clock. If this mode is turned on in other state, the system will trap in unknown mistake!
0	**32K_SPDUP**	**32.768kHz oscillator speed up mode control bit** 0: 32.768kHz oscillator normal mode, cleared by software 1: 32.768kHz oscillator speed up mode, set by hardware or software This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. And this bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when Power-down mode wakes up. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption. Only when code option OP_OSC is 011, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)

Notes:

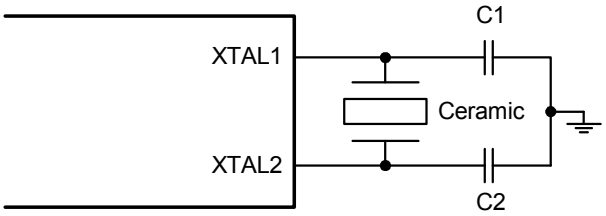
1. When system clock changed from 32.768kHz crystal oscillator to internal RC, the steps below must be done in sequence:
   a. Set RCON = 1 to turn on internal RC
   *b. Wait at least Oscillator Warm-up time (see **Oscillator Warm-up time**)*
   c. Set OXS = 1 to select internal RC as system clock
2. When system clock changed from internal RC to32.768kHz crystal oscillator, the steps below must be done in sequence:
   a. Set OXS = 0 to select 32.768kHz crystal oscillator
   b. Set RCON = 0 to turn off internal RC

7.5.4 Oscillator Type

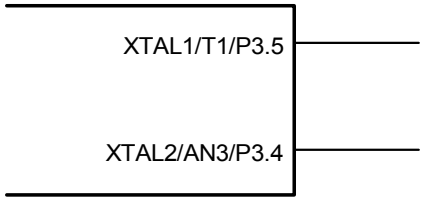
(1) Crystal oscillator: 32.768kHz or 400kHz - 8MHz



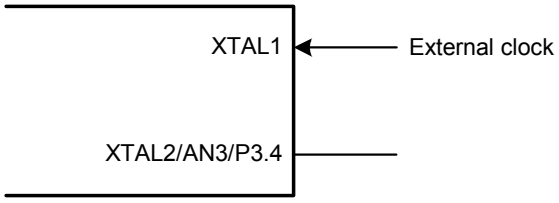
(2) Ceramic resonator: 455kHz



(3) Internal RC: 8MHz



(4) External clock: 400kHz - 8MHz



7.5.5 Capacitor selection for oscillator

Ceramic Resonator		
Frequency	**C1**	**C2**
455kHz	47 - 100pF	47 - 100pF

Crystal Oscillator		
Frequency	**C1**	**C2**
32.768kHz	5-12.5pF	5-12.5pF
4MHz	8-15pF	8-15pF
8MHz	8-15pF	8-15pF

Notes:

Capacitor values are used for design guidance only!

These capacitors were tested with the crystals listed above for basic start-up and operation. They are not optimized.
Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.
Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for recommended manufactures.

7.5.6 System Clock Monitor (SCM)

In order to enhance the system reliability, the SH79E02 contains a system clock monitor (SCM) module. If the system clock fails (for example the oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal 32k WDTCLK and set system clock monitor bit (SCMIF) to 1. And the SCM interrupt will be generated when EA and ESCM is enabled. If the oscillator comes back, SCM will switch the OSCCLK back to the oscillator and clears the SCMIF automatically.

Notes:

The SCMIF is read only register; it can be cleared to 0 or set to 1 by hardware only.
If SCMIF is cleared, the SCM switches the system clock to the state before system clock fail automatically.
If Internal RC is selected as OSCCLK by code option (Refer to code option section for detail), the SCM would not work.

Table 7.12 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	-	-	-	SCMIF	-	-	-	-
R/W	-	-	-	R	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
4	**SCMIF**	**System Clock Monitor bit** 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails

7.6 I/O Port

7.6.1 Feature

- 14 bi-directional I/O ports
- Share with alternative functions

The SH79E02 has 14 CMOS bi-directional I/O ports. The PORT data is put in P1, P3 register. The PORT control register (P1CR, P3CR) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by P1PCR, P3PCR when the PORT is used as input.

For SH79E02, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions be conflict when all the functions are enabled.

7.6.2 Register

Table 7.13 Port Control Register

E2H, E4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1CR (E2H)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P3CR (E4H)	-	-	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxCRy** **x = 1, y = 0-7;** **x = 3, y = 0-5**	**Port input/output direction control Register** 0: input mode 1: output mode

Table 7.14 Port Pull up Resistor Control Register

EAH, ECH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1PCR (EAH)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P3PCR (ECH)	-	-	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

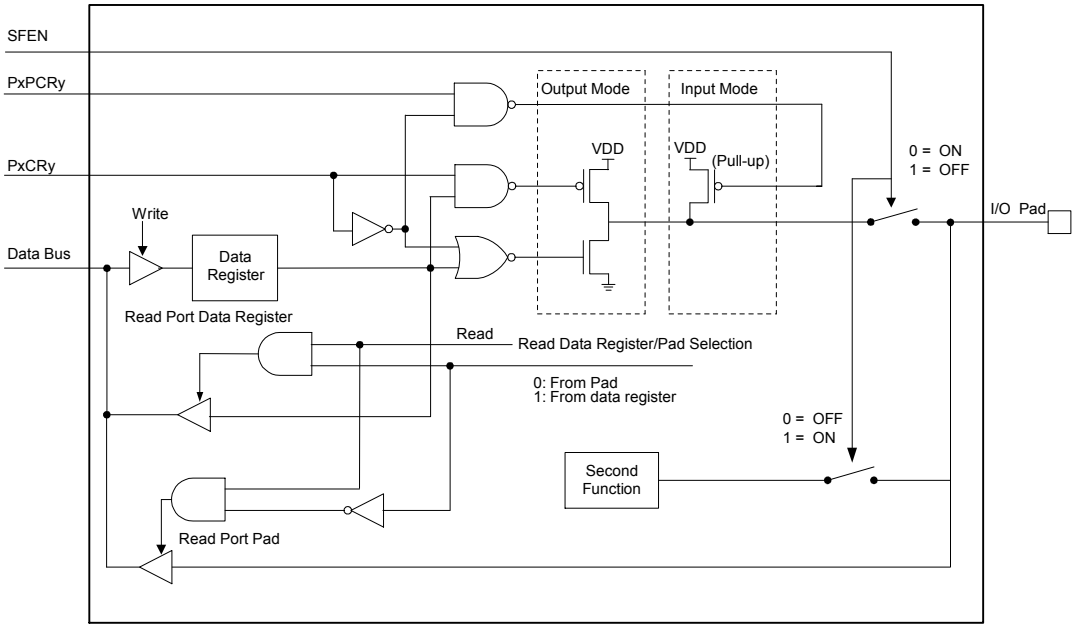
Bit Number	Bit Mnemonic	Description
7-0	**PxPCRy** **x = 1, y = 0-7;** **x = 3, y = 0-5**	**Input Port internal pull-high resistor enable/disable control** 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled

Table 7.15 Port Data Register

90H, B0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1 (90H)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P3 (B0H)	-	-	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**Px.y** **x = 1, y = 0-7;** **x = 3, y = 0-5**	Port Data Register

7.6.3 Port Diagram



Note:

(1) The input source of reading input port operation is from the input pin directly.
(2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly. The read Instruction distinguishes which path is selected: The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.
(3) The destination of writing port operation is the data register regardless the port shared as the second function or not.

7.6.4 Port Share

The 14 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Most Inner Lest** rule:

The out most pin function in Pin Configuration has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin , even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 1, 3), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register while the port pin keeps unchanged until all the share functions are disabled.

PORT1:

Table 7.16 Port1 Share Table

Pin No.	Priority	Function	Enable bit
9	1	OP1P	Code option: OP1 enable
	2	P1.0	Above condition is not met
10	1	OP1N	Code option: OP1 enable
	2	AN6	Set ADCH.6 bit in ADCH Register, SCH [2:0] = 110 in ADCON Register
	3	P1.1	Above condition is not met
11	1	OP1O	Code option: OP1 enable
	2	AN5	Set ADCH.5 bit in ADCH Register, SCH [2:0] = 101 in ADCON Register
	3	P1.2	Above condition is not met
12	1	INT1	Set EX1 bit in IEN0 Register, P1.3 in input mode
	2	AN4	Set ADCH.4 bit in ADCH Register, SCH [2:0] = 100 in ADCON Register
	3	P1.3	Above condition is not met
5	1	OP2P	Code option: OP2 enable
	2	P1.4	Above condition is not met
6	1	OP2N	Code option: OP2 enable
	2	P1.5	Above condition is not met
7	1	OP2O	Code option: OP2 enable
	2	AN7	Set ADCH.7 bit in ADCH Register, SCH [2:0] = 111 in ADCON Register
	3	P1.6	Above condition is not met
8	1	P1.7	

PORT3:

Table 7.17 Port3 Share Table

Pin No.	Priority	Function	Enable bit
15	1	INT0	Set EX0 bit in IEN0 Register, P3.0 in input mode
	2	CMPP	Set CMPEN bit in CMPCON Register
	3	AN0	Set ADCH.0 bit in ADCH Register, SCH [2:0] = 000 in ADCON Register
	4	P3.0	Above condition is not met
14	1	Vref	Set REFC bit in ADCON Register
	2	CMPN	Set CMPEN bit in CMPCON Register
	3	AN1	Set ADCH.1 bit in ADCH Register, SCH [2:0] = 001 in ADCON Register
	4	P3.1	Above condition is not met
13	1	T0	Set TR0 bit in TCON Register and C/T0 bit in TMOD Register
	2	CMPO	Set CMPEN and CMPOC bit in CMPCON Register
	3	AN2	Set ADCH.2 bit in ADCH Register, SCH [2:0] = 010 in ADCON Register
	4	P3.2	Above condition is not met
4	1	RESET	Code option: RESET pin enable
	2	P3.3	Above condition is not met
3	1	XTAL2	Code option: OP_OSC[2:0]=011, 101 or 110
	2	AN3	Set ADCH.3 bit in ADCH Register, SCH [2:0] = 011 in ADCON Register
	3	P3.4	Above condition is not met
2	1	XTAL1	Code option: OP_OSC[2:0]=010, 011, 101 or 110
	2	T1	Set TR1 bit in TCON Register and C/T1 bit in TMOD Register
	3	P3.5	Above condition is not met

7.7 Timer

7.7.1 Feature

- The SH79E02 has 2 Timers (Timer 0, 1)
- Timer 0 is compatible with the standard 8051
- Timer 1 is compatible with the standard 8051
- Timer0/1 clock source selectable

7.7.2 Timer 0, 1

Each timer is implemented as a 16-bit register accessed as two cascaded Timer x/ Counter x Data Registers: THx & TLx (x = 0, 1). They are controlled by the register TCON and TMOD. The Timer 0 & Timer 1 interrupts can be enabled by setting the ET0 & ET1 bit in the IEN0 register (Refer to **Interrupt** Section for details).

Timer 0 & Timer 1 Mode

Both timers operate in one of four primary modes selected by the Mode Select bits Mx1-Mx0 (x = 0, 1) in the Counter/Timer Mode register (TMOD).

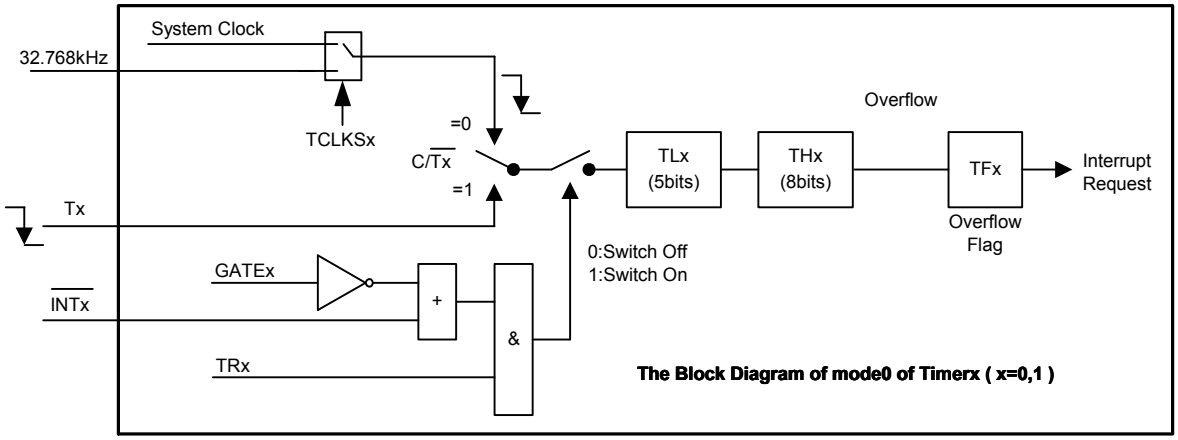
Mode 0: 13-bit Counter/Timer

Timer x operate as 13-bit counter/timers in Mode 0. The THx register holds the high eight bits of the 13-bit counter/timer, TLx holds the five low bits TLx.4-TLx.0. The three upper bits of TLx (TLx.7-TLx.5) are indeterminate and should be ignored when reading. As the 13-bit timer register increments and overflows, the timer overflow flag TFx is set and an interrupt will occur if Timer interrupts is enabled. The C/$\overline{T}$x bit selects the counter/timer's clock source.

If C/$\overline{T}$x = 1, high-to-low transitions at the Timer input pin (Tx) will increase the timer/Counter 0 Data register. Else if C/$\overline{T}$x = 0, selects the system clock to increase the timer/Counter Data register.

Setting the TRx bit enables the timer when either GATEx = 0, or GATEx = 1 and the input signal $\overline{INT}$x is active. Setting GATEx to '1' allows the timer to be controlled by the external input signal $\overline{INT}$x, facilitating positive pulse width in $\overline{INT}$x measurements. Setting TRx does not force the timer to reset. This means that if TRx is set, the timer register will count from the old value that was last stopped by clearing TRx. So the timer registers should be loaded with the desired initial value before the timer is enabled.

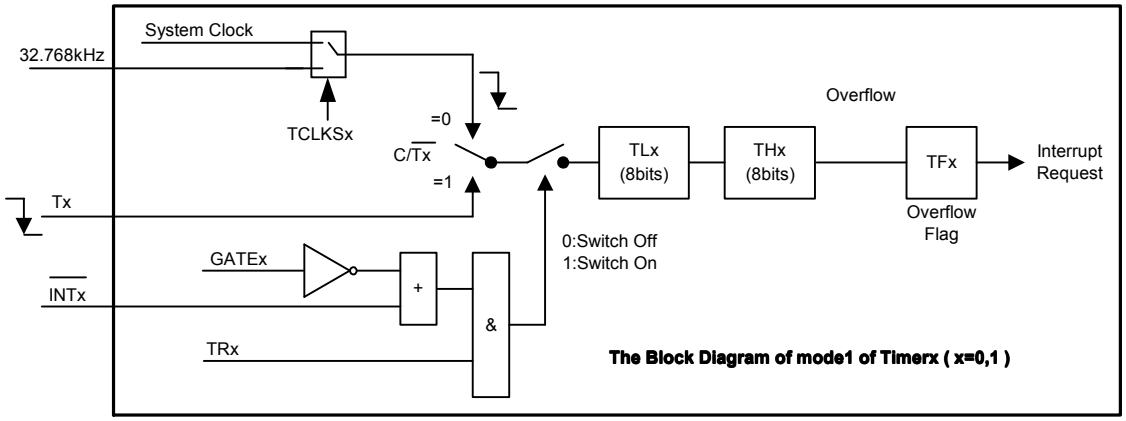
When as Timer, system clock or 32.768KHz can be selected as Timer x (x = 0, 1) clock source by configuring TCLKSx (x = 0, 1) in TCON1 Register. TCLKSx (x = 0, 1) are valid only when 32.768kHz Crystal oscillator is selected by code option. When 32.768kHz is selected as system clock and TCLKSx (x = 0, 1) is set "1", Timer x (x = 0, 1) can't count.



The Block Diagram of mode0 of Timerx (x=0,1)

Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

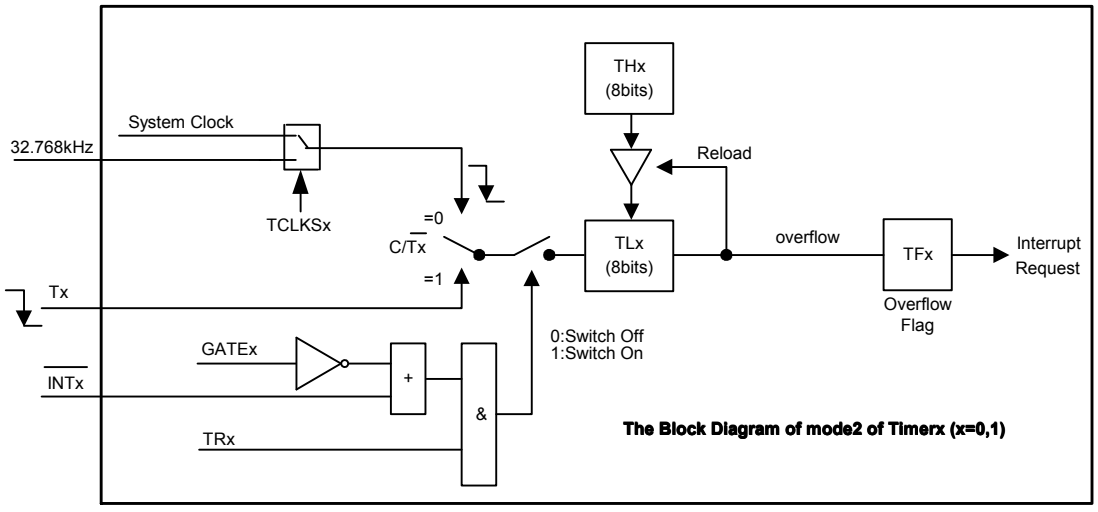


Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timerx to operate as 8-bit counter/timers with automatic reload of the start value. TLx holds the count and THx holds the reload value. When the counter in TLx overflows from all ones to 0x00, the timer overflow flag TFx is set and the counter in TLx is reloaded from THx. If Timer x interrupts are enabled, an interrupt will occur when the TFx flag is set. The reload value in THx is not changed. TLx must be initialized to the desired value before enabling the timer for the first count to be correct.

Except the Auto-Reload function, both counter / timers are enabled and configured in Mode 2 is the same as in Mode 0 & Mode 1.

When as Timer, system clock or 32.768KHz can be selected as Timer x (x = 0, 1) clock source by configuring TCLKSx (x = 0, 1) in TCON1 Register. TCLKSx (x = 0, 1) are valid only when 32.768kHz Crystal oscillator is selected by code option. When 32.768kHz is selected as system clock and TCLKSx (x = 0, 1) is set “1”, Timer x (x = 0, 1) can’t count.



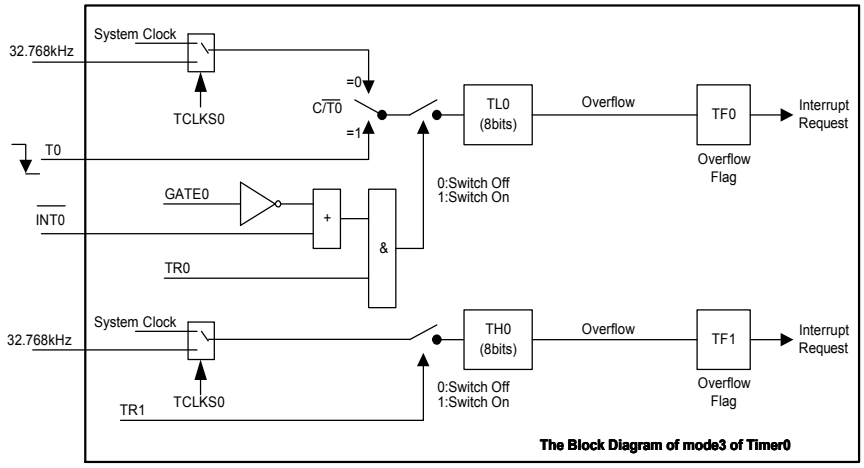
Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/$\overline{T0}$, GATE0 and TF0. TL0 can use either the system clock or 32.768kHz or an external input signal as its time base.

The TH0 is restricted to a timer function sourced by the system clock. TH0 is enabled using the Timer 1 control bit TR1. TH1 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

When timer 0 is operating in Mode 3, timer 1 can be operated in modes 0, 1 or 2, but it cannot set the TF1 flag and generate an interrupt. The Timer 1 overflow can generate baud-rates for the EUART. The TH1 and TL1 register is restricted to a timer function sourced by the system clock, and gate1 is invalid. And the pull high resistor of T1 input pin is also disabled. Timer 1 run control is handled through its mode settings, because TR1 is used by Time 0. When the timer 1 is in mode 0, 1, or 2, timer 1 is enable. When the timer 1 is in mode 3, timer 1 is disable.

When as Timer, system clock or 32.768KHz can be selected as Timer0 clock source by configuring TCLKS0 in TCON1 Register. TCLKS0 are valid only when 32.768kHz Crystal oscillator is selected by code option. When 32.768kHz is selected as system clock and TCLKS0 is set “1”, Timer0 can’t count.



The Block Diagram of mode3 of Timer0

7.7.3 Registers

Table 7.18 Timer/Counter x Control register (x = 0, 1)

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 5	**TFx** **x = 0, 1**	**Timer x overflow flag** 0: Timer x no overflow, can be cleared by software 1: Timer x overflow, set by hardware; set by software will cause a timer interrupt
6, 4	**TRx** **x = 0, 1**	**Timer x start, stop control bits** 0: Stop Timer x 1: Start Timer x
3, 1	**IEx** **x = 0, 1**	**External interrupt x request flag**
2, 0	**ITx** **x = 0, 1**	**External interrupt x trigger mode select bits**

Table 7.19 Timer/Counter x Mode register (x = 0, 1)

89H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMOD	GATE1	C/$\overline{T1}$	M11	M10	GATE0	C/$\overline{T0}$	M01	M00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 3	**GATEx x = 0, 1**	**Timer x Gate Control bits** 0: Timer x is enabled whenever TRx control bit is set 1: Timer x is enabled only while INTx pin is high and TRx control bit is set
6, 2	**C/$\overline{Tx}$ x = 0, 1**	**Timer x Timer / Counter mode selected bits** 0: Timer Mode 1: Counter Mode
5-4 1-0	**Mx[1:0] x = 0, 1**	**Timer x Timer mode selected bits** 00: Mode 0, 13-bit up counter/timer, bit7-5 of TLx is ignored 01: Mode 1, 16-bit up counter/timer 10: Mode 2, 8-bit auto-reload up counter/timer 11: Mode 3 (only for Timer0), two 8-bit up timer

Table 7.20 Timer/Counter x Data Register (x = 0, 1)

8AH - 8DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL0 (8AH)	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
TH0 (8CH)	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
TL1 (8BH)	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
TH1 (8DH)	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TLx.y, THx.y x = 0-1, y = 0-7**	Timer x Low & High byte counter

Table 7.21 Timer/Counter x Control register1 (x = 0, 1)

CEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON1	-	TCLKS1	TCLKS0	-	-	-	-	-
R/W	-	R/W	R/W	-	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	0	0	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
6-5	**TCLKSx x = 0, 1**	**Timer x Clock Source Control bits** 0: Select system clock as Timer x Clock Source 1: Select 32.768kHz as Timer x Clock Source

Note: *TCLKS0 and TCLKS1 are valid only when 32.768kHz crystal oscillator is selected as the system clock by code option.*

7.8 Interrupt

7.8.1 Feature

- 8 interrupt sources
- 4 interrupt priority levels

The SH79E02 provides total 8 interrupt sources: two external interrupts (INT0, INT1), two timer interrupts (timer 0, 1), ADC Interrupt, Comparator Interrupt, EEPROM interrupt and SCM interrupt.

7.8.2 Interrupt Enable

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

Table 7.22 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC	-	-	ET1	EX1	ET0	EX0
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**EA**	**All interrupt enable bit** 0: Disable all interrupt 1: Enable all interrupt
6	**EADC**	**ADC interrupt enable bit** 0: Disable ADC interrupt 1: Enable ADC interrupt
3	**ET1**	**Timer1 overflow interrupt enable bit** 0: Disable timer 1 overflow interrupt 1: Enable timer 1 overflow interrupt
2	**EX1**	**External interrupt 1 enable bit** 0: Disable external interrupt 1 1: Enable external interrupt 1
1	**ET0**	**Timer0 overflow interrupt enable bit** 0: Disable timer 0 overflow interrupt 1: Enable timer 0 overflow interrupt
0	**EX0**	**External interrupt 0 enable bit** 0: Disable external interrupt 0 1: Enable external interrupt 0

Table 7.23 Secondary Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	-	-	-	ESCM	-	EEIE	CMPIE	-
R/W	-	-	-	R/W	-	R/W	R/W	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	-	0	0	-

Bit Number	Bit Mnemonic	Description
4	**ESCM**	**SCM interrupt enable bit** 0: Disable SCM interrupt 1: Enable SCM interrupt
2	**EEIE**	**EEPROM interrupt enable bit** 0: Disable EEPROM interrupt 1: Enable EEPROM interrupt
1	**CMPIE**	**Comparator output interrupt enable bit** 0: Disable Comparator interrupt 1: Enable Comparator interrupt

7.8.3 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in Interrupt Summary table.

The **External Interrupt (INTx, x = 0,1)** is generated by external source on pin (INTx , x = 0, 1), which is set by hardware. If the interrupt was edge trigged, the flag (IEx, x = 0, 1) will be cleared by the hardware when the service routine is vectored. If the interrupt was level trigged, the external source's level directly controls the request flag, rather than the on-chip hardware.

The **Timer 0/1 Interrupt** is generated when they overflows, the flag (TFx, x = 0, 1) in TCON register, which is set by hardware, and will be automatically be cleared by hardware when the service routine is vectored.

The **ADC Interrupt** is generated by ADCIF bit in ADCON register, which is set by hardware. If an interrupt is generated, the converted result in ADDH/ADDL will be valid. If continuous compare function in ADC module is established, ADCIF will be set at each conversion. The flag must be cleared by software.

The **SCM Interrupt** is generated by SCMIF in CLKCON register, which is set by hardware. The flag can only be cleared by hardware.

The **Comparator interrupt** is generated by CMPIF in CMPCON register, which is set by hardware. The flag must be cleared by software.

The **EEPROM interrupt** is generated by EEIF in EECON register, which is set by hardware. The flag must be cleared by software.

Table 7.24 External Interrupt Flag Register

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 5	TFx (x = 0, 1)	**Timer x overflow flag bit**
6, 4	TRx (x = 0, 1)	**Timer x start, stop control bit**
3, 1	IEx (x = 0, 1)	**External interrupt x request flag bit** 0: No interrupt pending 1: Interrupt is pending
2, 0	ITx (x = 0, 1)	**External interrupt x trigger mode selection bit** 0: Low level trigger 1: Falling edge trigger

7.8.4 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in **Interrupt Summary table**.

7.8.5 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction cycle, an internal polling sequence determines which request is serviced.

Interrupt Priority Level		
Priority bits		**Interrupt Level Priority**
IPHx	IPLx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.25 Interrupt priority control registers

B8H, B4H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL0	-	PADCL	-	-	PT1L	PX1L	PT0L	PX0L
IPH0	-	PADCH	-	-	PT1H	PX1H	PT0H	PX0H
R/W	-	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	-	-	0	0	0	0
B9H, B5H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL1	-	-	-	PSCML	PCMPL	PEEL	-	-
IPH1	-	-	-	PSCMH	PCMPH	PEEH	-	-
R/W	-	-	-	R/W	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	0	0	-	-

Bit Number	**Bit Mnemonic**	**Description**
-	**PxxxL/H**	Corresponding interrupt source xxx's priority level selection bits

7.8.6 Interrupt Handling

The interrupt flags are sampled and polled at the fetch cycle of each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current cycle is not in the final cycle of the instruction in progress. This ensures that the instruction in progress is completed before vectoring to any service routine.

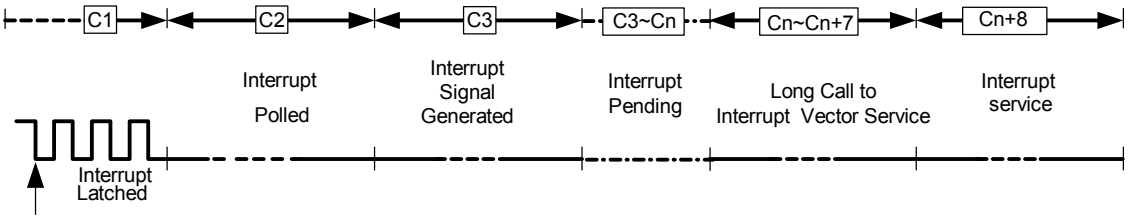
The instruction in progress is RETI. This ensures that if the instruction in progress is RETI then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Notes:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.

The polling cycle/LCALL sequence is illustrated below:



Interrupt Response Timing

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with corresponding address that depends on the source of the interrupt being vectored too, as shown in Interrupt Summary table.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt service. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt with this priority was still in progress. In this case, no interrupt of the same or lower priority level would be acknowledged.

7.8.7 Interrupt Response Time

If an interrupt is recognized, its request flag is set in every machine cycle after recognize. The value will be polled by the circuitry until the next machine cycle; the CPU will generate an interrupt at the third machine cycle. If the request is active and conditions are right for it to be acknowledged, hardware LCALL to the requested service routine will be the next instruction to be executed. Else the interrupt will pending. The call itself takes 7 machine cycles. Thus a minimum of 3+7 complete machine cycles will elapse between activation and external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine.

If the instruction in progress is not in its final cycle and the instruction in progress is RETI， the additional wait time is 8 machine cycles. For a single interrupt system, if the next instruction is 20 machine cycles long (the longest instructions DIV & MUL are 20 machine cycles long for 16 bit operation), adding the LCALL instruction 7 machine cycles the total response time is 2+8+20+7 machine cycles.

Thus interrupt response time is always more than 10 machine cycles and less than 37 machine cycles.

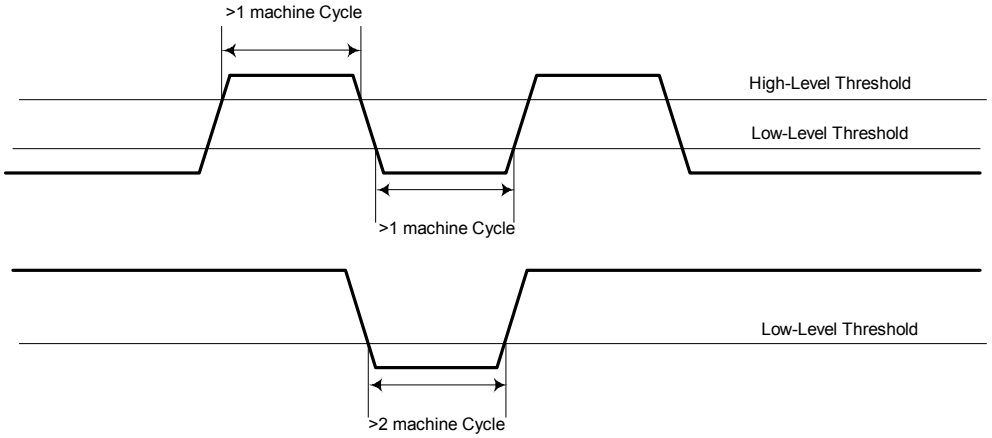
7.8.8 External Interrupt Inputs

The SH79E02 has two external interrupt inputs. External interrupt0/1 can be programmed to be low level-triggered or edge-triggered by clearing or setting bit IT1 or IT0 in register TCON. If ITx = 0 (x = 0, 1), external interrupt x is triggered by a low level detected at the INTx (x = 0, 1) pin. If ITx = 1 (x = 0, 1), external interrupt is edge triggered. In this mode if consecutive samples of the INTx pin show a high level in one cycle and a low level in the next cycle, interrupt request flag IEx in TCON is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

If the external interrupt is edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag IEx is set. IEx is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag IEx when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the SH79E02 is put into Power down or Idle mode, the interrupt occurence will cause the processor to wake up and resume operation. Refer to the **Power management** Section for details.



External Interrupt Detection

7.8.9 Interrupt Summary

Source	Vector Address	Enable bits	Flag bits	Polling Priority
Reset	0000h	-	-	0 (highest)
INT0	0003h	EX0	IE0	1
Timer0	000Bh	ET0	TF0	2
INT1	0013h	EX1	IE1	3
Timer1	001Bh	ET1	TF1	4
ADC	0033h	EADC	ADCIF	5
Comparator	0043h	CMPIE	CMPIF	6
EEPROM	004Bh	EEIE	EEIF	7
SCM	005Bh	ESCM	SCMIF	8 (lowest)

8. Enhanced Function

8.1 Analog Digital Converter (ADC)

8.1.1 Feature

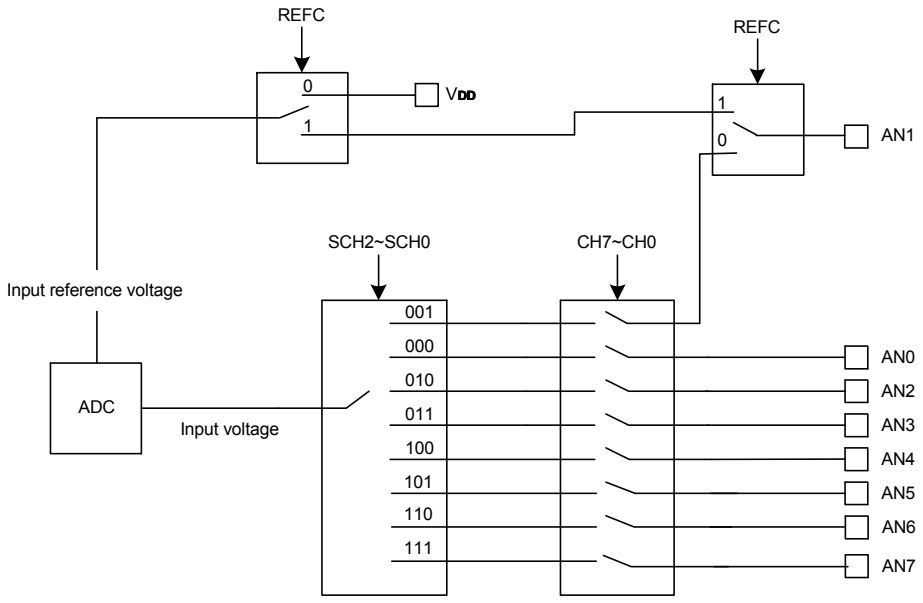
- 10-bit Resolution
- Build in V_{REF}
- Selectable external or built-in V_{REF}
- 8 Multiplexed Input Channels

The SH79E02 include a single ended, 10-bit SAR Analog to Digital Converter (ADC) with build in reference voltage connected to the V_{DD}, users also can select the V_{REF} pin input reference voltage. The 8 ADC channels are shared with 1 ADC module; each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. GO/$\overline{\text{DONE}}$ signal is available to start convert, and indicate end of convert. When conversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCON register will be set. If ADC Interrupt is enabled, the ADC interrupt will generate.

The ADC integrates a digital compare function to compare the value of analog input with the digital value in the AD converter. If this function is enabled (set EC bit in ADCON register) and ADC module is enabled (set ADON bit in ADCON register). When the corresponding digital value of analog input is larger than or equal to the value in compare value register (ADDH/L), the ADC interrupt will occur, otherwise no interrupt will be generated. The digital comparator can work continuously when GO/$\overline{\text{DONE}}$ bit is set until software clear, which behaviors different with the AD converter operation mode.

The ADC module including digital compare module can wok in Idle mode and the ADC interrupt will wake up the Idle mode, but is disabled in Power-Down mode.

8.1.2 ADC Diagram



8.1.3 Register

Table 8.1 ADC Control Register

93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	EC	REFC	SCH2	SCH1	SCH0	$\overline{\text{GO/DONE}}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**ADON**	**ADC Enable bit** 0: Disable the ADC module 1: Enable the ADC module
6	**ADCIF**	**ADC Interrupt Flag bit** 0: No ADC interrupt, cleared by software 1: Set by hardware to indicate that the AD Convert has been completed, or analog input is larger than or equal to ADDH/ADDL if compare is enabled
5	**EC**	**Compare Function Enable bit** 0: Compare function disabled 1: Compare function enabled
4	**REFC**	**Reference Voltage Select bit** 0: the reference voltage connected to V_{DD} 1: the reference voltage input from V_{REF} pin
3-1	**SCH [2:0]**	**ADC channel Select bits** 000: ADC channel AN0 001: ADC channel AN1 010: ADC channel AN2 011: ADC channel AN3 100: ADC channel AN4 101: ADC channel AN5 110: ADC channel AN6 111: ADC channel AN7
0	**$\overline{\text{GO/DONE}}$**	**ADC status flag bit** 0: Automatically cleared by hardware when AD convert is completed. Clearing this bit during converting time will stop current conversion. If Compare function is enabled, this bit will not be cleared by hardware until software clear 1: Set to start AD convert or digital compare

Notes:

When select the reference voltage input from V_{REF} pin (REFC = 1), the P3.1 is shared as V_{REF} input rather than AN1 input.

Table 8.2 ADC Time Control Register

94H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	TADC2	TADC1	TADC0	-	TS3	TS2	TS1	TS0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-5	**TADC[2:0]**	**ADC Clock Period Select bits** 000: ADC Clock Period t_{AD} = 2 t_{SYS} 001: ADC Clock Period t_{AD} = 4 t_{SYS} 010: ADC Clock Period t_{AD} = 6 t_{SYS} 011: ADC Clock Period t_{AD} = 8 t_{SYS} 100: ADC Clock Period t_{AD} = 12 t_{SYS} 101: ADC Clock Period t_{AD} = 16 t_{SYS} 110: ADC Clock Period t_{AD} = 24 t_{SYS} 111: ADC Clock Period t_{AD} = 32 t_{SYS}
3-0	**TS[3:0]**	**Sample time select bits** 2 t_{AD} ≤ Sample time = (TS [3:0]+1) * t_{AD} ≤ 15 t_{AD}

Note:

(1) Make sure that t_{AD} ≧ 1μs;

(2) The minimum sample time is 2 t_{AD}, even TS[3:0] = 0000;

(3) The maximum sample time is 15 t_{AD}, even TS[3:0] = 1111;

(4) Evaluate the series resistance connected with ADC input pin before set TS[3:0];

(5) Be sure that the series resistance connected with ADC input pin is no more than 10kΩ when 2 t_{AD} sample time is selected;

(6) Total conversion time is: 12 t_{AD} + sample time.

For Example:

System Clock (SYSCLK)	TADC[2:0]	t_{AD}	TS[3:0]	Sample Time	Conversion Time
32.768kHz	000	30.5 *2=61μs	0000	2*61=122μs	12*61+122=854μs
	000	30.5 *2=61μs	0111	8*61=488μs	12*61+488=1220μs
	000	30.5 *2=61μs	1111	15*61=915μs	12*61+915=1647μs
	111	30.5 *32=976μs	0000	2*976=1952μs	12*976+1952=13664μs
	111	30.5 *32=976μs	0111	8*976=7808μs	12*976+7808=19520μs
	111	30.5 *32=976μs	1111	15*976=14640μs	12*976+14640=26352μs
455kHz	000	2.197*2=4.39μs	0000	2*4.39=8.78μs	12*4.39+8.78=61.46μs
	000	2.197*2=4.39μs	0111	8*4.39=35.12μs	12*4.39+35.12=87.8μs
	000	2.197*2=4.39μs	1111	15*4.39=65.85μs	12*4.39+65.85=118.53μs
	001	2.197*4=8.78μs	0000	2*8.78=17.57μs	12*8.78+17.57=122.92μs
	001	2.197*4=8.78μs	0111	8*8.78=70.24μs	12*8.78+70.24=175.6μs
	001	2.197*4=8.78μs	1111	15*8.78=131.7μs	12*8.78+131.7=237.06μs
8MHz	000	0.125*2=0.25μs	-	-	(t_{AD}<1μs, not recommended)
	001	0.125*4=0.5μs	-	-	(t_{AD}<1μs, not recommended)
	010	0.125*6=0.725μs	-	-	(t_{AD}<1μs, not recommended)
	011	0.125*8=1μs	0000	2*1=2μs	12*1+2=14μs
	011	0.125*8=1μs	0111	8*1=8μs	12*1+8=20μs
	100	0.125*12=1.5μs	0000	2*1.5=3μs	12*1.5+3=21μs
	100	0.125*12=1.5μs	0111	8*1.5=12μs	12*1.5+12=30μs

Table 8.3 ADC Channel Configure Register

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**CH [7:0]**	**Channel Configuration bits** 0：P3.0-P3.4, P1.1-P1.3, P1.6 are IO pins 1：P3.0-P3.4, P1.1-P1.3, P1.6 are ADC channels

Table 8.4 AD converter Data Register (compare value register)

96H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDL	-	-	-	-	-	-	A1	A0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0
97H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDH	A9	A8	A7	A6	A5	A4	A3	A2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
1-0 **7-0**	**A9-A0**	**ADC Data register** Digital Value of sampled analog voltage, updated when conversion is completed If ADC Compare function is enabled (EC = 1), this is the value to be compared with the analog input

The approach for AD conversion:

1. Select the analog input channels and reference voltage.
2. Enable the ADC module with the selected analog channel.
3. Set GO/$\overline{\text{DONE}}$ = 1 to start the AD conversion.
4. Wait until GO/$\overline{\text{DONE}}$ = 0 or ADCIF = 1, if the ADC interrupt is enabled, the ADC interrupt will occur.
5. Acquire the converted data from ADDH/ADDL.
6. Repeat step 3-5 if another conversion is required.

The approach for digital compare function:

1. Select the analog input channels and reference voltage.
2. Set ADDH/ ADDL to the compare value.
3. Set EC = 1 to enable compare function.
4. Enable the ADC module with the selected analog channel.
5. Set GO/$\overline{\text{DONE}}$ = 1 to start the compare function.
6. If the analog input is lager than compare value set in ADDH/ADDL, the ADCIF will be set to 1. if the ADC interrupt is enabled, the ADC interrupt will occur.ADCIF must be cleared by software.
7. The compare function will continue work until the GO/$\overline{\text{DONE}}$ bit is cleared to 0.

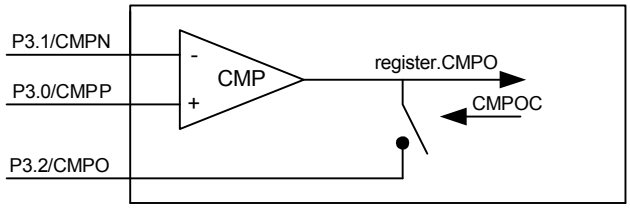
8.2 Comparator (CMP)

8.2.1 Feature

- Single power operation
- Output inversion control
- Work in Idle or Power-Down mode

The SH79E02 consists of one independent precision voltage comparator. The CMPP pin which be shared as P3.0 is the positive input of the Comparator. The CMPN pin which be shared as P3.1 is the negative input of the Comparator. The CMPO pin which be shared as P3.2 is the output of the Comparator, and it can be changed as the normal I/O port or other functions even under the condition of the comparator being enabled.

If CMPEN = 1 and CMPIE = 1, any change on the output value of the Comparator would generate an interrupt request (CMPIF = 1) and interrupt CPU. The Comparator interrupt can also wake the CPU from IDLE or Power-Down mode.



Built-in CMP

8.2.2 Register

Table 8.5 Comparator Control Register

92H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMPCON	CMPIF	-	-	-	CMPEN	CMPOC	CINV	CMPO
R/W	R/W	-	-	-	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**CMPIF**	**Comparator output Interrupt Flag** 0: Comparator output has not changed 1: Comparator output has changed (must be cleared by software)
3	**CMPEN**	**Comparator Enable Control bit** 0: Disable Comparator 1: Enable Comparator
2	**CMPOC**	**Comparator Output Control bit** 0: Comparator without output (P3.2 is shared as I/O or other functions) 1: Comparator with output(P3.2 is shared as CMPO)
1	**CINV**	**Comparator output Inversion bit** 0: Comparator output not Inverted 1: Comparator output Inverted
0	**CMPO**	**Comparator output bit** CMPO = 0, when CMPP < CMPN and CINV = 0 CMPO = 1, when CMPP > CMPN and CINV = 0 CMPO = 0, when CMPP > CMPN and CINV = 1 CMPO = 1, when CMPP < CMPN and CINV = 1

8.3 High-performance Operational Amplifier (OP)

8.3.1 Features

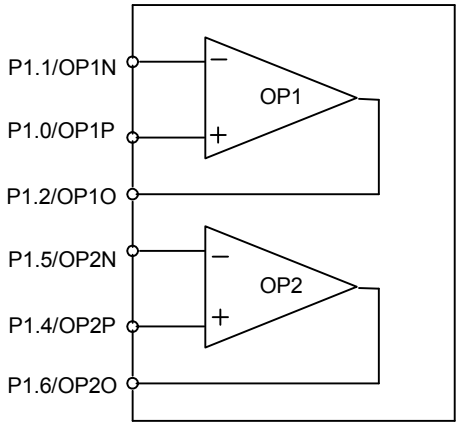
- Single power supply
- Internally frequency compensated

There are two high-performance operational amplifiers built in the SH79E02. It can operate from a single power supply with the stable and high gain performance, internally frequency compensated. These amplifiers have a unique characteristic that the input common-mode voltage ranges from ground to operating voltage.

Operational amplifier 1 (OP1) output pin is OP1O, OP1 negative input pin is OP1N, OP1 positive input is OP1P.

Operational amplifier 2 (OP2) output pin is OP2O, OP2 negative input pin is OP2N, OP2 positive input is OP2P.

The OP can be switch off by software to save power.



Built-in OP

8.3.2 Register

Table 8.6 OP Control Register

91H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPCON	-	-	-	-	-	-	OP2PC	OP1PC
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1	**OP2PC**	**OP2 enable Control bit** 0: disable OP2 function 1: enable OP2 function
0	**OP1PC**	**OP1 enable Control bit** 0: disable OP1 function 1: enable OP1 function

8.4 Data EEPROM Memory

8.4.1 Features

- 128 bytes EEPROM
- 100,000 write EEPROM high endurance
- The programming time is 1.8ms when write only or 3.4ms when erase and write in one operation
- Multi-step of writing data to protect EEPROM data

The SH79E02 has 128 bytes EEPROM. The EEPROM is readable and writable during normal operation over the whole V_{DD} range. The operation for EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

Reading the EEPROM Data Memory

Follow steps to read data from the EEPROM:

1. Set the EEPC bit to 1 for enable EEPROM power;
2. Clear the EEWE bit to 0;
3. Write the address to IB_OFFSET (128 bytes EEPROM address);
4. Set the EERD bit to 1 to initiate read cycle;
5. Wait for EERD to be cleared;
6. Read the 8-bit data value from IB_DATA for proper use;
7. For the next read operation, got step 3 as required;
8. If user wants to save power, clear EEPC.

Writing to the EEPROM Data Memory

Follow steps to write data to the EEPROM:

1. Set the EEPC bit to 1 for enable EEPROM power;
2. Set the EWSC bit and EEWE bit to 1;
3. Write the address to IB_OFFSET (128 bytes EEPROM address);
4. Write the 8-bit data value to IB_DATA;
5. Set the EEWR bit to 1 to initiate write cycle;
6. Fill in IB_CON1;
7. Fill in IB_CON2-5 sequentially;
8. Wait for EEWR to be cleared;
9. For the next write operation, got step 3 as required;
10. If user wants to save power, clear EWSC, EEWE and EEPC.

8.4.2 Register

Table 8.7 EEPROM Control Register

C0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EECON	EEPC	EEIF	EWSC	EEPM	WRERR	EEWE	EEWR	EERD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**EEPC**	**EEPROM Power Control bit** 0: Switch off the EEPROM 1: EEPROM is operating
6	**EEIF**	**EEPROM Write Interrupt Flag bit** 0: No EEPROM write operation interrupt 1: Set by hardware to indicate that the EEPROM write operation has been completed (must be cleared by software)
5	**EWSC**	**EEPROM Write and SSP Control bit** 0: SSP is enabled 1: EEPROM Write is enabled
4	**EEPM**	**EEPROM Programming Mode bit** 0: The programming time is 3.4ms (Erase and write in one operation) 1: The programming time is 1.8ms (write only)
3	**WRERR**	**EEPROM Error Flag bit** 0: The write operation completed 1: A write operation is prematurely terminated (any Pin Reset, any WDT Reset, any LVR during normal operation)
2	**EEWE**	**EEPROM Write Enable bit** 0: Inhibit write to the EEPROM 1: Allow write cycle
1	**EEWR**	**EEPROM Write Control bit** 0: Write cycle to the EEPROM is complete 1: Initiate a write cycle (EEWR can be set by software, EEWR is cleared by hardware after write cycle is completed)
0	**EERD**	**EEPROM Read Control bit** 0: EEPROM read is complete 1: Initiate an EEPROM read (EERD can be set by software, EERD is cleared by hardware after read instruction is completed)

Table 8.8 EEPROM Data Register

FCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_DATA[7:0]**	**EEPROM Data register** Byte value to write to or read from the EEPROM

Table 8.9 EEPROM Address Register

FBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	-	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-0	**IB_OFF SET[6:0]**	**EEPROM Address register** Specify one of 128 locations for EEPROM Read/Write Operation

Table 8.10 EEPROM Type Select Register

F2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_CON1[7:0]**	**EEPROM Type select** 0x55: EEPROM Write 0x66: EEPROM Erase and Write

Table 8.11 EEPROM Control Register2

F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON2[3:0]**	**Must be 05H, else EEPROM Programming will terminate**

Table 8.12 EEPROM Control Register3

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON3[3:0]**	**Must be 0AH, or else EEPROM Programming will terminate**

Table 8.13 EEPROM Control Register4

F5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON4[3:0]**	**Must be 09H, else EEPROM Programming will terminate**

Table 8.14 EEPROM Control Register5

F6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON5[3:0]**	**Must be 06H, else EEPROM Programming will terminate**

8.5 Low Voltage Reset (LVR)

8.5.1 Feature

- Enabled by the code option and V_{LVR} is 2.6V or 4.0V
- LVR de-bounce timer T_{LVR} is about 100μs
- An internal reset flag indicates low voltage reset generates

The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the voltage below the detect value. The LVR Debounce Time is about 100μs.

The LVR functions as below when the LVR function is enabled:

Generates a system reset when $V_{DD} \leq V_{LVR}$

Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$ but $t < T_{LVR}$.

The LVR function is enabled by the code option.

It is typically used in AC line or large battery supplier applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage. This feature can protect system from working under bad power supply environment.

8.6 Watchdog Timer (WDT) and Reset State

8.6.1 Feature

- Auto detect Program Counter (PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH79E02 builds in Program Counter(PC)over range detect circuit, if program counter value is larger than flash romsize, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash rom with A5H.

Watchdog

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled permanently by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow frequency. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

There are also some reset flags in this register as below:

8.6.2 Register

Table 8.15 Reset Control Register

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Mnemonic	Description
7	**WDOF**	**Watch Dog Timer Overflow or OVL Reset Flag** Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows and no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	**PORF**	**Power On Reset Flag** Set only by Power On Reset, cleared only by software 0: No Power On Reset 1: Power On Reset occurred
4	**LVRF**	**Low Voltage Reset Flag** Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	**CLRF**	**Pin Reset Flag** Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred
2-0	**WDT [2:0]**	**WDT Overflow period control bit** 000: Overflow period minimal value= 4096ms 001: Overflow period minimal value = 1024ms 010: Overflow period minimal value = 256ms 011: Overflow period minimal value = 128ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms ***Note:*** *If OP_WDT is enable in application, you must clear WatchDog periodically, and the interval must be less than the value list above.*

8.7 Power Management

8.7.1 Feature

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH79E02 supplies two power reduction modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

8.7.2 Idle Mode

In this mode, the clock to CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH79E02 enter idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter IDLE mode.

The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit idle mode:

(1) An interrupt generated, the clock to the CPU will be restored, and the hardware will clear SUSLO register and IDL bit in PCON register. Then the program will execute the interrupt service routine first, then jumps to the instruction immediately following the instruction that activated idle mode.

(2) Reset signal (logic LOW on the RESET pin, WDT RESET if enabled, LVR REST if enabled), this will restore the clock to the CPU, the SUSLO register and the IDL bit in PCON register will be cleared by hardware, finally the SH79E02 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

8.7.3 Power-Down Mode

The Power-Down mode places the SH79E02 in a very low power state. Power-Down mode will stop all the clocks including CPU and peripherals. If WDT is enabled, WDT block will keep on working. When entering Power-Down mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all be retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79E02 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear both SUSLO register and PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

The setting of PD bit will be the last instruction that CPU executed.

Note: *If IDL bit and PD bit are set simultaneously, the SH79E02 enters Power-Down mode. The CPU will not go in idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit from Power-Down mode.*

There are two ways to exit the Power-Down mode:

(1) External Interrupt (INT0 or INT1) and comparator interrupt. These interrupts will make the SH79E02 exit Power-Down mode. The oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) Reset signal (logic LOW on the RESET pin, WDT RESET if enabled, LVR RESET if enabled). This will restore the clock to the CPU after warm-up time, the SUSLO register and the PD bit in PCON register will be cleared by hardware, finally the SH79E02 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note: *In order to entering IDLE/POWER-DOWN mode, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.*

8.7.4 Register

Table 8.16 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	-	-	-	-	GF1	GF0	PD	IDL
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-2	**GF[1:0]**	**General purpose flags for software use**
1	**PD**	**Power-Down mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode
0	**IDL**	**Idle mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode

Table 8.17 Suspend Mode Control Register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SUSLO[7:0]**	This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise the either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle.

Note: *In Idle mode, CPU clock would be halted and the clocks of peripherals(obtained from the same system clock as CPU), such as Timer and ADC, would not be halted. The interrupts of peripherals could be used to exit Idle mode. In Power-down mode, all the clocks including CPU and peripherals would be stopped.*

Example:

```
IDLE_MODE:
        MOV     SUSLO, #55
        ORL     PCON, #01
        NOP
        NOP
        NOP

POWERDOWN_MODE:
        MOV     SUSLO, #55
        ORL     PCON, #02
        NOP
        NOP
        NOP
```

8.8 Warm-up Timer

8.8.1 Feature

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation startup

SH79E02 has a built-in power warm-up counter; it is designed to eliminate unstable state of power or to do some internal initial operation such as read customer operation etc.

SH79E02 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset Watchdog Reset and Wake up from Power-down mode.

After power-on, SH79E02 will do power warm-up procedure first, and then do oscillator warm-up procedure to eliminate unstable state of initial oscillation.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		**WDT Reset (Not in Power-Down Mode)**		**WDT Reset (Wakeup from Power-Down Mode)**		**Wakeup from Power-Down Mode (Only for interrupt)**	
TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*
11ms	YES	1000CKs	NO	1000CKs	YES	16CKs	YES

* OSC Warm up time please refers to following table.
** The clock source is internal 2M RC oscillator.

Oscillator Warm-up Time

Option OP_WMT / Oscillator type	**00**	**01**	**10**	**11**
Ceramic*	2^{13} X Tosc	2^{11} X Tosc	2^{9} X Tosc	2^{7} X Tosc
Crystal**	2^{17} X Tosc	2^{15} X Tosc	2^{13} X Tosc	2^{11} X Tosc
32k Crystal	2^{13} X Tosc			
Internal RC	2^{7} X Tosc			

* Only suitable for 455kHz ceramic.
** Also suitable for 500kHz - 8MHz ceramic.

8.9 Code Option

OP_OSC[2:0]:

000: Internal RC oscillator (8MHz) (default)
010: External Clock (400kHz - 8MHz)
011: 32.768kHz Crystal Oscillator
101: Crystal Oscillator (400kHz - 8MHz)/Ceramic Oscillator (500kHz - 8MHz)
110: Ceramic Oscillator (455kHz)
Others: Internal RC oscillator (8MHz)

OP_WDT[3]:

0: Disable WDT function (default)
1: Enable WDT function

OP_LVREN[4]:

0: Disable LVR function (default)
1: Enable LVR function

OP_LVRLE[5]:

0: 2.6V LVR Level 1 (default)
1: 4.0V LVR Level 2

OP_OP1[6]:

0: Disable OP1 function (default)
1: Enable OP1 function

OP_OP2[7]:

0: Disable OP2 function (default)
1: Enable OP2 function

OP_WMT[1:0] (Exclude 32k crystal and internal RC)

00: longest warm up time (default)
01: longer warm up time
10: shorter warm up time
11: shortest warm up time

OP_WDTPD[2]:

0: Disable WDT function in Power-Down mode (default)
1: Enable WDT function in Power-Down mode

OP_RST[3]:

0: P3.3 used as RST pin (default)
1: P3.3 used as I/O pin

9. Instruction Set

ARITHMETIC OPERATIONS					
Opcode		**Description**	**Code**	**Byte**	**Cycle**
ADD A, Rn		Add register to accumulator	0x28-0x2F	1	1
ADD A, direct		Add direct byte to accumulator	0x25	2	2
ADD A, @Ri		Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data		Add immediate data to accumulator	0x24	2	2
ADDC A, Rn		Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct		Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri		Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data		Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn		Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct		Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri		Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data		Subtract immediate data from A with borrow	0x94	2	2
INC A		Increment accumulator	0x04	1	1
INC Rn		Increment register	0x08-0x0F	1	2
INC direct		Increment direct byte	0x05	2	3
INC @Ri		Increment indirect RAM	0x06-0x07	1	3
DEC A		Decrement accumulator	0x14	1	1
DEC Rn		Decrement register	0x18-0x1F	1	2
DEC direct		Decrement direct byte	0x15	2	3
DEC @Ri		Decrement indirect RAM	0x16-0x17	1	3
INC DPTR		Increment data pointer	0xA3	1	4
MUL AB	8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB	8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A		Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16	Long subroutine call	0x12	3	7
RET	Return from subroutine	0x22	1	8
RETI	Return from interrupt	0x32	1	8
AJMP addr11	Absolute jump	0x01-0xE1	2	4
LJMP addr16	Long jump	0x02	3	5
SJMP rel	Short jump (relative address)	0x80	2	4
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	6
JZ rel (not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel (not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel (not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel (not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit,rel (not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit,rel (not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel (not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A, direct, rel (not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A, #data, rel (not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn, #data, rel (not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel (not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn,rel (not taken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel (not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP	No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

10. Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . .-0.3V to +6.0V

Input/Output Voltage . . . . . .GND-0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . . . .-40℃ to +85℃

Storage Temperature. . . ..-55℃ to +125℃

***Comments**

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics1 (V_{DD} = 2.7 - 5.5V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	4.5	5.0	5.5	V	30kHz ≤ f_{OSC} ≤ 8MHz
		2.7	3.0	5.5	V	30kHz ≤ f_{OSC} ≤ 4MHz
Operating Current	I_{OP}	-	5	10	mA	f_{OSC} = 8MHz, V_{DD} = 5.0V All output pins unload (including All digital input pins un-floating), CPU on (execute NOP instruction), all other function block off
		-	0.5	0.7	mA	f_{OSC} = 455kHz, V_{DD} = 5.0V Low power mode (LPCON = 1) All output pins unload (including All digital input pins un-floating), CPU on (execute NOP instruction), all other function block off
		-	100	120	μA	f_{OSC} = 32.768kHz, V_{DD} = 5.0V Low power mode (LPCON = 1) All output pins unload (including All digital input pins un-floating), CPU off (IDLE), all other function block off
Stand by Current (IDLE)	I_{SB1}	-	3	5	mA	f_{OSC} = 8MHz, V_{DD} = 5.0V All output pins unload (including All digital input pins un-floating), CPU off (IDLE), all other function block off
		-	0.3	0.5	mA	f_{OSC} = 455kHz, V_{DD} = 5.0V Low power mode (LPCON = 1) All output pins unload (including All digital input pins un-floating), CPU off (IDLE), all other function block off
		-	20	30	μA	f_{OSC} = 32.768kHz, V_{DD} = 5.0V, Low power mode (LPCON = 1) All output pins unload (including All digital input pins un-floating), CPU off (IDLE), all other function block off
Stand by Current (Power-Down)	I_{SB2}	-	-	3	μA	f_{OSC} = OFF, V_{DD} = 5.0V All output pins unload (including All digital input pins un-floating), CPU off (Power -Down), all other function block off
WDT Current	I_{WDT}	-	-	10	μA	WDT on
Input Low Voltage 1	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input High Voltage 1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input Low Voltage 2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$
Input High Voltage 2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T0, T1, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$

Continued

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN} = V_{DD} or GND
Pull-high Resistor	R_{PH}	-	30	-	kΩ	V_{DD} = 5.0V, V_{IN} = GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, I_{OH} = -10mA, V_{DD} = 5.0V
Output Low Voltage	V_{OL1}	-	-	GND + 0.6	V	I/O Ports, I_{OL} = 15mA, V_{DD} = 5.0V

Note:
Maximum value of the supply current from V_{DD} is 100mA.
Maximum value of the output current to GND is 150mA.

5V ADC Electrical Characteristics

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Supply Voltage	V_{AD}	4.5	5.0	5.5	V	
Resolution	N_R	-	10	-	bit	GND ≤ V_{AIN} ≤ V_{REF}
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor**	R_{AIN}	2	-	-	MΩ	V_{IN} = 5.0V
Recommended impedance of analog voltage source	Z_{AIN}	-	-	10	kΩ	
A/D conversion current	I_{AD}	-	1	3	mA	ADC module operating, V_{DD} = 5.0V
A/D Input current	I_{ADIN}	-	-	10	μA	V_{DD} = 5.0V
Differential linearity error	D_{LE}	-	-	±1	LSB	f_{OSC} = 8MHz, V_{DD} = 5.0V
Integral linearity error	I_{LE}	-	-	±2	LSB	f_{OSC} = 8MHz, V_{DD} = 5.0V
Full scale error	E_F	-	±1	±3	LSB	f_{OSC} = 8MHz, V_{DD} = 5.0V
Offset error	E_Z	-	±0.5	±2	LSB	f_{OSC} = 8MHz, V_{DD} = 5.0V
Total Absolute error	E_{AD}	-	-	±3	LSB	f_{OSC} = 8MHz, V_{DD} = 5.0V
Conversion time***	T_{CON}	14	-	-	μs	10 bit resolution and f_{OSC} = 8MHz, V_{DD} = 5.0V

Note:
**: Data in "Typ." Column is at 5.0V, 25°C, unless otherwise specified.*
***: A/D input resistance is the input resistance of ADC module under DC condition.*
****: The resistance of the signal souce connected to the ADC module should be less than 10KΩ.*

Analog Comparator Electrical Characteristics
(V_{DD} = 2.7 - 5.5V, GND = 0V, T_A = +25°C, f_{OSC} = 30KHz - 8MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage	$\|V_{IO}\|$	-	-	10	mV	
Input Common-Mode Voltage Range	V_{CM}	GND	-	V_{DD} - 1.3	V	
Response time	T_{RES}	-	250	500	ns	
Comparator enable to output valid time	T_{OV}	-	-	10	μs	
Input leakage current	I_{IL}	-	-	1	μA	0 < V_{IN} < V_{DD}

Operational Amplifier Electrical Characteristics
(V_{DD} = 2.7 - 5.5V, GND = 0V, T_A = +25°C, f_{OSC} = 30KHz - 8MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage	$\|V_{IO}\|$	-	-	5	mV	
Input Common-Mode Voltage Range	V_{CM}	GND + 0.1	-	V_{DD} - 1.0	V	
Input Offset Current	$\|I_{IO}\|$	-	-	0.1	μA	
Output Voltage Range	V_{OAR}	GND + 0.1	-	V_{DD} - 0.1	V	I_{SINK} or $I_{DRIVE} \leq$ 1.0mA
Voltage Gain	A_V	2	30	-	V/mV	$R_L \geq$ 15K (open loop voltage gain)
Output Sink Current	I_{SINK}	12	-	-	mA	VOAP_O increment ≤ 0.5V
Output Driving Current	I_{DRIVE}	10	-	-	mA	VOAP_O drop ≤ 1.0V
Input Resistance	R_I	10	-	-	MΩ	
Output Resistance	R_O	-	-	200	Ω	

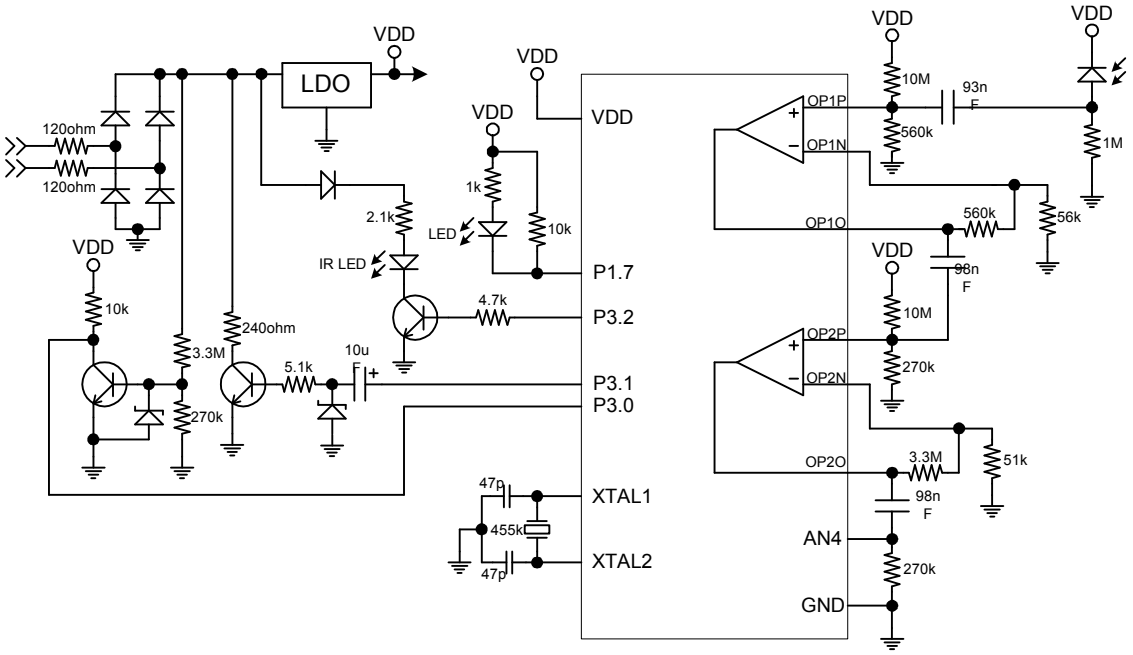
AC Electrical Characteristics
(V_{DD} = 2.7 - 5.5V, GND = 0V, T_A = +25°C, f_{OSC} = 30KHz - 8MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
RESET pulse width	t_{RESET}	10	-	-	μs	Low active
Oscillator start time 1	T_{OSC1}	-	1	2	s	32K crystal oscillator is used
Oscillator start time 2	T_{OSC2}	-	10	20	ms	455kHz ceramic resonator is used
WDT Period	T_{WDT}	1	-	-	ms	
Internal RC Frequency Variation	$\|\Delta F\|/F$	-	-	5	%	Internal RC Oscillator, Include chip-to-chip variation (V_{DD} = 5V, T_A = 25℃)

Low Voltage Reset Electrical Characteristics (V_{DD} = 2.7 - 5.5V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage level 1	V_{LVR1}	3.9	4.0	4.1	V	LVR enabled, V_{DD} = 4.5V - 5.5V
LVR Voltage level 2	V_{LVR2}	2.5	2.6	2.7	V	LVR enabled, V_{DD} = 2.7V - 5.5V

11. Application Circuit



SH79E02

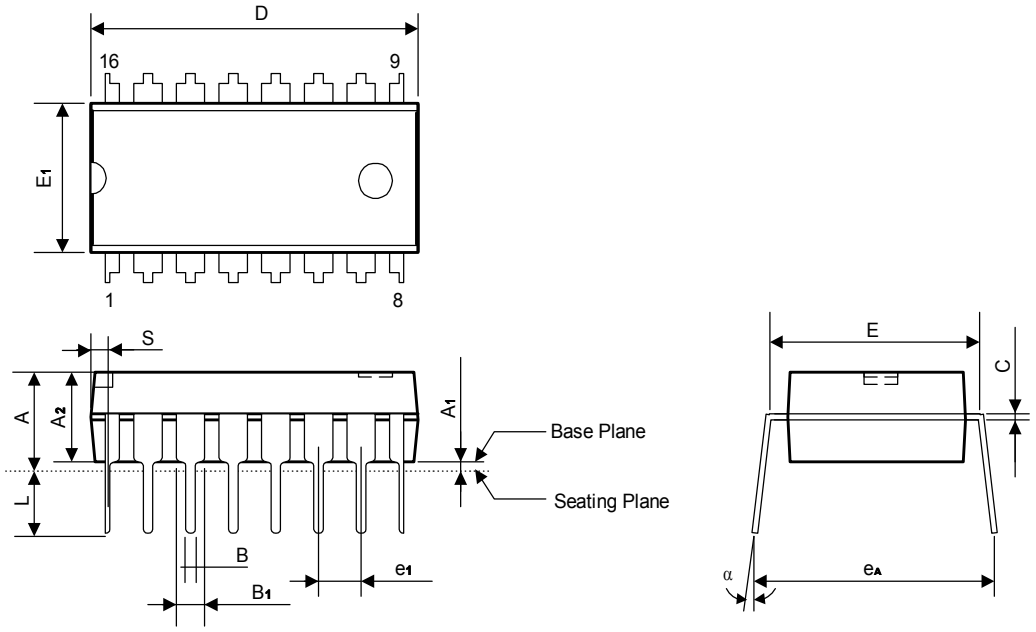
12. Ordering Information

Part NO.	Package
SH79E02M/016MU	SOP16
SH79E02D/016DU	DIP16
SH79E02X/020XU	TSSOP20

13. Package Information

P-DIP 16L Outline Dimensions

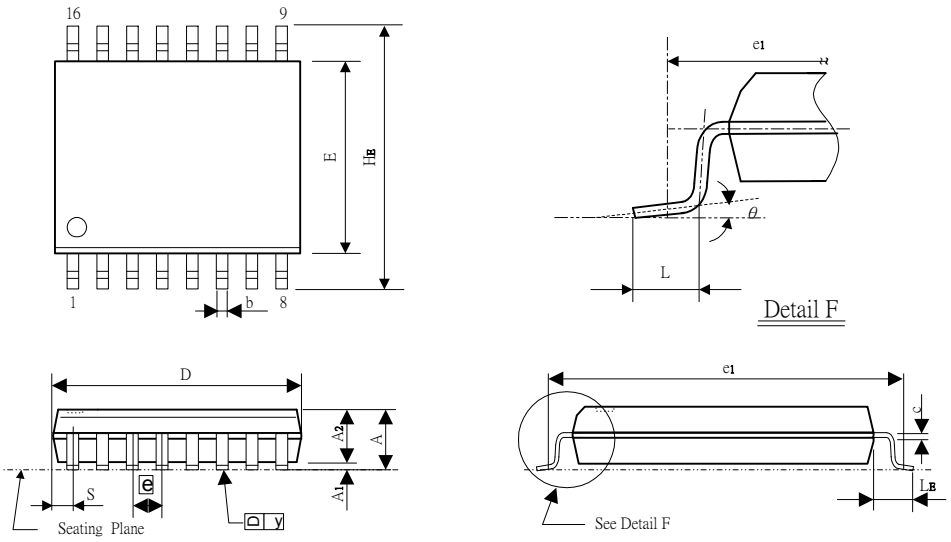
unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.210 Max.	5.33 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018+0.004 -0.002	0.46+0.10 -0.05
B_1	0.060+0.004 -0.002	1.52+0.10 -0.05
C	0.010+0.004 -0.002	0.25+0.10 -0.05
D	0.750 Typ. (0.770 Max.)	19.05 Typ. (19.56 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 TYP	2.54 TYP
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.040 Max.	1.02 Max.

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

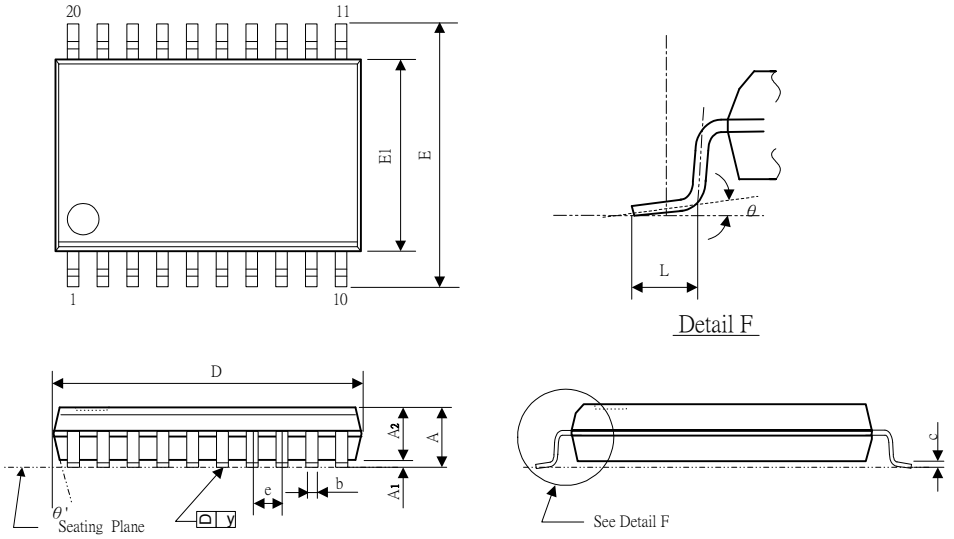
SOP 16L (W.B.) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	2.79 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.400 ± 0.014	10.16 ± 0.36
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 TYP	1.27 TYP
e_1	0.376 NOM.	9.55 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.030 ± 0.008	0.76 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.033 Max.	0.84 Max.
y	0.004 Max.	0.10 Max.
θ	0° - 10°	0° - 10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

TSSOP 20L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.048	---	---	1.20
A1	0.002	---	0.006	0.05	---	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
b	0.007	---	0.012	0.19	---	0.30
C	0.004	---	0.008	0.09	---	0.20
D	0.252	0.256	0.260	6.40	6.50	6.60
E	---	0.252	---	---	6.40	---
E1	0.169	0.173	0.177	4.30	4.40	4.50
e		0.026	---	---	0.65	---
L	0.018	0.024	0.030	0.45	0.60	0.75
y	---	---	0.004	---	---	0.10
θ	0°	---	8°	0°	---	8°
θ'	---	12°	---	---	12°	---

Notes:

1. Package body sizes exclude mold flash protrusions or gate burrs.
2. Tolerance±0.1mm unless otherwise specified.
3. Coplanarity:0.1mm.
4. Controlling dimension is millimeter.Converted inch dimensions are not necessarily exact.

14. Product SPEC. Change Notice

Version	Content	Date
1.0	Original	Jan. 2010

Content