



Enhanced 8051 Microcontroller with 10bit ADC

1. Features

- 8bits micro-controller with Pipe-line structured 8051 compatible instruction set
- Flash ROM: 8K Bytes
- RAM: internal 256 Bytes, external 256 Bytes, LCD RAM 19Bytes
- EEPROM-like: 1K Bytes
- Operation Voltage:
 $f_{OSC} = 32.768kHz - 12.3MHz$, $V_{DD} = 2V - 5.5V$
- Oscillator (code option)
 - Crystal oscillator: 32.768kHz
 - Crystal oscillator: 2MHz - 12.3MHz
 - Ceramic oscillator: 2MHz - 12.3MHz
 - Internal RC: 12.3MHz ($\pm 2\%$)/128K
- 26 CMOS bi-directional I/O pins
- Built-in pull-up resistor for input pin
- Four 16-bit timer/counters T2, T3, T4 and T5
- One 12-bit PWM
- Powerful interrupt sources:
 - Timer2, 3, 4, 5
 - INT2, 3
 - INT40, INT41, INT42, INT43
 - ADC, EUART, SCM, LPD
 - PWM
- EUART0
- 6channels 10-bits Analog Digital Converter (ADC), with comparator function built-in
- Buzzer
- LED driver:
 - 4 X 8 dots (1/4 duty)
- LCD driver:
 - 4 X 12 dots (1/4 duty 1/3 bias)
- Low Voltage Reset (LVR) function (enabled by code option)
 - LVR voltage level 1: 4.3V
 - LVR voltage level 2: 2.1V
- CPU Machine cycle:
1 oscillator clock
- Watch Dog Timer (WDT)
- Warm-up Timer
- Support Low power operation modes:
 - Idle Mode
 - Power-Down Mode
- Flash Type
- Package: SOP28

2. General Description

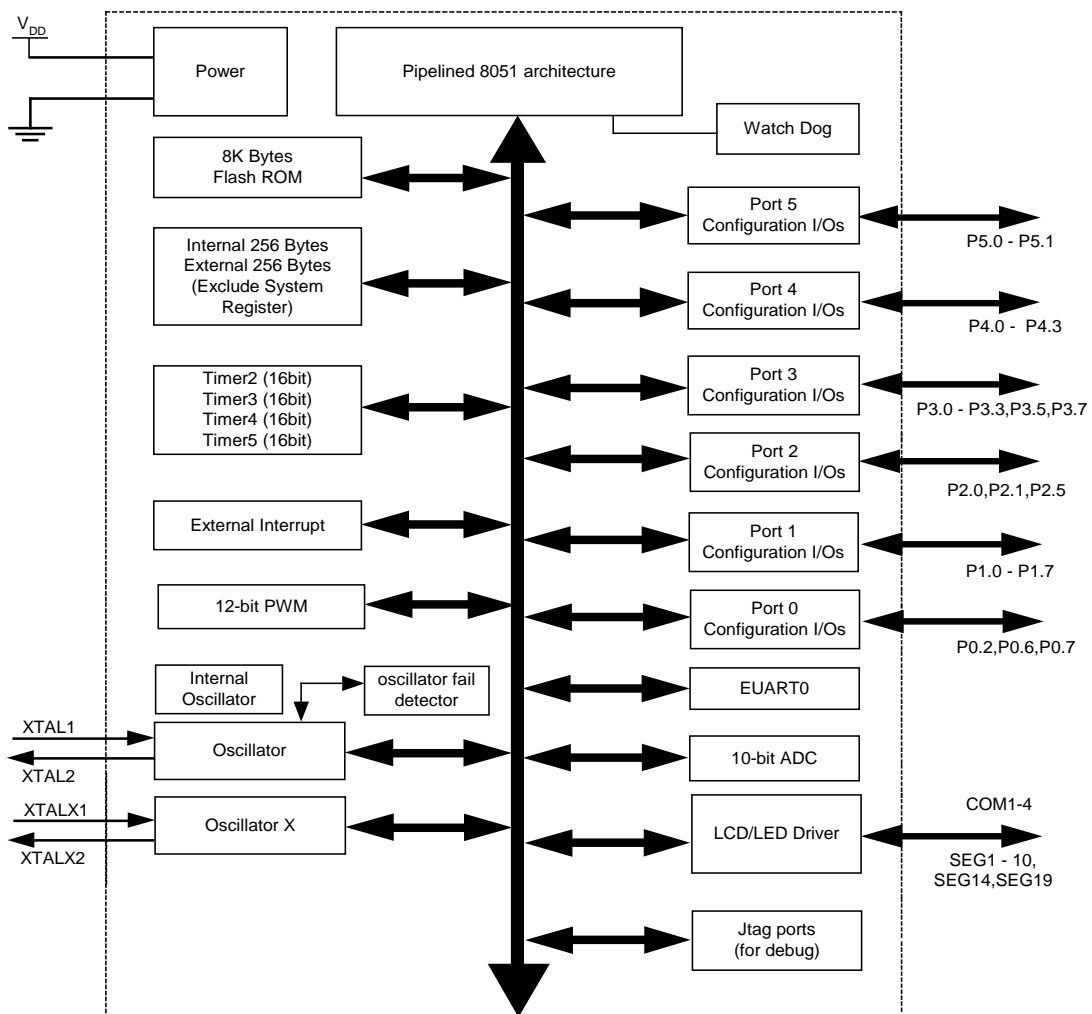
The SH79F0819 is a high performance 8051 compatible micro-controller, regard to its build-in Pipe-line instruction fetch structure, that helps the SH79F0819 can perform more fast operation speed and higher calculation performance, if compare SH79F0819 with standard 8051 at same clock speed.

The SH79F0819 retains most features of the standard 8051. These features include internal 256 bytes RAM, UART and Int2-3. In addition, the SH79F0819 provides external 256 bytes RAM, It also contains four 16-bit timer/counter (Timer2 - Timer5) and 8K bytes Flash memory block both for program and data. Also the ADC and PWM timer functions are incorporated in SH79F0819.

For high reliability and low power consumption, the SH79F0819 builds in Watchdog Timer, Low Voltage Reset function and SCM function. And SH79F0819 also supports two power saving modes to reduce power consumption.

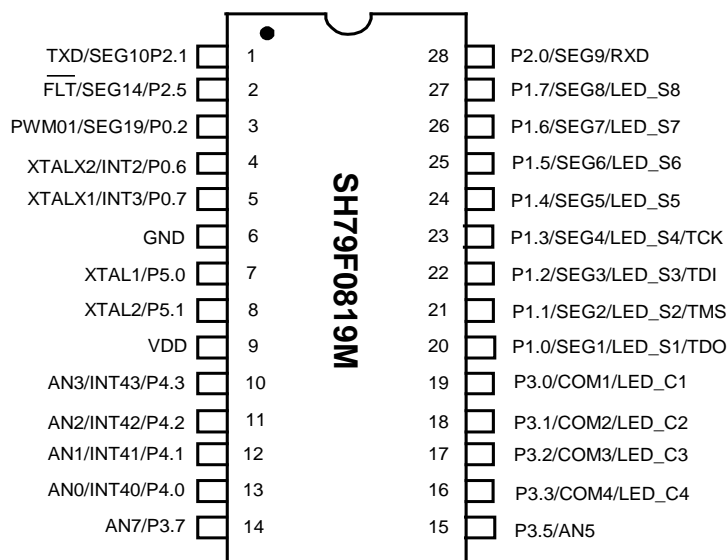


3. Block Diagram





4. Pin Configuration



Pin Configuration Diagram

Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram). This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function use.

Table 4.1 Pin Function

| Pin No. | Pin Name | Default function | Pin No. | Pin Name | Default function |
|---------|------------------|------------------|---------|------------------|------------------|
| 1 | TXD/SEG10/P2.1 | P2.1 | 15 | AN5/P3.5 | P3.5 |
| 2 | FLT/SEG14/P2.5 | P2.5 | 16 | LED_C4/COM4/P3.3 | P3.3 |
| 3 | PWM01/SEG19/P0.2 | P0.2 | 17 | LED_C3/COM3/P3.2 | P3.2 |
| 4 | XTALX2/INT2/P0.6 | P0.6 | 18 | LED_C2/COM2/P3.1 | P3.1 |
| 5 | XTALX1/INT3/P0.7 | P0.7 | 19 | LED_C1/COM1/P3.0 | P3.0 |
| 6 | V _{SS} | ---- | 20 | LED_S1/SEG1/P1.0 | P1.0 |
| 7 | XTAL1/P5.0 | ---- | 21 | LED_S2/SEG2/P1.1 | P1.1 |
| 8 | XTAL2/P5.1 | ---- | 22 | LED_S3/SEG3/P1.2 | P1.2 |
| 9 | V _{DD} | ---- | 23 | LED_S4/SEG4/P1.3 | P1.3 |
| 10 | AN3/INT43/P4.3 | P4.3 | 24 | LED_S5/SEG5/P1.4 | P1.4 |
| 11 | AN2/INT42/P4.2 | P4.2 | 25 | LED_S6/SEG6/P1.5 | P1.5 |
| 12 | AN1/INT41/P4.1 | P4.1 | 26 | LED_S7/SEG7/P1.6 | P1.6 |
| 13 | AN0/INT40/P4.0 | P4.0 | 27 | LED_S8/SEG8/P1.7 | P1.7 |
| 14 | AN7/P3.7 | P3.7 | 28 | RXD/SEG9/P2.0 | P2.0 |



5. Pin Description

| Pin No. | Type | Description |
|--|------|---|
| I/O PORT | | |
| P0.2, P0.6, P0.7 | I/O | 3 bit General purpose CMOS I/O |
| P1.0 - P1.7 | I/O | 8 bit General purpose CMOS I/O |
| P2.0, P2.1, P2.5 | I/O | 3 bit General purpose CMOS I/O |
| P3.0 - P3.3, P3.5, P3.7 | I/O | 6 bit General purpose CMOS I/O |
| P4.0 - P4.3 | I/O | 4 bit General purpose CMOS I/O |
| P5.0 - P5.1 | I/O | 2 bit General purpose CMOS I/O |
| Timer | | |
| T2 | I/O | Timer2 external input |
| T3 | I | Timer3 external input |
| T4 | I/O | Timer4 external input/Comparator output |
| T2EX | I | Timer2 Reload/Capture/Direction Control |
| PWM | | |
| PWM01 | O | Output pin for 12-bit PWM timer with fixed phase relationship of PWM0 |
| FLT | I | PWM Fault Detect input |
| EUART | | |
| RXD | I | EUART0 data input |
| TXD | O | EUART0 data output |
| ADC | | |
| AN0 - AN3, AN5, AN7 | I | ADC input channel |
| LCD | | |
| COM1 - COM4 | O | Common signal output for LCD display |
| SEG1 - SEG10, SEG14, SEG19 | O | Segment signal output for LCD display |
| LED | | |
| LED_C1 - LED_C4 | O | Common signal output for LED display |
| LED_S1 - LED_S8 | O | Segment signal output for LED display |
| Interrupt & Reset & Clock & Power | | |
| INT2 - INT3 | I | External interrupt 2-3 input source |
| INT40 - INT43 | I | External interrupt 40-43 input source |
| XTAL1 | I | Oscillator input |
| XTAL2 | O | Oscillator output |
| XTALX1 | I | OscillatorX input |
| XTALX2 | O | OscillatorX output |
| V _{SS} | P | Ground |
| V _{DD} | P | Power supply (2.0 - 5.5V) |
| Programmer | | |
| TDO (P1.0) | O | Debug interface: Test data out |
| TMS (P1.1) | I | Debug interface: Test mode select |
| TDI (P1.2) | I | Debug interface: Test data in |
| TCK (P1.3) | I | Debug interface: Test clock in |
| Note: When P1.0-1.3 used as debug interface, functions of P1.0-1.3 are blocked. | | |



6. SFR Mapping

The SH79F0819 provides 256 bytes of internal RAM to contain general-purpose data memory and Special Function Register (SFR). The SFR of the SH79F0819 fall into the following categories:

| | |
|---|--|
| CPU Core Registers: | ACC, B, PSW, SP, DPL, DPH |
| Enhanced CPU Core Registers: | AUXC, DPL1, DPH1, INSCON, XPAGE |
| Power and Clock Control Registers: | PCON, SUSLO |
| Flash Registers: | IB_OFFSET, IB_DATA, IB_CON1, IB_CON2, IB_CON3, IB_CON4, IB_CON5, FLASHCON |
| Data Memory Register: | XPAGE |
| Hardware Watchdog Timer Registers: | RSTSTAT |
| System Clock Control Register: | CLKCON |
| Interrupt System Registers: | IEN0, IEN1, IENC, IPH0, IPL0, IPH1, IPL1, EXF0, EXF1 |
| I/O Port Registers: | P0, P1, P2, P3, P4, P5, P0CR, P1CR, P2CR, P3CR, P4CR, P5CR, P0PCR, P1PCR, P2PCR, P3PCR, P4PCR, P5PCR, P0OS |
| Timer Registers: | T2CON, T2MOD, TH2, TL2, RCAP2L, RCAP2H, T3CON, TH3, TL3, T4CON, TH4, TL4, SWTHL, T5CON, TH5, TL5 |
| EUART Registers: | SCON, SBUF, SADEN, SADDR, PCON, RxCON |
| ADC Registers: | ADCON, ADT, ADCH, ADDL, ADDH |
| LCD Registers: | DISPCON, DISPCON1, DISPCLK0, DISPCLK1, P0SS, P1SS, P2SS, P3SS |
| LED Registers: | DISPCON, DISPCLK0, DISPCLK1, P1SS, P3SS |
| PWM Registers: | PWMEN, PWMEN1, PWMLO, PWM0C, PWM0PL, PWM0PH, PWM0DL, PWM0DH |
| LPD Registers: | LPDCON |



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Table 6.1 CPU Core SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------|-----|--------------------------|---------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| ACC | E0H | Accumulator | 00000000 | ACC.7 | ACC.6 | ACC.5 | ACC.4 | ACC.3 | ACC.2 | ACC.1 | ACC.0 |
| B | F0H | B Register | 00000000 | B.7 | B.6 | B.5 | B.4 | B.3 | B.2 | B.1 | B.0 |
| AUXC | F1H | C Register | 00000000 | C.7 | C.6 | C.5 | C.4 | C.3 | C.2 | C.1 | C.0 |
| PSW | D0H | Program Status Word | 00000000 | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| SP | 81H | Stack Pointer | 00000111 | SP.7 | SP.6 | SP.5 | SP.4 | SP.3 | SP.2 | SP.1 | SP.0 |
| DPL | 82H | Data Pointer Low byte | 00000000 | DPL0.7 | DPL0.6 | DPL0.5 | DPL0.4 | DPL0.3 | DPL0.2 | DPL0.1 | DPL0.0 |
| DPH | 83H | Data Pointer High byte | 00000000 | DPH0.7 | DPH0.6 | DPH0.5 | DPH0.4 | DPH0.3 | DPH0.2 | DPH0.1 | DPH0.0 |
| DPL1 | 84H | Data Pointer 1 Low byte | 00000000 | DPL1.7 | DPL1.6 | DPL1.5 | DPL1.4 | DPL1.3 | DPL1.2 | DPL1.1 | DPL1.0 |
| DPH1 | 85H | Data Pointer 1 High byte | 00000000 | DPH1.7 | DPH1.6 | DPH1.5 | DPH1.4 | DPH1.3 | DPH1.2 | DPH1.1 | DPH1.0 |
| INSCON | 86H | Data pointer select | -0--00-0 | - | BKS0 | - | - | DIV | MUL | - | DPS |

Table 6.2 Power and Clock control SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|-----|----------------------|---------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| PCON | 87H | Power Control | 00--0000 | SMOD | SSTAT | - | - | GF1 | GF0 | PD | IDL |
| SUSLO | 8EH | Suspend Mode Control | 00000000 | SUSLO.7 | SUSLO.6 | SUSLO.5 | SUSLO.4 | SUSLO.3 | SUSLO.2 | SUSLO.1 | SUSLO.0 |



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Table 6.3 Flash control SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------------|--------------|--|---------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| IB_OFF SET | FBH Bank0 | Low byte offset of flash memory for programming | 00000000 | IB_OFF SET.7 | IB_OFF SET.6 | IB_OFF SET.5 | IB_OFF SET.4 | IB_OFF SET.3 | IB_OFF SET.2 | IB_OFF SET.1 | IB_OFF SET.0 |
| IB_DATA | FCH Bank0 | Data Register for programming flash memory | 00000000 | IB_DATA.7 | IB_DATA.6 | IB_DATA.5 | IB_DATA.4 | IB_DATA.3 | IB_DATA.2 | IB_DATA.1 | IB_DATA.0 |
| IB_CON1 | F2H Bank0 | Flash Memory Control Register 1 | 00000000 | IB_CON1.7 | IB_CON1.6 | IB_CON1.5 | IB_CON1.4 | IB_CON1.3 | IB_CON1.2 | IB_CON1.1 | IB_CON1.0 |
| IB_CON2 | F3H Bank0 | Flash Memory Control Register 2 | ----0000 | - | - | - | - | IB_CON2.3 | IB_CON2.2 | IB_CON2.1 | IB_CON2.0 |
| IB_CON3 | F4H Bank0 | Flash Memory Control Register 3 | ----0000 | - | - | - | - | IB_CON3.3 | IB_CON3.2 | IB_CON3.1 | IB_CON3.0 |
| IB_CON4 | F5H Bank0 | Flash Memory Control Register 4 | ----0000 | - | - | - | - | IB_CON4.3 | IB_CON4.2 | IB_CON4.1 | IB_CON4.0 |
| IB_CON5 | F6H Bank0 | Flash Memory Control Register 5 | ----0000 | - | - | - | - | IB_CON5.3 | IB_CON5.2 | IB_CON5.1 | IB_CON5.0 |
| XPAGE | F7H Bank0 | Memory Page | ---00000 | - | - | - | XPAGE.4 | XPAGE.3 | XPAGE.2 | XPAGE.1 | XPAGE.0 |
| FLASHCON | A7H Bank0 | Flash access control | -----0 | - | - | - | - | - | - | - | FAC |

Table 6.4 WDT SFR

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---------|--------------|------------------------|---------------------------------|------|------|------|------|------|-------|-------|-------|
| RSTSTAT | B1H Bank0 | Watchdog Timer Control | 0-00-000* | WDOF | - | PORF | LVRF | - | WDT.2 | WDT.1 | WDT.0 |

***Note:** RSTSTAT initial value is determined by different RESET.

Table 6.5 CLKCON SFR

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------|--------------|-------------------------------|---------------------------------|---------------|-------|-------|-------|------|------|------|------|
| CLKCON | B2H Bank0 | System Clock Control Register | 111000-- | 32k_ SPDUP | CLKS1 | CLKS0 | SCMIF | HFON | FS | - | - |



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Table 6.6 Interrupt SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|--------------|------------------------------------|---------------------------------|-----------|-------|-------|-------|-------|-------|-------|-------|
| IEN0 | A8H Bank0 | Interrupt Enable Control 0 | 0000-000 | EA | EADC | ET2 | ES | - | EX1 | ET5 | EX0 |
| IEN1 | A9H Bank0 | Interrupt Enable Control 1 | 0000000- | ESCM/ELPD | ET4 | EPWM | ET3 | EX4 | EX3 | EX2 | - |
| IENC | BAH Bank0 | Interrupt 4channel enable control | ----0000 | - | - | - | - | EXS43 | EXS42 | EXS41 | EXS40 |
| IENC1 | BBH Bank0 | Interrupt channel enable control 1 | -----00 | - | - | - | - | - | - | ESCM1 | ELPD |
| IPH0 | B4H Bank0 | Interrupt Priority Control High 0 | -000—0- | - | PADCH | PT2H | PSH | - | - | PT5H | - |
| IPL0 | B8H Bank0 | Interrupt Priority Control Low 0 | -000—0- | - | PADCL | PT2L | PSL | - | - | PT5L | - |
| IPH1 | B5H Bank0 | Interrupt Priority Control High 1 | 0000000- | PSCMH | PT4H | PPWMH | PT3H | PX4H | PX3H | PX2H | - |
| IPL1 | B9H Bank0 | Interrupt Priority Control Low 1 | 0000000- | PSCML | PT4L | PPWML | PT3L | PX4L | PX3L | PX2L | - |
| EXF0 | E8H Bank0 | External interrupt Control 0 | 00000000 | IT4.1 | IT4.0 | IT3.1 | IT3.0 | IT2.1 | IT2.0 | IE3 | IE2 |
| EXF1 | D8H Bank0 | External interrupt Control 1 | ----0000 | - | - | - | - | IF43 | IF42 | IF41 | IF40 |



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Table 6.7 Port SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|--------------|--------------------------------------|---------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| P0 | 80H Bank0 | 3-bit Port 0 | 00---0-- | P0.7 | P0.6 | - | - | - | P0.2 | - | - |
| P1 | 90H Bank0 | 8-bit Port 1 | 00000000 | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 |
| P2 | A0H Bank0 | 3-bit Port 2 | --0---00 | - | - | P2.5 | - | - | - | P2.1 | P2.0 |
| P3 | B0H Bank0 | 6-bit Port 3 | 0-0-0000 | P3.7 | - | P3.5 | - | P3.3 | P3.2 | P3.1 | P3.0 |
| P4 | C0H Bank0 | 4-bit Port 4 | ----0000 | - | - | - | - | P4.3 | P4.2 | P4.1 | P4.0 |
| P5 | 80H Bank1 | 2-bit Port 5 | -----00 | - | - | - | - | - | - | P5.1 | P5.0 |
| P0CR | E1H Bank0 | Port0 input/output direction control | 00---0-- | P0CR.7 | P0CR.6 | - | - | - | P0CR.2 | - | - |
| P1CR | E2H Bank0 | Port1 input/output direction control | 00000000 | P1CR.7 | P1CR.6 | P1CR.5 | P1CR.4 | P1CR.3 | P1CR.2 | P1CR.1 | P1CR.0 |
| P2CR | E3H Bank0 | Port2 input/output direction control | --0---00 | - | - | P2CR.5 | - | - | - | P2CR.1 | P2CR.0 |
| P3CR | E4H Bank0 | Port3 input/output direction control | 0-0-0000 | P3CR.7 | - | P3CR.5 | - | P3CR.3 | P3CR.2 | P3CR.1 | P3CR.0 |
| P4CR | E5H Bank0 | Port4 input/output direction control | ----0000 | - | - | - | - | P4CR.3 | P4CR.2 | P4CR.1 | P4CR.0 |
| P5CR | E1H Bank1 | Port5 input/output direction control | -----00 | - | - | - | - | - | - | P5CR.1 | P5CR.0 |
| P0PCR | E9H Bank0 | Internal pull-high enable for Port0 | 00---0-- | P0PCR.7 | P0PCR.6 | - | - | - | P0PCR.2 | - | - |
| P1PCR | EAH Bank0 | Internal pull-high enable for Port1 | 00000000 | P1PCR.7 | P1PCR.6 | P1PCR.5 | P1PCR.4 | P1PCR.3 | P1PCR.2 | P1PCR.1 | P1PCR.0 |
| P2PCR | EBH Bank0 | Internal pull-high enable for Port2 | --0---00 | - | - | P2PCR.5 | - | - | - | P2PCR.1 | P2PCR.0 |
| P3PCR | ECH Bank0 | Internal pull-high enable for Port3 | 0-0-0000 | P3PCR.7 | - | P3PCR.5 | - | P3PCR.3 | P3PCR.2 | P3PCR.1 | P3PCR.0 |
| P4PCR | EDH Bank0 | Internal pull-high enable for Port4 | ----0000 | - | - | - | - | P4PCR.3 | P4PCR.2 | P4PCR.1 | P4PCR.0 |
| P5PCR | E9H Bank1 | Internal pull-high enable for Port5 | -----00 | - | - | - | - | - | - | P5PCR.1 | P5PCR.0 |
| P0OS | EFH Bank0 | Output mode control | --00---- | - | - | P0OS.5 | P0OS.4 | - | - | - | - |



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Table 6.8 Timer SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------|--------------|--|---------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| T2CON | C8H Bank0 | Timer/Counter 2 Control | 00000000 | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T2 | CP/RL2 |
| T2MOD | C9H Bank0 | Timer/Counter 2 Mode | -----00 | - | - | - | - | - | - | T2OE | DCEN |
| RCAP2L | CAH Bank0 | Timer/Counter 2 Reload /Caprure Low Byte | 00000000 | RCAP2L.7 | RCAP2L.6 | RCAP2L.5 | RCAP2L.4 | RCAP2L.3 | RCAP2L.2 | RCAP2L.1 | RCAP2L.0 |
| RCAP2H | CBH Bank0 | Timer/Counter 2 Reload /Caprure High Byte | 00000000 | RCAP2H.7 | RCAP2H.6 | RCAP2H.5 | RCAP2H.4 | RCAP2H.3 | RCAP2H.2 | RCAP2H.1 | RCAP2H.0 |
| TL2 | CCH Bank0 | Timer/Counter 2 Low Byte | 00000000 | TL2.7 | TL2.6 | TL2.5 | TL2.4 | TL2.3 | TL2.2 | TL2.1 | TL2.0 |
| TH2 | CDH Bank0 | Timer/Counter 2 High Byte | 00000000 | TH2.7 | TH2.6 | TH2.5 | TH2.4 | TH2.3 | TH2.2 | TH2.1 | TH2.0 |
| T3CON | 88H Bank1 | Timer/Counter 3 Control | 0-00-000 | TF3 | - | T3PS.1 | T3PS.0 | - | TR3 | T3CLKS.1 | T3CLKS.0 |
| SWTHL | 89H Bank1 | Timer/Counter data switch | -----00 | - | - | - | - | - | - | T5HLCON | T3HLCON |
| TL3 | 8CH Bank1 | Timer/Counter 3 Low Byte | 00000000 | TL3.7 | TL3.6 | TL3.5 | TL3.4 | TL3.3 | TL3.2 | TL3.1 | TL3.0 |
| TH3 | 8DH Bank1 | Timer/Counter 3 High Byte | 00000000 | TH3.7 | TH3.6 | TH3.5 | TH3.4 | TH3.3 | TH3.2 | TH3.1 | TH3.0 |
| T4CON | C8H Bank1 | Timer/Counter 4 Control | 00000000 | TF4 | TC4 | T4PS1 | T4PS0 | T4M1 | T4M0 | TR4 | T4CLKS |
| TL4 | CCH Bank1 | Timer/Counter 4 Low Byte | 00000000 | TL4.7 | TL4.6 | TL4.5 | TL4.4 | TL4.3 | TL4.2 | TL4.1 | TL4.0 |
| TH4 | CDH Bank1 | Timer/Counter 4 High Byte | 00000000 | TH4.7 | TH4.6 | TH4.5 | TH4.4 | TH4.3 | TH4.2 | TH4.1 | TH4.0 |
| T5CON | C0H Bank1 | Timer/Counter 5 Control | 0-00--0- | TF5 | - | T5PS1 | T5PS0 | - | - | TR5 | - |
| TL5 | CEH Bank1 | Timer/Counter 5 Low Byte | 00000000 | TL5.7 | TL5.6 | TL5.5 | TL5.4 | TL5.3 | TL5.2 | TL5.1 | TL5.0 |
| TH5 | CFH Bank1 | Timer/Counter 5 High Byte | 00000000 | TH5.7 | TH5.6 | TH5.5 | TH5.4 | TH5.3 | TH5.2 | TH5.1 | TH5.0 |



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Table 6.9 EUART SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|--------------|---------------------------------|---------------------------------|---------|----------|-----------|---------|---------|---------|---------|---------|
| SCON | 98H Bank0 | Serial Control | 00000000 | SM0/FE | SM1/RXOV | SM2/TXCOL | REN | TB8 | RB8 | TI | RI |
| SBUF | 99H Bank0 | Serial Data Buffer | 00000000 | SBUF.7 | SBUF.6 | SBUF.5 | SBUF.4 | SBUF.3 | SBUF.2 | SBUF.1 | SBUF.0 |
| SADEN | 9BH Bank0 | Slave Address Mask | 00000000 | SADEN.7 | SADEN.6 | SADEN.5 | SADEN.4 | SADEN.3 | SADEN.2 | SADEN.1 | SADEN.0 |
| SADDR | 9AH Bank0 | Slave Address | 00000000 | SADDR.7 | SADDR.6 | SADDR.5 | SADDR.4 | SADDR.3 | SADDR.2 | SADDR.1 | SADDR.0 |
| PCON | 87H Bank0 | Power & serial Control | 00--0000 | SMOD | SSTAT | - | - | GF1 | GF0 | PD | IDL |
| RxCON | 9FH Bank0 | Rxd pin Schmidt voltage Control | -----00 | - | - | - | - | - | - | RxCON1 | RxCON0 |

Table 6.10 ADC SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|--------------|---------------------------|---------------------------------|-------|-------|-------|------|------|------|------|---------|
| ADCON | 93H Bank0 | ADC Control | 00000000 | ADON | ADCIF | EC | REFC | SCH2 | SCH1 | SCH0 | GO/DONE |
| ADT | 94H Bank0 | ADC Time Configuration | 000-0000 | TADC2 | TADC1 | TADC0 | - | TS3 | TS2 | TS1 | TS0 |
| ADCH | 95H Bank0 | ADC Channel Configuration | 0-0-0000 | CH7 | - | CH5 | - | CH3 | CH2 | CH1 | CH0 |
| ADDL | 96H Bank0 | ADC Data Low Byte | -----00 | - | - | - | - | - | - | A1 | A0 |
| ADDH | 97H Bank0 | ADC Data High Byte | 00000000 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 |



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Table 6.11 LCD SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------|--------------|----------------|---------------------------------|---------|--------|--------|--------|--------|--------|--------|--------|
| DISPCON | ABH Bank0 | LCD Control | 00000000 | DISPSEL | LCDON | ELCC | DUTY | VOL3 | VOL2 | VOL1 | VOLO |
| DISPCON1 | ADH Bank0 | LCD Control 1 | ---00000 | - | - | - | RLCD | FCCTL1 | FCCTL0 | MOD1 | MOD0 |
| DISPCLK0 | ACH Bank0 | LCD clock 0 | 00000000 | DCK0.7 | DCK0.6 | DCK0.5 | DCK0.4 | DCK0.3 | DCK0.2 | DCK0.1 | DCK0.0 |
| DISPCLK1 | AAH Bank0 | LCD clock 1 | -----0 | - | - | - | - | - | - | - | DCK1.0 |
| P0SS | B6H Bank0 | P0 mode Select | ----0-- | - | - | - | - | - | P0S2 | - | - |
| P1SS | 9CH Bank0 | P1 mode Select | 00000000 | P1S7 | P1S6 | P1S5 | P1S4 | P1S3 | P1S2 | P1S1 | P1S0 |
| P2SS | 9DH Bank0 | P2 mode Select | --0---00 | - | - | P2S5 | - | - | - | P2S1 | P2S0 |
| P3SS | 9EH Bank0 | P3 mode Select | ----0000 | - | - | - | - | P3S3 | P3S2 | P3S1 | P3S0 |

Table 6.12 LED SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------|--------------|----------------|---------------------------------|---------|--------|--------|--------|--------|--------|--------|--------|
| DISPCON | ABH Bank0 | LED Control | 00-0---- | DISPSEL | LEDON | - | DUTY | - | - | - | - |
| DISPCLK0 | ACH Bank0 | LED clock 0 | 00000000 | DCK0.7 | DCK0.6 | DCK0.5 | DCK0.4 | DCK0.3 | DCK0.2 | DCK0.1 | DCK0.0 |
| DISPCLK1 | AAH Bank0 | LED clock 1 | -----0 | - | - | - | - | - | - | - | DCK1.0 |
| P1SS | 9CH Bank0 | P1 mode Select | 00000000 | P1S7 | P1S6 | P1S5 | P1S4 | P1S3 | P1S2 | P1S1 | P1S0 |
| P3SS | 9EH Bank0 | P3 mode Select | ----0000 | - | - | - | - | P3S3 | P3S2 | P3S1 | P3S0 |



SH79F0819

Table 6.13 PWM SFRs

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------|--------------|-------------------------------------|---------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| PWMEN | CFH Bank0 | PWM timer enable | -0--0--0 | - | EFLT | - | - | EPWM01 | - | - | EPWM0 |
| PWMEN1 | B7H Bank0 | PWM output enable | -----0 | - | - | - | - | - | - | - | PWM0 |
| PWMLO | E7H Bank0 | PWM register Lock | 00000000 | PWMLO.7 | PWMLO.6 | PWMLO.5 | PWMLO.4 | PWMLO.3 | PWMLO.2 | PWMLO.1 | PWMLO.0 |
| PWM0C | D2H Bank0 | 12-bit PWM Control | 00-00000 | PWM0IE | PWM0IF | - | FLTS | FLTC | PWM0S | TnCK01 | TnCK00 |
| PWM0PL | D3H Bank0 | 12-bit PWM Period Control low byte | 00000000 | PP0.7 | PP0.6 | PP0.5 | PP0.4 | PP0.3 | PP0.2 | PP0.1 | PP0.0 |
| PWM0PH | D4H Bank0 | 12-bit PWM Period Control high byte | ----0000 | - | - | - | - | PP0.11 | PP0.10 | PP0.9 | PP0.8 |
| PWM0DL | D5H Bank0 | 12-bit PWM Duty Control low byte | 00000000 | PD0.7 | PD0.6 | PD0.5 | PD0.4 | PD0.3 | PD0.2 | PD0.1 | PD0.0 |
| PWM0DH | D6H Bank0 | 12-bit PWM Duty Control high byte | ----0000 | - | - | - | - | PD0.11 | PD0.10 | PD0.9 | PD0.8 |

Table 6.14 LPD SFR

| Mnem | Add | Name | POR/WDT/LVR /PIN Reset Value | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------|--------------|-------------|---------------------------------|-------|------|-------|-------|-------|-------|-------|-------|
| LPDCON | B3H Bank0 | LPD control | 00000000 | LPDEN | LPDF | LPDMD | LPDIF | LPDS3 | LPDS2 | LPDS1 | LPDS0 |

Note: - :Unimplemented



SFR Map
Bank0

| | Bit | Non Bit addressable | | | | | | | | |
|-----|-------------|---------------------|----------|---------|-----------|----------|---------|----------|--|-----|
| | addressable | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | | 7/F |
| F8H | | | | | IB_OFFSET | IB_DATA | | | | FFH |
| F0H | B | AUXC | IB_CON1 | IB_CON2 | IB_CON3 | IB_CON4 | IB_CON5 | XPAGE | | F7H |
| E8H | EXF0 | P0PCR | P1PCR | P2PCR | P3PCR | P4PCR | | | | EFH |
| E0H | ACC | P0CR | P1CR | P2CR | P3CR | P4CR | | PWMLO | | E7H |
| D8H | EXF1 | | | | | | | | | DFH |
| D0H | PSW | | PWM0C | PWM0PL | PWM0PH | PWM0DL | PWM0DH | | | D7H |
| C8H | T2CON | | RCAP2L | RCAP2H | TL2 | TH2 | | PWMEN | | CFH |
| C0H | P4 | | | | | | | | | C7H |
| B8H | IPL0 | IPL1 | IENC | IENC1 | | | | | | BFH |
| B0H | P3 | RSTSTAT | CLKCON | LPDCON | IPH0 | IPH1 | P0SS | PWMEN1 | | B7H |
| A8H | IEN0 | IEN1 | DISPCLK1 | DISPCON | DISPCLK0 | DISPCON1 | | | | AFH |
| A0H | P2 | | | | | | | FLASHCON | | A7H |
| 98H | SCON | SBUF | SADDR | SADEN | P1SS | P2SS | P3SS | RxCON | | 9FH |
| 90H | P1 | | | ADCON | ADT | ADCH | ADDL | ADDH | | 97H |
| 88H | | | | | | | SUSLO | | | 8FH |
| 80H | P0 | SP | DPL | DPH | DPL1 | DPH1 | INSCON | PCON | | 87H |
| | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F | | |

Bank1

| | Bit | Non Bit addressable | | | | | | | | |
|-----|-------------|---------------------|-----|-----|------|------|--------|-------|--|-----|
| | addressable | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | | 7/F |
| F8H | | | | | | | | | | FFH |
| F0H | B | AUXC | | | | | | XPAGE | | F7H |
| E8H | | P5PCR | | | | | | | | EFH |
| E0H | ACC | P5CR | | | | | | | | E7H |
| D8H | | | | | | | | | | DFH |
| D0H | PSW | | | | | | | | | D7H |
| C8H | T4CON | | | | TL4 | TH4 | TL5 | TH5 | | CFH |
| C0H | T5CON | | | | | | | | | C7H |
| B8H | IPL0 | IPL1 | | | | | | | | BFH |
| B0H | | | | | IPH0 | IPH1 | | | | B7H |
| A8H | IEN0 | IEN1 | | | | | | | | AFH |
| A0H | | | | | | | | | | A7H |
| 98H | | | | | | | | | | 9FH |
| 90H | | | | | | | | | | 97H |
| 88H | T3CON | SWTHL | | | TL3 | TH3 | SUSLO | | | 8FH |
| 80H | P5 | SP | DPL | DPH | DPL1 | DPH1 | INSCON | PCON | | 87H |
| | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F | | |

Note: The unused addresses of SFR are not available.



7. Normal Function

7.1 CPU

7.1.1 CPU Core SFR

Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. Instruction system adopts A as mnemonic symbol of accumulator.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits special register, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

Table 7.1 PSW Register

| D0H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| PSW | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | CY | Carry flag bit 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation |
| 6 | AC | Auxiliary Carry flag bit 0: no auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation |
| 5 | F0 | F0 flag bit Available to the user for general purposes |
| 4-3 | RS[1:0] | R0-R7 Register bank select bits 00: Bank0 (Address to 00H-07H) 01: Bank1 (Address to 08H-0FH) 10: Bank2 (Address to 10H-17H) 11: Bank3 (Address to 18H-1FH) |
| 2 | OV | Overflow flag bit 0: no overflow happen 1: an overflow happen |
| 1 | F1 | F1 flag bit Available to the user for general purposes |
| 0 | P | Parity flag bit 0: In the Accumulator, the bits whose value is 1 is even number 1: In the Accumulator, the bits whose value is 1 is odd number |



7.1.2 Enhanced CPU core SFRs

- Extended 'MUL' and 'DIV' instructions: 16bit*8bit, 16bit/8bit
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH79F0819 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register AUXC is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

| | Operation | | Result | | |
|-----|---------------------------|--------------|-------------------|-------------|--------------------|
| | | | A | B | AUXC |
| MUL | INSCON.2 = 0; 8 bit mode | (A)*(B) | Low Byte | High Byte | --- |
| | INSCON.2 = 1; 16 bit mode | (AUXC A)*(B) | Low Byte | Middle Byte | High Byte |
| DIV | INSCON.3 = 0; 8 bit mode | (A)/(B) | Quotient Low Byte | Remainder | --- |
| | INSCON.3 = 1; 16 bit mode | (AUXC A)/(B) | Quotient Low Byte | Remainder | Quotient High Byte |

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is similar to DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer by setting 1 or 0. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

7.1.3 Register

Table 7.2 Data Pointer Select Register

| 86H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| INSCON | - | BKS0 | - | - | DIV | MUL | - | DPS |
| R/W | - | R/W | - | - | R/W | R/W | - | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | 0 | - | - | 0 | 0 | - | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 6 | BKS0 | SFR Bank Selection Bit 0: SFR Bank0 selected 1: SFR Bank1 selected |
| 3 | DIV | 16 bit/8 bit Divide Selection Bit 0: 8 bit Divide 1: 16 bit Divide |
| 2 | MUL | 16 bit/8 bit Multiply Selection Bit 0: 8 bit Multiply 1: 16 bit Multiply |
| 0 | DPS | Data Pointer Selection Bit 0: Data pointer 1: Data pointer1 |



7.2 RAM

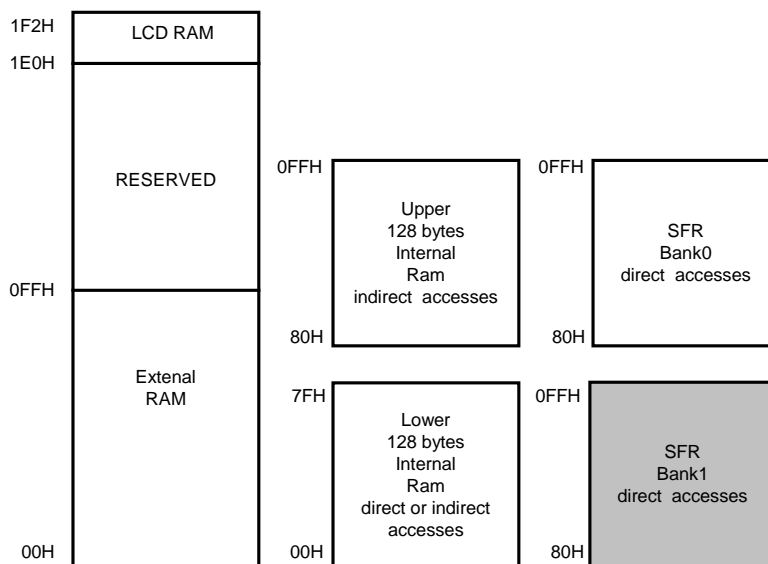
7.2.1 Features

SH79F0819 provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:

- The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.
- The 256 bytes of external RAM (addresses 00H to FFH) are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.

SH79F0819 provides an extra 256 bytes of RAM to support high-level language in external data space. SH79F0819 also provides the 19 bytes of LCD RAM (1E0H-1F2H).



The Internal and External RAM Configuration

The SH79F0819 provides traditional method for accessing of external RAM. Use *MOVXA, @Ri* or *MOVX @Ri, A*; to access external low 256 bytes RAM; *MOVX A, @DPTR* or *MOVX @DPTR, A* also to access external 275 bytes RAM.

In SH79F0819 the user can also use *XPAGE* register to access external RAM only with *MOVX A, @Ri* or *MOVX @Ri, A* instructions. The user can use *XPAGE* to represent the high byte address of RAM above 256 Bytes.

But SH79F0819 only has 256 bytes external RAM, *XPAGE* must be set as 0.

In Flash SSP mode, the *XPAGE* can also be used as sector selector (Refer to SSP Function).

7.2.2 Register

Table 7.3 Data Memory Page Register

| F7H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------------------------------------|------|------|---------|---------|---------|---------|---------|---------|
| XPAGE | - | - | XPAGE.5 | XPAGE.4 | XPAGE.3 | XPAGE.2 | XPAGE.1 | XPAGE.0 |
| R/W | - | - | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | 0 | 0 | 0 | 0 | 0 | 0 |

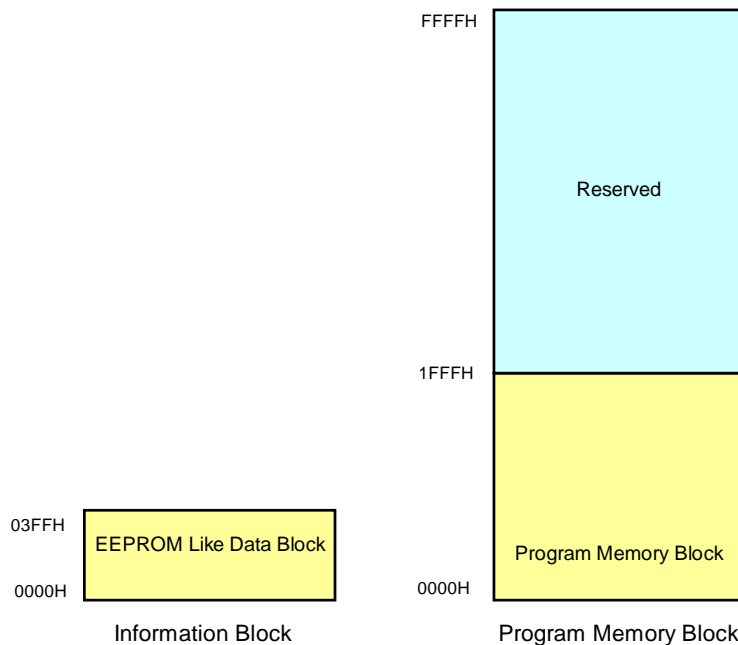
| Bit Number | Bit Mnemonic | Description |
|------------|--------------|-------------------|
| 5-0 | XPAGE[5:0] | RAM Page Selector |



7.3 Flash Program Memory

7.3.1 Features

- The program memory consists 8 X 1KB sectors, total 8KB
- Programming and erase can be done over the full operation voltage range
- Write, read and erase operation are all supported by In-Circuit Programming (ICP)
- Fast mass/sector erase and programming. Sector Erase: < 3ms. Byte Write < 30us
- Minimum program/erase cycles:
Main program memory: 1000
EEPROM like memory: 100,000
- Minimum years data retention: 10
- Low power consumption



The SH79F0819 embeds 8K flash program memory for program code. The flash program memory provides electrical erasure and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode. Every sector is 1024 bytes.

The SH79F0809 also embeds 1024 bytes EEPROM-like register for storing user data. Every sector is 256 bytes. It has 4 sectors.

Flash operation definition:

In-Circuit Programming (ICP): Through the Flash programmer to wipe the Flash memory, read and write operations.

Self-Sector Programming (SSP) mode: User Program code run in Program Memory to wipe the Flash memory, read and write operations.

Flash Memory Supports the Following Operations:

(1) Code Protection Control Mode

SH79F0819 code protection function provides a high-performance security measures for the user. Each partition has two modes are available.

Code protection mode 0: allow/forbid any programmer write/read operations (not including overall erasure).

Code protection mode 1: allow/forbid through MOVC instructions to read operation in other sectors, or through SSP mode to erased/write operation.

The user must use one of the following two ways to complete code protection control mode Settings:

Flash programmer in ICP mode is set to corresponding protection bit to enter the protected mode.

The SSP mode does not support code protection control mode programming.

**(2) Overall Erasure**

Regardless of the state of the code protection control mode, the overall erasure operation will erase all programs, code options, the code protection bit, but they will not erase EEPROM-like memory block.

The user must use the following way to complete the overall erasure:

Flash programmer in ICP mode send overall erasure instruction to run overall erasure.

The SSP mode does not support overall erasure mode.

(3) Sector Erasure

Sector erasure operations will erase the content of selected sector. The user program (SSP) and Flash programmer can perform this operation.

For user programs to perform the operation, code protection mode 1 in the selected sector must be forbidden.

For Flash programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden.

The user must use one of the following two ways to complete sector erasure:

1. Flash programmer in ICP mode send sector erasure instruction to run sector erasure.
2. Through the SSP function send sector erasure instruction to run sector erasure (see chapter SSP).

(4) EEPROM-like Memory Block Erasure

EEPROM-like memory block erasure operations will erase the content in EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.

The user must use one of the following two ways to complete EEPROM-like memory block erasure:

1. Flash programmer in ICP mode send EEPROM-like memory block erasure instruction to run EEPROM-like memory block erasure.
2. Through the SSP function send EEPROM-like memory block erasure instruction to run EEPROM-like memory block erasure (see chapter SSP).

(5) Write/Read Code

Write/read code operation can read or write code from flash memory block. The user program (SSP) and Flash programmer can perform this operation.

For user programs to perform the operation, code protection mode 1 in the selected sector must be forbidden. Regardless of the security bit Settings or not, the user program can read/write the sector which contains program itself .

For Flash programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden.

The user must use one of the following two ways to complete write/read code:

1. Flash programmer in ICP mode send write/read code instruction to run write/read code.
2. Through the SSP function send write/read code instruction to run write/read code.

(6) Write/Read EEPROM-like Memory Block

EEPROM-like memory block operation can read or write data from EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.

The user must use one of the following two ways to complete write/read EEPROM-like memory block:

1. Flash programmer in ICP mode send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.
2. Through the SSP function send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.

Flash Memory Block Operation Summary

| Operation | ICP | SSP |
|-------------------------------------|---------------------------|---------------------------|
| Code protection | Support | Non support |
| Sector erasure | Support (no security bit) | Support (no security bit) |
| Overall erasure | Support | Non support |
| EEPROM-like memory block erasure | Support | Support |
| Write/read code | Support (no security bit) | Support (no security bit) |
| Read/write EEPROM-like memory block | Support | Support |

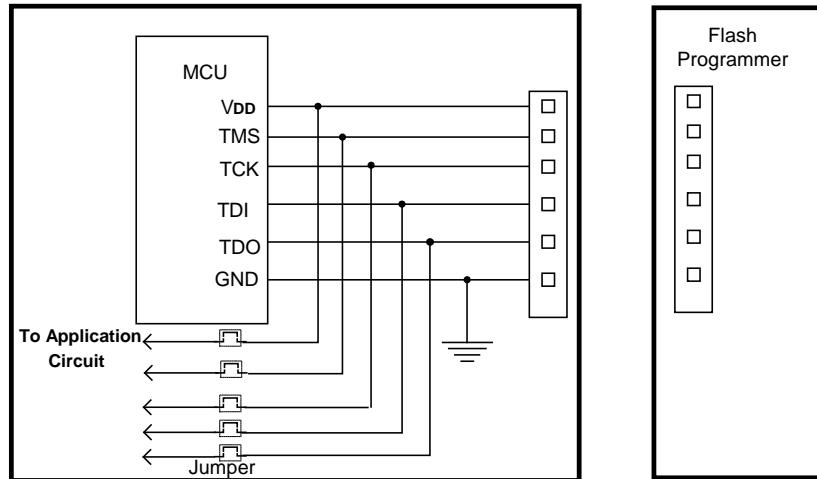


7.3.2 Flash Operation in ICP Mode

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 pins (V_{DD} , GND, TCK, TDI, TMS, TDO).

At first the four JTAG pins (TDO, TDI, TCK, TMS) are used to enter the programming mode. Only after the four pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the FLASH Programmer's user guide.

In ICP mode, all the flash operations are completed by the programmer through 6-wire interface. Since the program timing is very sensitive, 6 jumpers are needed (V_{DD} , GND, TDO, TDI, TCK, TMS) to separate the program pins from the application circuit as show in the following diagram.



The recommended steps are as following:

- (1) The jumpers must be open to separate the programming pins from the application circuit before programming.
- (2) Connect the programming interface with programmer and begin programming.
- (3) Disconnect programmer interface and connect jumpers to recover application circuit after programming is complete.



7.4 SSP Function

The SH79F0819 provides SSP (Self Sector Programming) function, each sector can be sector erased or programmed by the user's code if the selected sector is not be protected. But once sector has been programmed, it cannot be reprogrammed before sector erase.

The SH79F0819 builds in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON2-5), the SSP will be terminated.

7.4.1 SSP Register

Table 7.4 Offset Register for Programming

For program memory block, a sector is 1024 bytes, registers are defined as follows:

| F7H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|---------|---------|---------|---------|---------|
| XPAGE | - | - | - | XPAGE.4 | XPAGE.3 | XPAGE.2 | XPAGE.1 | XPAGE.0 |
| R/W | - | - | - | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 4-2 | XPAGE[4:2] | Sector of the flash memory to be programmed, 0000---means sector 0, and so on |
| 1-0 | XPAGE[1:0] | High 2 Address of the flash memory sector to be programmed |

Table 7.5 Offset Register for erasing and programming

For EEPROM-like memory, a sector is 256 bytes, registers are defined as follows:

| F7H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|---------|---------|---------|---------|---------|
| XPAGE | - | - | - | XPAGE.4 | XPAGE.3 | XPAGE.2 | XPAGE.1 | XPAGE.0 |
| R/W | - | - | - | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 4-2 | XPAGE[4:2] | Reserved |
| 1-0 | XPAGE[1:0] | For EEPROM-like sector,00 means sector 0, and so on |

Table 7.6 Offset of Flash Memory for Programming

| FBH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| IB_OFFSET | IB_OFF SET.7 | IB_OFF SET.6 | IB_OFF SET.5 | IB_OFF SET.4 | IB_OFF SET.3 | IB_OFF SET.2 | IB_OFF SET.1 | IB_OFF SET.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|----------------|---|
| 7-0 | IB_OFFSET[7:0] | Low 8 Address of the flash memory sector to be programmed |

Table 7.7 Data Register for Programming

| FCH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| IB_DATA | IB_DATA.7 | IB_DATA.6 | IB_DATA.5 | IB_DATA.4 | IB_DATA.3 | IB_DATA.2 | IB_DATA.1 | IB_DATA.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|-----------------------|
| 7-0 | IB_DATA[7:0] | Data to be programmed |



Table 7.8 SSP Type select Register

| F2H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| IB_CON1 | IB_CON1.7 | IB_CON1.6 | IB_CON1.5 | IB_CON1.4 | IB_CON1.3 | IB_CON1.2 | IB_CON1.1 | IB_CON1.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-0 | IB_CON1[7:0] | SSP Type select 0xE6: Sector Erase 0x6E: Sector Programming |

Table 7.9 SSP Flow Control Register1

| F3H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|-----------|-----------|-----------|-----------|
| IB_CON2 | - | - | - | - | IB_CON2.3 | IB_CON2.2 | IB_CON2.1 | IB_CON2.0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 3-0 | IB_CON2[3:0] | Must be 05H, otherwise Flash Programming will terminate |

Table 7.10 SSP Flow Control Register2

| F4H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|-----------|-----------|-----------|-----------|
| IB_CON3 | - | - | - | - | IB_CON3.3 | IB_CON3.2 | IB_CON3.1 | IB_CON3.0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 3-0 | IB_CON3[3:0] | Must be 0AH, otherwise Flash Programming will terminate |

Table 7.11 SSP Flow Control Register3

| F5H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|-----------|-----------|-----------|-----------|
| IB_CON4 | - | - | - | - | IB_CON4.3 | IB_CON4.2 | IB_CON4.1 | IB_CON4.0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 3-0 | IB_CON4[3:0] | Must be 09H, otherwise Flash Programming will terminate |

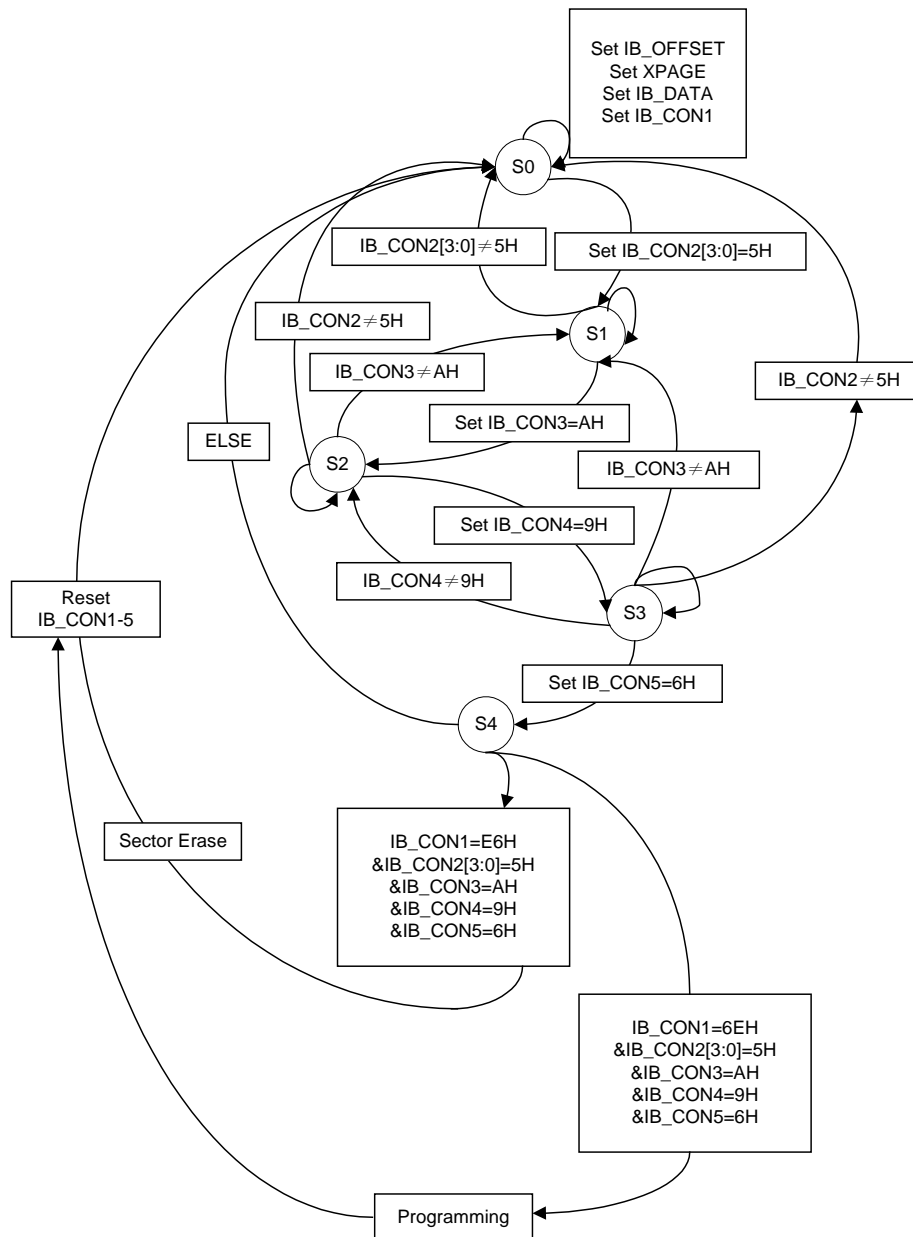
Table 7.12 SSP Flow Control Register4

| F6H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|-----------|-----------|-----------|-----------|
| IB_CON5 | - | - | - | - | IB_CON5.3 | IB_CON5.2 | IB_CON5.1 | IB_CON5.0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 3-0 | IB_CON5[3:0] | Must be 06H, otherwise Flash Programming will terminate |



7.4.2 Flash Control Flow





7.4.3 SSP Programming Notice

To successfully complete SSP programming, the user's software must be set as the following the steps:

(1) For Code/Data Programming:

1. Disable interrupt;
2. Fill in the XPAGE, IB_OFFSET for the corresponding address;
3. Fill in IB_DATA if programming is wanted;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Code/Data programming, CPU will be in IDLE mode;
7. Go to Step 2 if more data are to be programmed;
8. Clear XPAGE; enable interrupt if necessary.

(2) For Sector Erase:

1. Disable interrupt;
2. Fill in the XPAGE for the corresponding sector;
3. Fill in IB_CON1-5 sequentially;
4. Add 4 NOPs for more stable operation;
5. Sector Erase, CPU will be in IDLE mode;
6. Go to step 2 if more sectors are to be erased;
7. Clear XPAGE; enable interrupt if necessary.

(3) For Code Reading:

Just Use "MOVC A, @A+DPTR" or "MOVC A, @A+PC".

(4) For EEPROM-Like:

Steps is same as code programming,the diffenrences are:

1. Set FAC bit in FLASHCON register before programming or erase EEPROM-Like;
2. One sector of EEPROM-Like is 256 bytes.not 1024 bytes.

Note:

1. The system clock is not less than 200 KHZ to ensure normal FLASH programming
2. FAC must be cleared when you don't need to do EEPROM-like operation.

FLASHCON register description is as follows:

Table 7.13 Flash Access Control Register

| A7H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| FLASHCON | - | - | - | - | - | - | - | FAC |
| R/W | - | - | - | - | - | - | - | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | - | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-1 | - | Reserved |
| 0 | FAC | FAC: Flash access control 0: MOVC or SSP access main memory 1: MOVC or SSP access EEPROM-like |



7.5 System Clock and Oscillator

7.5.1 Features

- Four oscillator types: 32.768kHz crystal, crystal oscillator, ceramic oscillator and 12.3MHz/128kHz internal RC
- 4 Oscillator pin (XTAL1, XTAL2, XTALX1, XTALX2), one or two clocks are generated from those 4 kinds of oscillators
- Built-in 12.3MHz Internal RC
- Built-in 32.768kHz speed up circuit
- Built-in system clock prescaler

7.5.2 Clock Definition

The SH79F0819 have several internal clocks defined as follow:

OSCCLK: the oscillator clock is selected from the three oscillator types (32.768kHz crystal oscillator, crystal oscillator, ceramic oscillator and 12.3MHz/128kHz internal RC form XTAL input) f_{OSC} is defined as the OSCCLK frequency. t_{OSC} is defined as the OSCCLK period.

OSCXCLK: the oscillator clock is selected from the three oscillator types (crystal oscillator, ceramic oscillator and 12.3MHz internal RC from XTALX input) f_{OSCX} is defined as the OSCXCLK frequency. t_{OSCX} is defined as the OSCXCLK period.

Note: OSCXCLK does not exist when code option OP_OSC is not 0011, 0110, 1010, 1101. (32.768kHz oscillator/128kHz internal RC is not selected, Refer to **code option** section for details)

WDTCLK: the internal WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK period.

OSCSCLK: the input clock of system clock frequency prescaler. It can be OSCCLK or OSCXCLK. f_{OSCS} is defined as the OSCSCLK frequency. t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output clock of system clock frequency prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency. t_{SYS} is defined as the SYSCLK period.

7.5.3 Description

SH79F0819 has five oscillator types: 32.768kHz crystal oscillator, crystal oscillator (2MHz-12.3MHz), ceramic Oscillator (2MHz-12.3MHz) and internal RC (12.3MHz,128K), which is selected by code option OP_OSC (Refer to code option section for details). SH79F0819 have 4 Oscillator pin (XTAL1, XTAL2, XTALX1, XTALX2) and can generates one or two clock sources from four oscillator types. It is selected by code option OP_OSC (Refer to **code option** section for details). The oscillator generates the basic clock pulse that provides the system clock to supply CPU and on-chip peripherals.



7.5.4 Register

Table 7.14 System Clock Control Register

| B2H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-----------|-------|-------|-------|------|------|------|------|
| CLKCON | 32k_SPDUP | CLKS1 | CLKS0 | SCMIF | HFON | FS | - | - |
| R/W | R/W | R/W | R/W | R | R/W | R/W | - | - |
| Reset Value (POR/WDT/LVR/PIN) | 1 | 1 | 1 | 0 | 0 | 0 | - | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | 32k_SPDUP | <p>32.768kHz oscillator speed up mode control bit 0: 32.768kHz oscillator normal mode, cleared by software. 1: 32.768kHz oscillator speed up mode, set by hardware or software. This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. And this bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when Power-down mode wakes up. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption. Only when code option OP_OSC is 1010 or 1101, this bit is valid. (32.768kHz oscillator is selected, Refer to code option section for details)</p> |
| 6-5 | CLKS[1:0] | <p>SYCLK Prescaler Register 00: $f_{sys} = f_{osc}$ 01: $f_{sys} = f_{osc}/2$ 10: $f_{sys} = f_{osc}/4$ 11: $f_{sys} = f_{osc}/12$ If 32.768kHz oscillator is selected as OSCSCLK, these control bits is invalid.</p> |
| 3 | HFON | <p>OSCXCLK On-off control Register 0: turn off OSCXCLK 1: turn on OSCXCLK Only when code option OP_OSC is 0011, 0110, 1010, 1101. this bit is valid. (32.768kHz oscillator/128kHz internal RC is selected, Refer to code option section for details)</p> |
| 2 | FS | <p>Frequency Select Register 0: 32.768kHz/128kHz is selected as OSCSCLK 1: OSCXCLK is selected as OSCSCLK Only when code option OP_OSC is 0011, 0110, 1010, 1101. this bit is valid. (32.768kHz oscillator/128kHz internal RC is selected, Refer to code option section for details)</p> |

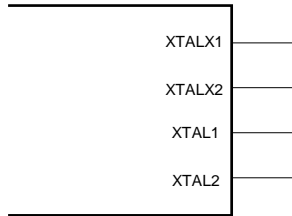
Note:

- (1) If code option OP_OSC is 0011, 1010, OSCXCLK is built-in 12.3MHzRC; if code option OP_OSC is 0110 or 1101, OSCXCLK is crystal or ceramic oscillator from XTALX input.
- (2) HFON and FS is valid only when code option OP_OSC is 0011, 0110, 1010, 1101.
- (3) When OSCXCLK is used as OSCSCLK (that is HFON = 1 and FS = 1), HFON is can't be cleared by software.
- (4) When OSCSCLK changed from 32.768kHz/128kHz to OSCXCLK, if OSCXCLK is off, the setting must be done as the following steps:
 - a. Set HFON = 1 to turn on the OSCXCLK
 - b. Wait at least Oscillator Warm-up timer (Refer to **Warm-up Timer** section for details)
 - c. Set FS = 1 to select OSCXCLK as OSCSCLK
- (5) When OSCSCLK changed from OSCXCLK to 32.768kHz/128kHz, the setting must be done as the following steps:
 - a. Clear FS to select 32.768kHz/128kHz as OSCSCLK
 - b. Add one nop
 - c. Clear HFON (reducing power consumption)

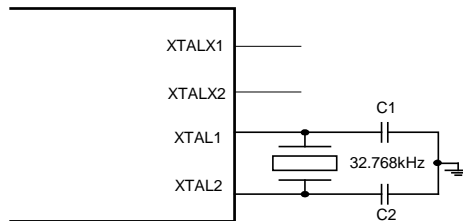


7.5.5 Oscillator Type

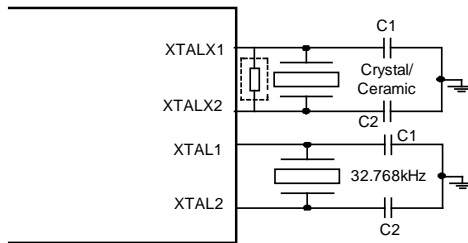
(1) OP_OSC = 0000, 0011: internal RC, XTAL and XTALX are shared with I/O



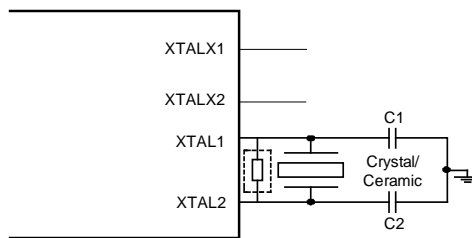
(2) OP_OSC = 1010: 32.768kHz Crystal Oscillator at XTAL, Internal RC can be enabled, XTALX is shared with I/O



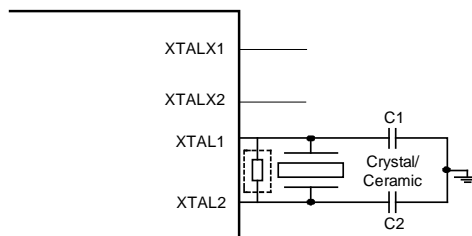
(3) OP_OSC = 1101: 32.768kHz Crystal Oscillator at XTAL, 2M - 12.3M Crystal/Ceramic Oscillator at XTALX*



(4) OP_OSC = 1110: 2M - 12.3M Crystal/Ceramic oscillator at XTAL*, XTALX is shared with I/O



(5) OP_OSC = 0110: 128kHz internal RC, 2M - 12.3M Crystal/Ceramic resonator at XTAL*, XTALX is shared with I/O



*: If the environment humidity is bigger, use the high frequency oscillator, advice plus 510k feedback resistance.



7.5.6 Capacitor Selection for Oscillator

| Ceramic Resonators | | |
|--------------------|----|----|
| Frequency | C1 | C2 |
| 3.58MHz | - | - |
| 4MHz | - | - |

| Crystal Oscillator | | |
|--------------------|-----------|-----------|
| Frequency | C1 | C2 |
| 32.768kHz | 10 - 12pF | 10 - 12pF |
| 4MHz | 8 - 15pF | 8 - 15pF |
| 12.3MHz | 8 - 15pF | 8 - 15pF |

Notes:

(1) **Capacitor values are used for design guidance only!**

(2) These capacitors were tested with the crystals listed above for basic start-up and operation. They are **not optimized**.

(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit <http://www.sinowealth.com> for more recommended manufactures.



7.6 System Clock Monitor (SCM)

In order to enhance the system reliability, SH79F0819 contains a system clock monitor (SCM) module. If the system clock breaks down (for example the external oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal 32k WDTCLK and set system clock monitor bit (SCMIF) to 1. And the SCM interrupt will be generated when EA and ESCM is enabled. If the external oscillator comes back, SCM will switch the OSCCLK back to the oscillator and clears the SCMIF automatically.

Notes:

The SCMIF is read only register; it can be clear to 0 or set to 1 by hardware only.

If SCMIF is cleared, the SCM switches the system clock to the state before system clock fail automatically.

If Internal RC is selected as OSCCLK by code option (Refer to **code option** section for detail), the SCM can not work.

Table 7.15 System Clock Control Register

| B2H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|------|------|------|-------|------|------|------|------|
| CLKCON | - | - | - | SCMIF | - | - | - | - |
| R/W | - | - | - | R | - | - | - | - |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | 0 | - | - | - | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 4 | SCMIF | System Clock Monitor flag bit 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails |



7.7 I/O Port

7.7.1 Features

- 26 bi-directional I/O ports
- Share with alternative functions

The SH79F0819 has 26 bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x = 0-5, y = 0-7).

For SH79F0819, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions conflicts when all the functions are enabled. (Refer to **Port Share** Section for details).

7.7.2 Register

Table 7.16 Port Control Register

| E1H - E5H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| P0CR (E1H, Bank0) | P0CR.7 | P0CR.6 | - | - | - | P0CR.2 | - | - |
| P1CR (E2H, Bank0) | P1CR.7 | P1CR.6 | P1CR.5 | P1CR.4 | P1CR.3 | P1CR.2 | P1CR.1 | P1CR.0 |
| P2CR (E3H, Bank0) | - | - | P2CR.5 | - | - | - | P2CR.1 | P2CR.0 |
| P3CR (E4H, Bank0) | P3CR.7 | - | P3CR.5 | - | P3CR.3 | P3CR.2 | P3CR.1 | P3CR.0 |
| P4CR (E5H, Bank0) | - | - | - | - | P4CR.3 | P4CR.2 | P4CR.1 | P4CR.0 |
| P5CR (E1H, Bank1) | - | - | - | - | - | - | P5CR.1 | P5CR.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|---------------------------|---|
| 7-0 | PxCRy x = 0-5, y = 0-7 | Port input/output control Register 0: input mode 1: output mode |

Table 7.17 Port Pull up Resistor Control Register

| E9H - ECH | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| P0PCR (E9H, Bank0) | P0PCR.7 | P0PCR.6 | - | - | - | P0PCR.2 | - | - |
| P1PCR (EAH, Bank0) | P1PCR.7 | P1PCR.6 | P1PCR.5 | P1PCR.4 | P1PCR.3 | P1PCR.2 | P1PCR.1 | P1PCR.0 |
| P2PCR (EBH, Bank0) | - | - | P2PCR.5 | - | - | - | P2PCR.1 | P2PCR.0 |
| P3PCR (ECH, Bank0) | P3PCR.7 | - | P3PCR.5 | - | P3PCR.3 | P3PCR.2 | P3PCR.1 | P3PCR.0 |
| P4PCR (EDH, Bank0) | - | - | - | - | P4PCR.3 | P4PCR.2 | P4PCR.1 | P4PCR.0 |
| P5PCR (E9H, Bank1) | - | - | - | - | - | - | P5PCR.1 | P5PCR.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|----------------------------|--|
| 7-0 | PxPCRy x = 0-5, y = 0-7 | Input Port internal pull-high resistor enable/disable control 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled |

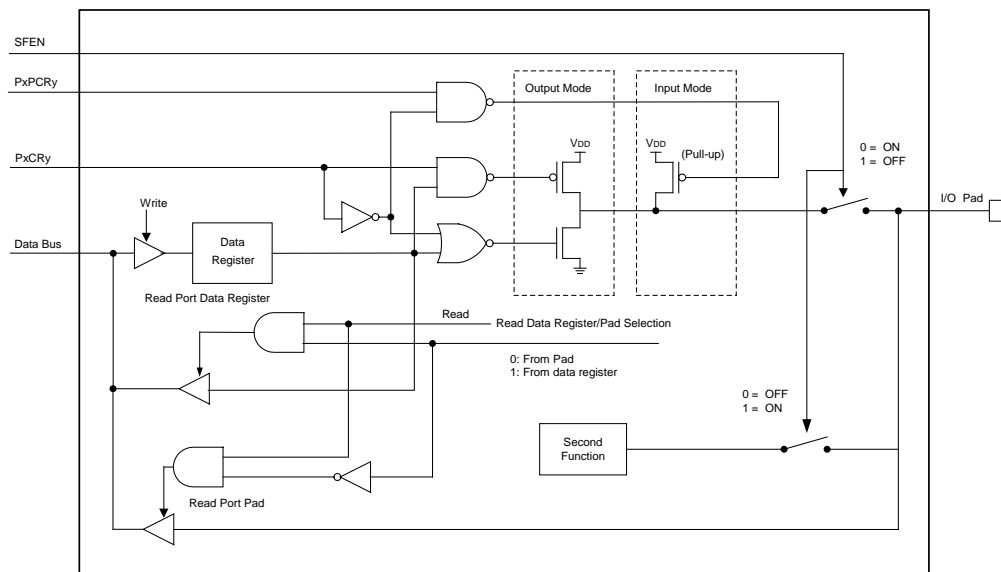


Table 7.18 Port Data Register

| 80H - C0H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P0 (80H, Bank0) | P0.7 | P0.6 | - | - | - | P0.2 | - | - |
| P1 (90H, Bank0) | P1.7 | P1.6 | P1.5 | P1.4 | P1.3 | P1.2 | P1.1 | P1.0 |
| P2 (A0H, Bank0) | - | - | P2.5 | - | - | - | P2.1 | P2.0 |
| P3 (B0H, Bank0) | P3.7 | - | P3.5 | - | P3.3 | P3.2 | P3.1 | P3.0 |
| P4 (C0H, Bank0) | - | - | - | - | P4.3 | P4.2 | P4.1 | P4.0 |
| P5 (80H, Bank1) | - | - | - | - | - | - | P5.1 | P5.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------------------|--------------------|
| 7-0 | Px.y x = 0-5, y = 0-7 | Port Data Register |

7.7.3 Port Diagram



Note:

- (1) The input source of reading input port operation is from the input pin directly.
- (2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly.
- (3) The read Instruction distinguishes which path is selected: The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.
- (4) The destination of writing port operation is the data register regardless of the port shared as the second function or not



7.7.4 Port Share

The 26 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Most Inner Lest** rule:

The out most pin function in **Pin Configuration** has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin, even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resistor is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 0-5), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register The value of the port pin keeps unchanged until the second function was disabled.

PORT0:

- LCD Segment19 (P0.2)
- PWM01: PWM01 output (P0.2)
- INT2: external interrupt2 (P0.6)
- INT3: external interrupt3 (P0.7)
- XTALX1: XTAL input (P0.7)
- XTALX2: XTAL output (P0.6)

Table 7.19 PORT0 Share Table

| Pin No. | Priority | Function | Enable bit |
|---------|----------|----------|---|
| 3 | 1 | PWM01 | Set EPWM01 bit in PWMEN register |
| | 2 | SEG19 | Clear DISPSEL bit in DISPCON register and set P0S2 bit in P0SS register |
| | 3 | P0.2 | Above condition is not met |
| 4 | 1 | XTALX2 | Selected by Code Option |
| | 2 | INT2 | Set EX2 bit in IEN1 Register and P0.6 is in input mode |
| | 3 | P0.6 | Above condition is not met |
| 5 | 1 | XTALX1 | Selected by Code Option |
| | 2 | INT3 | Set EX3 bit in IEN1 Register and P0.7 is in input mode |
| | 3 | P0.7 | Above condition is not met |

PORT1:

- LED Segment 1-8 (P1.0-P1.7)
- LCD Segment 1-8 (P1.0-P1.7)

Table 7.20 PORT1 Share Table

| Pin No. | Priority | Function | Enable bit |
|---------|----------|------------|--|
| 20-27 | 1 | LED S1-8 | Set DISPSEL bit in DISPCON register and set P1S0-P1S7 bit in P1SS register |
| | 2 | LCD SEG1-8 | Clear DISPSEL bit in DISPCON register and set P1S0-P1S7 bit in P1SS register |
| | 3 | P1.0-P1.7 | Above condition is not met |



PORT2:

- RXD: EUART data input (P2.0)
- TXD: EUART data output (P2.1)
- FLT: Fault input pin (P2.5)
- LCD Segment 9, 10, 14 (P2.0, P2.1, P2.5)

Table 7.21 PORT2 Share Table

| Pin No. | Priority | Function | Enable bit |
|---------|----------|----------|---|
| 28 | 1 | RXD | Set REN bit in SCON Register (Auto Pull up) |
| | 2 | SEG9 | Clear DISPSEL bit in DISPCON register and set P2S0 bit in P2SS register |
| | 3 | P2.0 | Above condition is not met |
| 1 | 1 | TXD | When Write to SBUF Register |
| | 2 | SEG10 | Clear DISPSEL bit in DISPCON register and set P2S1 bit in P2SS register |
| | 3 | P2.1 | Above condition is not met |
| 2 | 1 | FLT | Set EFLT bit in PWMEN register |
| | 2 | SEG14 | Clear DISPSEL bit in DISPCON register and set P2S5 bit in P2SS register |
| | 3 | P2.5 | Above condition is not met |

PORT3:

- LED COM1-COM4 (P3.0-P3.3)
- LCD COM1-COM4 (P3.0-P3.3)
- AN5, AN7: ADC input channel (P3.5, P3.7)

Table 7.22 PORT3 Share Table

| Pin No. | Priority | Function | Enable bit |
|---------|----------|-------------------|---|
| 14, 15 | 1 | AN7, AN5 | Set CH7, CH5 bits in ADCH Register and set ADON bit in ADCON Register, and set SCH[2:0] |
| | 2 | P3.7, P3.5 | Above condition is not met |
| 16-19 | 1 | LED_C4 -LED_C1 | Set P3S3-P3S0 bits in P3SS register and set DISPSEL bit and DUTY bit in DISPCON register |
| | 2 | COM4-COM1 | Set P3S3-P3S0 bits in P3SS register, clear DISPSEL bit in DISPCON register |
| | 3 | P3.3-P3.0 | Above condition is not met |

PORT4:

- INT40-INT43 (P4.0-P4.3): External interrupt input
- AN0-AN3 (P4.0-P4.3): ADC input channel

Table 7.23 PORT4 Share Table

| Pin No. | Priority | Function | Enable bit |
|---------|----------|-------------|---|
| 16-19 | 1 | AN3-AN0 | Set CH3-0 bit in ADCH Register and set SCH[2:0] |
| | 2 | INT43-INT40 | Set EX4 bit in IEN1 register and EXS43-40 bit in IENC register, P4.3-P4.0 in input mode |
| | 3 | P4.3-P4.0 | Above condition is not met |

PORT5:

- XTAL1 (P5.0): XTAL input
- XTAL2 (P5.1): XTAL output

Table 7.24 PORT5 Share Table

| Pin No. | Priority | Function | Enable bit |
|---------|----------|----------|----------------------------|
| 8 | 1 | XTAL1 | Selected by Code Option |
| | 2 | P5.0 | Above condition is not met |
| 9 | 1 | XTAL2 | Selected by Code Option |
| | 2 | P5.1 | Above condition is not met |



7.8 Timer

7.8.1 Features

- The SH79F0819 has four timers (Timer2, 3, 4, 5)
- Timer2 & Timer4 are 16-bit auto-reload timer, they can be selected as a baud-rate generator.
- Timer3 is a 16-bit auto-reload timer and can operate even in Power-Down mode
- Timer5 is a 16-bit auto-reload timer

7.8.2 Timer2

The Timer 2 is implemented as a 16-bit register accessed as two cascaded data registers: TH2 and TL2. It is controlled by the register T2CON and T2MOD. The Timer2 interrupt can be enabled by setting the ET2 bit in the IEN0 register. (Refer to Interrupt Section for details)

Timer2 Modes

Timer2 has 2 operating modes: Auto-reload mode with up counter and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2.

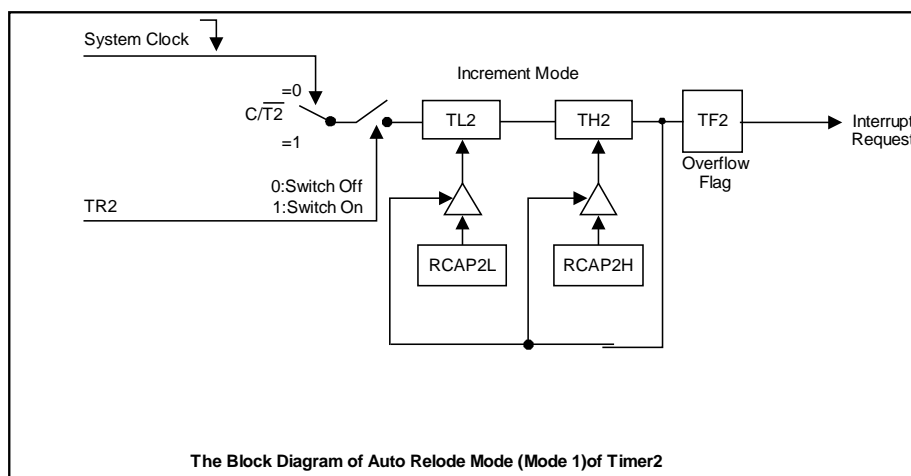
Table 7.25 Timer2 Mode select

| C/T2 | T2OE | DCEN | TR2 | CP/RL2 | RCLK | TCLK | Mode | |
|------|------|------|-----|--------|------|------|------|--------------------------|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 16 bit auto-reload timer |
| 0 | 0 | 0 | 1 | 0 | 1 | X | 2 | Baud-Rate generator |
| | | | | | X | 1 | | |

Mode1: 16 bit auto-reload Timer

Set CP/RL2 = 0, C/T2 = 0, EXEN2 = 0 and T2MOD is cleared. The Timer 2 is implemented as a 16-bit auto-reload timer with up counter.

Timer2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded to TH2&TL2 registers with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software. The TF2 bit can generate an interrupt if ET2 is enabled.





Mode2: Baud-Rate Generator

Timer2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be different if Timer2 is used for the receiver or transmitter and Timer4 is used for the other.

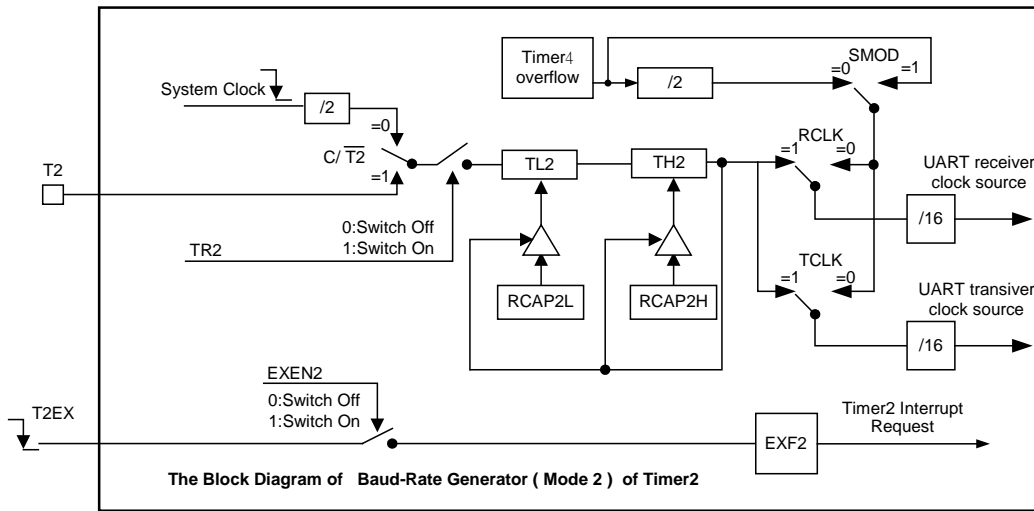
Setting RCLK and/or TCLK will put Timer2 into its baud rate generator mode, which is similar to the auto-reload mode.

Set CP/RL2 = 0, C/T2 = 0, EXEN2 = 0 and T2MOD is cleared.

Over flow of Timer2 will causes the Timer2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L that preset by software. But this will not generate an interrupt.

The baud rate in EUART Modes1 and 3 is determined by Timer2's overflow rate according to the following equation.

$$\text{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{\text{SYS}}}{65536 - [\text{RCAP2H}, \text{RCAP2L}]} ; \overline{\text{C/T2}} = 0$$



Note:

- (1) Set TF2 to 1 when incident happens or at anytime by software, only software&hardware reset can clear it.
- (2) When EA = 1 and ET2 = 1, setting TF2 to 1 to generate Timer2 interrupt.
- (3) When Timer2 is used as baud-rate generator, write in TH2/TL2. Write in RCAP2H/RCAP2L will effect the veracity of baud rate. It also will cause communication error.



Registers

Table 7.26 Timer2 Control Register

| C8H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|-------|------|--------------------|----------------------|
| T2CON | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T $\overline{2}$ | CP/RL $\overline{2}$ |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|----------------------|--|
| 7 | TF2 | Timer2 overflow flag bit 0: No overflow(must be cleared by software) 1: Overflow (Set by hardware if RCLK = 0 & TCLK = 0) |
| 6 | EXF2 | This bit must write 0 |
| 5 | RCLK | EUART0 Receive Clock control bit 0: Timer 4 generates receiveing baud-rate 1: Timer 2 generates receiveing baud-rate |
| 4 | TCLK | EUART0 Transmit Clock control bit 0: Timer4 generates transmitting baud-rate 1: Timer 2 generates transmitting baud-rate |
| 3 | EXEN2 | This bit must write 0 |
| 2 | TR2 | Timer2 start/stop control bit 0: Stop Timer2 1: Start Timer2 |
| 1 | C/T $\overline{2}$ | This bit must write 0 |
| 0 | CP/RL $\overline{2}$ | This bit must write 0 |

Table 7.27 Timer2 Mode Control Register

| C9H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| T2MOD | - | - | - | - | - | - | T2OE | DCEN |
| R/W | - | - | - | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|------------------------------|
| 1 | T2OE | This bit must write 0 |
| 0 | DCEN | This bit must write 0 |



Table 7.28 Timer2 Reload/Capture & Data Registers

| CAH-CDH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--|----------|----------|----------|----------|----------|----------|----------|----------|
| RCAP2L | RCAP2L.7 | RCAP2L.6 | RCAP2L.5 | RCAP2L.4 | RCAP2L.3 | RCAP2L.2 | RCAP2L.1 | RCAP2L.0 |
| RCAP2H | RCAP2H.7 | RCAP2H.6 | RCAP2H.5 | RCAP2H.4 | RCAP2H.3 | RCAP2H.2 | RCAP2H.1 | RCAP2H.0 |
| TL2 | TL2.7 | TL2.6 | TL2.5 | TL2.4 | TL2.3 | TL2.2 | TL2.1 | TL2.0 |
| TH2 | TH2.7 | TH2.6 | TH2.5 | TH2.4 | TH2.3 | TH2.2 | TH2.1 | TH2.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-0 | RCAP2L.x | Timer2 Reload/Capturer Data Low & High byte, x = 0 - 7 |
| | RCAP2H.x | |
| 7-0 | TL2.x | Timer2 Low & High byte counter, x = 0 - 7 |
| | TH2.x | |



7.8.3 Timer3

Timer3 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH3 and TL3. It is controlled by the T3CON register. The Timer3 interrupt can be enabled by setting ET3 bit in IEN1 register (Refer to **Interrupt** Section for details).

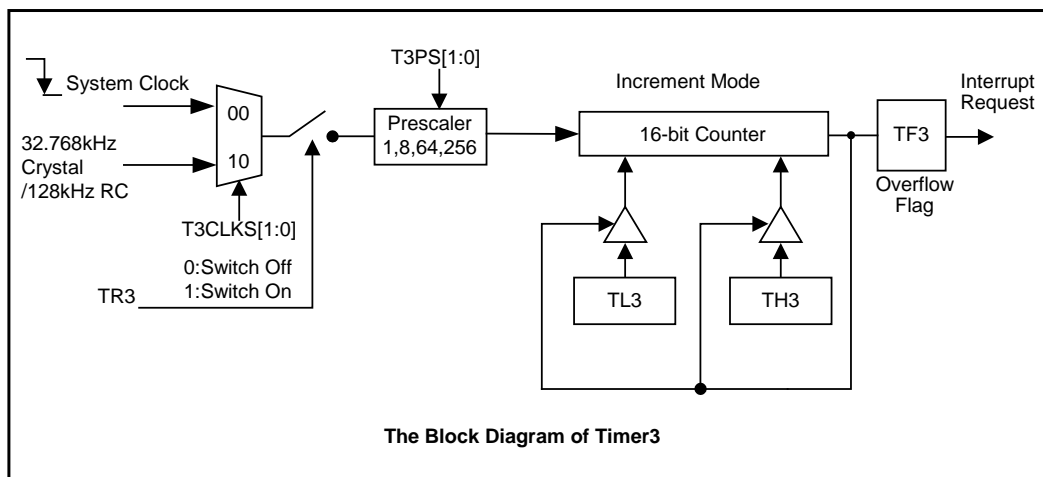
Timer3 has only one operating mode: 16-bit Counter/Timer with auto-reload. Timer3 also supports the following features: selectable pre-scaler setting and Operation during CPU Power-Down mode.

Timer3 consists of a 16-bit Counter/Timer register (TH3, TL3). When writing to TH3 and TL3, they are used as timer reload register. When reading from TH3 and TL3, they are used as Counter register. Setting the TR3 bit enables Timer 3 to count up. The Timer will overflow from 0xFFFF to 0x0000 and set the TF3 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH3 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH3 and TL3 should follow these steps:

Write operation: Low bits first, High bits followed.

Read operation: High bits first, Low bits followed.



Timer3 can operate even in Power-Down mode.

When OP_OSC[3:0] (Refer to Code Option Section for details) is 1010, 1101, 0011 or 0110, T3CLKS[1:0] can select 00 or 10. When OP_OSC[3:0] is not 1010, 1101, 0011 or 0110, T3CLKS[1:0] can select 00, and 10 will be an invalid value.

If T3CLKS[1:0] is 00, Timer 3 can't work in Power Down mode. If T3CLKS[1:0] is 10 and OP_OSC[3:0] is 1010, 1101, 0011 or 0110, Timer3 can work in CPU normal operating or Power Down mode. If T3CLKS[1:0] is 10 and OP_OSC[3:0] is not 1010, 1101, 0011 or 0110, Timer3 can't work. It can be described in the following table.

| OP_OSC[3:0] | T3CLKS[1:0] | Can work in normal mode | Can work in Power Down mode |
|------------------------------|-------------|-------------------------|-----------------------------|
| 1010, 1101, 0011 or 0110 | 00 | YES | NO |
| | 10 | YES | YES |
| Not 1010, 1101, 0011 or 0110 | 00 | YES | NO |
| | 10 | NO | NO |

Note: When TH3 and TL3 read or written, must make sure TR3 = 0.



Registers

Table 7.29 Timer3 Control Register

| 88H, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|--------|--------|------|------|----------|----------|
| T3CON | TF3 | - | T3PS.1 | T3PS.0 | - | TR3 | T3CLKS.1 | T3CLKS.0 |
| R/W | R/W | - | R/W | R/W | - | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | - | 0 | 0 | - | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | TF3 | Timer3 overflow flag bit 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware) |
| 5-4 | T3PS[1:0] | Timer3 input clock Prescaler Select bits 00: 1/1 01: 1/8 10: 1/64 11: 1/256 |
| 2 | TR3 | Timer3 start/stop control bit 0: Stop Timer3 1: Start Timer3 |
| 1-0 | T3CLKS[1:0] | Timer3 Counter/Timer mode select bits 00: System clock 01: Reserved 10: 32.768kHz from external Crystal or 128k RC 11: Reserved |

Table 7.30 Timer3 Reload/Counter Data Registers

| 8CH-8DH, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| TL3 | TL3.7 | TL3.6 | TL3.5 | TL3.4 | TL3.3 | TL3.2 | TL3.1 | TL3.0 |
| TH3 | TH3.7 | TH3.6 | TH3.5 | TH3.4 | TH3.3 | TH3.2 | TH3.1 | TH3.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|----------------|---|
| 7-0 | TL3.x TH3.x | Timer3 Low & High byte counter, x = 0 - 7 |

Table 7.31 Timer3 Reload/Count Data Register

| 89H, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|--------|--------|
| SWTHL | - | - | - | - | - | - | T5HLCN | T3HLCN |
| R/W | - | - | - | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 0 | T3HLCN | 0: when read TH3, TL3, return T3 count data 1: when read TH3, TL3, return T3 reload register data |



7.8.4 Timer4

Timer4 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH4 and TL4. It is controlled by the T4CON register. The Timer 4 interrupt can be enabled by setting ET4 bit in IEN1 register (Refer to **interrupt** Section for details).

When writing to TH4 and TL4, they are used as timer reload register. When reading from TH4 and TL4, they are used as counter register. Setting the TR4 bit enables Timer 4 to count up. The timer will overflow from 0xFFFF to 0x0000 and set the TF4 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH4 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH4 and TL4 should follow these steps:

Write operation: Low bits first, High bits followed

Read operation: High bits first, Low bits followed

Timer4 Modes

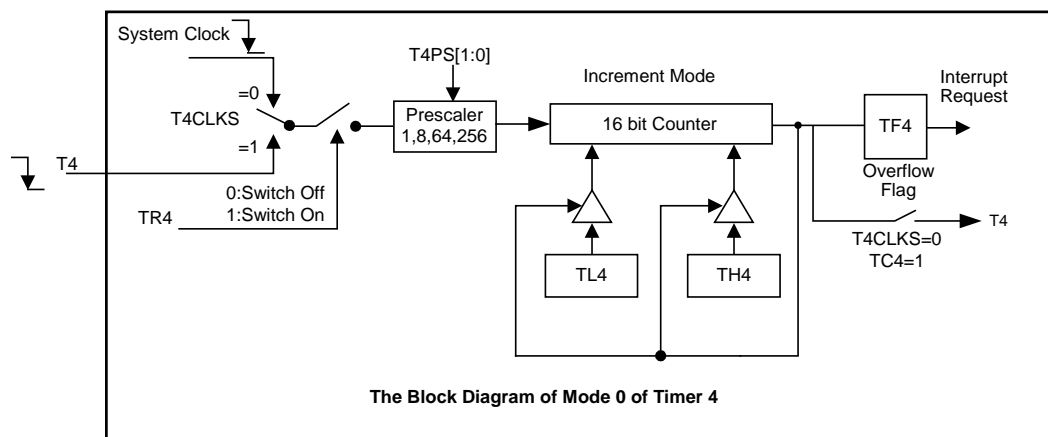
Timer4 has 2 operating modes: 16-bit auto-reload counter/timer, Baud Rate Generator. These modes are selected by T4M[1:0] bits in T4CON Register.

Mode0: 16 bit Auto-Reload Counter/Timer

Timer4 operates as 16-bit counter/timer in Mode 0. The TH4 register holds the high eight bits of the 16-bit counter/timer, TL4 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF4 (T4CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer 4 interrupts is enabled.

The T4CLKS bit (T4CON.0) selects the counter/timer's clock source.

Setting the TR4 bit (T4CON.1) enables the timer. Setting TR4 does not force the timer to reset. The timer load register should be loaded with the desired initial value before the timer is enabled.



Mode1: Baud-Rate Generator

Timer4 is selected as the baud rate generator by setting T4M[1:0] bit in T4CON register. The baud rates for transmit and receive can be different if Timer2 is used for the receiver or transmitter and Timer4 is used for the other.

The mode is similar to the auto-reload mode. Overflow of Timer4 will causes the Timer4 counter register to be reloaded with the 16-bit value in timer load register. But this will not generate an interrupt.

The baud rates in EUART mode1 and mode3 are determined by Timer4's overflow rate according to the following equation.

$$\text{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{\text{SYS}} / \text{PRESCALER}}{65536 - [\text{TH4}, \text{TL4}]}, \quad \text{T4CLKS} = 0$$

Here, TH4 and TL4 stand for Timer4 reload register.

Note:

When Timer4 is running (TR4 = 1) as a timer in the baud rate generator mode, TH4 or TL4 should not be written. Because timer may increase at every state time, it can cause an accurate result about read or write. So Timer4 must be turned off (TR4 = 0) before visiting TH4/TL4.



Registers

Table 7.32 Timer4 Control Register

| C8H, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|-------|-------|------|------|------|--------|
| T4CON | TF4 | - | T4PS1 | T4PS0 | T4M1 | T4M0 | TR4 | T4CLKS |
| R/W | R/W | - | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | TF4 | Timer4 overflow flag bit 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware) |
| 6 | - | This bit must write 0 |
| 5-4 | T4PS[1:0] | Timer4 input clock Prescale Select bits 00: 1/1 01: 1/8 10: 1/64 11: 1/256 |
| 3-2 | T4M[1:0] | Timer4 Mode Select bit 00: Mode0, 16-bit auto-reload counter/timer 01: Mode1, baud-rate generator for EUART 10: Reserved 11: Reserved |
| 1 | TR4 | Timer4 start/stop control bit 0: Stop Timer4 1: Start Timer4 |
| 0 | T4CLKS | Timer4 Clock Source select bit 0: System clock 1: Reserved |

Note: T4CLKS bit must be set to 0, select System clock.

Table 7.33 Timer4 Reload/Counter Data Registers

| CCH-CDH, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| TL4 | TL4.7 | TL4.6 | TL4.5 | TL4.4 | TL4.3 | TL4.2 | TL4.1 | TL4.0 |
| TH4 | TH4.7 | TH4.6 | TH4.5 | TH4.4 | TH4.3 | TH4.2 | TH4.1 | TH4.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|----------------|---|
| 7-0 | TL4.x TH4.x | Timer4 Low & High byte counter, x = 0 - 7 |



7.8.5 Timer5

Timer5 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH5 and TL5. It is controlled by the T5CON register. The interrupt can be enabled by setting ET5 bit in IEN0 register (Refer to **interrupt** Section for details).

When writing to TH5 and TL5, they are used as timer reload register. When reading from TH5 and TL5, they are used as counter register. Setting the TR5 bit enables Timer5 to count up. The timer will overflow from 0xFFFF to 0x0000 and set the TF5 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH5 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH5 and TL5 should follow these steps:

Write operation: Low bits first, High bits followed

Read operation: High bits first, Low bits followed

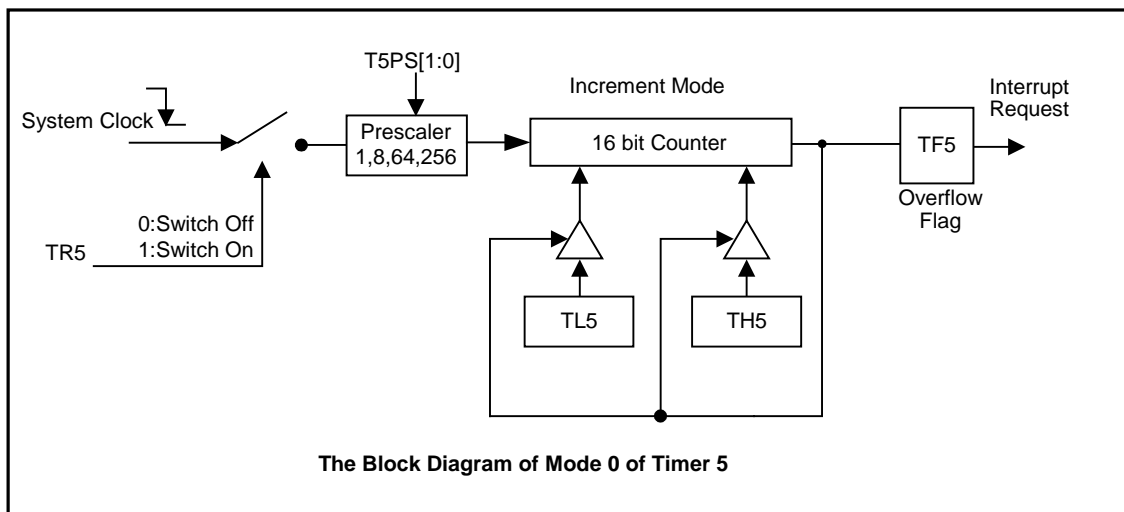
Timer5 Modes

Timer5 has one operating modes: 16-bit auto-reload counter/timer.

16 bit Auto-Reload Counter/Timer

Timer5 operates as 16-bit counter/timer in Mode 0. The TH5 register holds the high eight bits of the 16-bit counter/timer, TL5 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF5 (T5CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer 5 interrupts is enabled.

Setting the TR5 bit (T5CON.1) enables the timer. Setting TR5 does not force the timer to reset. The timer load register should be loaded with the desired initial value before the timer is enabled.





Registers

Table 7.34 Timer5 Control Register

| C0H, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|-------|-------|------|------|------|------|
| T5CON | TF5 | - | T5PS1 | T5PS0 | - | - | TR5 | - |
| R/W | R/W | - | R/W | R/W | - | - | R/W | - |
| Reset Value (POR/WDT/LVR/PIN) | 0 | - | 0 | 0 | - | - | 0 | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | TF5 | Timer5 overflow flag bit 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware) |
| 5-4 | T5PS[1:0] | Timer5 input clock Prescale Select bits 00: 1/1 01: 1/8 10: 1/64 11: 1/256 |
| 1 | TR5 | Timer5 start/stop control bit 0: Stop Timer5 1: Start Timer5 |

Table 7.35 Timer5 Reload/Counter Data Registers

| CEH-CFH, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| TL5 | TL5.7 | TL5.6 | TL5.5 | TL5.4 | TL5.3 | TL5.2 | TL5.1 | TL5.0 |
| TH5 | TH5.7 | TH5.6 | TH5.5 | TH5.4 | TH5.3 | TH5.2 | TH5.1 | TH5.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|----------------|---|
| 7-0 | TL5.x TH5.x | Timer5 Low & High byte counter, x = 0 - 7 |

Table 7.36 Timer5 Reload/Count Data Register

| 89H, Bank1 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|---------|---------|
| SWTHL | - | - | - | - | - | - | T5HLCON | T3HLCON |
| R/W | - | - | - | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 1 | T5HLCON | 0: when read TH5, TL5, return T5 count data 1: when read TH5, TL5, return T5 reload register data |



7.9 Interrupt

7.9.1 Feature

- 12 interrupt sources
- 4 interrupt priority levels

The SH79F0819 provides total 12 interrupt sources: 3 external interrupts (INT2/3/4; INT4 including INT40-43, which share the same vector address), 4 timer interrupts (Timer2, 3, 4, 5), one EUART interrupt, ADC interrupt, PWM interrupts, SCM interrupt and LPD interrupt.

7.9.2 Interrupt Enable Control

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

7.9.3 Registers

Table 7.37 Primary Interrupt Enable Register

| A8H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|------|------|------|------|------|------|------|------|
| IEN0 | EA | EADC | ET2 | ES | - | EX1 | ET5 | EX0 |
| R/W | R/W | R/W | R/W | R/W | - | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | - | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | EA | All interrupt enable bit 0: Disable all interrupt 1: Enable all interrupt |
| 6 | EADC | ADC interrupt enable bit 0: Disable ADC interrupt 1: Enable ADC interrupt |
| 5 | ET2 | Timer2 overflow interrupt enable bit 0: Disable Timer2 overflow interrupt 1: Enable Timer2 overflow interrupt |
| 4 | ES | EUART0 interrupt enable bit 0: Disable EUART0 interrupt 1: Enable EUART0 interrupt |
| 2 | EX1 | This bit must write 0 |
| 1 | ET5 | Timer5 overflow interrupt enable bit 0: Disable Timer5 overflow interrupt 1: Enable Timer5 overflow interrupt |
| 0 | EX0 | This bit must write 0 |

Note: Register IEN0[0] and IEN0[2] must be set to 0.



Table 7.38 Secondary Interrupt Enable Register

| A9H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|-----------|------|------|------|------|------|------|------|
| IEN1 | ESCM/ELPD | ET4 | EPWM | ET3 | EX4 | EX3 | EX2 | - |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | - |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | ESCM/ELPD | SCM/LPD interrupt enable bit 0: Disable SCM/LPD interrupt 1: Enable SCM/LPD interrupt |
| 6 | ET4 | Timer4 overflow interrupt enable bit 0: Disable Timer4 overflow interrupt 1: Enable Timer4 overflow interrupt |
| 5 | EPWM | PWM interrupt enable bit 0: Disable PWM interrupt 1: Enable PWM interrupt |
| 4 | ET3 | Timer3 overflow interrupt enable bit 0: Disable timer3 overflow interrupt 1: Enable timer3 overflow interrupt |
| 3 | EX4 | External interrupt4 enable bit 0: Disable external interrupt4 1: Enable external interrupt4 |
| 2 | EX3 | External interrupt3 enable bit 0: Disable external interrupt3 1: Enable external interrupt3 |
| 1 | EX2 | External interrupt2 enable bit 0: Disable external interrupt2 1: Enable external interrupt2 |

Note:

- (1) To enable External interrupt2/3/4, the corresponding port must be set to input mode before using it.
- (2) To enable PWM timer interrupt, the EPWM bit here should be set. Also, the PWMIE in PWM interrupt control register should be set.

Table 7.39 Interrupt channel Enable Register

| BAH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|------|------|------|------|-------|-------|-------|-------|
| IENC | - | - | - | - | EXS43 | EXS42 | EXS41 | EXS40 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------------|--|
| 3-0 | EXS4x (x = 3-0) | External interrupt4 channel select bit (x = 3-0) 0: Disable external interrupt 4x 1: Enable external interrupt 4x |



Table 7.40 Interrupt channel Enable Register1

| BBH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|------|------|------|------|------|------|-------|------|
| IENC1 | - | - | - | - | - | - | ESCM1 | ELPD |
| R/W | - | - | - | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 1 | ESCM1 | SCM interrupt enable bit 0: Disable SCM interrupt 1: Enable SCM interrupt |
| 0 | ELPD | LPD interrupt enable bit 0: Disable LPD interrupt 1: Enable LPD interrupt |

7.9.4 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in interrupt abstract table.

When an external interrupt INT2/3 is generated, if the interrupt was edge triggered, the flag IEx (x = 0-3) that generated this interrupt is cleared by hardware when the service routine is vectored. If the interrupt was level triggered, then the requesting external source directly controls the request flag, rather than the on-chip hardware.

When INT4 generates an interrupt, the flag (IF4x (x = 0-3) in EXF1 register) that generated this interrupt should be cleared by user's program because the same vector entrance was used in INT4x. But if INT4x is set up as level triggered, the flag can't be cleared by user's program, it only be controlled by peripheral signal level that connect to INT source pin.

The **Timer2 interrupt** is generated by the logical OR of flag TF2 in T2CON register, which is set by hardware. None of these flags can be cleared by hardware after CPU responses to the interrupt, the flag must be cleared by software.

When the Timer3 counter overflow, set interrupt flag bit TF3 in T3CON to 1 to generate Timer3 interrupt. The flag will be cleared automatically by hardware after CPU responses to the interrupt.

When the Timer4 counter overflow, set interrupt flag bit TF4 in T4CON to 1 to generate Timer4 interrupt. The flag will be cleared automatically by hardware after CPU responses to the interrupt.

When the Timer5 counter overflow, set interrupt flag bit TF5 in T5CON to 1 to generate Timer5 interrupt. The flag will be cleared automatically by hardware after CPU responses to the interrupt.

The **EUART interrupt** is generated by the logical OR of flag RI and TI in SCON register, which is set by hardware. Neither of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the receive interrupt flag or the transmission interrupt flag that generated the interrupt, so the flag must be cleared by software.

The **ADC interrupt** is generated by ADCIF bit in ADCON. If an interrupt is generated, the converted result in ADCDH/ADCDL will be valid. If continuous compare function in ADC module is Enable, ADCIF will not be clear at each conversion when conversion results is less than the compare value. But if converted result is larger than compare value, ADCIF bit will be 1. The flag must be cleared by software.

The **SCM interrupt** is generated by SCMIF in SCM register, which is set by hardware. And the flag can only be cleared by hardware.

The **LPD interrupt** is generated by LPDF in LPDCON register. And the flag can only be cleared by hardware. By setting the LPDMD, can choose when the V_{DD} voltage is above or below the LPD set generated when the detecting voltage interruption of LPD.

The **PWM interrupts** are generated by PWM0IF in PWM0C. The flags can be cleared by software.



Table 7.41 External Interrupt Flag Register

| E8H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|------|------|
| EXF0 | IT4.1 | IT4.0 | IT3.1 | IT3.0 | IT2.1 | IT2.0 | IE3 | IE2 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-6 | IT4[1:0] | External interrupt4 trigger mode selection bit 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge IT4 [1:0] is effect on external interrupt 4x at the same mode |
| 5-4 | IT3[1:0] | External interrupt3 trigger mode selection bit 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge |
| 3-2 | IT2[1:0] | External interrupt2 trigger mode selection bit 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge |
| 1 | IE3 | External interrupt3 request flag bit 0: No interrupt pending 1: Interrupt is pending |
| 0 | IE2 | External interrupt2 request flag bit 0: No interrupt pending 1: Interrupt is pending |

Table 7.42 External Interrupt4 Flag Register

| D8H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| EXF1 | - | - | - | - | IF43 | IF42 | IF41 | IF40 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|-------------------|--|
| 3-0 | IF4x (x = 3-0) | External interrupt4 request flag bit 0: No interrupt pending 1: Interrupt is pending IF4x is cleared by software |



7.9.5 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in **Interrupt Summary table**.

7.9.6 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If the same priority interrupt source apply for the interrupt at the beginning of the instruction cycle at the same time, an internal polling sequence determines which request is serviced.

| Interrupt Priority | | |
|--------------------|------|----------------------------|
| Priority bits | | Interrupt Level Priority |
| IPHx | IPLx | |
| 0 | 0 | Level 0 (lowest priority) |
| 0 | 1 | Level 1 |
| 1 | 0 | Level 2 |
| 1 | 1 | Level 3 (highest priority) |

Table 7.43 Interrupt Priority Control Registers

| B8H, B4H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|------|------|------|------|------|
| IPL0 | - | PADCL | PT2L | PSL | - | - | PT5L | - |
| IPH0 | - | PADCH | PT2H | PSH | - | - | PT5H | - |
| R/W | - | R/W | R/W | R/W | - | - | R/W | - |
| Reset Value (POR/WDT/LVR/PIN) | - | 0 | 0 | 0 | - | - | 0 | - |
| B9H, B5H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| IPL1 | PSCML | PT4L | PPWML | PT3L | PX4L | PX3L | PX2L | - |
| IPH1 | PSCMH | PT4H | PPWMH | PT3H | PX4H | PX3H | PX2H | - |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | - |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-0 | PxxxL/H | Corresponding interrupt source xxx's priority level selection bits |



7.9.7 Interrupt Handling

The interrupt flags are sampled and captured at each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, LCALL generated by hardware is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current cycle is not in the final cycle of the instruction in progress. In other words, any interrupt request can not get response before executing instructions to complete.

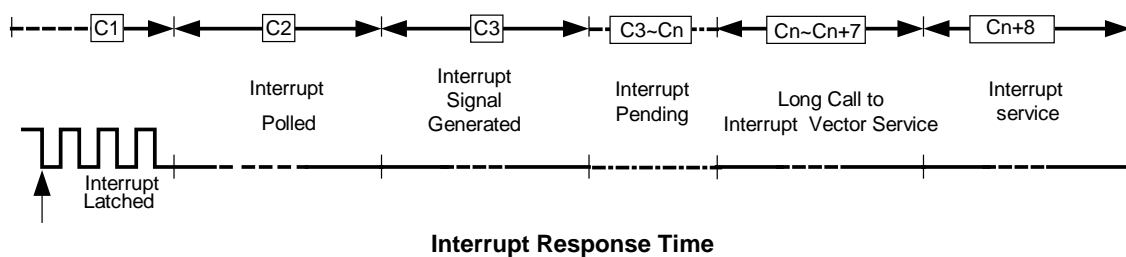
The instruction in progress is RETI or visit the special register IEN01 or IPLH instruction. This ensures that if the instruction in progress is RETI or read and write IEN01 or IPLH then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Note:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.

The polling cycle/LCALL sequence is illustrated below:



Interrupt Response Time

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW). Then vector address of the corresponding interrupt source (referring to the interrupt vector table) will be stored in the program counter.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. The RET instruction can also return to the original address to continue, but the interrupt priority control system still think the interrupt in a same priority is responded, in this case, the same priority or lower priority interrupt will not be responded.

7.9.8 Interrupt Response Time

If an interrupt is detected, its request flag will be set in every machine cycle after detection. The value will be kept by the internal circuitry until the next machine cycle; the CPU will generate an interrupt at the third machine cycle. If the request is active and conditions are right for it to be acknowledged, hardware instruction LCALL will call service routine which request interrupt at the next instruction to be executed. Otherwise the interrupt will pending. The call itself takes 7 machine cycles. Therefore, from the external interrupt request to start the implementation of interrupt program requires at least 3+7 completed machine cycle.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the length of the other interrupt's service routine.

If the instruction in progress is not in its final cycle and the instruction in progress is RETI, the additional wait time is 8 machine cycles. For a single interrupt system, if the next instruction is 20 machine cycles long (the longest instructions DIV & MUL are 20 machine cycles long for 16 bit operation), adding the LCALL instruction 7 machine cycles the total response time is 2+8+20+7 machine cycles.

Thus interrupt response time is always more than 10 machine cycles and less than 37 machine cycles.



7.9.9 External Interrupt Inputs

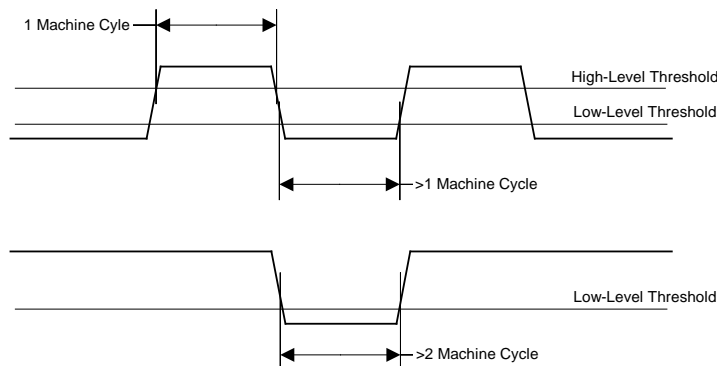
The SH79F0819 has 3 external interrupt inputs. External interrupt2-3 each has one vector address. External interrupt 4 has 4 inputs sharing an interrupt vector address. These external interrupts can be programmed to be level-triggered by clearing or setting bit ITx[1:0] (x = 2-4) in register EXF0. In the falling edge trigger mode, INTx (x = 2, 3) pin continue to be sampled as the high level in a period and it will be sampled as low level at next period. when the interrupt request flag bit in register EXF0 is set to 1, it will send an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

If the external interrupt is edge-triggered, the external source has to hold the request pin high level (low level) for at least one machine cycle, and then hold it low level (high level) for at least one machine cycle. This ensures that the edge can be detected to set IEx (x = 2-3) or IF4x (x = 0-3) to 1. When calling the interrupt service program, CPU will automatically clear IEx. IF4x will be cleared by software.

If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 system clock cycles. If the external interrupt is still valid when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag IEx (x = 2, 3) or IF4x (x = 0-3) when the interrupt is triggered by level, it simply tracks the input pin level.

If an external interrupt is enabled when the SH79F0819 is put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation. (Refer to "Power Management" section for details)

Note: IE2-3 is automatically cleared by hardware when the service routine is called while IF40-43 should be cleared by software.



7.9.10 Interrupt Summary

| Source | Vector Address | Enable bits | Flag bits | Polling Priority | Interrupt number (C51) |
|---------|----------------|-----------------|------------|------------------|------------------------|
| Reset | 0000H | - | - | 0 (highest) | - |
| Timer5 | 000BH | ET5 | TF5 | 1 | 1 |
| EUART | 0023H | ES | RI+TI | 2 | 4 |
| Timer2 | 002BH | ET2 | TF2 | 3 | 5 |
| ADC | 0033H | EADC | ADCIF | 4 | 6 |
| INT2 | 0043H | EX2 | IE2 | 5 | 8 |
| INT3 | 004BH | EX3 | IE3 | 6 | 9 |
| INT4 | 0053H | EX4+IENC | IF43-40 | 7 | 10 |
| Timer3 | 005BH | ET3 | TF3 | 8 | 11 |
| PWM | 0063H | EPWM | PWMIF | 9 | 12 |
| Timer4 | 006BH | ET4 | TF4 | 10 | 13 |
| SCM/LPD | 0073H | ESCM+ESCM1/ELPD | SCMIF/LPDF | 11 (Lowest) | 14 |



8. Enhanced Function

8.1 Normal Resistor LCD Driver

The Traditional Resistance Type/Fast Charge LCD Mode

The LCD driver contains a controller, a duty cycle generator with 4 Common signal pins and 12 Segment driver pins. It is controlled by the P0SS, P1SS, P2SS & P3SS register. Segment 1-12 and COM1-COM4 can also be used as I/O port, LCD COM1-COM4 also can be shared with LED. The 19 bytes display data RAM is addressed to 1E0H-1F2H, which could be used as data memory if needed.

The MCU consists normal display topologies with contrast adjustment which supports both 1/4duty-1/3bias driving mode, DISPSEL (DISPCON.7) must be cleared before LCD working. When ELCC in DISPCON is set, the LCD supply power V_{LCD} is selected by VOL[3:0]. When ELCC is cleared, V_{LCD} equals to V_{DD} .

When MCU enters the Power-Down mode, the LCD will be turned off. If 32.768kHz crystal/128kHz RC works in Power-down mode, the LCD is still working, but the data of LCD RAM keeps the value. During the Power on Reset or Pin Reset or LVR Reset or Watch-dog Reset, the LCD will be turned off, and Common and Segment will output low.

The features of the LCD Normal Display Mode include the following:

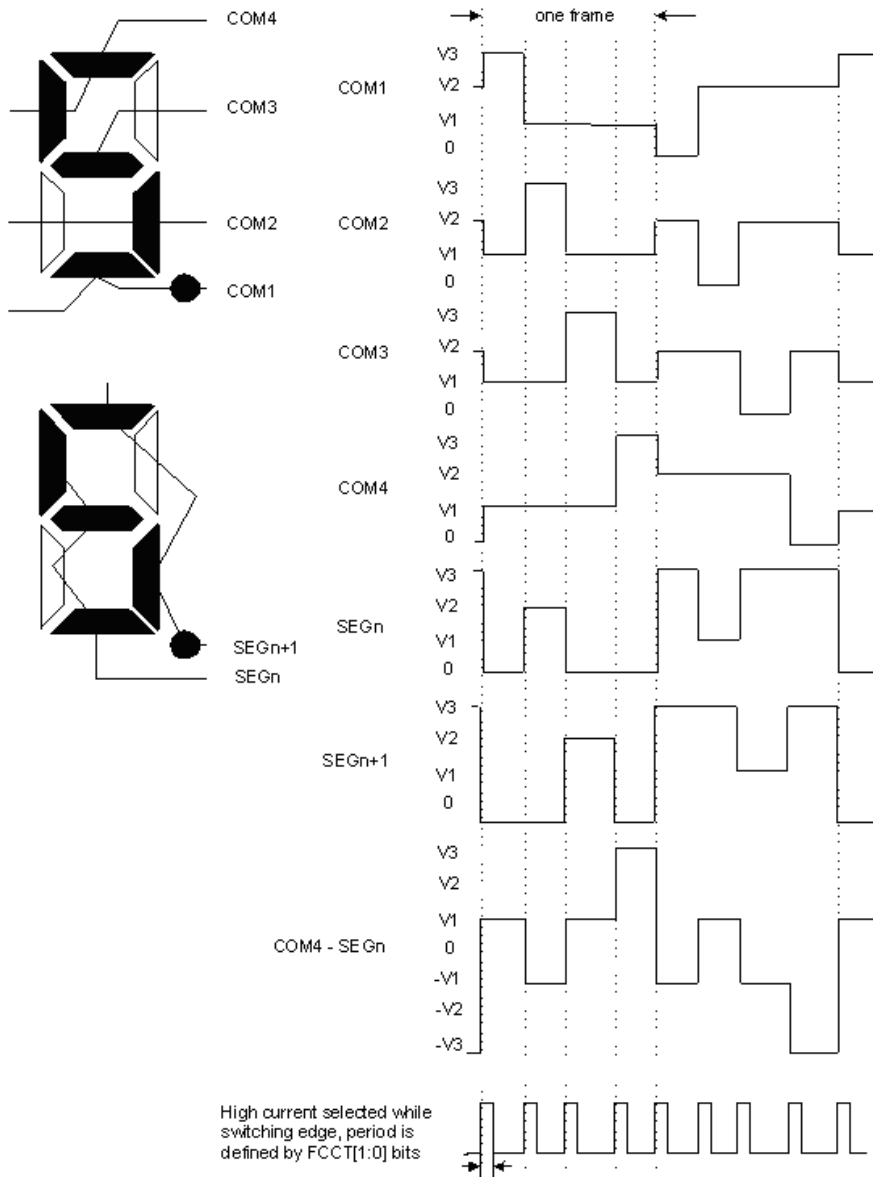
- LCD clock source is decided by code option OP_OSC:
- When OP_OSC[3:0] is 1010, 1101, LCD clock source is 32.768kHz, DISPCLK register is invalid, LCD frame is 64Hz.
- When OP_OSC[3:0] is 0011, 0110, LCD clock source is 128kHz, DISPCLK register is invalid, LCD frame is 64Hz.
- When OP_OSC[3:0] is 0000, LCD clock source is internal RC (12.3MHz), LCD clock = internal RC (12.3MHz)/DISPCLK, LCD frame = LCD clock/512.
- When OP_OSC[3:0] is 1110, LCD clock source is crystal or ceramic, LCD clock = crystal or ceramic /DISPCLK.
- 1/4duty -1/3 bias by configuring the DUTY bit in DISPCON register.
- LCD frame = LCD clock/512.
- 16 levels contrast adjustment by configuring the VOL[3:0] bits in DISPCON register.
- LCD bias resistor (R_{LCD}) can be selected as 20K/75K/300K Ω in 1/3 bias mode, bias resistance sum are 60K/225K/900K.

It is controlled by MOD[1:0] bit in DISPCON1 register to select as traditional resistance LCD or Fast Charge Mode to reduce power consumption.

The relatively high current drain through the 20k resistor will get better LCD display effect, but it may not be suitable for some low current consume application. Lowering this current is possible by configuring the RLCD[2:0] for switching the R_{LCD} value to 75/300K. It will get lower power consumptions, but LCD display effect will get worse.

Therefore, SH79F0819 provides both the low power consumption and display effect of the display mode: fast charge mode.

Set MOD[1:0] = 10 to select this mode. When refresh the display data 20k bias resistors are selected to provide larger current. When keep the display data 75/300K bias resistors are selected to save drive current. Charging time is selected as 1/8, 1/16, 1/32 or 1/64 of LCD com period by FCCTL[1:0] in DISPCON1 register.



LCD Waveform (1/4duty, 1/3bias)



8.1.1 Registers

Table 8.1 LCD Control Register

| ABH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|---------|-------|------|------|------|------|------|------|
| DISPCON | DISPSEL | LCDON | ELCC | DUTY | VOL3 | VOL2 | VOL1 | VOL0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7 | DISPSEL | LCD/LED control bit 0: select LCD driver 1: select LED drive |
| 6 | LCDON | LCD on/off control bit 0: Disable LCD driver 1: Enable LCD drive |
| 5 | ELCC | LCD contrast on/off control bit 0: disable contrast 1: enable contrast |
| 4 | DUTY | LCD duty selection bit 0: 1/4 duty, 1/3 bias 1: Reserved |
| 3-0 | VOL[3:0] | LCD contrast control bits 0000: $V_{LCD} = 0.531 V_{DD}$ 0001: $V_{LCD} = 0.563 V_{DD}$ 0010: $V_{LCD} = 0.594 V_{DD}$ 0011: $V_{LCD} = 0.625 V_{DD}$ 0100: $V_{LCD} = 0.656 V_{DD}$ 0101: $V_{LCD} = 0.688 V_{DD}$ 0110: $V_{LCD} = 0.719 V_{DD}$ 0111: $V_{LCD} = 0.750 V_{DD}$ 1000: $V_{LCD} = 0.781 V_{DD}$ 1001: $V_{LCD} = 0.813 V_{DD}$ 1010: $V_{LCD} = 0.844 V_{DD}$ 1011: $V_{LCD} = 0.875 V_{DD}$ 1100: $V_{LCD} = 0.906 V_{DD}$ 1101: $V_{LCD} = 0.938 V_{DD}$ 1111/1110: $V_{LCD} = 1.000 V_{DD}$ |

Note:

- (1) SH79F0819 has LCD and LED driver, but can not work in the same time. When DISPSEL = 1, LCD is disable, DISPSEL = 0, LED is disable.
- (2) Duty bit can only be set to 0 to select 1/4 duty, 1/3 bias mode.



Table 8.2 LCD Control Register1

| ADH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|--------|--------|------|------|
| DISPCON1 | - | - | - | RLCD | FCCTL1 | FCCTL2 | MOD1 | MOD0 |
| R/W | - | - | - | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 1-0 | MOD[1:0] | LCD Drive mode control bit 00: traditional mode, bias resistor sum is 225K/900K 01: traditional mode, bias resistor sum is 60K 10: fast charge mode, bias resistor sum switch between 60K and 225K/900K |
| 3-2 | FCCTL[1:0] | Fast charge time control bit 00: 1/8 LCD com period 01: 1/16 LCD com period 10: 1/32 LCD com period 11: 1/64 LCD com period |
| 4 | RLCD | LCD bias resistor control bit 0: LCD bias resistor sum is 225K 1: LCD bias resistor sum is 900K |

Table 8.3 LCD CONTRAST Register

| ACH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| DISPCLK0 | DCK0.7 | DCK0.6 | DCK0.5 | DCK0.4 | DCK0.3 | DCK0.2 | DCK0.1 | DCK0.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AAH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| DISPCLK1 | - | - | - | - | - | - | - | DCK1.0 |
| R/W | - | - | - | - | - | - | - | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | - | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|---------------------|---|
| 0 7-0 | DCK1.0 DCK0[7:0] | LCD clock select 0x000: LCD clock = oscillator frequency Others: LCD clock = internal RC or crystal or ceramic/DISPCLK |

Note:

Only when OP_OSC[3:0] is 0000, 1110, DISPCLK register is available.

When [DISPCLK 1, DISPCLK 0] = 0X000, LCD clock = OSCCLK

LCD frame = LCD clock/512.

For example:

When LCD is COM4, OP_OSC[3:0] = 1110, oscillator is 12MHz to get 64HZ LCD frame, DISPCLK = 12M/512/64 = 0x16E, LCD frame = 12M/366/512 = 64.04Hz in fact.

When LCD is COM4, OP_OSC[3:0] = 1110, oscillator is 2MHz to get 64HZ LCD frame, DISPCLK = 2M/512/64 = 0x03D, LCD frame = 2M/61/512 = 64.04Hz in fact.



Table 8.4 P0 Mode Select Register

| B6H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P0SS | - | - | - | - | - | P0S2 | - | - |
| R/W | - | - | - | - | - | R/W | - | - |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | 0 | - | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-3 | - | This bit must write 0 |
| 2 | P0S2 | P0 mode select 0: P0.2 is I/O 1: P0.2 is Segment (Segment19) |
| 1-0 | - | This bit must write 0 |

Table 8.5 P1 Mode Select Register

| 9CH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P1SS | P1S7 | P1S6 | P1S5 | P1S4 | P1S3 | P1S2 | P1S1 | P1S0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-0 | P1S[7:0] | P1 mode select 0: P1.0-P1.7 is I/O 1: P1.0-P1.7 is Segment (Segment1-8) |

Table 8.6 P2 Mode Select Register

| 9DH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P2SS | - | - | P2S5 | - | - | - | P2S1 | P2S0 |
| R/W | - | - | R/W | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | 0 | - | - | - | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-6 | - | This bit must write 0 |
| 5 | P2S5 | P2 mode select bit 0: P2.5 is I/O 1: P2.5 share as Segment (SEG14) |
| 4-2 | - | This bit must write 0 |
| 1-0 | P2S[1:0] | P2 mode select bit 0: P2.1-P2.0 is I/O 1: P2.1-P2.0 share as Segment (SEG9-SEG10) |



Table 8.7 P3 Mode Select Register

| 9EH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P3SS | - | - | - | - | P3S3 | P3S2 | P3S1 | P3S0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-4 | - | This bit must write 0 |
| 3-0 | P3S[7:0] | P3 mode select bit 0: P3.0-P3.3 is I/O 1: P3.0-P3.3 share as Common (COM1-COM4) |

8.1.2 Configuration of LCD RAM

LCD 1/4 duty, 1/3 bias (COM1 - 4, SEG1 - 10, 14, 19)

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-------|-------|-------|-------|
| | - | - | - | - | COM4 | COM3 | COM2 | COM1 |
| 1E0H | - | - | - | - | SEG1 | SEG1 | SEG1 | SEG1 |
| 1E1H | - | - | - | - | SEG2 | SEG2 | SEG2 | SEG2 |
| 1E2H | - | - | - | - | SEG3 | SEG3 | SEG3 | SEG3 |
| 1E3H | - | - | - | - | SEG4 | SEG4 | SEG4 | SEG4 |
| 1E4H | - | - | - | - | SEG5 | SEG5 | SEG5 | SEG5 |
| 1E5H | - | - | - | - | SEG6 | SEG6 | SEG6 | SEG6 |
| 1E6H | - | - | - | - | SEG7 | SEG7 | SEG7 | SEG7 |
| 1E7H | - | - | - | - | SEG8 | SEG8 | SEG8 | SEG8 |
| 1E8H | - | - | - | - | SEG9 | SEG9 | SEG9 | SEG9 |
| 1E9H | - | - | - | - | SEG10 | SEG10 | SEG10 | SEG10 |
| 1EAH | - | - | - | - | - | - | - | - |
| 1EBH | - | - | - | - | - | - | - | - |
| 1ECH | - | - | - | - | - | - | - | - |
| 1EDH | - | - | - | - | SEG14 | SEG14 | SEG14 | SEG14 |
| 1EEH | - | - | - | - | - | - | - | - |
| 1EFH | - | - | - | - | - | - | - | - |
| 1F0H | - | - | - | - | - | - | - | - |
| 1F1H | - | - | - | - | - | - | - | - |
| 1F2H | - | - | - | - | SEG19 | SEG19 | SEG19 | SEG19 |



8.2 LED Driver

The LED driver contains a controller, a duty cycle generator with 4 Common signal pins and 8 Segment driver pins. When DISPSEL bit is set, LED function is enable, and LCD is disable. LED provides 1/4 duty voltage driving mode. The controller consists of display data RAM memory block and a duty generator.

LED_SEG1-8 can be used as I/O port. When DISPSEL is 1, LED is valid, LCD is invalid. P0SS, P2SS register is invalid, P1SS and P3SS individually are used to control LED_SEG1-8, LCD_C1-4 and I/O mode selection.

DISPSEL must be set to 1 before LED is driven.

When MCU enters the Power-Down mode, the LED will be turned off, If 32.768kHz crystal or 128k internal RC works in Power-down mode, the LED is still working. During Power on Reset, Pin Reset, LVR or Watch Dog Reset, LED will be turned off.

8.2.1 Register

Table 8.8 LED Control Register

| ABH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|---------|-------|------|------|------|------|------|------|
| DISPCON | DISPSEL | LEDON | - | DUTY | - | - | - | - |
| R/W | R/W | R/W | - | R/W | - | - | - | - |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | - | 0 | - | - | - | - |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7 | DISPSEL | LCD/LED control bit 0: select LCD driver 1: select LCD drive |
| 6 | LEDON | LED on/off control bit 0: Disable LED driver 1: Enable LED drive |
| 4 | DUTY | LED duty selection bit 0: 1/4 duty 1: Reserved |

Note:

- (1) SH79F0819 has LCD and LED driver, but can not work in the same time. When DISPSEL = 1, LCD is disable, DISPSEL = 0, LED is disable.
- (2) Duty bit can only be set to 0 to select 1/4 duty mode.

Table 8.9 LED Clock Control Register

| ACH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| DISPCLK0 | DCK0.7 | DCK0.6 | DCK0.5 | DCK0.4 | DCK0.3 | DCK0.2 | DCK0.1 | DCK0.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AAH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| DISPCLK1 | - | - | - | - | - | - | - | DCK1.0 |
| R/W | - | - | - | - | - | - | - | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | - | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|---------------------|---|
| 0 7-0 | DCK1.0 DCK0[7:0] | LED clock select 0x000: LCD clock = oscillator frequency Others: LCD clock = internal RC or crystal or ceramic/DISPCLK |

Note: Only when OP_OSC[3:0] is 0000, 1110, DISPCLK register is available.



Table 8.10 P1 Mode Select Register

| 9CH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P1SS | P1S7 | P1S6 | P1S5 | P1S4 | P1S3 | P1S2 | P1S1 | P1S0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-0 | P1S[7:0] | P1 mode select (x = 0-7) 0: P1.0-P1.7 are I/O 1: P1.0-P1.7 are Segment (LED_S1-LED_S8) |

Table 8.11 P3 Mode Select Register

| 9EH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| P3SS | - | - | - | - | P3S3 | P3S2 | P3S1 | P3S0 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

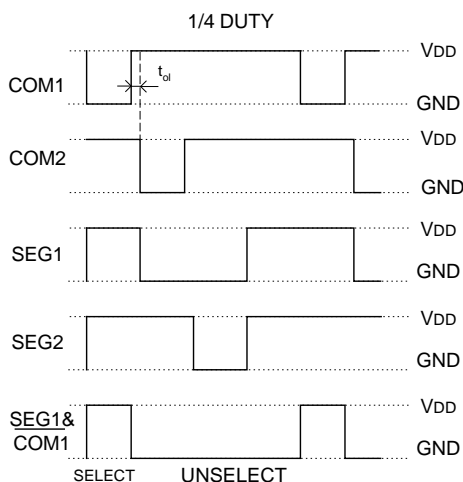
| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-4 | - | This bit must write 0 |
| 3-0 | P3S[3:0] | P3 mode select (x = 0-3) 0: P3.0-P3.3 are I/O 1: P3.0-P3.3 are COM (LED_C1-LED_C4) |

8.2.2 Configuration of LED RAM

LED 1/4 duty (LED_C1 - 4, LED_S1 - 8)

| Address | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|------|
| 1E0H | COM1 | SEG8 | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |
| 1E1H | COM2 | SEG8 | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |
| 1E2H | COM3 | SEG8 | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |
| 1E3H | COM4 | SEG8 | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |

LED Waveform
OP_LEDCOM = 0



Note: t_{OL} is overlap time of LED Common, $t_{OL} = 20\mu s - 40\mu s$.



8.3 PWM (Pulse Width Modulation)

8.3.1 Feature

- Provided interrupt function on period
- Selectable output polarity
- Fault Detect function provided to disable PWM output immediately
- Lock register provided to avoid PWM control register to be unexpected change

The SH79F0819 has one 12-bit PWM module. Which can provide the pulse width modulation waveform with the period and the duty being controlled individually by corresponding register.

PWM timer can be turned to inactive state by the input of FLT pin automatically if EFLT is set.

PWM timer also provides 1 interrupts for PWM0. This makes it possible to change period or duty in every PWM period.

8.3.2 PWM Module Enable

Table 8.12 PWM Module Enable Register

| CFH | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|--------|------|------|-------|
| PWMEN | - | EFLT | - | - | EPWM01 | - | - | EPWM0 |
| R/W | - | R/W | - | - | R/W | - | - | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | 0 | - | - | 0 | - | - | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 6 | EFLT | FLT pin configuration: 0: general purpose I/O or \overline{SS} pin (default) 1: PWM Fault Detect input pin |
| 3 | EPWM01 | PWM01 output enable 0: I/O port 1: PWM01 output |
| 0 | EPWM0 | This bit must write 0 |

PWM output will be disable at the same time when the PWM Enable register is clear to 0.

The main purpose of the FLT pin is to inactivate the PWM output signals and drive them into an inactive state. The action of the FLT is performed directly in hardware so that when a fault occurs, it can be managed quickly and the PWMs outputs are put into an inactive state to save the power devices connected to the PWMs. The FLT pin has no internal pull-high resistor.

If EFLT is set to 0, it means the level on FLT pin has no effect on PWM timers.

Table 8.13 PWM Module Enable Register

| B7H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| PWMEN1 | - | - | - | - | - | - | - | PWM0 |
| R/W | - | - | - | - | - | - | - | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | - | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 0 | PWM0 | Enable 12-bit PWM0 0: PWM output enable 1: PWM output disable, PWM01 as I/O, but PWM timer can work normally, Trigger interrupt |



8.3.3 PWM Timer Lock Register

This register is used to control the change of PWM timer enable register, PWM control register, PWM period register, PWM duty register and PWM dead time control register. Only when the data in this register is #55h, it is possible to change these register. Otherwise they cannot be changed.

This register is to enhance the anti-noise ability of SH79F0819.

Table 8.14 PWM Timer Lock Register

| E7H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| PWMLO | PWMLO.7 | PWMLO.6 | PWMLO.5 | PWMLO.4 | PWMLO.3 | PWMLO.2 | PWMLO.1 | PWMLO.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-0 | PWMLO[7:0] | PWM lock register 55h: enable to change PWM related registers else: disable to change PWM related registers |



8.3.4 12-bit PWM Timer

The SH79F0819 has one 12-bit PWM module. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMPH/L is used to control the period cycle of the PWM output waveform. PWMDH/L is used to control the duty in the waveform of the PWM module output.

It is acceptable to change these 3 registers during PWM output Enable. All the change will take affect at the next PWM period.

Table 8.15 12-bit PWM Control Register

| D2H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|--------|--------|------|------|------|-------|--------|--------|
| PWM0C | PWM0IE | PWM0IF | - | FLTS | FLTC | PWM0S | TnCK01 | TnCK00 |
| R/W | R/W | R/W | - | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | PWM0IE | PWM0 interrupt enable bit (When EPWM bit in IEN1 is set) 0: Disable PWM0 interrupt 1: Enable PWM0 interrupt |
| 6 | PWM0IF | PWM0 interrupt flag 0: Clear by software 1: Set by hardware to indicate that the PWM0 period counter overflow |
| 4 | FLTS | FLT status bit 0: PWM is in normal status, cleared by software 1: PWM is in inactive status, set automatically by hardware |
| 3 | FLTC | FLT pin configuration 0: Inactivate the PWM output when FLT is low level 1: Inactivate the PWM output when FLT is high level |
| 2 | PWM0S | PWM0 output normal mode of duty cycle 0: high active, PWM0 output high during duty time, output low during remain period time 1: low active, PWM0 output low during duty time, output high during remain period time |
| 1-0 | TnCK0[1:0] | 12-bit PWM clock selector: 00: Oscillator clock/2 01: Oscillator/4 10: Oscillator/8 11: Oscillator/16 Note: When OP_OSC is 0000, 0011 or 1010, PWM clock source is internal RC, When OP_OSC is 1110 or 0110, PWM clock source is crystal or ceramic, When OP_OSC is 1101, PWM clock source is crystal or ceramic in XTALX pins. |

Note:

- (1) Inactivate PWM here means PWM01 outputs keep Low (if PWM0S = 0) or High (if PWM0S = 1).
- (2) The PWM outputs will remain in the inactive states as soon as the high/low level of FLT pin is detected.
- (3) When FLT input signal is valid, FLTS bit can not be cleared. Only when FLT input signal disappears, can FLTS state bit will be cleared.



Table 8.16 PWM Period Control Register (PWM0PL)

| D3H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| PWM0PL | PP0.7 | PP0.6 | PP0.5 | PP0.4 | PP0.3 | PP0.2 | PP0.1 | PP0.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-0 | PP0[7:0] | 12-bit PWM period low 8 bits registers |

Table 8.17 PWM Period Control Register (PWM0PH)

| D4H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|--------|--------|-------|-------|
| PWM0PH | - | - | - | - | PP0.11 | PP0.10 | PP0.9 | PP0.8 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 3-0 | PP0[11:8] | 12-bit PWM period high 4 bits registers |

PWM output period cycle = [PP0.11, PP0.0] X PWM clock.

When [PP0.11, PP0.0] = 000H, PWM0 outputs high if the PWM0S bit is set to “0” regardless of PWM duty cycle.

When [PP0.11, PP0.0] = 000H, PWM0 outputs GND level if the PWM0S bit is set to “1” regardless of PWM duty cycle.

Table 8.18 PWM Duty Control Register (PWM0DL)

| D5H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| PWM0DL | PD0.7 | PD0.6 | PD0.5 | PD0.4 | PD0.3 | PD0.2 | PD0.1 | PD0.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--------------------------------------|
| 7-0 | PD0[7:0] | 12-bit PWM duty low 8 bits registers |

Table 8.19 PWM Duty Control Register (PWM0DH)

| D6H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|--------|--------|-------|-------|
| PWM0DH | - | - | - | - | PD0.11 | PD0.10 | PD0.9 | PD0.8 |
| R/W | - | - | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---------------------------------------|
| 3-0 | PD0[11:8] | 12-bit PWM duty high 4 bits registers |

PWM output duty cycle = [PD0.11, PD0.0] X PWM clock.

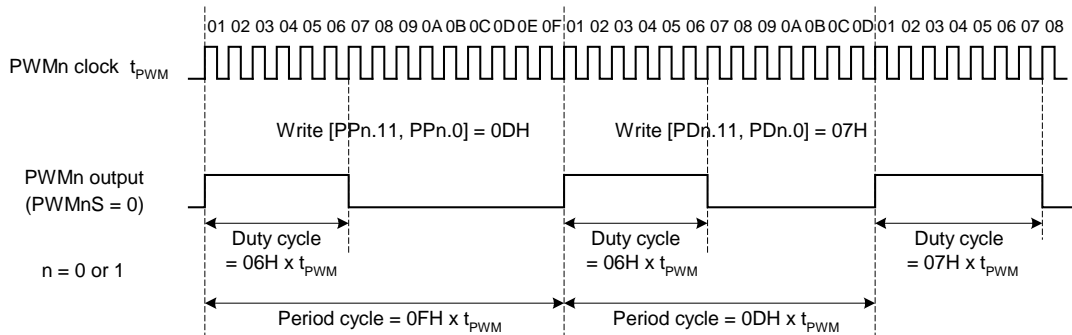
If [PP0.11, PP0.0] ≤ [PD0.11, PD0.0], PWM0 outputs GND level when the PWM0S bit is set to “0”.

If [PP0.11, PP0.0] > [PD0.11, PD0.0], PWM0 outputs high level when the PWM0S bit is set to “1”.



Programming Note:

- (1) Set PWML0 register to 55H and select the PWM module system clock.
- (2) Set the PWM period/duty cycle by writing proper value to the PWM period control register (PWMP) or PWM duty control register (PWMD). First set the low Byte, then the high Byte. Note that even if the value of high bits keep unchanged, it also need to rewrite once, otherwise, the low modify is invalid
- (3) Select the PWM output mode of the duty cycle by writing the PWM0S bit in the PWM control register (PWMC). (High level valid or low level valid)
- (4) In order to output the desired PWM waveform, enable the PWM module by writing "1" to the EPWM01 bit in the PWM control register (PWMC).
- (5) If the PWM period cycle or duty cycle is to be changed, the writing flow should be followed as described in step 2 or step 3. Then the revised data are loaded into the re-load counter and the PWM module starts counting at next period.
- (6) Change the data in PWML0 register not equal to 55h in order to enhance the anti-noise ability.



PWM Output Period or Duty Cycle Changing Example



8.4 EUART

8.4.1 Feature

- The SH79F0819 has one enhanced EUART which are compatible with the conventional 8051
- The baud rate can be selected from the divided frequency of the system clock or Timer4/2 overflow rate
- Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
- The EUART can be operated in four modes

8.4.2 EUART0 Mode Description

The EUART can be operated in 4 modes. Users must initialize the SCON before any communication can take place. This involves selection of the Mode and the baud rate. The Timer4/2 should also be initialized if the mode 1 or the mode 3 is used. In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TXD pin and shift in 8 bits on the RXD pin. Reception is initiated in the other modes by the input start bit if REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

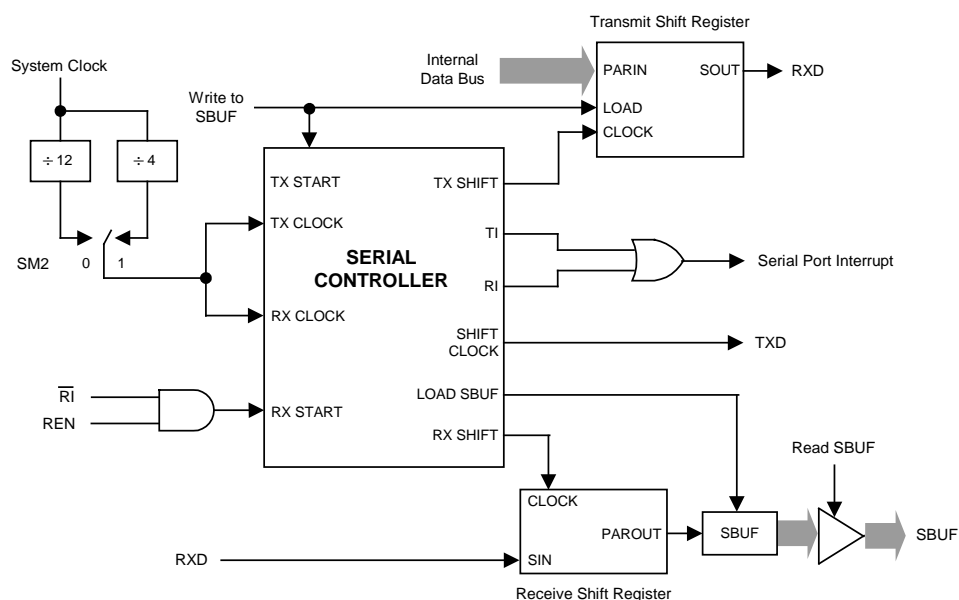
| SM0 | SM1 | Mode | Type | Baud Clock | Frame Size | Start Bit | Stop Bit | Bit 9 |
|-----|-----|------|--------|---------------------------------------|------------|-----------|----------|-------|
| 0 | 0 | 0 | Synch | $f_{SYS}/(4 \text{ or } 12)$ | 8 bits | None | None | None |
| 0 | 1 | 1 | Asynch | Timer 4 or 2 overflow rate/(16 or 32) | 10 bits | 1 | 1 | None |
| 1 | 0 | 2 | Asynch | $f_{SYS}/(32 \text{ or } 64)$ | 11 bits | 1 | 1 | 0, 1 |
| 1 | 1 | 3 | Asynch | Timer 4 or 2 overflow rate/(16 or 32) | 11 bits | 1 | 1 | 0, 1 |

Mode0: Synchronous Mode, Half duplex

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD pin. TXD is used to output the shift clock. The TXD clock is provided by the SH79F0819 whether the device is transmitting or receiving. Therefore, this mode is a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first.

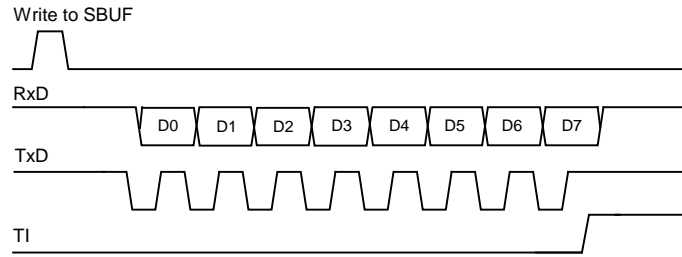
The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock. The only difference from standard 8051 is that SH79F0819 in the mode 0 has variable baud rate.

The functional block diagram is shown below. Data enters and exits the serial port on the RXD pin. The TXD pin is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the SH79F0819.



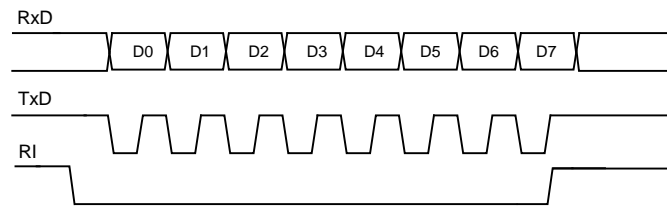


Any instruction that uses SBUF as a destination register ("write to SBUF" signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position from left to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivate SEND and sets TI (SCON.1) at the rising edge of the next system clock.



Send Timing of Mode 0

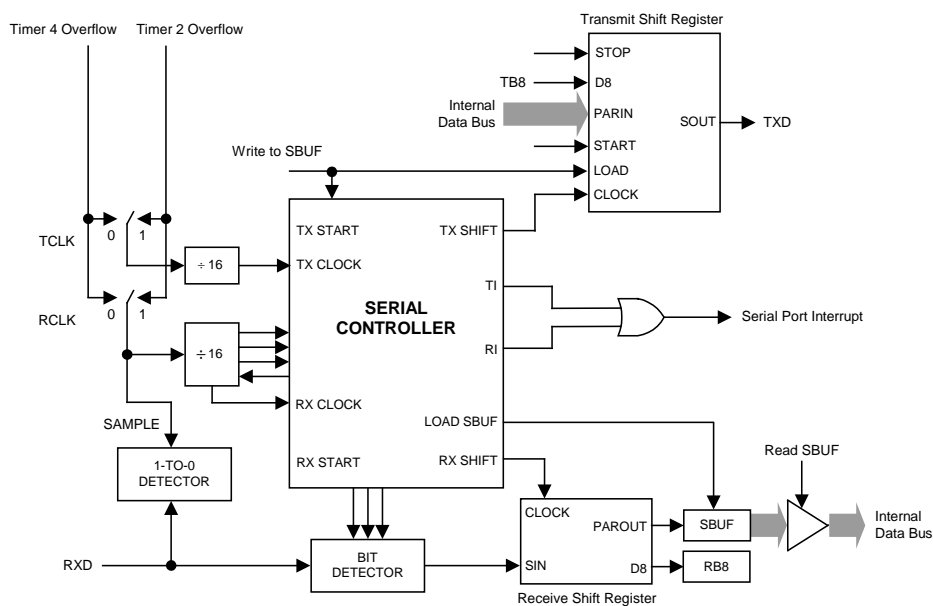
Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivate RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.



Receive Timing of Mode 0

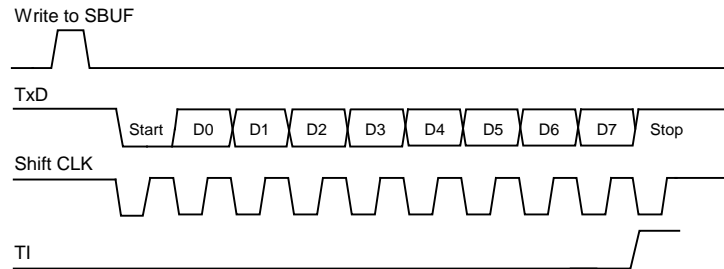
Mode1: 8-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The serial receive and transmit baud rate is 1/16 of the Timer4/2 overflow. (Refer to **Baud Rate** Section for details). The functional block diagram is shown below.





Transmission begins with a “write to SBUF” signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal. The start bit is firstly put out on TxD pin, then are the 8 bits of data. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time that the stop is send.



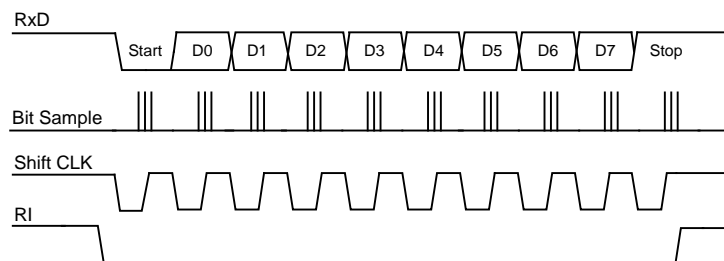
Send Timing of Mode 1

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps the divide-by-16 counter to synchronize with the serial datas of RxD pin. The divide-by-16 counter divides each bit time into 16 states. The bit detector samples the value of RxD at the 7th, 8th and 9th counter states of each bit time. At least 2 the sampling values have no difference in the state of the three samples, data can be received This is done for noise rejection. If the first bit after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD pin. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set ,if the following conditions are met:

- 1. RI must be 0
- 2. Either SM2 = 0, or the received stop bit = 1

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.

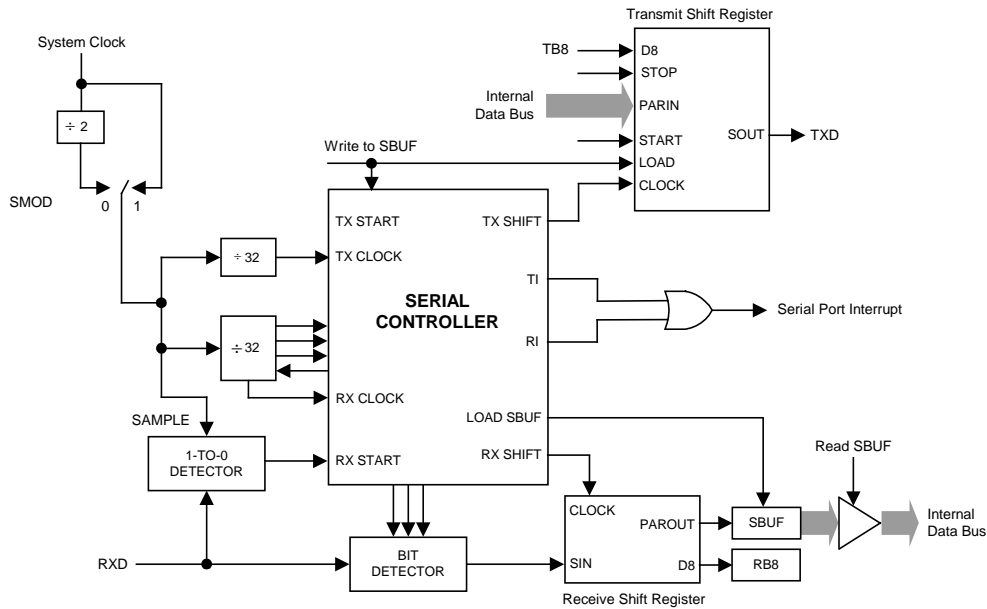


Receive Timing of Mode 1

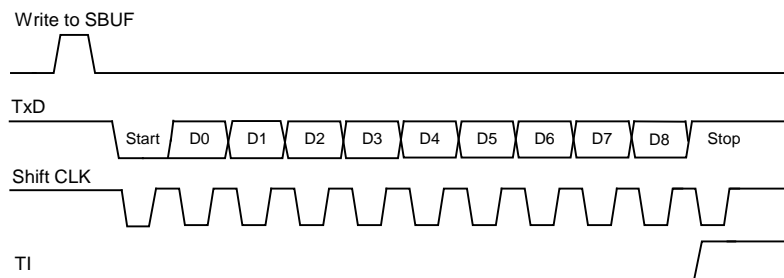


Mode2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

This mode provides the 11 bits full duplex asynchronous communication. The 11 bit consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition (Refer to Multiprocessor Communication Section for details). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below:



Transmission begins with a “write to SBUF” signal, the “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal). The start bit is firstly put out on TxD pin, then are the 9 bits of data. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time.



Send Timing of Mode 2

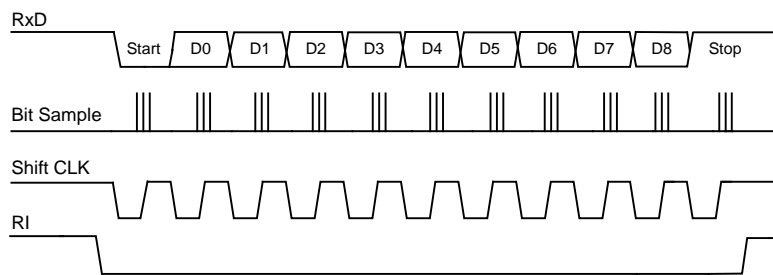


Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps the divide-by-16 counter to synchronize with the serial data of RxD pin. The divide-by-16 counter divides each bit time into 16 states. The bit detector samples the value of RxD at the 7th, 8th and 9th counter state of each bit time. At least 2 of the sampling values have no difference in the state of the three samples, data can be received. This is done for noise rejection. If the first bit detected after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD pin. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set, if the following conditions are met:

1. RI must be 0
2. Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

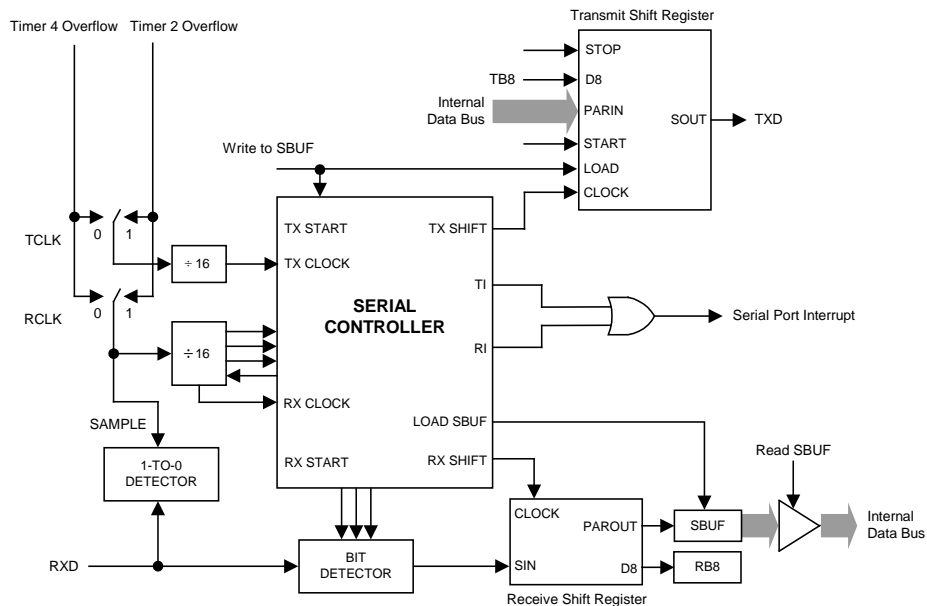
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

Mode3: 9-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

Mode3 uses transmission protocol of the Mode2 and baud rate generation of the Mode1.





8.4.3 Baud Rate Generate

In Mode0, the baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined by SM2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

In Mode1 & Mode3, the baud rate can be selected from Timer4/2 overflow rate.

Individually setting TCLK (T2CON.4) and RCLK (T2CON.5) to 1 to select Timer2 as baud clock source of TX & RX (Refer to "Timer" section for details). Whether TCLK or RCLK to logic 1, Timer2 is baud rate generator mode. If TCLK and RCLK are logic 0, Timer4 will be used as the baud clock source of TX&RX.

The Mode1 & 3 baud rate equations are shown below, where [RCAP2H, RCAP2L] is the 16-bit auto-reload register for Timer2, [TH4, TL4] is the 16-bit reload register for Timer4.

$$\text{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{\text{SYS}}}{65536 - [\text{RCAP2H}, \text{RCAP2L}]}, \text{ Baud Rate using Timer2, the clock source of Timer2 is system clock.}$$

$$\text{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{\text{SYS}} / \text{PRESCALER}}{65536 - [\text{TH4}, \text{TL4}]}, \text{ Baud Rate using Timer4, the clock source of Timer4 is system clock.}$$

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, the serial port runs at 1/64 of the clock. When set to 1, the serial port runs at 1/32 of the clock.

$$\text{BaudRate} = 2^{\text{SMOD}} \times \left(\frac{f_{\text{SYS}}}{64} \right)$$

8.4.4 Multi-Processor Communication

Software Address Recognition

Modes 2 and 3 of the EUART have a special function for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the serial port interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte by using the 9th bit. The 9th bit is 1 in an address byte, the 9th bit is 0 in a data byte.

If SM2 is 1, slave will not respond to data byte interrupt. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed keep their SM2 setting and go on with their business, ignoring the incoming data bytes.

Note: In Mode0, SM2 is used to select baud rate doubling. In Mode1, SM2 can be used to check the validity of the stop bit. If SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Automatic (Hardware) Address Recognition

In Mode2 & 3, setting the SM2 bit will configure EUART act as following: when a stop bit is received, EUART will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts to receive the following data byte(s).

The 9-bit mode requires that the 9th information bit is 1 to indicate that the received information is address rather than data. When the master processor wants to transmit a block of data to one of the slaves, it must first send out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the address matching slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the address matching slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all not address byte in transmission until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address (SADDR) and the address shield (SADEN). The slave address is an 8-bit byte stored in the SADDR register. The SADEN register is actually used to define whether the byte value in SADDR is valid or not. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is i. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR. Use of the Given Address allows multiple slaves to be recognized while excluding others.



| | Slave 1 | Slave 2 |
|-------------------------------------|----------|----------|
| SADDR | 10100100 | 10100111 |
| SADEN(bit=0 will be ignored) | 11111010 | 11111001 |
| Given Address | 10100x0x | 10100xx1 |
| Broadcast Address (SADDRorSADEN) | 1111111x | 11111111 |

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is ignore LSB, while for slave 2 LSB is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and ignore the bit 1 for slave 2. Hence to communicate only with slave 2, the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is ignored for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as neglect. In most cases, the Broadcast Address is FFh, this address will be responded by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. The two results set Given Address and Broadcast Address to XXXXXXXX (all bits are ignored). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUART will reply to any address, which it is compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor communication by software recognition address according to the above mentioned method.

8.4.5 Frame Error Detection

Frame error detection is available when the SSTAT bit in register PCON is set to logic 1. All the 3 error flag bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Note: The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).

Transmit Collision

The Transmit Collision bit (TXCOL bit in register SCON) set '1' when a transmission is still in progress and user software writes data to the SBUF register. If collision occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overflow

The Receive Overflow bit (RXOV in register SCON) set '1' if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happens.

Frame Error

The Frame Error bit (FE in register SCON) set '1' if an invalid (low) STOP bit is detected.

Break Detection

A break is detected when any 11 consecutive bits are detected as low. Since a break condition also satisfies the requirements for a framing error, a break condition will also result in reporting a framing error. Once a break condition has been detected, the UART will go into an idle state and remain in this idle state until a valid stop bit (rising edge on RxD pin) has been received.



8.4.6 Register

Table 8.20 EUART Control & Status Register

| 98H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|---------|-----------|------------|------|------|------|------|------|
| SCON | SM0 /FE | SM1 /RXOV | SM2 /TXCOL | REN | TB8 | RB8 | TI | RI |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-6 | SM[0:1] | EUART Serial mode control bit, when SSTAT = 0 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8 bit Asynchronous Mode, variable baud rate 10: mode 2, 9 bit Asynchronous Mode, fixed baud rate 11: mode 3, 9 bit Asynchronous Mode, variable baud rate |
| 7 | FE | EUART Frame Error flag, when FE bit is read, SSTAT bit must be set 1 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware |
| 6 | RXOV | EUART Receive Over flag, when RXOV bit is read, SSTAT bit must be set 1 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware |
| 5 | SM2 | EUART Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0 0: In Mode0, baud-rate is 1/12 of system clock In Mode1, disable stop bit validation check, any stop bit will set RI to generate interrupt In Mode2 & 3, any byte will set RI to generate interrupt 1: In Mode0, baud-rate is 1/4 of system clock In Mode1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In Mode2 & 3, only address byte (9 th bit = 1) will set RI to generate interrupt |
| 5 | TXCOL | EUART Transmit Collision flag, when TXCOL bit is read, SSTAT bit must be set 1 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware |
| 4 | REN | EUART Receiver enable bit 0: Receive Disable 1: Receive Enable |
| 3 | TB8 | The 9th bit to be transmitted in Mode2 & 3 of EUART, set or clear by software |
| 2 | RB8 | The 9th bit to be received in Mode1, 2 & 3 of EUART In Mode0, RB8 is not used In Mode1, if receive interrupt occurs, RB8 is the stop bit that was received In Modes2 & 3 it is the 9 th bit that was received |
| 1 | TI | Transmit interrupt flag of EUART 0: cleared by software 1: Set by hardware at the end of the 8 th bit time in Mode0, or at the beginning of the stop bit in other modes |
| 0 | RI | Receive interrupt flag of EUART 0: cleared by software 1: Set by hardware at the end of the 8 th bit time in Mode0, or at the beginning of the stop bit in other modes |



Table 8.21 EUART Data Buffer Register

| 99H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| SBUF | SBUF.7 | SBUF.6 | SBUF.5 | SBUF.4 | SBUF.3 | SBUF.2 | SBUF.1 | SBUF.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|------------------|---|
| 7-0 | SBUF[7:0] | This SFR accesses two registers; a transmit shift register and a receive latch register A write of SBUF will send the byte to the transmit shift register and then initiate a transmission A read of SBUF returns the contents of the receive latch |

Table 8.22 Power Control Register

| 87H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------------------------------------|------|-------|------|------|------|------|------|------|
| PCON | SMOD | SSTAT | - | - | GF1 | GF0 | PD | IDL |
| R/W | R/W | R/W | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | SMOD | Baud rate doubler If set in Mode1 & 3, SMOD = 0, the baud-rate of EUART is doubled if using time4 as baud-rate generator If set in Mode2, SMOD = 1, the baud-rate of EUART is doubled |
| 6 | SSTAT | SCON[7:5] function select bit 0: SCON[7:5] operates as SM0, SM1, SM2 1: SCON[7:5] operates as FE, RXOV, TXCOL |
| 3-0 | - | Other: refer to "Power Management" section for details |

Table 8.23 EUART Slave Address & Address Mask Register

| 9AH-9BH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|--------------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SADDR | SADDR.7 | SADDR.6 | SADDR.5 | SADDR.4 | SADDR.3 | SADDR.2 | SADDR.1 | SADDR.0 |
| SADEN | SADEN.7 | SADEN.6 | SADEN.5 | SADEN.4 | SADEN.3 | SADEN.2 | SADEN.1 | SADEN.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|-------------------|---|
| 7-0 | SADDR[7:0] | EUART's slave address SFR SADDR defines the EUART's slave address |
| 7-0 | SADEN[7:0] | SFR SADEN is a bit mask to determine which bits of SADDR are checked against a received address 0: Corresponding bit in SADDR is ignored 1: Corresponding bit in SADDR is checked against a received address |



Table 8.24 Rxd Pin Schmitt Voltage Control Register

| 9FH, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|------|------|------|------|------|------|--------|--------|
| RxCON | - | - | - | - | - | - | RxCON1 | RxCON0 |
| R/W | - | - | - | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 1-0 | RxCON[1:0] | Rxd pin Schmitt voltage control 00: input low voltage is $0.2 V_{DD}$ 01: input low voltage is $0.4 V_{DD}$ 10: input low voltage is $0.5 V_{DD}$ 11: normal IO |

Note: RxCON is available when EUART is enable, input low voltage is measured at 25°C. Refer to **Electrical Characteristics** for detail.



8.5 Analog Digital Converter (ADC)

8.5.1 Feature

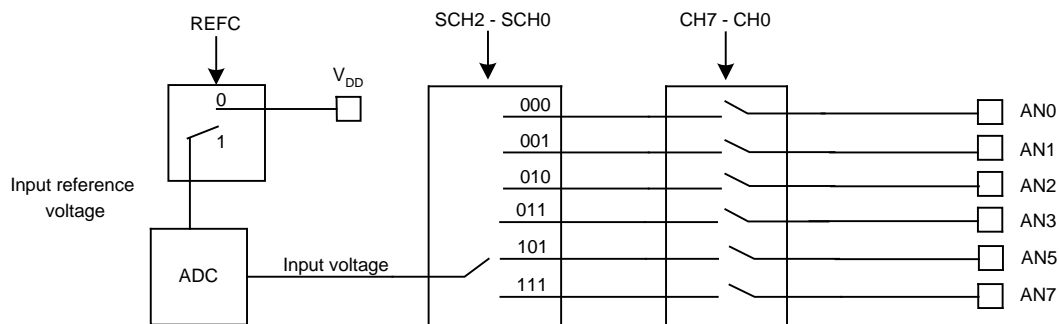
- 10-bit Resolution
- Built in V_{REF}
- 6 Multiplexed Input Channels

The SH79F0819 includes a single ended, 10-bit SAR Analog to Digital Converter (ADC) with build in reference voltage connected to the V_{DD} , users also can select the AVREF port input reference voltage. The 6 ADC channels are shared with 1 ADC module; each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. GO/\overline{DONE} signal is available to start convert, and indicate end of convert. When conversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCON register will be set. If ADC Interrupt is enabled, the ADC interrupt will be generated.

The ADC integrates a digital compare function to compare the value of analog input and the digital value in the AD converter. If this function is enabled (set EC bit in ADCON register) and ADC module is enabled (set ADON bit in ADCON register). When the corresponding digital value of analog input is larger than the compare value in register (ADDH/L), the ADC interrupt will occur, otherwise no interrupt will be generated. The digital comparator can work continuously when GO/\overline{DONE} bit is set until software clear, which behaviors different with the AD converter operation mode.

The ADC module including digital compare module can wok in Idle mode and the ADC interrupt will wake up the Idle mode, but is disabled in Power-Down mode.

8.5.2 ADC Diagram



ADC Diagram



8.5.3 ADC Register

Table 8.25 ADC Control Register

| 93H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|------|-------|------|------|------|------|------|---------|
| ADCON | ADON | ADCIF | EC | REFC | SCH2 | SCH1 | SCH0 | GO/DONE |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | ADON | ADC Enable bit 0: Disable the ADC module 1: Enable the ADC module |
| 6 | ADCIF | ADC Interrupt Flag bit 0: No ADC interrupt, cleared by software. 1: Set by hardware to indicate that the AD Convert has been completed, or analog input is larger than ADDATH/L if compare is enabled |
| 5 | EC | Compare Function Enable bit 0: Compare function disabled 1: Compare function enabled |
| 4 | REFC | Reference Voltage Select bit 0: the reference voltage connected to V_{DD} 1: reserved |
| 3-1 | SCH[2:0] | ADC channel Select bits 000: ADC channel AN0 001: ADC channel AN1 010: ADC channel AN2 011: ADC channel AN3 100: reserved 101: ADC channel AN5 110: reserved 111: ADC channel AN7 |
| 0 | GO/DONE | ADC status flag bit 0: Automatically cleared by hardware when AD convert is completed. Clearing this bit during converting time will stop current conversion. If Compare function is enabled, this bit will not be cleared by hardware until software clear. 1: Set to start AD convert or digital compare. |

Note:

- (1) REFC bit is only selected as 0, internal V_{DD} is reference voltage.
(2) SCH[2:0] bit 100 and 110 are reserved, please don't select them.



Table 8.26 ADC Time Configuration Register

| 94H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|-------|-------|-------|------|------|------|------|------|
| ADT | TADC2 | TADC1 | TADC0 | - | TS3 | TS2 | TS1 | TS0 |
| R/W | R/W | R/W | R/W | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7-5 | TADC[2:0] | ADC Clock Period Select bits 000: ADC Clock Period $t_{AD} = 2 t_{SYS}$ 001: ADC Clock Period $t_{AD} = 4 t_{SYS}$ 010: ADC Clock Period $t_{AD} = 6 t_{SYS}$ 011: ADC Clock Period $t_{AD} = 8 t_{SYS}$ 100: ADC Clock Period $t_{AD} = 12 t_{SYS}$ 101: ADC Clock Period $t_{AD} = 16 t_{SYS}$ 110: ADC Clock Period $t_{AD} = 24 t_{SYS}$ 111: ADC Clock Period $t_{AD} = 32 t_{SYS}$ |
| 3-0 | TS[3:0] | Sample time select bits $2 t_{AD} \leq \text{Sample time} = (\text{TS} [3:0]+1) * t_{AD} \leq 15 t_{AD}$ |

Note:

- (1) Make sure that $t_{AD} \geq 1\mu\text{s}$;
- (2) The minimum sample time is $2 t_{AD}$, even $\text{TS}[3:0] = 0000$;
- (3) The maximum sample time is $15 t_{AD}$, even $\text{TS}[3:0] = 1111$;
- (4) Evaluate the series resistance connected with ADC input pin before set $\text{TS}[3:0]$;
- (5) Be sure that the series resistance connected with ADC input pin is no more than $10\text{k}\Omega$ when $2 t_{AD}$ sample time is selected;
- (6) Total conversion time is: $12 t_{AD} + \text{sample time}$.

For Example

| System Clock (SYSCLK) | TADC[2:0] | t_{AD} | TS[3:0] | Sample Time | Conversion Time |
|-----------------------|-----------|--------------------------------|---------|-------------------------------|--|
| 32.768kHz | 000 | $30.5 * 2 = 61\mu\text{s}$ | 0000 | $2 * 61 = 122\mu\text{s}$ | $12 * 61 + 122 = 854\mu\text{s}$ |
| | 000 | $30.5 * 2 = 61\mu\text{s}$ | 0111 | $8 * 61 = 488\mu\text{s}$ | $12 * 61 + 488 = 1220\mu\text{s}$ |
| | 000 | $30.5 * 2 = 61\mu\text{s}$ | 1111 | $15 * 61 = 915\mu\text{s}$ | $12 * 61 + 915 = 1647\mu\text{s}$ |
| | 111 | $30.5 * 32 = 976\mu\text{s}$ | 0000 | $2 * 976 = 1952\mu\text{s}$ | $12 * 976 + 1952 = 13664\mu\text{s}$ |
| | 111 | $30.5 * 32 = 976\mu\text{s}$ | 0111 | $8 * 976 = 7808\mu\text{s}$ | $12 * 976 + 7808 = 19520\mu\text{s}$ |
| | 111 | $30.5 * 32 = 976\mu\text{s}$ | 1111 | $15 * 976 = 14640\mu\text{s}$ | $12 * 976 + 14640 = 26352\mu\text{s}$ |
| 4MHz | 000 | $0.25 * 2 = 0.5\mu\text{s}$ | - | - | ($t_{AD} < 1\mu\text{s}$, not recommended) |
| | 001 | $0.25 * 4 = 1\mu\text{s}$ | 0000 | $2 * 1 = 2\mu\text{s}$ | $12 * 1 + 2 = 14\mu\text{s}$ |
| | 001 | $0.25 * 4 = 1\mu\text{s}$ | 0111 | $8 * 1 = 8\mu\text{s}$ | $12 * 1 + 8 = 20\mu\text{s}$ |
| | 001 | $0.25 * 4 = 1\mu\text{s}$ | 1111 | $15 * 1 = 15\mu\text{s}$ | $12 * 1 + 15 = 27\mu\text{s}$ |
| | 111 | $0.25 * 32 = 8\mu\text{s}$ | 0000 | $2 * 8 = 16\mu\text{s}$ | $12 * 8 + 16 = 112\mu\text{s}$ |
| | 111 | $0.25 * 32 = 8\mu\text{s}$ | 0111 | $8 * 8 = 64\mu\text{s}$ | $12 * 8 + 64 = 160\mu\text{s}$ |
| 12.3MHz | 000 | $0.083 * 2 = 0.166\mu\text{s}$ | - | - | ($t_{AD} < 1\mu\text{s}$, not recommended) |
| | 100 | $0.083 * 12 = 1\mu\text{s}$ | 0000 | $2 * 1 = 2\mu\text{s}$ | $12 * 1 + 2 = 14\mu\text{s}$ |
| | 100 | $0.083 * 12 = 1\mu\text{s}$ | 0111 | $8 * 1 = 8\mu\text{s}$ | $12 * 1 + 8 = 20\mu\text{s}$ |
| | 100 | $0.083 * 12 = 1\mu\text{s}$ | 1111 | $15 * 1 = 15\mu\text{s}$ | $12 * 1 + 15 = 27\mu\text{s}$ |
| | 111 | $0.083 * 32 = 2.7\mu\text{s}$ | 0000 | $2 * 2.7 = 5.4\mu\text{s}$ | $12 * 2.7 + 5.4 = 37.8\mu\text{s}$ |
| | 111 | $0.083 * 32 = 2.7\mu\text{s}$ | 0111 | $8 * 2.7 = 21.6\mu\text{s}$ | $12 * 2.7 + 21.6 = 54\mu\text{s}$ |
| | 111 | $0.083 * 32 = 2.7\mu\text{s}$ | 1111 | $15 * 2.7 = 40.5\mu\text{s}$ | $12 * 2.7 + 40.5 = 72.9\mu\text{s}$ |



Table 8.27 ADC Channel Configure Register

| 95H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| ADCH | CH7 | - | CH5 | - | CH3 | CH2 | CH1 | CH0 |
| R/W | R/W | - | R/W | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | - | 0 | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7 | CH7 | Channel Configuration bits 0: P3.7 is I/O port 1: P3.7 is ADC input port |
| 5 | CH5 | Channel Configuration bits 0: P3.5 is I/O port 1: P3.5 is ADC input port |
| 3-0 | CH[3:0] | Channel Configuration bits 0: P4.0-4.3 is I/O port 1: P4.0-4.3 is ADC input port |

Table 8.28 AD Converter Data Register (Compare Value Register)

| 96H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| ADDL | - | - | - | - | - | - | A1 | A0 |
| R/W | - | - | - | - | - | - | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | - | - | - | - | - | - | 0 | 0 |

| 97H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|------|------|------|------|------|------|------|
| ADDH | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 1-0 7-0 | A9-A0 | ADC Data register Digital Value of sampled analog voltage, updated when conversion is completed If ADC Compare function is enabled (EC = 1), the value will be compared with the analog input |

The Approach for AD Conversion:

- (1) Select the analog input channels and reference voltage.
- (2) Enable the ADC module with the selected analog channel.
- (3) Set $\overline{GO/DONE} = 1$ to start the AD conversion.
- (4) Wait until $\overline{GO/DONE} = 0$ or $ADCIF = 1$, if the ADC interrupt is enabled, the ADC interrupt will occur, user need clear $ADCIF$ by software.
- (5) Acquire the converted data from $ADDH/ADDL$.
- (6) Repeat step 3-5 if another conversion is required.

The Approach for Digital Compare Function:

- (1) Select the analog input channels and reference voltage.
- (2) Write $ADDH/ADDL$ to set the compare value.
- (3) Set $EC = 1$ to enable compare function.
- (4) Enable the ADC module with the selected analog channel.
- (5) Set $\overline{GO/DONE} = 1$ to start the compare function.
- (6) If the analog input is larger than compare value set in $ADDH/ADDL$, the $ADCIF$ will be set to 1. if the ADC interrupt is enabled, the ADC interrupt will occur, user need clear $ADCIF$ by software.
- (7) The compare function will continue work until the $\overline{GO/DONE}$ bit is cleared to 0.



8.6 Low Power Detect (LPD)

8.6.1 Feature

- Low power detect and generate interrupt
- LPD detect voltage is selectable
- LPD de-bounce timer T_{LPD} is about 30-60 μ s

The low power detect (LPD) is used to monitor the supply voltage and generate an internal flag if the voltage decrease below the specified value. It is used to inform CPU whether the power is shut off or the battery is used out, so the software may do some protection action before the voltage drop down to the minimal operation voltage.

The LPD interrupt can wake the power down mode up.

8.6.2 Register

Table 8.29 Low Power Detection Control Register

| B3H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------------------------------|-------|-------------------|-------|-------|-------|-------|-------|-------|
| LPDCON | LPDEN | LPDF [*] | LPDMD | LPDIF | LPDS3 | LPDS2 | LPDS1 | LPDS0 |
| R/W | R/W | R [*] | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7 | LPDEN | LPD Enable bit 0: Disable lower power detection 1: Enable lower power detection |
| 6 | LPDF | LPD status Flag bit 0: No LPD happened, clear by hardware, 1: LPD happened, set by hardware |
| 5 | LPDMD | LPD mode select bit 0: When V_{DD} below LPD voltage, LPDF is set 1: When V_{DD} above LPD voltage, LPDF is set |
| 4 | LPDIF | LPD interrupt flag bit 0: No LPD happened, clear by software 1: LPD happened, set by hardware |
| 3-0 | LPDS[3:0] | LPD Voltage Select bit 0000: 2.40V 0001: 2.55V 0010: 2.70V 0011: 2.85V 0100: 3.00V 0101: 3.15V 0110: 3.30V 0111: 3.45V 1000: 3.60V 1001: 3.75V 1010: 3.90V 1011: 4.05V 1100: 4.20V 1101: 4.35V 1110: 4.50V 1111: 4.65V |

*: LPDIF can only be write 0, it can't be set to 1.



8.7 Low Voltage Reset (LVR)

8.7.1 Feature

- Enabled by the code option and V_{LVR} is 4.3V or 2.1V
- LVR de-bounce timer T_{LVR} is 30-60 μ s
- When the power supply voltage is lower than the set voltage V_{LVR} , it will cause the internal reset

The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage below the specified value V_{LVR} . The LVR de-bounce timer T_{LVR} is about 30 μ s-60 μ s.

The LVR circuit has the following feature when the LVR function is enabled: (t means the time of the supply voltage below V_{LVR})

Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq T_{LVR}$;

Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$, but $t < T_{LVR}$.

The LVR function is enabled by the code option.

It is typically used in AC line or large capacity battery applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage.

Low voltage reset can be applied to this, protecting system generates valid reset in the below set voltages.



8.8 Watchdog Timer (WDT) and Reset State

8.8.1 Feature

- Auto detect Program Counter (PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH79F0819 built in Program Counter (PC) over range detect circuit, if program counter value is larger than flash rom size, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash rom with A5H.

Watchdog Timer

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow time. The watchdog timer overflow flag (WDOF) will be automatically set to "1" by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

There are also some reset flags in this register as below:



8.8.2 Register

Table 8.30 Reset Control Register

| B1H, Bank0 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------|------|------|------|------|------|-------|-------|-------|
| RSTSTAT | WDOF | - | PORF | LVRF | - | WDT.2 | WDT.1 | WDT.0 |
| R/W | R/W | - | R/W | R/W | - | R/W | R/W | R/W |
| Reset Value (POR) | 0 | - | 1 | 0 | - | 0 | 0 | 0 |
| Reset Value (WDT) | 1 | - | u | u | - | 0 | 0 | 0 |
| Reset Value (LVR) | u | - | u | 1 | - | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | WDOF | <p>Watch Dog Timer Overflow or OVL Reset Flag Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows or no OVL reset generated 1: Watch Dog overflow or OVL reset occurred</p> |
| 5 | PORF | <p>Power On Reset Flag Set only by Power On Reset, cleared only by software 0: No Power On Reset 1: Power On Reset occurred</p> |
| 4 | LVRF | <p>Low Voltage Reset Flag Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred</p> |
| 3 | CLRF | <p>Pin Reset Flag Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred</p> |
| 2-0 | WDT[2:0] | <p>WDT Overflow period control bit 000: Overflow period minimal value= 4096ms 001: Overflow period minimal value= 1024ms 010: Overflow period minimal value = 256ms 011: Overflow period minimal value = 128ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms Notes: If WDT_opt is enable in application, you must clear WatchDog periodically, and the interval must be less than the minimum value listed above.</p> |



8.9 Power Management

8.9.1 Feature

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH79F0819 supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

8.9.2 Idle Mode

In this mode, the clock of CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH79F0819 enter Idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter Idle mode. The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

- (1) An interrupt generated. After warm-up time, the clock of the CPU will be restored, and the hardware will clear SUSLO register and IDL bit in PCON register. Then the program will execute the interrupt service routine first, and then jumps to the instruction immediately following the instruction that activated Idle mode.
- (2) Reset signal (WDT RESET if enabled, LVR RESET if enabled), this will restore the clock of the CPU, the SUSLO register and the IDL bit in PCON register will be cleared by hardware, finally the SH79F0819 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

8.9.3 Power-Down Mode

The Power-Down mode places the SH79F0819 in a very low power state.

When single clock signal input (OP_OSC[3:0] is 0000 or 1110), Power-Down mode will stop all the clocks including CPU and peripherals. When double clock signal input (OP_OSC[3:0] is 0011, 0110, 1010 or 1101), if system clock is 32.768kHz or 128kHz RC, Power-Down mode will stop all the clocks including CPU and peripherals. If high frequency oscillator is used as system clock, the clock which is used in LCD (or LED) and 32.768kHz or 128kHz RC used in Timer3 in Power-Down mode will be opened. In Power-Down mode, if WDT is enabled, WDT block will keep on working. When entering Power-Down mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained. By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79F0819 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79F0819 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

The setting of PD bit will be the last instruction that CPU executed.

Note: If IDL bit and PD bit are set simultaneously, the SH79F0819 enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit from Power-Down mode.

There are three ways to exit the Power-Down mode:

- (1) An active external Interrupt (such as INT2, INT3 & INT4) and LPD interrupt will make SH79F0819 exit Power-Down mode. The oscillator will start after interrupt happens, after warm-up time, the clocks of the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, the instructions which jumped to enter Power-Down mode will continue to run.
- (2) Timer3 interrupt will make SH79F0819 exit Power-Down mode when 32.768kHz or 128kHz RC is the clock source. The oscillator will start after interrupt happens, after warm-up time, the clocks of the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, the instructions which jumped to enter Power-Down mode will continue to run.
- (3) Reset signal (WDT RESET if enabled, LVR RESET if enabled). This will restore the clock of the CPU after warm-up time, the SUSLO register and the PD bit in PCON register will be cleared by hardware, finally the SH79F0819 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note: In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.



8.9.4 Register

Table 8.31 Power Control Register

| 87H | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|------|-------|------|------|------|------|------|------|
| PCON | SMOD | SSTAT | - | - | GF1 | GF0 | PD | IDL |
| R/W | R/W | R/W | - | - | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | - | - | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | SMOD | Baud rate double bit |
| 6 | SSTAT | SCON[7:5] function selection bit |
| 3-2 | GF[1:0] | General purpose flags for software use |
| 1 | PD | Power-Down mode control bit 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode |
| 0 | IDL | Idle mode control bit 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode |

Table 8.32 Suspend Mode Control Register

| 8EH | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| SUSLO | SUSLO.7 | SUSLO.6 | SUSLO.5 | SUSLO.4 | SUSLO.3 | SUSLO.2 | SUSLO.1 | SUSLO.0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value (POR/WDT/LVR/PIN) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7-0 | SUSLO[7:0] | This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise the either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle. |

Example:

```

IDLE_MODE:
    MOV     SUSLO, #55H
    ORL     PCON, #01H
    NOP
    NOP
    NOP

POWERDOWN_MODE:
    MOV     SUSLO, #55H
    ORL     PCON, #02H
    NOP
    NOP
    NOP
    
```



8.10 Warm-up Timer

8.10.1 Feature

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation start up

SH79F0819 has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read internal customer code option etc.

SH79F0819 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from low power consumption mode.

After power-on, SH79F0819 will start power warm-up procedure first, and then oscillator warm-up procedure. Began to run the program after the overflow.

Power Warm-up Time

| Power On Reset/ Pin Reset/ Low Voltage Reset | | WDT Reset (Not in Power-Down Mode) | | WDT Reset (Wakeup from Power-Down Mode) | | Wakeup from Power-Down Mode (Only for interrupt) | |
|--|-----------------|---------------------------------------|-----------------|---|-----------------|--|-----------------|
| TPWRT** | OSC Warm up* | TPWRT** | OSC Warm up* | TPWRT** | OSC Warm up* | TPWRT** | OSC Warm up* |
| 11ms | YES | ≈1ms | NO | 11ms | YES | ≈1ms | NO |

OSC Warm-up Time

| Option: OP_WMT Oscillator Type | 00 | 01 | 10 | 11 |
|--------------------------------------|-------------------------|-------------------------|-------------------------|----------------------|
| Ceramic/Crystal | $2^{17} \times T_{osc}$ | $2^{14} \times T_{osc}$ | $2^{11} \times T_{osc}$ | $2^8 \times T_{osc}$ |
| 32kHz Crystal | $2^{13} \times T_{osc}$ | | | |
| Internal RC | $2^7 \times T_{osc}$ | | | |



8.11 Code Option

OP_SCM:

- 0: SCM is invalid in warm up period
- 1: SCM is valid in warm up period

OP_LEDCOM:

- 0: LED common signal is normal (default)
- 1: LED common signal is inverted

OP_WDTPD:

- 0: Disable WDT function in Power-Down mode
- 1: Enable WDT function in Power-Down mode

OP_WDT:

- 0: Disable WDT function
- 1: Enable WDT function

OP_LVREN:

- 0: Disable LVR function
- 1: Enable LVR function

OP_LVRLE:

- 0: 4.3V LVR level 1
- 1: 2.1V LVR level 2

OP_WMT: (unavailable for 32kHz crystal and Internal RC)

- 00: longest warm up time
- 01: longer warm up time
- 10: shorter warm up time
- 11: shortest warm up time

OP_OSC:

- 0000: Oscillator1 is internal 12M RC, oscillator2 is disabled
- 0011: Oscillator1 is internal 128k RC, oscillator2 is internal 12M RC
- 0110: Oscillator1 is internal 128k RC, oscillator2 is 2M-12M crystal/ceramic oscillator
- 1010: Oscillator1 is 32.768k crystal oscillator, oscillator2 is internal 12M RC
- 1101: Oscillator1 is 32.768k crystal oscillator, oscillator2 is 2M-12M crystal/ceramic oscillator
- 1110: Oscillator1 is 2M-12M crystal/ceramic oscillator, oscillator2 is disabled
- Others: Oscillator1 is internal 12M RC, oscillator2 is disabled

OP_OSCDRIVE:

- 011: 8M-12M crystal
- 001: 4M crystal
- 111: 12M ceramic
- 101: 8M ceramic
- 110: 4M ceramic
- 100: 2M ceramic

OP_PORTDRIVE: (unavailable for P3)

- 0: Port drive ability normal mode
- 1: Port drive ability large mode (default)

OP_P3.3-P3.0:

- 0: port3 [3:0] sink ability normal mode
- 1: port3 [3:0] sink ability large mode (default)

OP_P3.7-P3.4:

- 0: port3 [7:4] sink ability large mode (default)
- 1: port3 [7:4] sink ability normal mode

**8.12 Programming Note**

1. Set the registers as follows in programming:

Register BUZCON (BDH, Bank0) must be written 0.

Program example:

```
MOV BUZCON, #00H
```

2. In order to improve reliability, unused bit of PxCR (x = 0-5) register should be written 1, unused bit of PxPCR (x = 0-5) register should be written 0, unused bit of Px (x = 0-5) register should be written 0.

Example Program (P0):

```
MOV P0CR, # 11XX1XXXB ; P0CR unused bit write 1, X is user's settings  
MOV P0PCR, # 00XX0XXXB; P0PCR unused bit write 1, X is user's settings  
MOV P0, # 00XX0XXXB ; P0 unused bit write 1, X is user's settings
```

3. LCD/LED:

In order to improve reliability, unused bit of PxSS (x = 0-3) register should be written 0.



9. Instruction Set

| ARITHMETIC OPERATIONS | | | | |
|-----------------------|---|------------------|------|---------|
| Opcode | Description | Code | Byte | Cycle |
| ADD A, Rn | Add register to accumulator | 0x28-0x2F | 1 | 1 |
| ADD A, direct | Add direct byte to accumulator | 0x25 | 2 | 2 |
| ADD A, @Ri | Add indirect RAM to accumulator | 0x26-0x27 | 1 | 2 |
| ADD A, #data | Add immediate data to accumulator | 0x24 | 2 | 2 |
| ADDC A, Rn | Add register to accumulator with carry flag | 0x38-0x3F | 1 | 1 |
| ADDC A, direct | Add direct byte to A with carry flag | 0x35 | 2 | 2 |
| ADDC A, @Ri | Add indirect RAM to A with carry flag | 0x36-0x37 | 1 | 2 |
| ADDC A, #data | Add immediate data to A with carry flag | 0x34 | 2 | 2 |
| SUBB A, Rn | Subtract register from A with borrow | 0x98-0x9F | 1 | 1 |
| SUBB A, direct | Subtract direct byte from A with borrow | 0x95 | 2 | 2 |
| SUBB A, @Ri | Subtract indirect RAM from A with borrow | 0x96-0x97 | 1 | 2 |
| SUBB A, #data | Subtract immediate data from A with borrow | 0x94 | 2 | 2 |
| INC A | Increment accumulator | 0x04 | 1 | 1 |
| INC Rn | Increment register | 0x08-0x0F | 1 | 2 |
| INC direct | Increment direct byte | 0x05 | 2 | 3 |
| INC @Ri | Increment indirect RAM | 0x06-0x07 | 1 | 3 |
| DEC A | Decrement accumulator | 0x14 | 1 | 1 |
| DEC Rn | Decrement register | 0x18-0x1F | 1 | 2 |
| DEC direct | Decrement direct byte | 0x15 | 2 | 3 |
| DEC @Ri | Decrement indirect RAM | 0x16-0x17 | 1 | 3 |
| INC DPTR | Increment data pointer | 0xA3 | 1 | 4 |
| MUL AB | 8 X 8 16 X 8 | Multiply A and B | 0xA4 | 1 20 |
| DIV AB | 8 / 8 16 / 8 | Divide A by B | 0x84 | 1 20 |
| DA A | Decimal adjust accumulator | 0xD4 | 1 | 1 |



| LOGIC OPERATIONS | | | | |
|-------------------|--|-----------|------|-------|
| Opcode | Description | Code | Byte | Cycle |
| ANL A, Rn | AND register to accumulator | 0x58-0x5F | 1 | 1 |
| ANL A, direct | AND direct byte to accumulator | 0x55 | 2 | 2 |
| ANL A, @Ri | AND indirect RAM to accumulator | 0x56-0x57 | 1 | 2 |
| ANL A, #data | AND immediate data to accumulator | 0x54 | 2 | 2 |
| ANL direct, A | AND accumulator to direct byte | 0x52 | 2 | 3 |
| ANL direct, #data | AND immediate data to direct byte | 0x53 | 3 | 3 |
| ORL A, Rn | OR register to accumulator | 0x48-0x4F | 1 | 1 |
| ORL A, direct | OR direct byte to accumulator | 0x45 | 2 | 2 |
| ORL A, @Ri | OR indirect RAM to accumulator | 0x46-0x47 | 1 | 2 |
| ORL A, #data | OR immediate data to accumulator | 0x44 | 2 | 2 |
| ORL direct, A | OR accumulator to direct byte | 0x42 | 2 | 3 |
| ORL direct, #data | OR immediate data to direct byte | 0x43 | 3 | 3 |
| XRL A, Rn | Exclusive OR register to accumulator | 0x68-0x6F | 1 | 1 |
| XRL A, direct | Exclusive OR direct byte to accumulator | 0x65 | 2 | 2 |
| XRL A, @Ri | Exclusive OR indirect RAM to accumulator | 0x66-0x67 | 1 | 2 |
| XRL A, #data | Exclusive OR immediate data to accumulator | 0x64 | 2 | 2 |
| XRL direct, A | Exclusive OR accumulator to direct byte | 0x62 | 2 | 3 |
| XRL direct, #data | Exclusive OR immediate data to direct byte | 0x63 | 3 | 3 |
| CLR A | Clear accumulator | 0xE4 | 1 | 1 |
| CPL A | Complement accumulator | 0xF4 | 1 | 1 |
| RL A | Rotate accumulator left | 0x23 | 1 | 1 |
| RLC A | Rotate accumulator left through carry | 0x33 | 1 | 1 |
| RR A | Rotate accumulator right | 0x03 | 1 | 1 |
| RRC A | Rotate accumulator right through carry | 0x13 | 1 | 1 |
| SWAP A | Swap nibbles within the accumulator | 0xC4 | 1 | 4 |



| DATA TRANSFERS | | | | |
|----------------------|---|-----------|------|-------|
| Opcode | Description | Code | Byte | Cycle |
| MOV A, Rn | Move register to accumulator | 0xE8-0xEF | 1 | 1 |
| MOV A, direct | Move direct byte to accumulator | 0xE5 | 2 | 2 |
| MOV A, @Ri | Move indirect RAM to accumulator | 0xE6-0xE7 | 1 | 2 |
| MOV A, #data | Move immediate data to accumulator | 0x74 | 2 | 2 |
| MOV Rn, A | Move accumulator to register | 0xF8-0xFF | 1 | 2 |
| MOV Rn, direct | Move direct byte to register | 0xA8-0xAF | 2 | 3 |
| MOV Rn, #data | Move immediate data to register | 0x78-0x7F | 2 | 2 |
| MOV direct, A | Move accumulator to direct byte | 0xF5 | 2 | 2 |
| MOV direct, Rn | Move register to direct byte | 0x88-0x8F | 2 | 2 |
| MOV direct1, direct2 | Move direct byte to direct byte | 0x85 | 3 | 3 |
| MOV direct, @Ri | Move indirect RAM to direct byte | 0x86-0x87 | 2 | 3 |
| MOV direct, #data | Move immediate data to direct byte | 0x75 | 3 | 3 |
| MOV @Ri, A | Move accumulator to indirect RAM | 0xF6-0xF7 | 1 | 2 |
| MOV @Ri, direct | Move direct byte to indirect RAM | 0xA6-0xA7 | 2 | 3 |
| MOV @Ri, #data | Move immediate data to indirect RAM | 0x76-0x77 | 2 | 2 |
| MOV DPTR, #data16 | Load data pointer with a 16-bit constant | 0x90 | 3 | 3 |
| MOVC A, @A+DPTR | Move code byte relative to DPTR to A | 0x93 | 1 | 7 |
| MOVC A, @A+PC | Move code byte relative to PC to A | 0x83 | 1 | 8 |
| MOVX A, @Ri | Move external RAM (8-bit address) to A | 0xE2-0xE3 | 1 | 5 |
| MOVX A, @DPTR | Move external RAM (16-bit address) to A | 0xE0 | 1 | 6 |
| MOVX @Ri, A | Move A to external RAM (8-bit address) | 0xF2-F3 | 1 | 4 |
| MOVX @DPTR, A | Move A to external RAM (16-bit address) | 0xF0 | 1 | 5 |
| PUSH direct | Push direct byte onto stack | 0xC0 | 2 | 5 |
| POP direct | Pop direct byte from stack | 0xD0 | 2 | 4 |
| XCH A, Rn | Exchange register with accumulator | 0xC8-0xCF | 1 | 3 |
| XCH A, direct | Exchange direct byte with accumulator | 0xC5 | 2 | 4 |
| XCH A, @Ri | Exchange indirect RAM with accumulator | 0xC6-0xC7 | 1 | 4 |
| XCHD A, @Ri | Exchange low-order nibble indirect RAM with A | 0xD6-0xD7 | 1 | 4 |



| PROGRAM BRANCHES | | | | |
|---|---|-----------|------|--------|
| Opcode | Description | Code | Byte | Cycle |
| ACALL addr11 | Absolute subroutine call | 0x11-0xF1 | 2 | 7 |
| LCALL addr16 | Long subroutine call | 0x12 | 3 | 7 |
| RET | Return from subroutine | 0x22 | 1 | 8 |
| RETI | Return from interrupt | 0x32 | 1 | 8 |
| AJMP addr11 | Absolute jump | 0x01-0xE1 | 2 | 4 |
| LJMP addr16 | Long jump | 0x02 | 3 | 5 |
| SJMP rel | Short jump (relative address) | 0x80 | 2 | 4 |
| JMP @A+DPTR | Jump indirect relative to the DPTR | 0x73 | 1 | 6 |
| JZ rel (not taken) (taken) | Jump if accumulator is zero | 0x60 | 2 | 3 5 |
| JNZ rel (not taken) (taken) | Jump if accumulator is not zero | 0x70 | 2 | 3 5 |
| JC rel (not taken) (taken) | Jump if carry flag is set | 0x40 | 2 | 2 4 |
| JNC rel (not taken) (taken) | Jump if carry flag is not set | 0x50 | 2 | 2 4 |
| JB bit, rel (not taken) (taken) | Jump if direct bit is set | 0x20 | 3 | 4 6 |
| JNB bit, rel (not taken) (taken) | Jump if direct bit is not set | 0x30 | 3 | 4 6 |
| JBC bit, rel (not taken) (taken) | Jump if direct bit is set and clear bit | 0x10 | 3 | 4 6 |
| CJNE A, direct, rel (not taken) (taken) | Compare direct byte to A and jump if not equal | 0xB5 | 3 | 4 6 |
| CJNE A, #data, rel (not taken) (taken) | Compare immediate to A and jump if not equal | 0xB4 | 3 | 4 6 |
| CJNE Rn, #data, rel (not taken) (taken) | Compare immediate to reg. and jump if not equal | 0xB8-0xBF | 3 | 4 6 |
| CJNE @Ri, #data, rel (not taken) (taken) | Compare immediate to Ri and jump if not equal | 0xB6-0xB7 | 3 | 4 6 |
| DJNZ Rn, rel (not taken) (taken) | Decrement register and jump if not zero | 0xD8-0xDF | 2 | 3 5 |
| DJNZ direct, rel (not taken) (taken) | Decrement direct byte and jump if not zero | 0xD5 | 3 | 4 6 |
| NOP | No operation | 0 | 1 | 1 |



| BOOLEAN MANIPULATION | | | | |
|-----------------------------|---------------------------------------|-------------|-------------|--------------|
| Opcode | Description | Code | Byte | Cycle |
| CLR C | Clear carry flag | 0xC3 | 1 | 1 |
| CLR bit | Clear direct bit | 0xC2 | 2 | 3 |
| SETB C | Set carry flag | 0xD3 | 1 | 1 |
| SETB bit | Set direct bit | 0xD2 | 2 | 3 |
| CPL C | Complement carry flag | 0xB3 | 1 | 1 |
| CPL bit | Complement direct bit | 0xB2 | 2 | 3 |
| ANL C, bit | AND direct bit to carry flag | 0x82 | 2 | 2 |
| ANL C, /bit | AND complement of direct bit to carry | 0xB0 | 2 | 2 |
| ORL C, bit | OR direct bit to carry flag | 0x72 | 2 | 2 |
| ORL C, /bit | OR complement of direct bit to carry | 0xA0 | 2 | 2 |
| MOV C, bit | Move direct bit to carry flag | 0xA2 | 2 | 2 |
| MOV bit, C | Move carry flag to direct bit | 0x92 | 2 | 3 |



10. Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage. -0.3V to +6.0V
 Input/Output Voltage. GND-0.3V to V_{DD}+0.3V
 Operating Ambient Temperature. -40°C to +85°C
 Storage Temperature. -55°C to +125°C
 FLASH write/erase operating. 0°C to +85°C

***Comments**

Stresses exceed those listed under “**Absolute Maximum Ratings**” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 2.0V - 5.5V, GND = 0V, T_A = +25°C, unless otherwise specified)

| Parameter | Symbol | Min. | Typ.* | Max. | Unit | Condition |
|-------------------------------|------------------|-----------------------|-------|-----------------------|------|---|
| Operating Voltage | V _{DD} | 2.0 | 5.0 | 5.5 | V | 32.768kHz or 2MHz ≤ f _{OSC} ≤ 12.3MHz |
| Operating Current | I _{OP} | - | 5 | 10 | mA | f _{OSC} = 12.3MHz, V _{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, all other function block off |
| | I _{OP2} | - | 25 | 35 | μA | f _{OSC} = 32.768kHz, OSCX off, V _{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), LVR off, WDT off, all other function block off |
| Stand by Current (IDLE) | I _{SB1} | - | 3 | 5 | mA | f _{OSC} = 12.3MHz, V _{DD} = 5.0V All output pins unload (including all digital input pins unfloating), CPU off (IDLE), WDT off, LVR on, LCD on(not including LCD panel), all other function block off |
| | I _{SB2} | - | 15 | 20 | μA | f _{OSC} = 32.768kHz, OSCX off, V _{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU off (IDLE), WDT off, LVR on, LCD on(not including LCD panel), all other function block off |
| Stand by Current (Power-Down) | I _{SB3} | - | 2 | 10 | μA | Osc off, V _{DD} = 5.0V All output pins unload(including all digital input pins unfloating), CPU off (Power-Down), LVR on, LCD off, WDT off, all other function block off |
| | I _{SB4} | - | 4 | 15 | μA | f _{OSC} = 32.768kHz, OSCX off, V _{DD} = 5.0V All output pins unload (including all digital input pins unfloating), CPU off (Power-Down), LVR on, LCD off, WDT off, all other function block off |
| WDT Current | I _{WDT} | - | 1 | 3 | μA | All output pins unload, WDT on, V _{DD} = 5.0V |
| LCD Current | I _{LCD} | - | 6 | 7 | μA | traditional resistance LCD mode, V _{DD} = 5.0V 300kΩ LCD bias resistance, contrast[3:0] = 1111 |
| LPD Current | I _{LPD} | - | - | 1 | μA | V _{DD} = 2.0 - 5.5V |
| Input Low Voltage 1 | V _{IL1} | GND | - | 0.3 X V _{DD} | V | I/O Ports, RXD (RxDCON[1:0] = 11) |
| Input High Voltage 1 | V _{IH1} | 0.7 X V _{DD} | - | V _{DD} | V | I/O Ports |

(to be continued)



(continue)

| Parameter | Symbol | Min. | Typ.* | Max. | Unit | Condition |
|--|------------------|-----------------------|-------|-----------------------|------|---|
| Input Low Voltage 2 | V _{IL2} | GND | - | 0.2 X V _{DD} | V | RST, INT2/3/4, RXD (RxDCON[1:0] = 00), FLT, V _{DD} = 2.4 - 5.5V |
| | | GND | - | 0.4 X V _{DD} | V | RXD (RxDCON[1:0] = 01), V _{DD} = 2.4 - 5.5V |
| | | GND | - | 0.5 X V _{DD} | V | RXD (RxDCON[1:0] = 10), V _{DD} = 2.4 - 5.5V |
| Input High Voltage 2 | V _{IH2} | 0.8 X V _{DD} | - | V _{DD} | V | RST, INT2/3/4, RXD, FLT, V _{DD} = 2.4 - 5.5V |
| Input Leakage Current | I _{IL} | -1 | - | 1 | μA | Input pad, V _{IN} = V _{DD} or GND |
| Output Leakage Current | I _{OL} | -1 | - | 1 | μA | Open-drain output, V _{DD} = 5.0V V _{OUT} = V _{DD} or GND |
| Pull-high Resistor | R _{PH} | - | 30 | - | kΩ | V _{DD} = 5.0V, V _{IN} = GND |
| Rest pin Pull-high Resistor | R _{RPH} | - | 30 | - | kΩ | V _{DD} = 5.0V, V _{IN} = GND |
| Output High Voltage1 | V _{OH1} | V _{DD} - 0.7 | - | - | V | I/O port (P3), IOH = -10mA, V _{DD} = 5.0V |
| Output High Voltage2 | V _{OH2} | V _{DD} - 0.7 | - | - | V | I/O ports (P0, P1, P2, and P4, and P5), IOH = -10mA, V _{DD} = 5.0V OP_PORTDRIVE select normal mode (Code Option) |
| Output High Voltage3 | V _{OH3} | V _{DD} - 0.7 | - | - | V | I/O ports (P0, P1, P2, and P4, and P5), IOH = -20mA, V _{DD} = 5.0V OP_PORTDRIVE select large mode(Code Option) |
| Output Low Voltage1 | V _{OL1} | - | - | GND + 0.6 | V | I/O Ports, (P0, P1, P2, P4, P5) I _{OL} = 15mA, V _{DD} = 5.0V |
| Output Low Voltage2 | V _{OL2} | - | - | GND + 0.6 | V | I/O ports (P3), IOL = 15mA, V _{DD} = 5.0V OP_P3.3-P3.0 and OP_P3.7-P3.4 both select normal mode(Code Option) |
| large drive port sink current capability | I _{OL} | 120 | 140 | - | mA | I/O port (P3), V _{DD} = 5.0V, V _{OL} = GND + 1.5V OP_P3.3-P3.0 and OP_P3.7-P3.4 both select large mode(Code Option) |
| LCD Resistor | R _{ON} | - | 5 | - | kΩ | SEG1 - 10, 14, 19, COM1 - 4, V _{DD} = 3.6V - 5.0V The voltage variation of V1, V2, V3 is less than 0.2V |

Note:

- (1) "*" Data in "Typ." Column is at 5.0V, 25°C, unless otherwise specified.
 (2) Maximum value of the supply current to V_{DD} is 150mA.
 (3) Maximum value of the output current from GND is 200mA.



A/D Converter Electrical Characteristics ($V_{DD} = 3V$, $GND = 0V$, $T_A = 25^\circ C$, Unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|------------|------|-----------|-----------|-----------|--|
| Supply Voltage | V_{AD} | 2.5 | 3 | 3.5 | V | |
| Resolution | N_R | - | 10 | - | bit | $GND \leq V_{AIN} \leq V_{REF}$ |
| A/D Input Voltage | V_{AIN} | GND | - | V_{REF} | V | |
| A/D Input Resistor* | R_{AIN} | 2 | - | - | $M\Omega$ | $V_{IN} = 3.0V$ |
| Recommended impedance of analog voltage source | Z_{AIN} | - | - | 10 | $k\Omega$ | |
| A/D conversion current | I_{AD} | - | 1 | 3 | mA | ADC module operating, $V_{DD} = 3.0V$ |
| A/D Input current | I_{ADIN} | - | - | 10 | μA | $V_{DD} = 3.0V$ |
| Differential linearity error | D_{LE} | - | - | ± 1 | LSB | $f_{OSC} = 12.3MHz$, $V_{DD} = 3.0V$ |
| Integral linearity error | I_{LE} | - | - | ± 2 | LSB | $f_{OSC} = 12.3MHz$, $V_{DD} = 3.0V$ |
| Full scale error | E_F | - | ± 1 | ± 3 | LSB | $f_{OSC} = 12.3MHz$, $V_{DD} = 3.0V$ |
| Offset error | E_Z | - | ± 0.5 | ± 3 | LSB | $f_{OSC} = 12.3MHz$, $V_{DD} = 3.0V$ |
| Total Absolute error | E_{AD} | - | - | ± 3 | LSB | $f_{OSC} = 12.3MHz$, $V_{DD} = 3.0V$ |
| Total Conversion time** | T_{CON} | 14 | - | - | t_{AD} | 10 bit Resolution, $V_{DD} = 3.0V$, $t_{AD} = 1\mu s$ |

Note:

- (1) "*" shows ADC input resistance is ADC itself input resistance under the condition of DC.
- (2) "**" suggest the signal source resistance is less than $10k\Omega$, which is connected with the ADC.

AC Electrical Characteristics ($V_{DD} = 2.0V - 5.5V$, $GND = 0V$, $T_A = 25^\circ C$, $f_{OSC} = 12.3MHz$, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--------------------------|----------------|------|---------|---------|---------|--|
| Oscillator start time | T_{OSC} | - | - | 1 | s | $f_{OSC} = 32.768kHz$ |
| | T_{OSC} | - | 1 | 2 | ms | $f_{OSC} = 12.3MHz$ |
| RESET pulse width | t_{RESET} | 10 | - | - | μs | Low active |
| WDT RC Frequency | f_{WDT} | - | 2 | 3 | kHz | |
| Frequency Stability (RC) | $ \Delta F /F$ | - | ± 1 | ± 2 | % | RC Oscillator $ F - 12.3MHz /12.3MHz$ ($V_{DD} = 2.0 - 5.0V$, $T_A = -40^\circ C$ to $+85^\circ C$) |
| | | - | - | ± 2 | % | RC Oscillator $ F - 128kHz /128kHz$ ($V_{DD} = 2.0 - 5.0V$, $T_A = 25^\circ C$) |

Low Voltage Reset Electrical Characteristics ($V_{DD} = 2.0V - 5.5V$, $GND = 0V$, $T_A = +25^\circ C$, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-------------------------------|------------|------|------|------|---------|-------------------------------------|
| LVR Voltage1 | V_{LVR1} | 4.2 | 4.3 | 4.4 | V | LVR enabled $V_{DD} = 2.0 - 5.0V$, |
| LVR Voltage2 | V_{LVR2} | 2.0 | 2.1 | 2.2 | V | LVR enabled $V_{DD} = 2.0 - 5.0V$, |
| Drop-Down Pulse Width for LVR | T_{LVR} | - | 60 | - | μs | |

12.3MHz crystal Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------|-----------|------|------|------|------|-----------|
| Frequency | F_{12M} | - | 12.3 | - | MHz | |
| Capacitor | C_L | - | 12.5 | - | pF | |

32.768kHz crystal Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------|-----------|------|-------|------|------|-----------|
| Frequency | F_{32k} | - | 32768 | - | Hz | |
| Capacitor | C_L | - | 12.5 | - | pF | |



11. Ordering Information

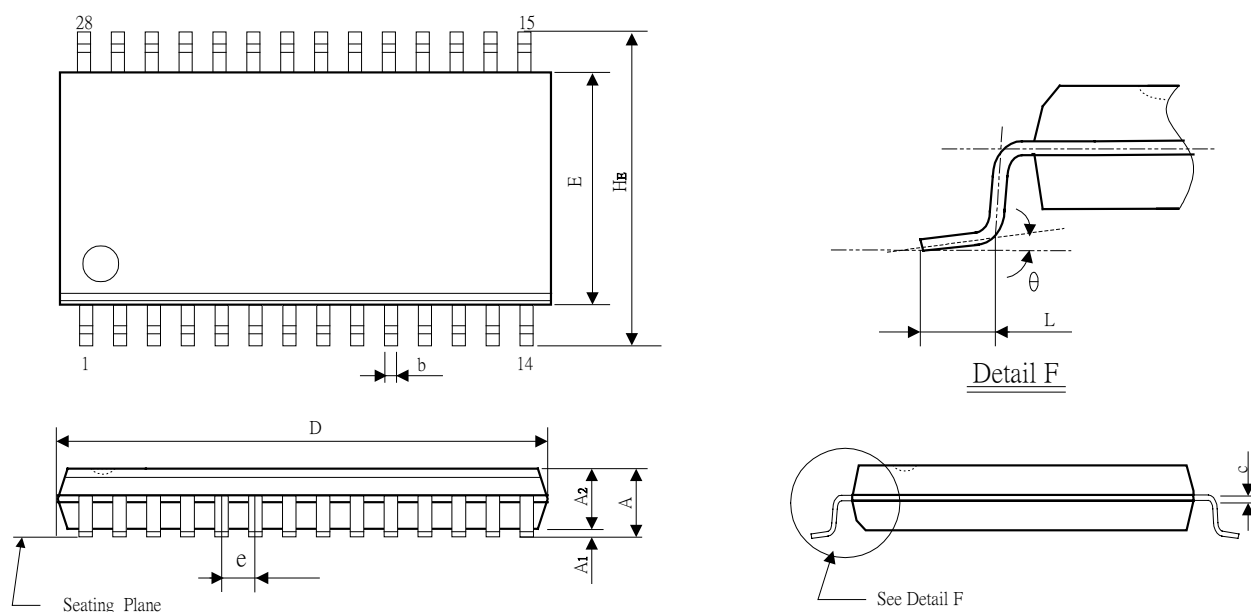
| Part No. | Package |
|------------------|----------------|
| SH79F0819M/028MU | SOP28 |



12. Package Information

SOP28L Outline Dimensions

unit: inches/mm



| Symbol | Dimensions in inches | | Dimensions in mm | |
|----------------|----------------------|-------|------------------|-------|
| | Min | Max | Min | Max |
| A | 0.085 | 0.104 | 2.15 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| A2 | 0.081 | 0.098 | 2.05 | 2.50 |
| b | 0.013 | 0.02 | 0.33 | 0.51 |
| c | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.697 | 0.715 | 17.70 | 18.15 |
| E | 0.291 | 0.3 | 7.40 | 7.62 |
| e | 0.050(BSC) | | 1.27(BSC) | |
| H _E | 0.402 | 0.418 | 10.21 | 10.61 |
| L | 0.016 | 0.05 | 0.40 | 1.27 |
| θ | 0° | 8° | 0° | 8° |

Notes:

1. The maximum of Dimension D includes burrs at the end.
2. Dimension E do not include resin fins.
3. Dimension e1 is designed for pin space of PC board interface, it is only for reference.
4. Dimension S includes burrs at the end.



13. Product SPEC. Change Notice

| Version | Content | Date |
|----------------|----------------------------|-------------|
| 2.1 | Update Package Information | Jun. 2015 |
| 2.0 | Original | May. 2014 |



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