SINO WEALTH

SH79F085/SH79F165

Enhanced 8051 Microcontroller with 20-Bit ADC

1. Features

- 8051 compatible Pipe-lined instruction based on the single-chip 8-bit microcontroller
- Flash ROM：
  - SH79F085: 8K Bytes
  - SH79F165: 16K Bytes
- RAM: internal 256 Bytes, external 256 Bytes
- EEPROM: internal 512 Bytes
- Operation Voltage: V_{DD} = 3.0V - 5.5V
- Oscillator (code option):
  - Crystal oscillator: 400kHz - 16.6MHz
  - Crystal oscillator: 32.768kHz
  - Internal RC: 16.6MHz
  - Internal RC: 128kHz
- 15/19 CMOS bi-directional I/O pins
  - SH79F085: 15/19 I/O
  - SH79F165: 19 I/O
- Built-in pull-up resistor for input pin
- Four 16-bit timer/counters: T0, T1, T2, T3
- Built-in EUART
- Powerful interrupt sources:
  - Timer0, Timer1, Timer2, Timer3
  - INT0 - 2
  - ADC, EUART, SCM
- Built-in Buzzer
- In system programming (ISP)
- Built-in regulator
  - Output voltage: 2.7V
- 20-Bit Σ-ΔAnalog Digital Converter (ADC)
  - 20-bit data output, 16-bit resolution
  - SH79F085: 2 differential input
  - SH79F165: 3 differential input
- Built-in Programmable Gain Amplifier (PGA)
  - Gain: 12.5X - 200X
- Built-in Low Voltage Reset (LVR) function
  - LVR Voltage: 3.1V
  - LVR Voltage: 4.3V
- CPU Machine cycle: 1 oscillator clock
- Built-in Watch Dog Timer (WDT) (code option)
- Built-in oscillator Warm-up Timer
- Support low power operation modes:
  - IDLE Mode
  - Power-Down Mode
- Flash Type
- Package:
  - SH79F085: TSSOP20/SOP24
  - SH79F165: SOP24

2. General Description

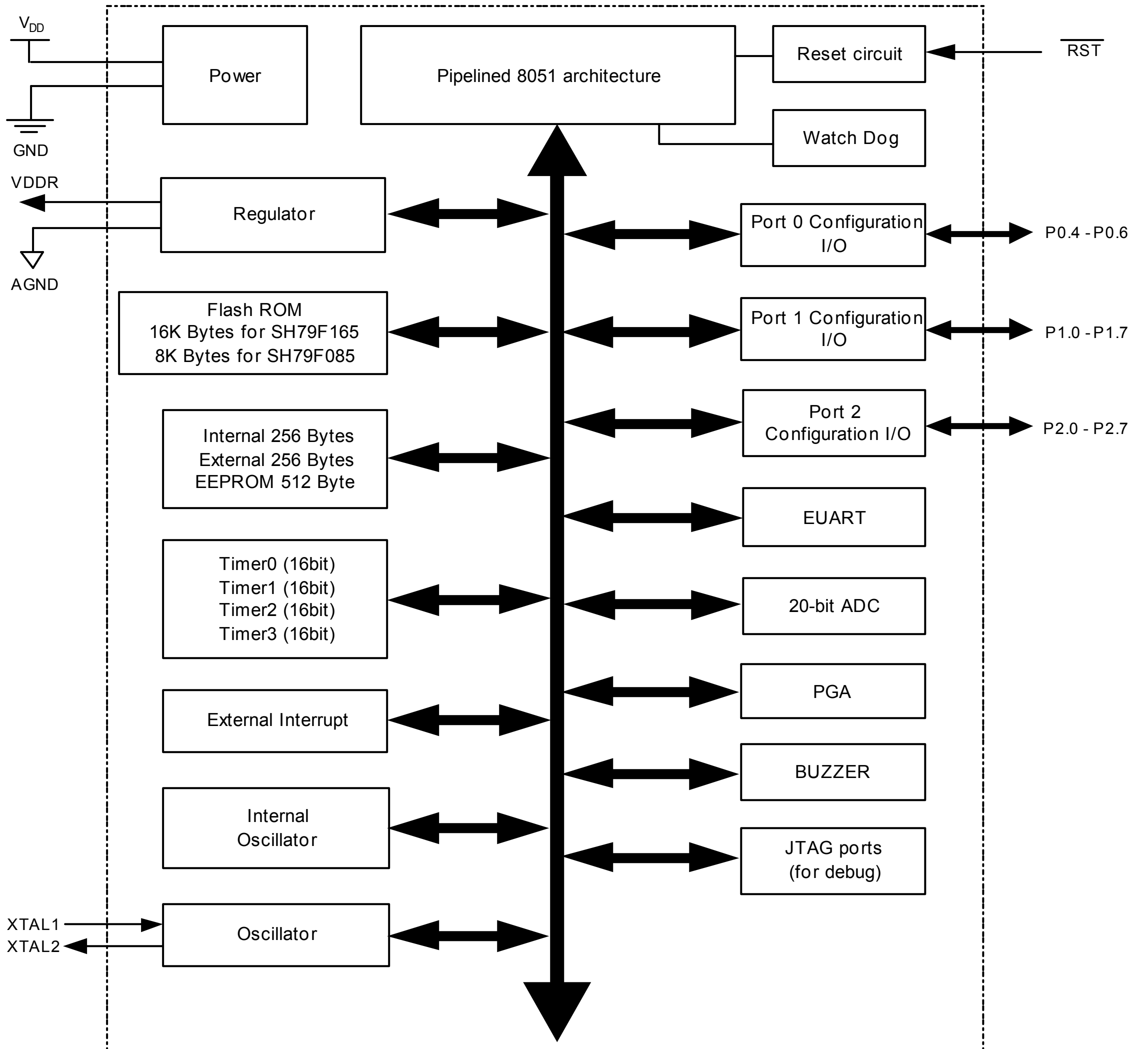
The SH79F085/SH79F165 is a fast 8051 compatible micro-controller with a redesigned CPU of no wasted clock and memory cycles. Typically, it will be faster and exhibit better performance than the traditional 8051 at the same oscillator frequency.

The SH79F085/SH79F165 retains most features of the standard 8051. These features include internal 256 bytes RAM and four 16-bit timer/counters, one UART, and external interrupt INT0, INT1 & INT2. The SH79F085 contains 8K bytes Flash memory block both for program and data. The SH79F165 contains 16K bytes Flash memory block both for program and data.

Some standard communication modes such as EUART are supported in the SH79F085/SH79F165. Also the 20-bit Σ-Δ analog to digital converter (ADC) are incorporated in SH79F085/SH79F165.

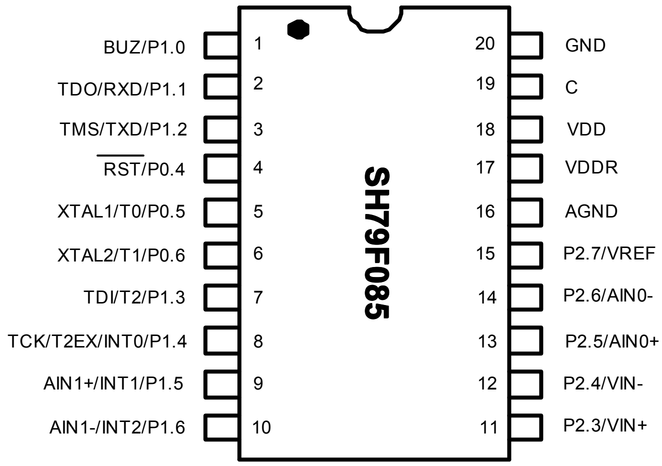
For high reliability and low cost, the SH79F085/SH79F165 builds in Watchdog Timer and Low Voltage Reset function. And SH79F085/SH79F165 also supports two power saving modes to reduce power consumption.

3. Block Diagram

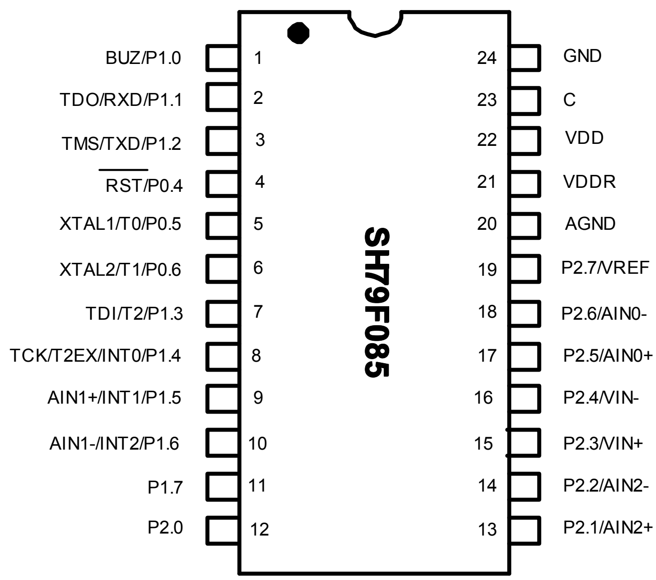


4. Pin Configuration

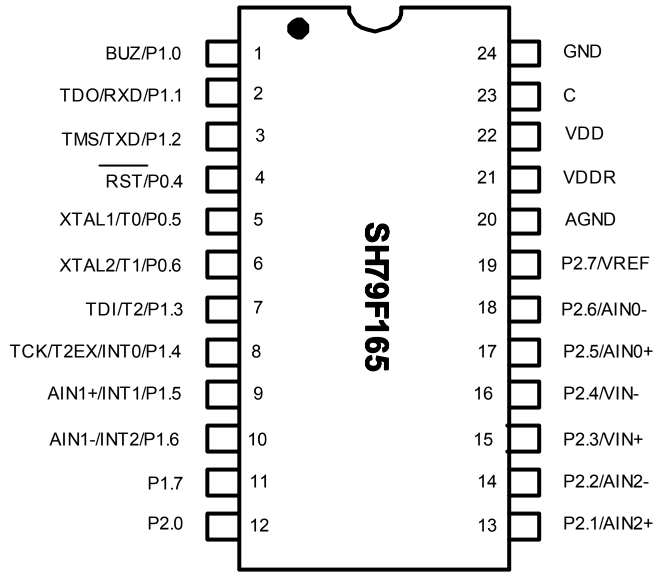
SH79F085 Package: TSSOP20



SH79F085 Package: SOP24



SH79F165 Package: SOP24



Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram). This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function use.

Table 4.1 Pin Function

Pin No.			Pin Name	Default Function
SH79F085 (TSSOP20)	SH79F085 (SOP24)	SH79F165 (SOP24)		
1	1	1	BUZ/P1.0	P1.0
2	2	2	TDO/RXD/P1.1	P1.1
3	3	3	TMS/TXD/P1.2	P1.2
4	4	4	$\overline{RST}$/P0.4	P0.4 or reset pin, controlled by code option
5	5	5	XTAL1/T0/P0.5	P0.5 or XTAL1, controlled by code option
6	6	6	XTAL2/T1/P0.6	P0.6 or XTAL2, controlled by code option
7	7	7	TDI/T2/P1.3	P1.3
8	8	8	TCK/T2EX/INT0/P1.4	P1.4
9	9	9	AIN1+/INT1/P1.5	P1.5
10	10	10	AIN1-/INT2/P1.6	P1.6
-	11	11	P1.7	P1.7
-	12	12	P2.0	P2.0
-	13	13	AIN2+/P2.1	P2.1
-	14	14	AIN2-/P2.2	P2.2
11	15	15	VIN+/P2.3	P2.3
12	16	16	VIN-/P2.4	P2.4
13	17	17	AIN0+/P2.5	P2.5
14	18	18	AIN0-/P2.6	P2.6
15	19	19	VREF/P2.7	P2.7
16	20	20	AGND	AGND
17	21	21	VDDR	VDDR
18	22	22	V_{DD}	V_{DD}
19	23	23	C	C
20	24	24	GND	GND

5. Pin Description

Pin No.	Type	Description
Port		
P0.4 - P0.6	I/O	3-bit bi-directional I/O port
P1.0 - P1.7	I/O	8-bit bi-directional I/O port
P2.0 - P2.7	I/O	8-bit bi-directional I/O port
Timer		
T0	I/O	Timer0 external input/comparator output
T1	I/O	Timer1 external input/comparator output
T2	I/O	Timer2 external input/baud rate output
T3	I	Timer3 external input
T2EX	I	Timer2 Reload/Capture/Direction control
EUART		
RXD	I	EUART data input
TXD	O	EUART data output
Buzzer		
BUZ	O	Buzzer output pin
ADC		
AIN0-	I	Negative differential input 0
AIN0+	I	Positive differential input 0
AIN1-	I	Negative differential input 1
AIN1+	I	Positive differential input 1
AIN2-	I	Negative differential input 2
AIN2+	I	Positive differential input 2
VREF	I/O	Reference voltage input/output pin
VIN+	I/O	PGA positive input/output pin
VIN-	I/O	PGA negative input/output pin

(to be continued)

(continue)

Pin No.	Type	Description
Interrupt & Reset & Clock & Power		
INT0 - INT2	I	Interrupt 0 - 2
$\overline{RST}$	I	A Low on this pin for 10us longer will reset the device. An internal diffused resistor to V_{DD} permits a power-on reset using only an external capacitor to GND
XTAL1	I	External oscillator input
XTAL2	O	External oscillator output
GND	P	Ground
AGND	P	Analog ground
V_{DD}	P	Power supply (3.0 - 5.5V)
VDDR	P	Built-in regulator output for analog (2.7V), connect 47µF capacitor
C	P	Built-in regulator output for core (1.8V), connect 47µF capacitor
Programmer		
TDO (P1.1)	O	Debug interface: Test data out
TMS (P1.2)	I	Debug interface: Test mode select
TDI (P1.3)	I	Debug interface: Test data in
TCK (P1.4)	I	Debug interface: Test clock in

Note:
When P1.1-1.4 used as debug interface，P1.1-1.4 function are blocked

6. SFR Mapping

The SH79F085/SH79F165 provides 256 bytes of internal RAM to contain general-purpose data memory and Special Function Register (SFR). The SFR of the SH79F085/SH79F165 fall into the following categories:

CPU Core Registers:	ACC, B, PSW, SP, DPL, DPH
Enhanced C51 Core Registers:	AUXC, DPL1, DPH1, INSCON, XPAGE
Power and Clock Control Registers:	PCON, SUSLO
Flash Registers:	IB_OFFSET, IB_DATA, IB_CON1, IB_CON2, IB_CON3, IB_CON4, IB_CON5, FLASHCON
Data Memory Register:	XPAGE
Hardware Watch Dog Timer Register:	RSTSTAT
System Clock Control Register:	CLKCON
Interrupt System Registers:	IEN0, IEN1, IPH0, IPL0, IPH1, IPL1, EXF0
I/O Port Registers:	P0, P1, P2, P0CR, P1CR, P2CR, P0PCR, P1PCR, P2PCR
Timer Registers:	TCON, TMOD, TH0, TH1, TL0, TL1, T2CON, T2MOD, TH2, TL2, RCAP2L, RCAP2H, TCON1, T3CON, TL3, TH3
EUART Registers:	SCON, SBUF, SADEN, SADDR, PCON
Regulator Register:	REGCON
PGA Register:	PGAM
ADC Register:	ADCON, ADT, ADCH, ADDL, ADDM, ADDH, ADRAND
BUZZER Register:	BUZCON

Table 6.1 C51 Core SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	00--00-0	BKS1	BKS0	-	-	DIV	MUL	-	DPS

Table 6.2 Power and Clock Control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 6.3 Regulator SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REGCON	A1H	Regulator Control	-------0	-	-	-	-	-	-	-	REGEN

Table 6.4 Flash Control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFF SET	FBH	Offset Register for Programming	00000000	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
IB_DATA	FCH	Data Register for Programming	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1	F2H	SSP Type Select Register	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2	F3H	Flash Memory Control Register 1	----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3	F4H	Flash Memory Control Register 2	----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4	F5H	Flash Memory Control Register 3	----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5	F6H	Flash Memory Control Register 4	----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
XPAGE	F7H	Memory Page	--000000	-	-	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
FLASHCON	A7H	Flash Access Control	-------0	-	-	-	-	-	-	-	FAC

Table 6.5 WDT SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H	Watchdog Timer Control	*-***000	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

***Note:** *RSTSTAT initial value is determined by different RESET.*

Table 6.6 System Clock Control SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	B2H	System Clock Control	-11-00--	-	CLKS1	CLKS0	-	HFON	FS	-	-

Table 6.7 Interrupt SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H	Interrupt Enable Control0	00000000	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
IEN1	A9H	Interrupt Enable Control1	0--0--0-	ESCM	-	-	ET3	-	-	EX2	-
IPH0	B4H	Interrupt Priority Control High0	-0000000	-	PADCH	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H
IPL0	B8H	Interrupt Priority Control Low0	-0000000	-	PADCL	PT2L	PS0L	PT1L	PX1L	PT0L	PX0L
IPH1	B5H	Interrupt Priority Control High1	0--0--0-	PSCML	-	-	PT3H	-	-	PX2H	-
IPL1	B9H	Interrupt Priority Control Low1	0--0--0-	PSCMH	-	-	PT3L	-	-	PX2L	-
EXF0	E8H	External Interrupt Control0	----00-0	-	-	-	-	IT2.1	IT2.0	-	IE2

Table 6.8 Port SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	80H	3-bit Port0	-000----	-	P0.6	P0.5	P0.4	-	-	-	-
P1	90H	8-bit Port1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2	A0H	8-bit Port2	00000000	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P0CR	E1H	Port0 input/output direction control	-000----	-	P0CR.6	P0CR.5	P0CR.4	-	-	-	-
P1CR	E2H	Port1 input/output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR	E3H	Port1 input/output direction control	00000000	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P0PCR	E9H	Internal pull-high enable for Port0	-000----	-	P0PCR.6	P0PCR.5	P0PCR.4	-	-	-	-
P1PCR	EAH	Internal pull-high enable for Port1	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR	EBH	Internal pull-high enable for Port2	00000000	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0

Table 6.9 Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	88H	Timer/Counter0/1 Control	00000000	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89H	Timer/Counter0/1 Mode	00000000	GATE1	$C/\overline{T1}$	M11	M10	GATE0	$C/\overline{T0}$	M01	M00
TL0	8AH	Timer/Counter0 Low Byte	00000000	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
TH0	8CH	Timer/Counter0 High Byte	00000000	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
TL1	8BH	Timer/Counter1 Low Byte	00000000	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.1
TH1	8DH	Timer/Counter1 High Byte	00000000	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.1
T2CON	C8H	Timer/Counter2 Control	00000000	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	CP/RL2
T2MOD	C9H	Timer/Counter2 Mode	0----00	TCLKP2	-	-	-	-	-	T2OE	DCEN
RCAP2L	CAH	Timer/Counter 2 Reload/Capture Low Byte	00000000	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	CBH	Timer/Counter 2 Reload/Capture High Byte	00000000	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH	Timer/Counter4 Control	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH	Timer/Counter4 Low Byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
TCON1	CEH	Timer/Counter4 High Byte	-00-0000	-	TCLK_S1	TCLK_S0	-	TCLKP1	TCLKP0	TC1	TC0
T3CON	88H Bank1	Timer3 Control	0-00-000	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
TL3	8CH Bank1	Timer3 Reload/Counter Low Byte	00000000	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	8DH Bank1	Timer3 Reload/Counter High Byte	00000000	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0

Table 6.10 EUART SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	98H	Serial Control	00000000	SM0/FE	SM1/RXOV	SM2/TXCOL	REN	TB8	RB8	TI	RI
SBUF	99H	Serial Data Buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADEN	9BH	Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
SADDR	9AH	Slave Address	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
PCON	87H	Power & Serial Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL

Table 6.11 PGA SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGAM	A3H	PGA模式控制寄存器	0000-000	PGAEN	GAIN2	GAIN1	GAIN0	-	CHOPEN	CHOPC1	CHOPC0

Table 6.12 ADC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	93H	ADC Control	0000-000	ADON	ADCIF	ADCM	REFC	-	SCH2	SCH1	SCH0
ADT	94H	ADC Clock Control	00000000	TADC7	TADC6	TADC5	TADC4	TADC3	TADC2	TADC1	TADC0
ADCH	95H	ADC Channel Configuration	00000000	VREF2	VREF1	VREF0	CTR1	P27OS	CH2	CH1	CH0
ADDL	91H	ADC Data Low Byte	----0000	-	-	-	-	A3	A2	A1	A0
ADDM	96H	ADC Data Middle Byte	00000000	A11	A10	A9	A8	A7	A6	A5	A4
ADDH	97H	ADC Data High Byte	00000000	A19	A18	A17	A16	A15	A14	A13	A12
ADRAND	B7H	ADC Random Clock Control	0---0000	RANDEN	-	-	-	RAND3	RAND2	RAND1	RAND0

Table 6.13 Buzzer SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUZCON	BDH	Buzzer Output Control	---00000	-	-	-	BCA3	BCA2	BCA1	BCA0	BZEN

Note: *-: unimplemented*

SFR Map

Bank0

	Bit Addressable	Non Bit Addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H				IB_OFFSET	IB_DATA				FFH
F0H	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7H
E8H	EXF0	P0PCR	P1PCR	P2PCR					EFH
E0H	ACC	P0CR	P1CR	P2CR					E7H
D8H									DFH
D0H	PSW								D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	TCON1		CFH
C0H									C7H
B8H	IPL0	IPL1				BUZCON			BFH
B0H		RSTSTAT	CLKCON		IPH0	IPH1		ADRAND	B7H
A8H	IEN0	IEN1							AFH
A0H	P2	REGCON		PGAM				FLASHCON	A7H
98H	SCON	SBUF	SADDR	SADEN					9FH
90H	P1	ADDL		ADCON	ADT	ADCH	ADDM	ADDH	97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	SUSLO		8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	7/F	

Note: *The unused addresses of SFR are not available.*

Bank1

	Bit Addressable	Non Bit Addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H									FFH
F0H	B	C						XPAGE	F7H
E8H									EFH
E0H	ACC								E7H
D8H									DFH
D0H	PSW								D7H
C8H									CFH
C0H									C7H
B8H	IPL0	IPL1							BFH
B0H					IPH0	IPH1			B7H
A8H	IEN0	IEN1							AFH
A0H									A7H
98H									9FH
90H									97H
88H	T3CON				TL3	TH3	SUSLO		8FH
80H		SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

Note: *The unused addresses of SFR are not available.*

7. Normal Function

7.1 CPU

7.1.1 CPU Core SFR

Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Table 7.1 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**CY**	**Carry flag bit** 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	**AC**	**Auxiliary Carry flag bit** 0: an auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	**F0**	**F0 flag bit** Available to the user for general purposes
4-3	**RS[1:0]**	**R0-R7 Register bank select bits** 00: Bank0 (Address to 00H-07H) 01: Bank1 (Address to 08H-0FH) 10: Bank2 (Address to 10H-17H) 11: Bank3 (Address to 18H-1FH)
2	**OV**	**Overflow flag bit** 0: no overflow happen 1: an overflow happen
1	**F1**	**F1 flag bit** Available to the user for general purposes
0	**P**	**Parity flag bit** 0: an even number of "one" bits in the Accumulator 1: an odd number of "one" bits in the Accumulator

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

7.1.2 Enhanced CPU core SFRs

- Extended 'MUL' and 'DIV' instructions: 16bit*8bit, 16bit/8bit
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH79F085/SH79F165 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8 bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16 bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8 bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16 bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is the same with DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

7.1.3 Register

Table 7.2 Data Pointer Select Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	-	BKS0	-	-	DIV	MUL	-	DPS
R/W	-	R/W	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	-	-	0	0	-	0

Bit Number	Bit Mnemonic	Description
6	**BKS0**	**SFR Bank Selection Bit** 0: SFR Bank0 selected 1: SFR Bank1 selected
3	**DIV**	**16 bit/8 bit Divide Selection Bit** 0: 8 bit Divide 1: 16 bit Divide
2	**MUL**	**16 bit/8 bit Multiply Selection Bit** 0: 8 bit Multiply 1: 16 bit Multiply
0	**DPS**	**Data Pointer Selection Bit** 0: Data pointer 1: Data pointer1

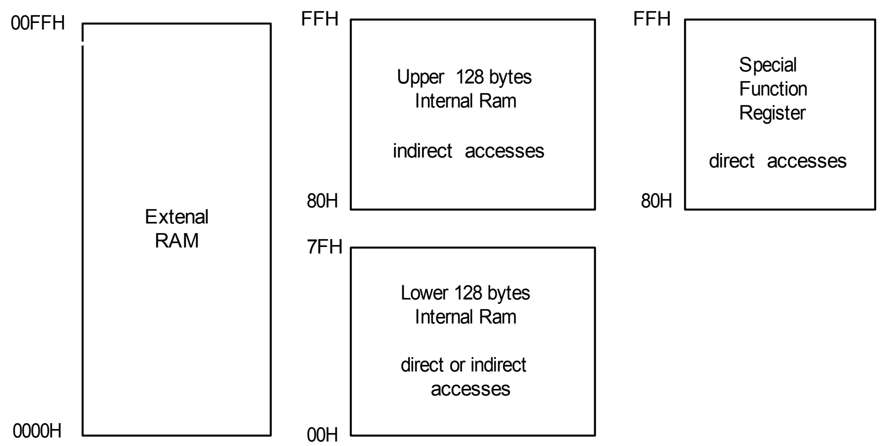
7.2 RAM

7.2.1 Feature

SH79F085/SH79F165 provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:

- The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.
- The external RAM are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.



The Internal and External RAM Configuration

The SH79F085/SH79F165 provides traditional method for accessing of external RAM. Use *MOVXA, @Ri* or *MOVX @Ri, A;* to access external low 256 bytes RAM; *MOVX A, @DPTR* or *MOVX @DPTR, A* also to access external 256 bytes RAM.

In SH79F085/SH79F165 the user can also use XPAGE register to access external RAM only with *MOVX A, @Ri* or *MOVX @Ri, A* instructions. The user can use XPAGE to represent the high byte address of RAM above 256 Bytes.

In Flash SSP mode, the XPAGE can also be used as sector selector (Refer to SSP Function).

7.2.2 Register

Table 7.3 Data Memory Page Register

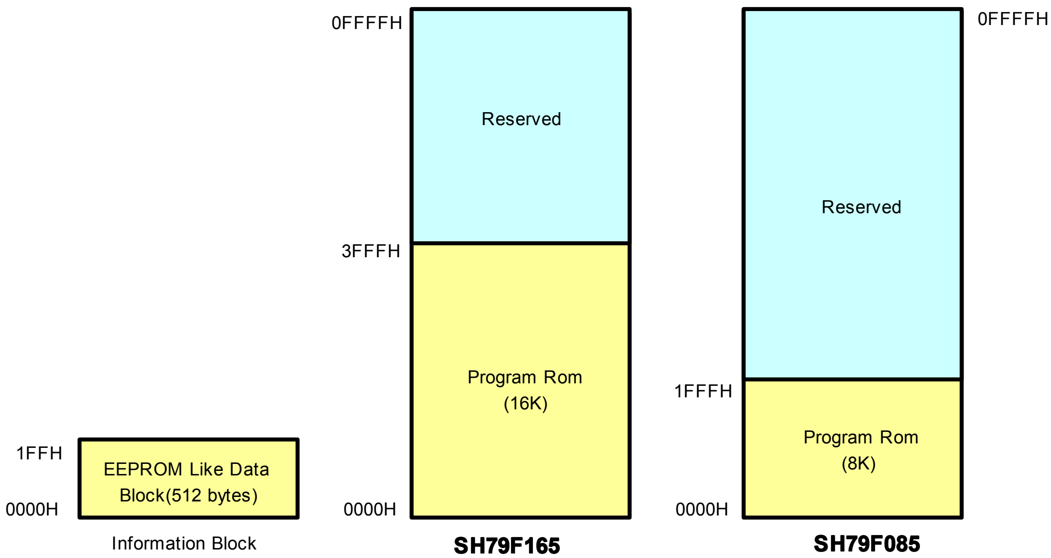
F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**XPAGE[7:0]**	RAM Page Selector

7.3 Flash Program Memory

7.3.1 Feature

- The program memory consists 8/16 X 1KB sectors, total 8/16KB
- Programming and erase can be done over the full operation voltage range
- Write, read and erase operation are all supported by In-Circuit Programming (ICP)
- Fast mass/sector erase and programming
- Minimum program/erase cycles: 100,000
- Minimum years data retention: 10
- Low power consumption



The SH79F085/SH79F165 embeds 8/16K flash program memory for program code. The flash program memory provides electrical erasure and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode.

The SH79F085/SH79F165 embeds 512 byte EEPROM-like for data. One sector consists of 256 bytes, total 2 sectors.

The ICP Mode Supports the following Operations:

(1) Code-Protect Control Mode Programming

SH79F085/SH79F165 implements code-protect function to offer high safeguard for customer code. Two modes are available for each sector.

Code-protect Control Mode0: Used to enable/disable the write/read operation (except mass erase) from any programmer.

Code-protect Control Mode1: Used to enable/disable the read operation through MOVC instruction from other sectors; or the sector erase/write operation through **SSP** Function.

To enable the wanted protect mode, the user must use the **Flash Programmer** to set the corresponding protect bit.

(2) Mass Erase

The mass erase operation will erase all the contents of program code, code option, code protect bit and customer code ID, regardless the status of code-protect control mode. (The Flash Programmer supplies customer code ID setting function for customer to distinguish their product.)

Mass erase is only available in Flash Programmer.

(3) Sector Erase

The sector erase operation will erase the contents of program code of selected sector. This operation can be done by Flash Programmer or the user's program.

If done by the Flash Programmer, the code-protect control mode 0 of the selected sector must be disabled.

(4) EEPROM-Like Erase

The EEPROM-Like erase operation will erase the contents of program code of EEPROM-Like. This operation can be done by Flash Programmer or the user's program.

(5) Write/Read Code

The Write/Read Code operation will write the customer code into the Flash Programming Memory or read the customer code from the Flash Programming Memory. This operation can be done by Flash Programmer or the user's program.

If done by the user's program, the code-protect control mode 1 of the selected sector must be disabled. But the program can read/write its own sector regardless of its security bit.

If done by the Flash Programmer, the code-protect control mode 0 of the selected sector must be disabled.

(6) Write/Read EEPROM-Like

The Write/Read EEPROM-Like operation will write the customer data into the EEPROM-Like or read the customer data from the EEPROM-Like. This operation can be done by Flash Programmer or the user's program.

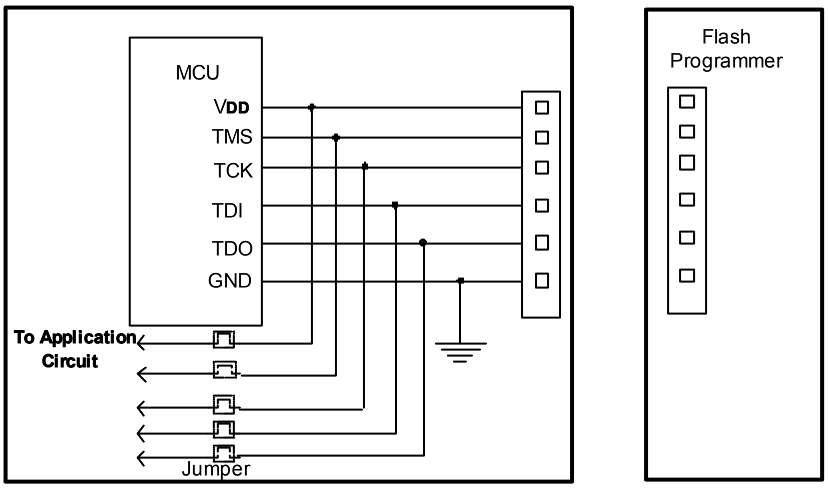
Operation	SSP	ICP
Code Protection	No	Yes
Sector Erase	Yes (without security bit)	Yes (without security bit)
Mass Erase	No	Yes
EEPROM-like Erase	Yes	Yes
Write/Read	Yes (without security bit or its own sector)	Yes (without security bit)
EEPROM-like Write/Read	Yes	Yes

7.3.2 Flash Operation in ICP Mode

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 wires (V_{DD}, GND, TCK, TDI, TMS, TDO).

At first the four JTAG pins (TDO, TDI, TCK, TMS) are used to enter the programming mode. Only after the three pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the FLASH Programmer's user guide.

In ICP mode, all the flash operations are completed by the programmer through 6-wire interface. Since the program timing is very sensitive, five jumpers are needed (V_{DD}, TDO, TDI, TCK, TMS) to separate the program pins from the application circuit as the following diagram.



The recommended steps are as following:

(1) The jumpers must be open to separate the programming pins from the application circuit before programming.
(2) Connect the programming interface with programmer and begin programming.
(3) Disconnect programmer and short these jumpers after programming is complete.

7.3.3 Flash Download in ISP Mode

The SH79F085/SH79F165 provides ISP (In System Programming) function and contains Boot Rom. The Startup program is downloaded to Boot Rom in factory. The user's program can refresh the program memory by UART port through PC software. When using this function, the TXD&RXD of UART port connect to corresponding pin of programmer. If ISP function is enabled by the code option and selection: Enter ISP mode only when P1.5 and P1.6 are connected to GND, simultaneously. The program can refresh correctly, therefore P1.5 and P1.6 must be connected with GND simultaneously.

Refer to pc software's guide for details.

7.4 SSP Function

The SH79F085/SH79F165 provides SSP (Self Sector Programming) function, each sector can be sector erased (except the last sector, sector 15) or programmed by the user's code if the selected sector is not be protected. But once sector has been programmed, it cannot be reprogrammed before sector erase.

The SH79F085/SH79F165 builds in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON2-5), the SSP will be terminated.

7.4.1 SSP Register

Table 7.4 Offset Register for Programming

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Flash memory, one sector is 1024 bytes

Bit Number	Bit Mnemonic	Description
5-2	**XPAGE[5:2]**	Sector of the flash memory to be programmed, 0000 means sector 0, and so on
1-0	**XPAGE[1:0]**	High Address of Offset of the flash memory sector to be programmed

EEPROM-like memory, one sector is 256 bytes, total 2 sectors

Bit Number	Bit Mnemonic	Description
7-1	**XPAGE[7:1]**	**Reserved**
0	**XPAGE.0**	**Sector of the flash memory to be programmed** 0: sector0 1: sector1

Table 7.5 Offset of Flash Memory for Programming

FBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_OFFSET[7:0]**	Low Address of Offset of the flash memory sector to be programmed

Table 7.6 Data Register for Programming

FCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_DATA[7:0]**	Data to be programmed

Table 7.7 SSP Type select Register

F2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_CON1[7:0]**	**SSP Type select** 0xE6: Sector Erase 0x6E: Sector Programming

Table 7.8 SSP Flow Control Register1

F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON2[3:0]**	Must be 05H, else Flash Programming will terminate

Table 7.9 SSP Flow Control Register2

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON3[3:0]**	Must be 0AH else Flash Programming will terminate

Table 7.10 SSP Flow Control Register3

F5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

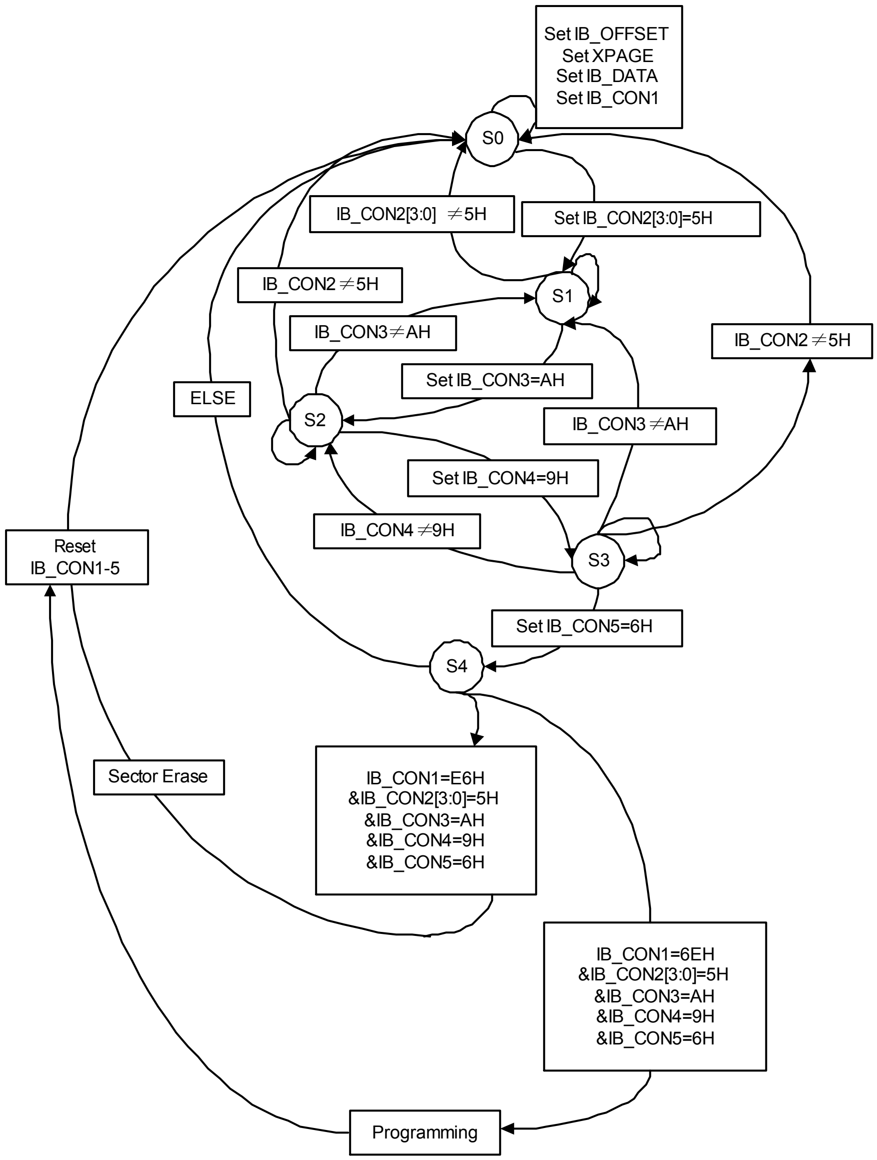
Bit Number	Bit Mnemonic	Description
3-0	**IB_CON4[3:0]**	Must be 09H, else Flash Programming will terminate

Table 7.11 SSP Flow Control Register4

F6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON5[3:0]**	Must be 06H, else Flash Programming will terminate

7.4.2 Flash Control Flow



7.4.3 SSP Programming Notice

To successfully complete SSP programming, the user's software must following the steps below:

(1) For Code/Data Programming:

1. Disable interrupt;
2. Fill in the XPAGE, IB_OFFSET for the corresponding address;
3. Fill in IB_DATA if programming is wanted;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Code/Data programming, CPU will be in IDLE mode;
7. Go to Step 2 if more data are to be programmed;
8. Clear XPAGE; enable interrupt if necessary.

(2) For Sector Erase:

1. Disable interrupt;
2. Fill in the XPAGE for the corresponding sector;
3. Fill in IB_CON1-5 sequentially;
4. Add 4 NOPs for more stable operation;
5. Sector Erase, CPU will be in IDLE mode;
6. Go to step 2 if more sectors are to be erased;
7. Clear XPAGE; enable interrupt if necessary.

(3) For Code Reading:

Just Use "MOVC A, @A+DPTR" or "MOVC A, @A+PC".

(4) For EEPROM-Like:

Steps is same as code programming, the diffenrences are:

1. Set FAC bit in FLASHCON register before programming or erase EEPROM-Like.
2. One sector of EEPROM-Like is 256 bytes. Not 1024 bytes.

Table 7.12 Flash Access Control Register

A7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FLASHCON	-	-	-	-	-	-	-	FAC
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Mnemonic	Description
0	**FAC**	**FAC: Flash access control** 0: MOVC or SSP access main memory 1: MOVC or SSP access EEPROM-like

7.5 System Clock and Oscillator

7.5.1 Feature

- Five oscillator types: 32.768kHz crystal, crystal oscillator, ceramic oscillator, Internal 128K RC and Internal16.6M RC
- Built-in 128kHz RC
- Built-in 16.6MHz RC
- Built-in system clock prescaler

7.5.2 Clock Definition

The SH79F085/SH79F165 have several internal clocks defined as below:

OSCCLK: the oscillator clock from one of the five oscillator types (32.768kHz crystal, crystal oscillator, ceramic oscillator, Internal 128K RC or Internal 16.6M RC). f_{OSC} is defined as the OSCCLK frequency. t_{OSC} is defined as the OSCCLK period.

WDTCLK: the internal 2kHz WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK period.

OSCSCLK: the input of system clock prescaler. It can be OSCCLK. f_{OSCS} is defined as the OSCSCLK frequency. t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output of system clock prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency. t_{SYS} is defined as the SYSCLK period.

7.5.3 Description

The SH79F085/SH79F165 has 5 oscillator types: 32.768kHz crystal, crystal oscillator (400kHz-16.6MHz), ceramic oscillator (400KHz-16.6MHz), Internal 128K RC and internal 16.6MHz RC, which is selected by code option OP_OSC (Refer to **code option** section for details). The oscillator generates the basic clock pulse that provides the system clock to supply CPU and on-chip peripherals.

7.5.4 Register

Table 7.13 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	32K_SPDUP	CLKS1	CLKS0	-	HFON	FS	-	-
R/W	R/W	R/W	R/W	-	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	1	1	1	-	0	0	-	-

Bit Number	Bit Mnemonic	Description
7	32K_SPDUP	**32.768kHz oscillator speed up mode control bit** 0: 32.768kHz oscillator normal mode, cleared by software 1: 32.768kHz oscillator speed up mode, set by hardware or software This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. And this bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when Power-down mode wakes up. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption. Only when code option OP_OSC is 1010, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)
6-5	CLKS[1: 0]	**SYSCLK Prescaler bits** 00: $f_{SYS} = f_{OSCS}$ 01: $f_{SYS} = f_{OSCS}/2$ 10: $f_{SYS} = f_{OSCS}/4$ 11: $f_{SYS} = f_{OSCS}/12$ If 32.768kHz oscillator is selected as OSCSCLK, these control bits is invalid
3	HFON	**High frequency control bit** 0: Cleared to turn off internal 16.6MHz RC or Crystal/Ceramic oscillator (400kHz - 16.6MHz) 1: Set to turn on internal 16.6MHz RC or Crystal/Ceramic oscillator (400 - 16.6MHz)
2	FS	**Frequency select bit** 0: 32.768kHz oscillator or 128kHz RC oscillator is selected as OSCSCLK 1: Internal16.6MHz RC or crystal/ceramic oscillator is selected as OSCSCLK

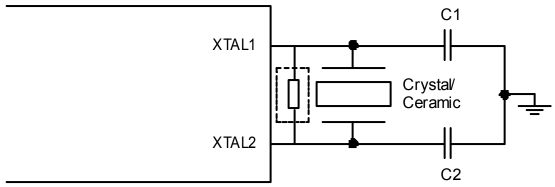
Note:

To select High frequency as OSCSCLK (internal 16.6MHz RC or Crystal/Ceramic oscillator), the steps below must be done in sequence:

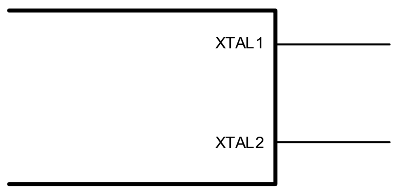
1. Set HFON = 1, turn on high frequency oscillator;
2. Wait at least 2ms;
3. Set FS = 1, select high frequency oscillator as OSCSCLK

7.5.5 Oscillator Type

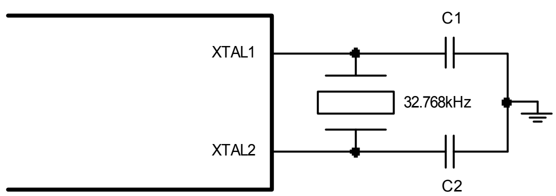
(1) Internal 128KHz RC oscillator and Crystal/Ceramic oscillator (400kHz - 16.6MHz)*



(2) Internal 128KHz RC oscillator and internal 16.6MHz RC oscillator



(3) 32.768kHz oscillator and internal 16.6MHz RC oscillator



*: *If the environment humidity is bigger, use the high frequency oscillator, advice plus 510k feedback resistance.*

7.5.6 Capacitor selection for Oscillator

Ceramic Resonator			Recommend Type	Manufacturer
Frequency	C1	C2		
455kHz	47 - 100pF	47 - 100pF	ZTB 455kHz	Vectron International
			ZT 455E	Shenzhen DGJB Electronic Co.,Ltd.
3.58MHz	-	-	ZTT 3.580M	Vectron International
			ZT 3.58M*	Shenzhen DGJB Electronic Co.,Ltd.
4MHz	-	-	ZTT 4.000M	Vectron International
			ZT 4M*	Shenzhen DGJB Electronic Co.,Ltd.

*- The specified ceramic resonator has internal built-in load capacity.

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS
			φ 3x8 - 32.768KHz	Vectron International
4MHz	8 - 15pF	8 - 15pF	HC-49U/S 4.000MHz	Vectron International
			49S-4.000M-F16E	Shenzhen DGJB Electronic Co.,Ltd.
8MHz	8 - 15pF	8 - 15pF	HC-49U/S 8.000MHz	Vectron International
			49S-8.000M-F16E	Shenzhen DGJB Electronic Co.,Ltd.

Note:

(1) ***Capacitor values are used for design guidance only!***

(2) These capacitors were tested with the crystals listed above for basic start-up and operation. ***They are not optimized.***

(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

7.6 System Clock Monitor (SCM)

In order to enhance the system reliability, SH79F085/SH79F165 contains a system clock monitor (SCM) module. If the system clock fails (for example the oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal 32k WDTCLK and set system clock monitor bit (SCMIF) to 1. And the SCM interrupt will be generated when EA and ESCM is enabled. If the OSCCLK comes back, SCM will switch the OSCCLK back to the oscillator and clears the SCMIF automatically.

Note:

The SCMIF is read only register; it can be clear to 0 or set to 1 by hardware only.
If SCMIF is cleared, the SCM switches the system clock to the state before system clock fail automatically.
If Internal RC is selected as OSCCLK by code option (Refer to code option section for detail), the SCM can not work.

Table 7.14 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	-	-	-	SCMIF	-	-	-	-
R/W	-	-	-	R	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
4	**SCMIF**	**System Clock Monitor bit** 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails

7.7 I/O Port

7.7.1 Feature

- 5/19 bi-directional I/O ports
- Share with alternative functions

The SH79F085/SH79F165 has 15/19 bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x = 0-2, y = 0-7).

For SH79F085/SH79F165, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions be conflict when all the functions are enabled. (Refer to **Port Share** Section for details).

7.7.2 Register

Table 7.15 Port Control Register

E1H - E3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CR (E1H)	-	P0CR.6	P0CR.5	P0CR.4	-	-	-	-
P1CR (E2H)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR (E3H)	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxCRy x = 0-2, y = 0-7**	**Port input/output direction control Register** 0: input mode 1: output mode *Note:BIT 0-3 in P0CR must be set,when initialization.*

Table 7.16 Port Pull up Resistor Control Register

E9H - EBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PCR (E9H)	-	P0PCR.6	P0PCR.5	P0PCR.4	-	-	-	-
P1PCR (EAH)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR (EBH)	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

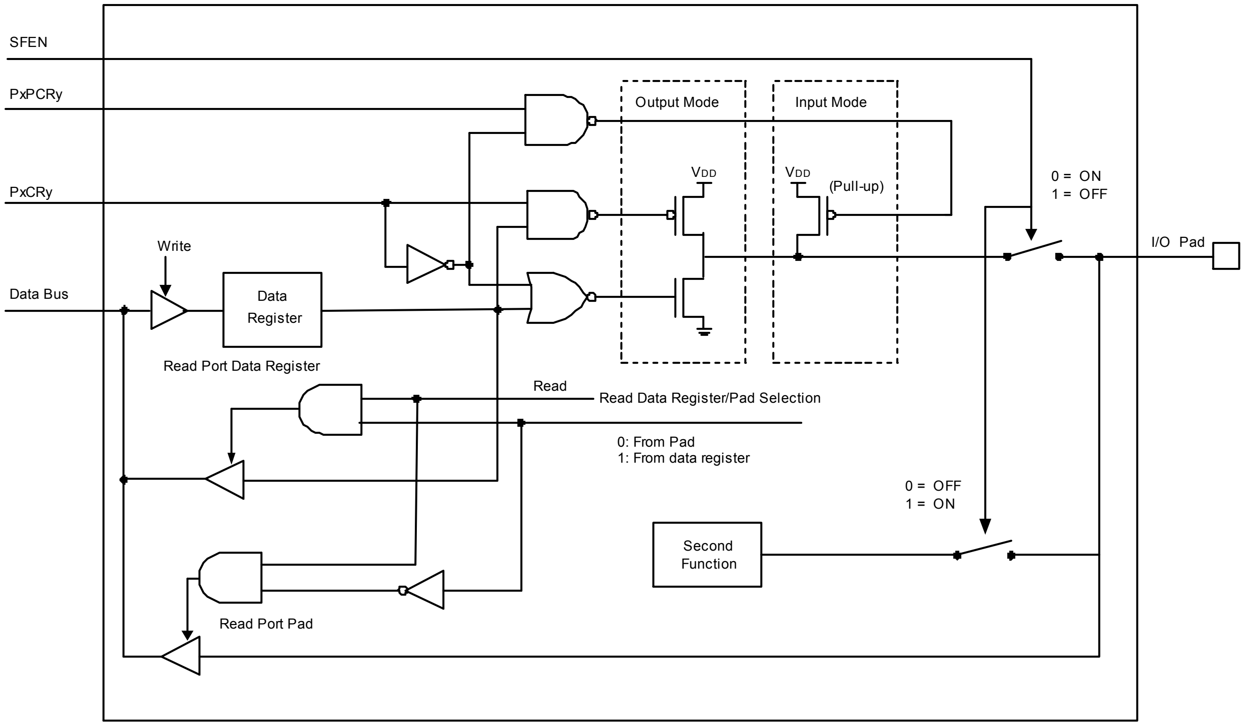
Bit Number	Bit Mnemonic	Description
7-0	**PxPCRy x = 0-2, y = 0-7**	**Input Port internal pull-high resistor enable/disable control** 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled

Table 7.17 Port Data Register

80H, 90H, A0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0 (80H)	-	P0.6	P0.5	P0.4	-	-	-	-
P1 (90H)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2 (A0H)	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**Px.y x = 0-2, y = 0-7**	**Port Data Register**

7.7.3 Port Diagram



Note:

(1) The input source of reading input port operation is from the input pin directly.

(2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly. The read Instruction distinguishes which path is selected: The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.

(3) The destination of writing port operation is the data register regardless the port shared as the second function or not.

(4) In power saving mode: SOP24 packaging need software set the address of bit 0 to bit 3 in P0CR as 1, or set as 0 and set bit 0 to bit3 in P0PCR;SOP20 packaging need software set bit 0 to bit 3 in P0CR, bit 7 in P2CR and bit 0 to bit 2 in P2CR as 1,or set as 0 and set corresponding bit in PxPCR(x=0,1,2) as 1, so as to avoid leakage current.

7.7.4 Port Share

The 15/19 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Most Inner Lest** rule:

The out most pin function in **Pin Configuration** has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin , even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 0-2), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register while the port pin keeps unchanged until all the share functions are disabled.

PORT0:

- $\overline{RST}$ (P0.4): Reset pin
- XTAL1 (P0.5): External oscillator input
- XTAL2 (P0.6): External oscillator output
- T0 (P0.5): Timer0 external input/comparator output
- T1 (P0.6): Timer1 external input/comparator output

Table 7.18 PORT0 Share Table

Pin No.			Priority	Function	Enable bit
SH79F085 (TSSOP20)	SH79F085 (SOP24)	SH79F165 (SOP24)			
4	4	4	1	$\overline{RST}$	Selected by code option
			2	P0.4	Selected by code option
5	5	5	1	XTAL1	Selected by code option, OP_OSC[3:0] = 0110/1010
			2	T0	Set TR0 bit in TCON register and set C/T0 bit in TMOD register (Auto pull-up)
			3	P0.5	Above condition is not met
6	6	6	1	XTAL2	Selected by code option, OP_OSC[3:0] = 0110/1010
			2	T1	Set TR1 bit in TCON register and set C/T1 bit in TMOD register (Auto pull-up)
			3	P0.6	Above condition is not met

PORT1:

- BUZ (P1.0): Buzzer output
- RXD (P1.1): EUART data input
- TXD (P1.2): EUART data output
- T2 (P1.3): Timer2 external input/programmable clock output
- T2EX (P1.4): Timer2 reload/capture/direction control
- INT0 (P1.4): External interrupt0 input
- AIN1+ (P1.5): Positive differential ADC input1
- AIN1- (P1.6): Negative differential ADC input1

Table 7.19 PORT1 Share Table

Pin No.			Priority	Function	Enable bit
SH79F085 (TSSOP20)	SH79F085 (SOP24)	SH79F165 (SOP24)			
1	1	1	1	BUZ	Set BZEN bit in BUZCON register
			2	P1.0	Above condition is not met
2	2	2	1	RXD	Set REN bit in SCON register (Auto pull up)
			2	P1.1	Above condition is not met
3	3	3	1	TXD	When write to SBUF register
			2	P1.2	Above condition is not met
7	7	7	1	T2	Set TR2 bit and C/$\overline{T2}$ bit in T2CON register or clear C/$\overline{T2}$ bit and set T2OE bit in T2MOD register
			2	P1.3	Above condition is not met
8	8	8	1	T2EX	In mode0,2,3,set EXEN2 bit in T2CON register, or in mode 1 set DCEN bit in T2CON register or in mode1, clear DCEN bit and set EXEN2 bit
			2	INT0	Set EX0 bit in IEN0 Register and Port1.4 is in input mode
			3	P1.4	Above condition is not met
9	9	9	1	AIN1+	SCH[2:0] = 001 in ADCON register and set CH1 bit in ADCH register
			2	INT1	Set EX1 bit in IEN0 Register and Port1.5 is in input mode
			3	P1.5	Above condition is not met
10	10	10	1	AIN1-	SCH[2:0] = 001 in ADCON register and set CH1 bit in ADCH register
			2	INT2	Set EX2 bit in IEN1 Register and Port1.6 is in input mode
			3	P1.6	Above condition is not met

PORT2:
- AIN2+ (P2.1): Positive differential ADC input2
- AIN2- (P2.2): Negative differential ADC input2
- VIN+ (P2.3): Positive differential PGA input/output
- VIN- (P2.4): Negative differential PGA input/output
- AIN0+ (P2.5): Positive differential ADC input0
- AIN0- (P2.6): Negative differential ADC input0
- VREF (P2.7): ADC reference voltage input/output

Table 7.20 PORT2 Share Table

Pin No.			Priority	Function	Enable bit
SH79F085 (TSSOP20)	SH79F085 (SOP24)	SH79F165 (SOP24)			
-	13	13	1	AIN2+	SCH[2:0] = 010 in ADCON register and set CH2 bit in ADCH register
			2	P2.1	Above condition is not met
-	14	14	1	AIN2-	SCH[2:0] = 010 in ADCON register and set CH2 bit in ADCH register
			2	P2.2	Above condition is not met
11	15	15	1	VIN+	Set ADON bit in ADCON register
			2	P2.3	Above condition is not met
12	16	16	1	VIN-	Set ADON bit in ADCON register
			2	P2.4	Above condition is not met
13	17	17	1	AIN0+	SCH[2:0] = 000 in ADCON register and set CH0 bit in ADCH register
			2	P2.5	Above condition is not met
14	18	18	1	AIN0-	SCH[2:0] = 000 in ADCON register and set CH0 bit in ADCH register
			2	P2.6	Above condition is not met
15	19	19	1	VERF	Set P27OS bit in ADCH register
			2	P2.7	Above condition is not met

7.8 Timer

7.8.1 Feature

- SH79F085/SH79F165 has four timers (Timer0, 1, 2, 3)
- Timer 0 compatible with the standard 8051
- Timer 1 compatible with the standard 8051
- Timer 2 compatible with the standard 8052 and has up or down counting and programmable clock output function
- Timer 3 a 16-bit auto-reload timer and can operate even in Power-Down mode
- Timer0/1 compare function
- Timer0/1 clock source selectable
- Timer0/1 clock source prescaler function

7.8.2 Timer0/1

Each timer is implemented as a 16-bit register accessed as two cascaded Timer x/Counter x Data Registers: THx & TLx (x = 0, 1). They are controlled by the register TCON and TMOD. The Timer0 & Timer1 interrupts can be enabled by setting the ET0 & ET1 bit in the IEN0 register (Refer to **Interrupt** Section for details).

Timer0 & Timer1 Mode

Both timers operate in one of four primary modes selected by the Mode Select bits Mx1-Mx0 (x = 0, 1) in the Counter/Timer Mode register (TMOD).

Mode0: 13-bit Counter/Timer

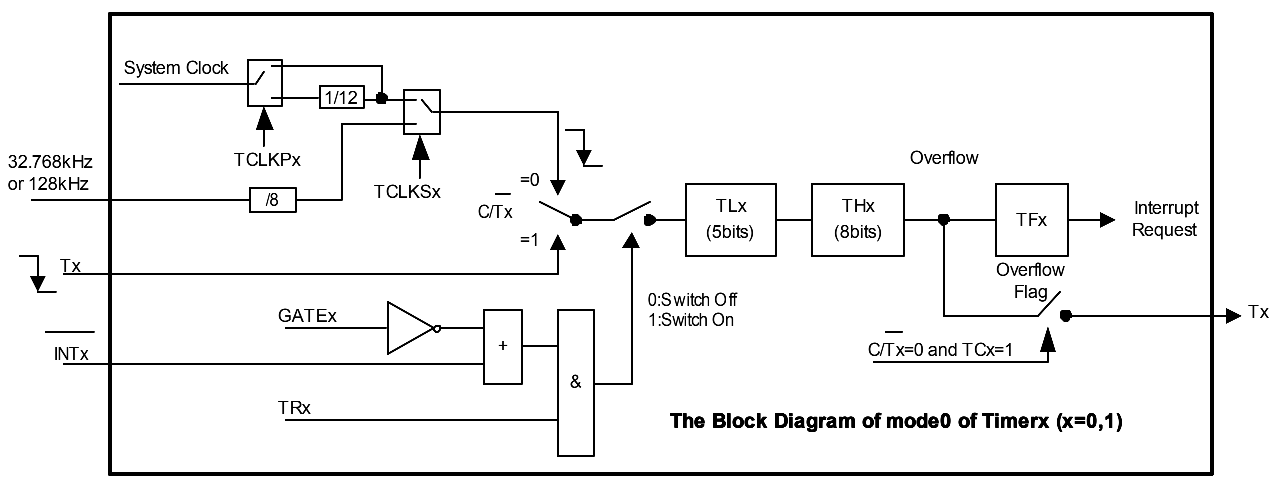
Timer x operate as 13-bit counter/timers in Mode 0. The THx register holds the high eight bits of the 13-bit counter/timer, TLx holds the five low bits TLx.4- TLx.0. The three upper bits (TLx.7 - TLx.5) of TLx are indeterminate and should be ignored when reading. As the 13-bit timer register increments and overflows, the timer overflow flag TFx is set and an interrupt will occur if Timer interrupts is enabled. The $C/\overline{Tx}$ bit selects the counter/timer's clock source.

If $C/\overline{Tx}$ = 1, high-to-low transitions at the Timer input pin (Tx) will increase the timer/Counter Data register. Else if $C/\overline{Tx}$ = 0, selects the system clock to increase the timer/Counter Data register. Setting the TRx bit enables the timer when either GATEx = 0, or GATEx = 1 and the input signal $\overline{INTx}$ is active. Setting GATEx to '1' allows the timer to be controlled by the external input signal $\overline{INTx}$, facilitating positive pulse width in $\overline{INTx}$ measurements. Setting TRx does not force the timer to reset. This means that if TRx is set, the timer register will count from the old value that was last stopped by clearing TRx. So the timer registers should be loaded with the desired initial value before the timer is enabled.

When as Timer, system clock or 32.768KHz/8 or128KHz/8. can be selected as Timer x (x = 0, 1) clock source by configuring TCLKSx (x = 0, 1) in TCON1 Register. TCLKSx (x = 0, 1) are valid only when 32.768kHz Crystal oscillator is selected by code option. When 32.768kHz is selected as system clock and TCLKSx (x = 0, 1) is set "1", Timer x (x = 0, 1) can't count.

System clock or 1/12 of system clock can be selected as Timer x (x = 0, 1) clock source by configuring TCLKPx (x = 0, 1) in TCON1 Register.

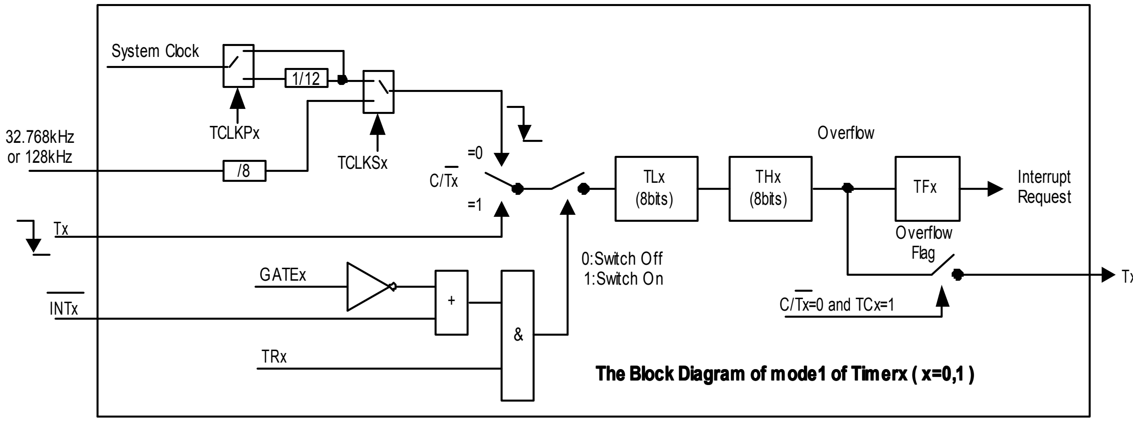
When as Timer, the T0/T1 pin can automatically toggle upon Timer0/1 overflow by configuring TC0/1 in TCON1 Register. The T0/T1 pin is automatically set as output by hardware when TC0/1 is set.



The Block Diagram of mode0 of Timerx (x=0,1)

Mode1: 16-bit Counter/Timer

Mode1 operation is the same as Mode0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode1 in the same manner as for Mode0.



The Block Diagram of mode1 of Timerx (x=0,1)

Mode2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TLx holds the count and THx holds the reload value. When the counter in TLx overflows from 0xFF to THx, the timer overflow flag TFx is set and the counter in TLx is reloaded from THx. If Timer 0 interrupts are enabled, an interrupt will occur when the TFx flag is set. The reload value in TH0 is not changed. TLx 0 must be initialized to the desired value before enabling the timer for the first count to be correct.

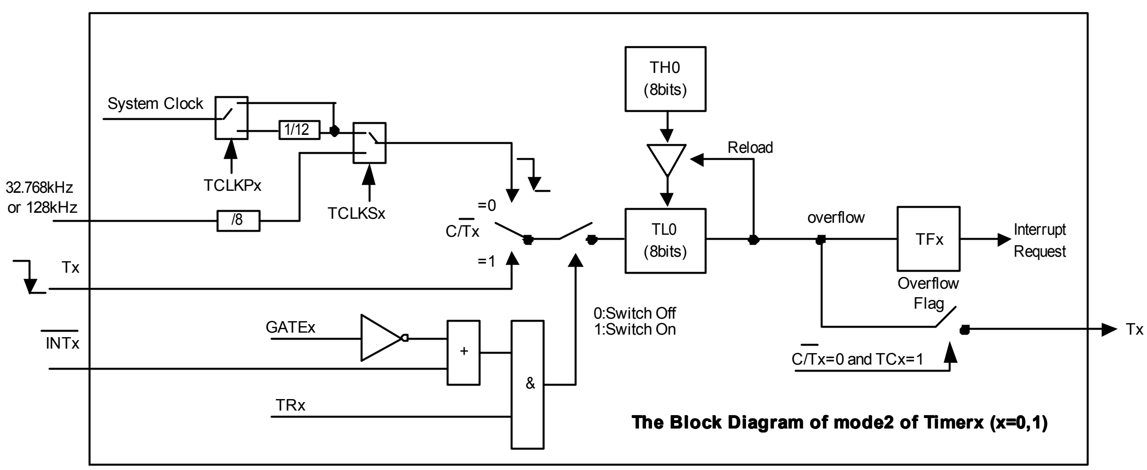
Except the Auto-Reload function, both counter/timers are enabled and configured in Mode 2 is the same as in Mode0 & Mode1.

When as Timer, system clock or 32.768KHz/8 or 128kHz/8. can be selected as Timer x (x = 0, 1) clock source by configuring TCLKSx (x = 0, 1) in TCON1 Register. TCLKSx (x = 0, 1) are valid only when 32.768kHz Crystal oscillator is selected by code option.

When 32.768kHz is selected as system clock and TCLKSx (x = 0, 1) is set "1", Timer x (x = 0, 1) can't count.

System clock or 1/12 of system clock can be selected as Timer x (x = 0, 1) clock source by configuring TCLKPx (x = 0, 1) in TCON1 Register.

When as Timer, the T0/T1 pin can automatically toggle upon Timer0/1 overflow by configuring TC0/1 in TCON1 Register. The T0/T1 pin is automatically set as output by hardware when TC0/1 is set.



The Block Diagram of mode2 of Timerx (x=0,1)

Mode3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/$\overline{T0}$, GATE0 and TF0. TL0 can use either the system clock or 32.768KHz/8 or 128kHz/8. or an external input signal as its time base.

The TH0 is restricted to a timer function sourced by the system clock. TH0 is enabled using the Timer 1 control bit TR1. THx sets the Timer1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

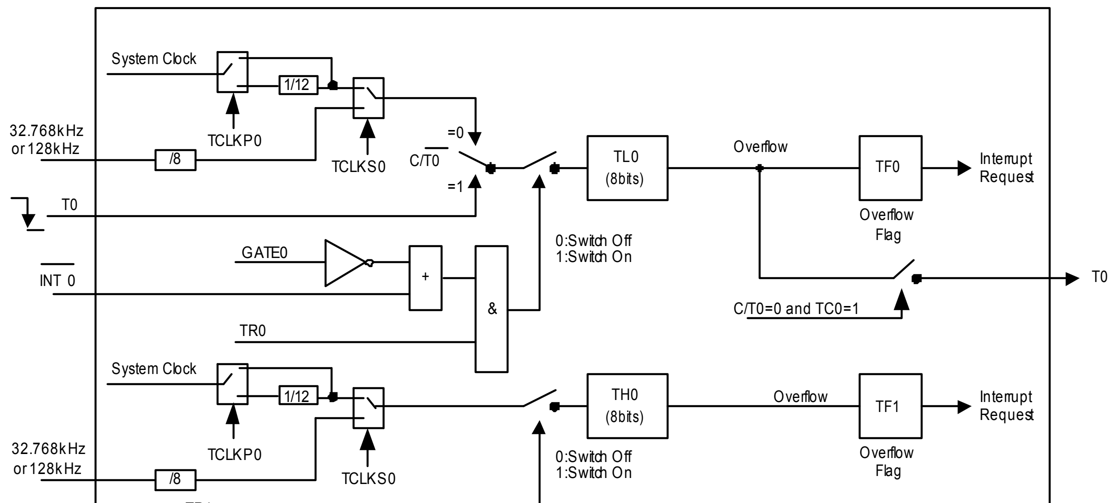
When timer 0 is operating in Mode 3, timer 1 can be operated in mode0, 1 or 2, but it cannot set the TF1 flag and generate an interrupt. The Timer1 overflow can generate baud-rates for the EUART. The TH1 and TL1 register is restricted to a timer function sourced by the system clock, and gate1 is invalid. And the pull high resistor of T1 input pin is also disabled. Timer1 run control is handled through its mode settings, because TR1 is used by Time 0. When the timer 1 is in mode0, 1, or 2, Timer1 is enable. When the Timer1 is in mode3, Timer1 is disabled.

When as Timer, system clock or 32.768KHz/8 or 128kHz/8. can be selected as Timer0 clock source by configuring TCLKS0 in TCON1 Register. TCLKS0 are valid only when 32.768kHz Crystal oscillator is selected by code option.

When 32.768kHz is selected as system clock and TCLKS0 is set “1”, Timer0 can’t count.

System clock or 1/12 of system clock can be selected as Timer0 clock source by configuring TCLKP0 in TCON1 Register.

When as Timer, the T0 pin can automatically toggle upon Timer0 overflow by configuring TC0 in TCON1 Register. The T0 pin is automatically set as output by hardware when TC0 is set.



The Block Diagram of mode3 of Timer0

Note:

While Timer1 is used as baud rate generator, reading or writing TH1/TL1 will affect the accuracy of baud rate, thus might make cause communication error.

Register

Table 7.21 Timer/Counter x Control Register (x = 0, 1)

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 5	**TFx** **x = 0, 1**	**Timer x overflow flag** 0: Timer x no overflow, can be cleared by software 1: Timer x overflow, set by hardware; set by software will cause a timer interrupt
6, 4	**TRx** **x = 0, 1**	**Timer x start, stop control bits** 0: Stop timer x 1: Start timer x
3, 1	**IEx** **x = 0, 1**	**External interrupt x request flag**
2, 0	**ITx** **x = 0, 1**	**External interrupt x trigger mode select bits**

Table 7.22 Timer/Counter x Mode Register (x = 0, 1)

89H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMOD	GATE1	$C/\overline{T1}$	M11	M10	GATE0	$C/\overline{T0}$	M01	M00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 3	**GATEx** **x = 0, 1**	**Timer x Gate Control bits** 0: Timer x is enabled whenever TRx control bit is set 1: Timer x is enabled only while INTx pin is high and TRx control bit is set
6, 2	**$C/\overline{Tx}$** **x = 0, 1**	**Timer x Timer/Counter mode selected bits** 0: Timer Mode, T0 or T1 pin is used as I/O port 1: Counter Mode
5-4 **1-0**	**Mx [1:0]** **x = 0, 1**	**Timer x Timer mode selected bits** 00: Mode0, 13-bit up counter/timer, bit7-5 of TLx is ignored 01: Mode1, 16-bit up counter/timer 10: Mode2, 8-bit auto-reload up counter/timer 11: Mode3 (only for Timer0), two 8-bit up timer

Table 7.23 Timer/Counter x Data Register (x = 0, 1)

8AH-8DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL0 (8AH)	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
TH0 (8CH)	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
TL1 (8BH)	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
TH1 (8DH)	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TLx.y, THx.y x=0-1, y=0-7**	Timer x Low & High byte counter

Table 7.24 Timer/Counter x Control Register1 (x = 0, 1)

CEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON1	-	TCLK_S1	TCLK_S0	-	TCLKP1	TCLKP0	TC1	TC0
R/W	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
6, 5	**TCLK_Sx x = 0, 1**	**Timer x Clock Source Control bits** 0: Select system clock as Timer x Clock Source 1: Select 32.768kHz/8 or 128kHz/8 as Timer x Clock Source
3-2	**TCLKPx x = 0, 1**	**Timer x Clock Source Prescaler bits** 0: Select 1/12 of system clock as Timer x Clock Source 1: Select system clock as Timer x Clock Source
1-0	**TCx x = 0, 1**	**Compare function Enable bits** 0: Disable compare function of Timer x 1: Enable compare function of Timer x

7.8.3 Timer2

The Timer 2 is implemented as a 16-bit register accessed as two cascaded data registers: TH2 and TL2. It is controlled by the register T2CON and T2MOD. The Timer2 interrupt can be enabled by setting the ET2 bit in the IEN0 register. (Refer to Interrupt Section for details)

C/$\overline{\text{T2}}$ selects system clock (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows Timer 2/Counter 2 Data Register to increment by the selected input.

Timer2 Modes

Timer2 has 4 operating modes: Capture/Reload, Auto-reload mode with up or down counter, Baud Rate Generator and Programmable clock-output. These modes are selected by the combination of RCLK, TCLK and CP/RL2.

Timer2 Mode select

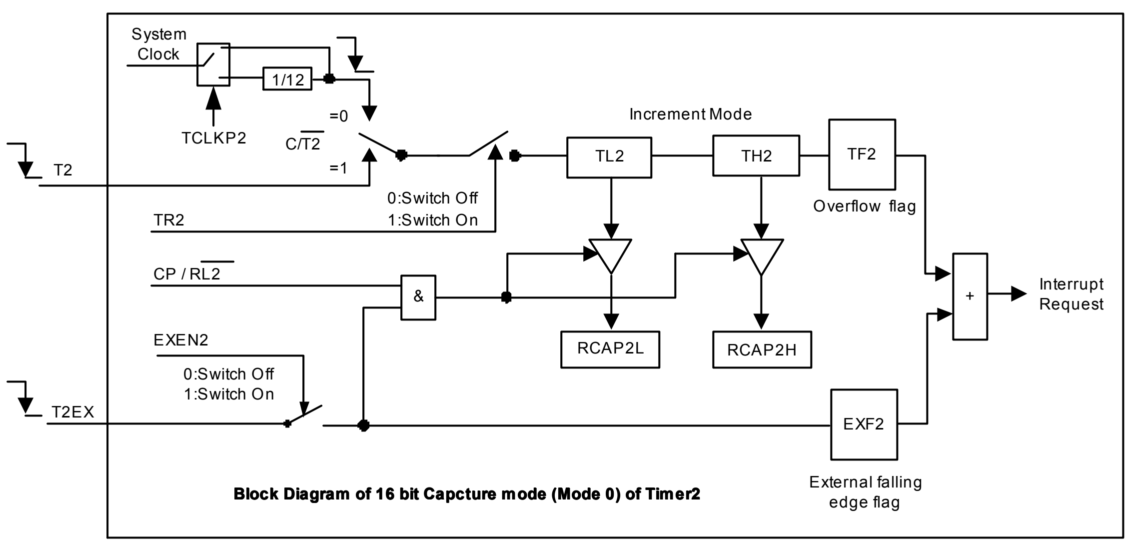
C/$\overline{\text{T2}}$	T2OE	DCEN	TR2	CP/RL2	RCLK	TCLK	Mode	Description
X	0	X	1	1	0	0	0	16 bit capture
X	0	0	1	0	0	0	1	16 bit auto-reload timer
X	0	1	1	0	0	0	1	16 bit auto-reload timer
X	0	X	1	X	1	X	2	Baud-Rate generator
X	0	X	1	X	X	1	2	Baud-Rate generator
0	1	X	1	X	0	0	3	Programmable clock-output only
0	1	X	1	X	1	X	3	Programmable clock-output, with Baud-rate generator
0	1	X	1	X	X	1	3	Programmable clock-output, with Baud-rate generator
1	1	X	1	X	X	X		Not recommending
X	X	X	0	X	X	X	X	Timer2 stop, the T2EX path still enable

Mode0: 16 bit Capture

In the capture mode, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which will set TF2 on overflow to generate an interrupt if ET2 is enabled.

If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L respectively, In addition, a 1-to-0 transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can also generate an interrupt if ET2 is enabled.



Block Diagram of 16 bit Capcture mode (Mode 0) of Timer2

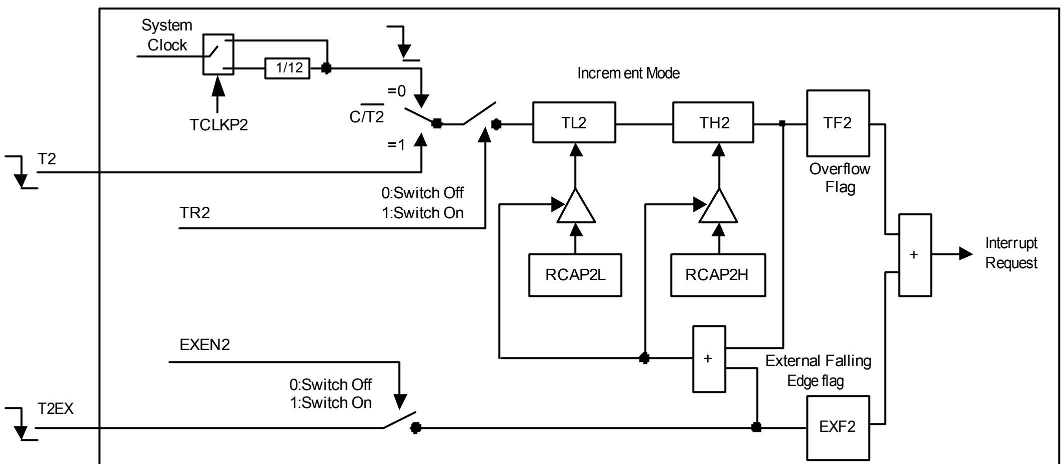
Mode1: 16 bit auto-reload Timer

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit in T2MOD. After reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

When DCEN = 0, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software.

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if ET2 is enabled.



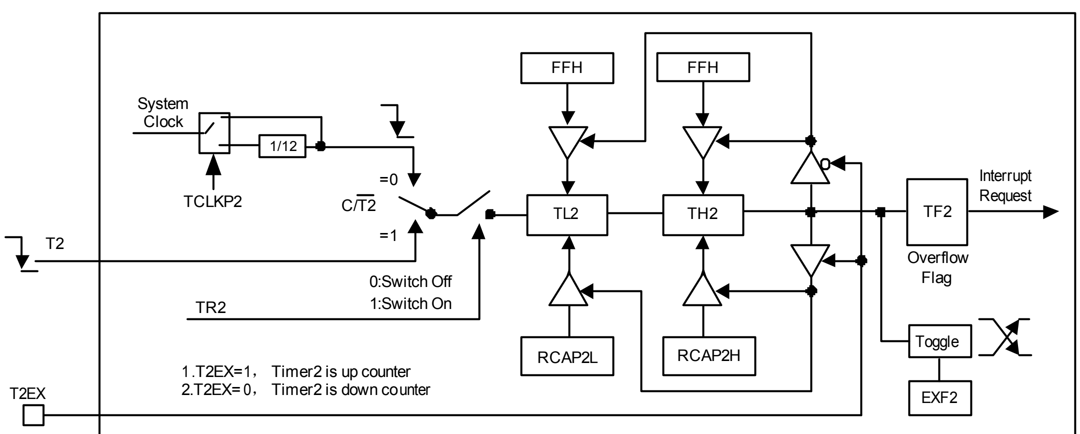
The Block Diagram of Auto Relode Mode (Mode 1)of Timer2 (DCEN=0)

Setting the DCEN bit enables Timer 2 to count up or down. When DCEN = 1, the T2EX pin controls the direction of the count, and EXEN2's control is invalid.

A logical "1" at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logical "0" at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.



The Block Diagram of Auto-Reload Mode (Mode 1) of Timer2 (DCEN=1)

Mode2: Baud-Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 4 is used for the other.

Setting RCLK and/or TCLK will put Timer 2 into its baud rate generator mode, which is similar to the auto-reload mode.

Over flow of Timer 2 will causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L that preset by software. But this will not generate an interrupt.

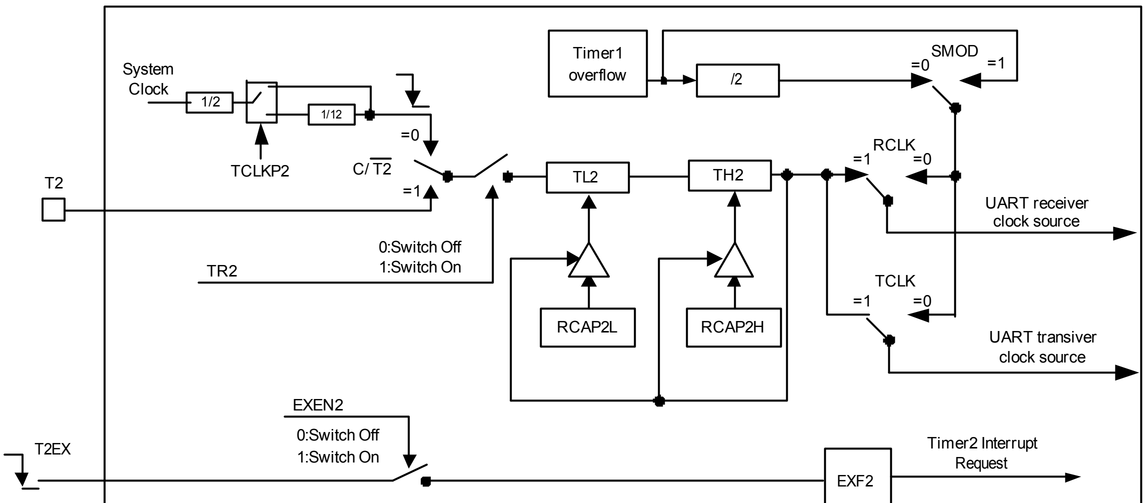
If EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload. Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

The baud rates in EUART Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$BaudRate = \frac{1}{2\times 12\times 16}\times\frac{f_{SYS}}{65536-[RCAP2H, RCAP2L]};\quad C/\overline{T2}=0,\ TCLKP2=0$$

$$BaudRate = \frac{1}{2\times 16}\times\frac{f_{SYS}}{65536-[RCAP2H, RCAP2L]};\quad C/\overline{T2}=0,\ TCLKP2=1$$

$$BaudRate = \frac{1}{16}\times\frac{f_{T2}}{65536-[RCAP2H, RCAP2L]};\quad C/\overline{T2}=1$$



The Block Diagram of Baud-Rate Generator (Mode 2) of Timer2

Mode3: Programmable Clock Output

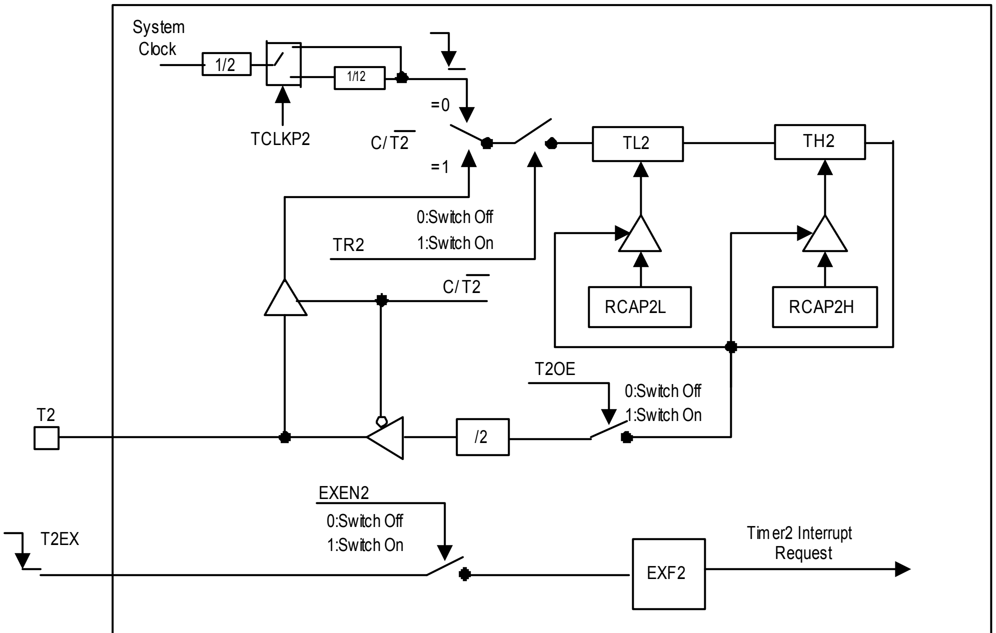
A 50% duty cycle clock can be programmed to come out on P0.5. To configure the Timer 2 as a clock generator, bit $C/\overline{T2}$ must be cleared and bit T2OE must be set. Bit TR2 starts and stops the timer.

In this mode T2 will output a 50% duty cycle clock,

$$Clock\ \ Out\ \ Frequency = \frac{1}{2\times2\times12}\times\frac{f_{SYS}}{65536-[RCAP2H,RCAP2L]}\qquad ;\ TCLKP2 = 0$$

$$Clock\ \ Out\ \ Frequency = \frac{1}{2\times2}\times\frac{f_{SYS}}{65536-[RCAP2H,RCAP2L]}\qquad ;\ TCLKP2 = 1$$

Timer2 overflow will not generate an interrupt, so it is possible to use Timer2 as a baud-rate generator and a clock output simultaneously with the same frequency.



The Block Diagram of Programmable Clock output(Mode 3) of Timer2

Note:

1. Both TF2 and EXF2 can cause timer2 interrupt request, and they have the same vector address.

2. TF2 and EXF2 are set as 1 by hardware while event occurs. But they can also be set by software at any time. Only the software and the hardware reset will be able to clear TF2 & EXF2 to 0.

3. When EA = 1 & ET2 = 1, setting TF2 or EXF2 as 1 will cause a timer2 interrupt.

4. While Timer2 is used as baud rate generator, writing TH2/TL2, writing RCAPH2/RCAPL2 will affect the accuracy of baud rate, thus might make cause communication error.

Register

Table 7.25 Timer2 Control Register

C8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF2**	**Timer2 overflow flag bit** 0: No overflow 1: Overflow (Set by hardware if RCLK = 0 & TCLK = 0)
6	**EXF2**	**External event input (falling edge) from T2EX pin detected flag bit** 0: No external event input (Must be cleared by software) 1: Detected external event input (Set by hardware if EXEN2 = 1)
5	**RCLK**	**EUART0 Receive Clock control bit** 0: Timer1 generates receiving baud-rate 1: Timer2 generates receiving baud-rate
4	**TCLK**	**EUART0 Transmit Clock control bit** 0: Timer1 generates transmitting baud-rate 1: Timer2 generates transmitting baud-rate
3	**EXEN2**	**External event input (falling edge) from T2EX pin used as Reload/Capture trigger enable/disable control bit** 0: Ignore events on T2EX pin 1: Cause a capture or reload when a negative edge on T2EX pin is detected, when Timer2 is not used to clock the EUART (T2EX always has a pull up resistor)
2	**TR2**	**Timer2 start/stop control bit** 0: Stop Timer2 1: Start Timer2
1	**$C/\overline{T2}$**	**Timer 2 Timer/Counter mode selected bit** 0: Timer Mode, T2 pin is used as I/O port 1: Counter Mode, the internal pull-up resister is turned on
0	**$CP/\overline{RL2}$**	**Capture/Reload mode selected bit** 0: 16 bits timer/counter with reload function 1: 16 bits timer/counter with capture function

Table 7.26 Timer2 Mode Control Register

C9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	TCLKP2	-	-	-	-	-	T2OE	DCEN
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7	**TCLKP2**	**Timer2 Clock Source Prescaler bit** 0: Select 1/12 of system clock as Timer2 Clock Source 1: Select system clock as Timer2 Clock Source
1	**T2OE**	**Timer2 Output Enable bit** 0: Set P0.5/T2 as clock input or I/O port 1: Set P0.5/T2 as clock output (Baud-Rate generator mode)
0	**DCEN**	**Down Counter Enable bit** 0: Disable Timer2 as up/down counter, Timer2 is an up counter 1: Enable Timer2 as up/down counter

Table 7.27 Timer2 Reload/Capture & Data Register

CAH-CDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCAP2L	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**RCAP2L.x** **RCAP2H.x**	Timer2 Reload/Capturer Data, x = 0-7
7-0	**TL2.x** **TH2.x**	Timer2 Low & High byte counter, x = 0-7

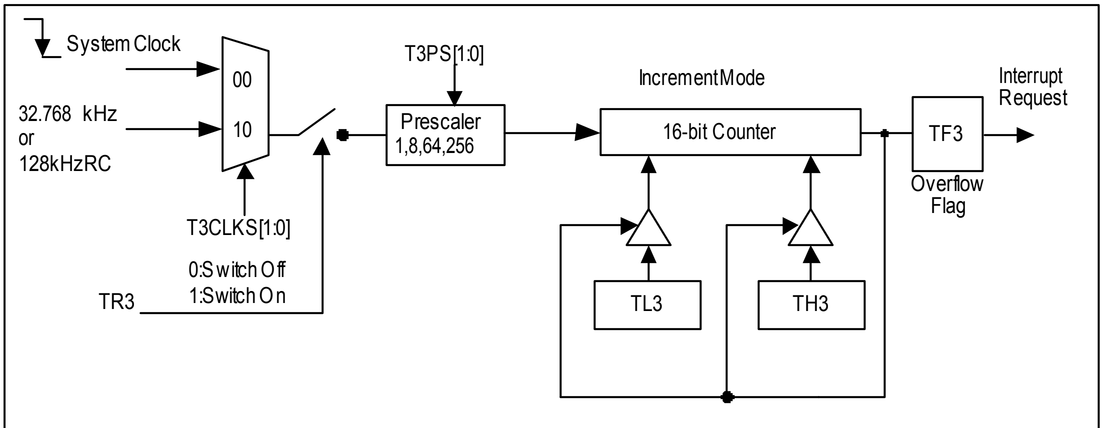
7.8.4 Timer3

Timer 3 is a 16-bit auto-reload timer. It is implemented as a 16-bit register accessed as two cascaded Data Registers: TH3 and TL3. It is controlled by the T3CON register. The Timer 3 interrupt can be enabled by setting ET3 bit in IEN1 register (Refer to **Interrupt** Section for details).

Timer 3 has only one operating mode: 16-bit Counter/Timer with auto-reload. Timer3 also supports the following features: selectable prescaler setting and Operation during CPU Power-Down mode.

Timer 3 consists of a 16-bit counter/reload register (TH3, TL3). When writing to TH3 and TL3, they are used as timer load register. When reading from TH3 and TL3, they are used as timer counter register. Setting the TR3 bit enables Timer 3 to count up. The Timer will overflow from 0xFFFF to 0x0000 and set the TF3 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH3 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH3 and TL3 should follow these steps:
Write operation: Low nibble first, High nibble to update the counter
Read operation: High nibble first, Low nibble followed.



The Block Diagram of Timer3

Timer 3 can operate even in Power-Down mode.

When OP_OSC [2:0] (Refer to **Code Option** Section for details) is 011, 100 or 111, T3CLKS [1:0] can select 00 or 10. When OP_OSC [2:0] is not 011, 100 or 111, T3CLKS [1:0] can select 00, and 10 will be an invalid value.

If T3CLKS [1:0] is 00, Timer 3 can't work in Power Down mode. If T3CLKS [1:0] is 10 and OP_OSC [2:0] is 011, 100 or 111, Timer 3 can work in CPU normal operating or Power Down mode(entering Power Down mode when system clock is high frequency). If T3CLKS [1:0] is 10 and OP_OSC [2:0] is not 011, 100 and 111, Timer 3 can't work. It can be described in the following table.

OP_OSC[2:0]	T3CLKS[1:0]	Can work in normal mode	Can work in Power Down mode
011, 100 or 111	00	YES	NO
	10	YES	YES
Not 011, 100 and 111	00	YES	NO
	10	NO	NO

Note:

1. When TH3 and TL3 read or written, must make sure TR3 = 0.

2. When T3 is selected as Timer3 clock source and TR3 is set 0 to 1, the first T3 down edge will be ignored.

Register

Table 7.28 Timer3 Control Register

88H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T3CON	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
R/W	R/W	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF3**	**Timer3 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T3PS[1:0]**	**Timer3 input clock Prescaler Select bits** 00: 1:1 01: 1:8 10: 1:64 11: 1:256
2	**TR3**	**Timer3 start/stop control bit** 0: Stop Timer3 1: Start Timer3
1-0	**T3CLKS[1:0]**	**Timer3 Clock Source select bits** 00: System clock, T3 pin is used as I/O port 10: External 32.768kHz Crystal or internal 128kHz RC 11: Reserved

Table 7.29 Timer3 Reload/Counter Data Register

8CH-8DH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL3	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL3.x** **TH3.x**	Timer3 Low & High byte counter, x = 0-7

7.9 Interrupt

7.9.1 Feature

- 10 interrupt sources
- 4 interrupt priority levels

SH79F085/SH79F165 provides total 10 interrupt sources: 3 external interrupts (INT0/1/2); 4 Timers interrupts (Timer0, 1, 2), one EUART interrupt, ADC Interrupt and SCM interrupts.

7.9.2 Interrupt Enable Control

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

7.9.3 Register

Table 7.30 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**EA**	**All interrupt enable bit** 0: Disable all interrupt 1: Enable all interrupt
6	**EADC**	**ADC interrupt enable bit** 0: Disable ADC interrupt 1: Enable ADC interrupt
5	**ET2**	**Timer2 overflow interrupt enable bit** 0: Disable Timer2 overflow interrupt 1: Enable Timer2 overflow interrupt
4	**ES**	**EUART interrupt enable bit** 0: Disable EUART interrupt 1: Enable EUART interrupt
3	**ET1**	**Timer1 overflow interrupt enable bit** 0: Disable Timer1 overflow interrupt 1: Enable Timer1 overflow interrupt
2	**EX1**	**External interrupt 1 enable bit** 0: Disable external interrupt1 1: Enable external interrupt1
1	**ET0**	**Timer0 overflow interrupt enable bit** 0: Disable Timer0 overflow interrupt 1: Enable Timer0 overflow interrupt
0	**EX0**	**External interrupt 0 enable bit** 0: Disable external interrupt0 1: Enable external interrupt0

Table 7.31 Secondary Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	ESCM	-	-	ET3	-	-	EX2	-
R/W	R/W	-	-	R/W	-	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	-	-	0	-	-	0	-

Bit Number	Bit Mnemonic	Description
7	**ESCM**	**SCM interrupt enable bit** 0: Disable SCM interrupt 1: Enable SCM interrupt
4	**ET3**	**Timer3 overflow interrupt enable bit** 0: Disable Timer3 overflow interrupt 1: Enable Timer3 overflow interrupt
1	**EX2**	**External interrupt2 enable bit** 0: Disable external interrupt2 1: Enable external interrupt2

7.9.4 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in Table bellow.

For **external interrupt (INT0/1/2)**, when an external interrupt0/1/2 is generated, if the interrupt was edge trigged, the flag (IE0-2 in TCON) that generated this interrupt is cleared by hardware when the service routine is vectored. If the interrupt was level trigged, then the requesting external source directly controls the request flag, rather than the on-chip hardware.

The **Timer 0 /1 interrupt** is generated when they overflows, the flag (TFx, x = 0, 1) in TCON register, which is set by hardware, and will be automatically be cleared by hardware when the service routine is vectored.

The **timer 2 interrupt** is generated by the logical OR of flag TF2 and bit EXF2 in T2CON register, which is set by hardware. None of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, so the flag must be cleared by software.

The **timer 3 interrupt** is generated when they overflow, the flag TF3 in T3CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **EUART interrupt** is generated by the logical OR of flag RI and TI in SCON register, which is set by hardware. Neither of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the receive interrupt flag or the transmission interrupt flag that generated the interrupt, so the flag must be cleared by software.

The **ADC interrupt** is generated by ADCIF bit in ADCON register, which is set by hardware. If an interrupt is generated, the converted result in ADCDH/ADCDM/ADCDL will be valid. The flag must be cleared by software.

The **SCM interrupt** is generated by SCMIF in SCM register, which is set by hardware. And the flag can only be cleared by hardware.

Table 7.32 External Interrupt Flag Register (x = 0, 1)

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 5	**TFx (x = 0, 1)**	**Timer x overflow flag bit** 0: Timer x no overflow 1: Timer x overflow
6, 4	**TRx (x = 0, 1)**	**Timer x start, stop control bit** 0: Stop timer x 1: Start timer x
3, 1	**IEx (x = 0, 1)**	**External interrupt x request flag bit** 0: No interrupt pending 1: Interrupt is pending
2, 0	**ITx (x = 0, 1)**	**External interrupt x trigger mode selection bit** 0: Low level trigger 1: Falling edge trigger

Table 7.33 External Interrupt Flag Register0

E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF0	-	-	-	-	IT2.1	IT2.0	-	IE2
R/W	-	-	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	-	0

Bit Number	Bit Mnemonic	Description
3-2	**IT2[1:0]**	**External interrupt2 trigger mode selection bit** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
0	**IE2**	**External interrupt2 request flag bit** 0: No interrupt pending 1: Interrupt is pending

7.9.5 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in **Interrupt Summary table**.

7.9.6 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. But the OVL NMI interrupt has the highest Priority Level (except RESET) of all the interrupt sources, with no IPH/IPL control. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction cycle, an internal polling sequence determines which request is serviced.

Interrupt Priority		
Priority bits		**Interrupt Lever Priority**
IPHx	IPLx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.34 Interrupt Priority Control Register

B8H, B4H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL0	-	PADCL	PT2L	PS0L	PT1L	PX1L	PT0L	PX0L
IPH0	-	PADCH	PT2H	PS0H	PT1H	PX1H	PT0H	PX0H
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0
B9H, B5H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL1	PSCML	-	-	PT3L	-	-	PX2L	-
IPH1	PSCMH	-	-	PT3H	-	-	PX2H	-
R/W	R/W	-	-	R/W	-	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	-	-	0	-	-	0	-

Bit Number	**Bit Mnemonic**	**Description**
7-0	**PxxxL/H**	Corresponding interrupt source xxx's priority level selection bits

7.9.7 Interrupt Handling

The interrupt flags are sampled and polled at the fetch cycle of each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current cycle is not in the final cycle of the instruction in progress. This ensures that the instruction in progress is completed before vectoring to any service routine.

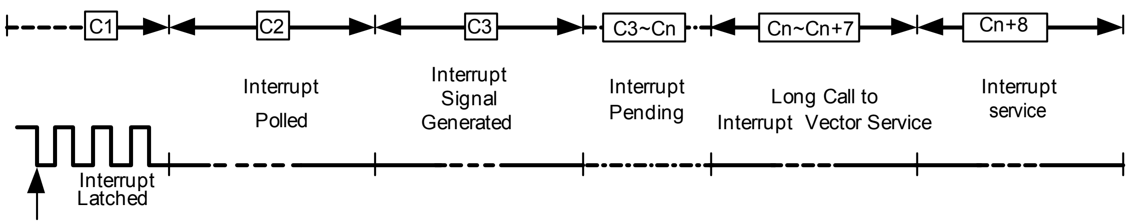
The instruction in progress is RETI. This ensures that if the instruction in progress is RETI then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Notes:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.

The polling cycle/LCALL sequence is illustrated below:



Interrupt Response Timing

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with corresponding address that depends on the source of the interrupt being vectored too, as shown in Interrupt Summary table.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt service. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt with this priority was still in progress. In this case, no interrupt of the same or lower priority level would be acknowledged.

7.9.8 Interrupt Response Time

If an interrupt is recognized, its request flag is set in every machine cycle after recognize. The value will be polled by the circuitry until the next machine cycle; the CPU will generate an interrupt at the third machine cycle. If the request is active and conditions are right for it to be acknowledged, hardware LCALL to the requested service routine will be the next instruction to be executed. Else the interrupt will pending. The call itself takes 7 machine cycles. Thus a minimum of 3+7 complete machine cycles will elapse between activation and external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine.

If the instruction in progress is not in its final cycle and the instruction in progress is RETI, the additional wait time is 8 machine cycles. For a single interrupt system, if the next instruction is 20 machine cycles long (the longest instructions DIV & MUL are 20 machine cycles long for 16 bit operation), adding the LCALL instruction 7 machine cycles the total response time is 2+8+20+7 machine cycles.

Thus interrupt response time is always more than 10 machine cycles and less than 37 machine cycles.

7.9.9 External Interrupt Inputs

The SH79F085/SH79F165 has3 external interrupt inputs. External interrupt0-2 each has one vector address. External interrupt0/1 can be programmed to be low level-triggered or edge-triggered by clearing or setting bit IT1 or IT0 in register TCON. If ITx = 0 (x = 0, 1), external interrupt x (x = 0, 1) is triggered by a low level detected at the INTx (x = 0, 1) pin. If ITx = 1 (x = 0, 1), external interrupt x (x = 0, 1) is edge triggered. In this mode if consecutive samples of the INTx (x = 0, 1) pin show a high level in one cycle and a low level in the next cycle, interrupt request flag in register TCON is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

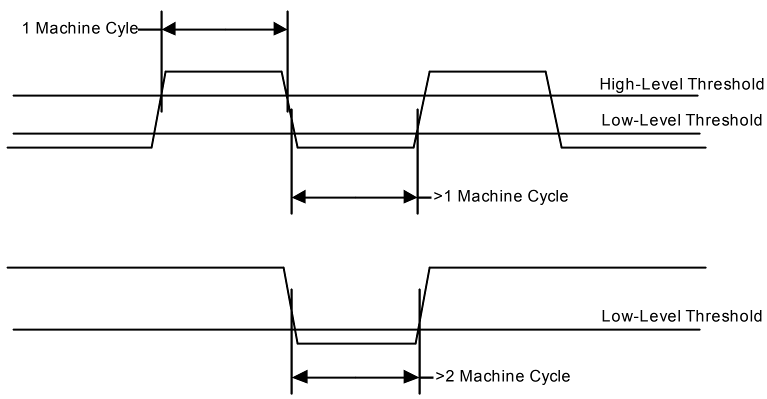
If the external interrupt is falling edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag is set.

If the external interrupt is low level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag IEx (x = 0, 1, 2,) when the interrupt is level sensitive, it simply tracks the input pin level.

External interrupt2 operates in the similar ways except have different registers and have more selection of trigger.

If an external interrupt is enabled when the SH79F085/SH79F165 is put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation. Refer to Power management Section for details.

Note: *IE0-2 is automatically cleared by CPU when the service routine is called.*



External Interrupt Detection

7.9.10 Interrupt Summary

Source	Vector Address	Enable bits	Flag bits	Polling Priority	Interrupt number (c language)
Reset	0000H	-	-	0 (highest)	-
INT0	0003H	EX0	IE0	1	0
Timer0	000BH	ET0	TF0	2	1
INT1	0013H	EX1	IE1	3	2
Timer1	001BH	ET1	TF1	4	3
EUART	0023H	ES	RI+TI	5	4
Timer2	002BH	ET2	TF2+EXF2	6	5
ADC	0033H	EADC	ADCIF	7	6
INT2	0043H	EX2	IE2	8	8
Timer3	005BH	ET3	TF3	9	11
SCM	0073H	ESCM	SCMIF	11 (lowest)	14

8. Enhanced Function

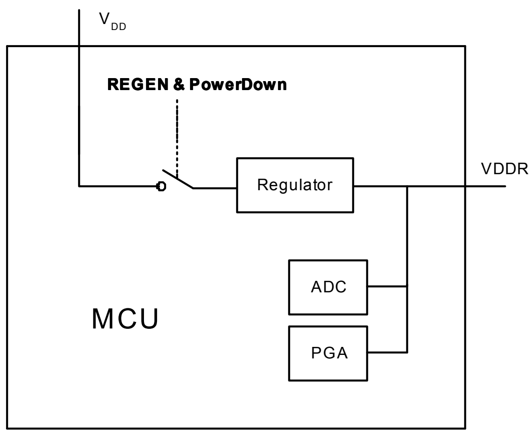
8.1 Regulator

8.1.1 Feature

- Stable voltage output
- Regulator output voltage can be shutdown

The SH79F085/SH79F165 built-in regulator. This regulator can output stable voltage for analog device such as PGA and ADC. The regulator can also output stable voltage for weight sensor.

The regulator can be shutdown or start function by setting or REGEN bit in REGCON register. This regulator must shut down by clearing REGEN bit in REGCON register before MCU enter Power-Down mode. Thus result in stand-by power consumption reduction of system.



8.1.2 Regulator

Table 8.1 Regulator Control Register

A1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REGCON	-	-	-	-	-	-	-	REGEN
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Mnemonic	Description
0	**REGEN**	**Regulator Control bit** 0: Shutdown regulator 1: Start regulator The regulator must shutdown by software when MCU in Power-Down mode

8.2 Enhanced Universal Asynchronous Receiver-Transmitter (EUART)

8.2.1 Feature

- SH79F085/SH79F165 has a EUART which is compatible with the conventional 8051
- The baud rate can be selected from the divided clock of the system clock, or Timer1/2 overflow rate
- Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
- The EUART can be operated in four modes

8.2.2 EUART Mode Description

The EUART can be operated in 4 modes. Users must initialize the SCON before any communication can take place. This involves selection of the Mode and the baud rate. The Timer1 or Timer2 should also be initialized if the mode 1 or the mode 3 is used.

In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if RI = 0 and REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

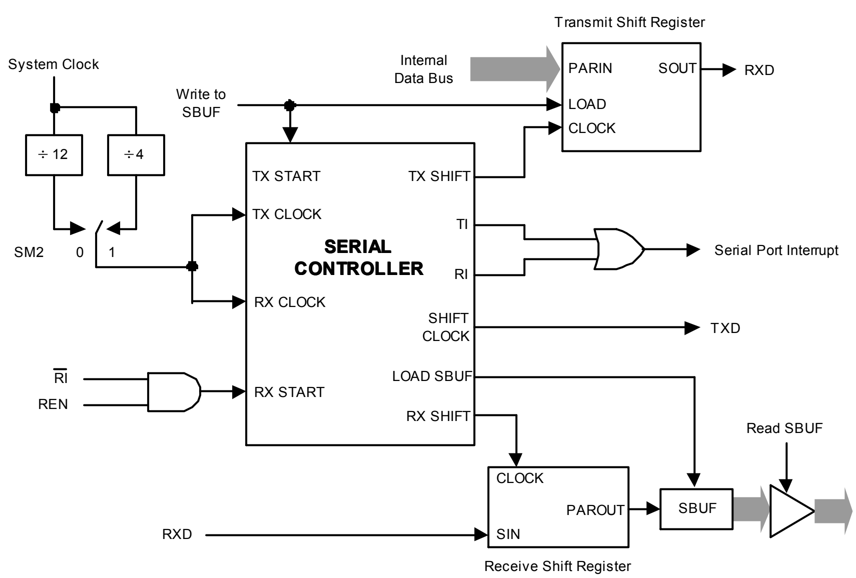
SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th Bit
0	0	0	Synch	f_{SYS}/(4 or 12)	8 bits	NO	NO	None
0	1	1	Asynch	Timer1 or 2 overflow rate/(16 or 32)	10 bits	1	1	None
1	0	2	Asynch	f_{SYS}/(32 or 64)	11 bits	1	1	0, 1
1	1	3	Asynch	Timer1 or 2 overflow rate/(16 or 32)	11 bits	1	1	0, 1

Mode0: Synchronous Mode, Half duplex

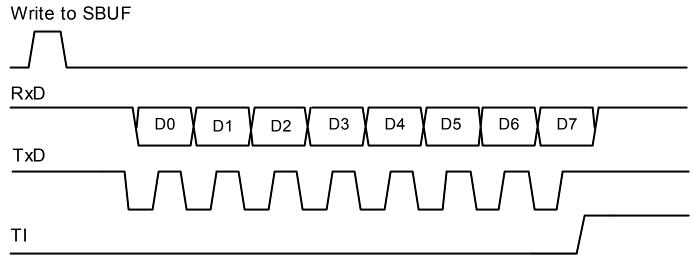
This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RxD line. TxD is used to output the shift clock. The TxD clock is provided by the SH79F085/SH79F165 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first.

The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

The functional block diagram is shown below. Data enters and exits the serial port on the RxD line. The TxD line is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the SH79F085/SH79F165.

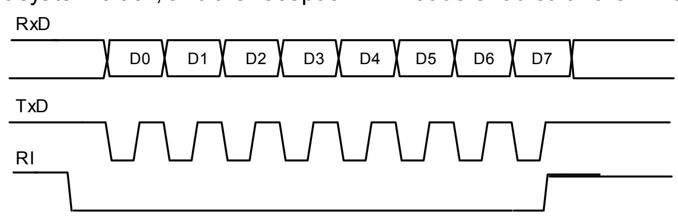


Any instruction that uses SBUF as a destination register (“write to SBUF” signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivates SEND and sets TI (SCON.1) at the rising edge of the next system clock.



Send Timing of Mode 0

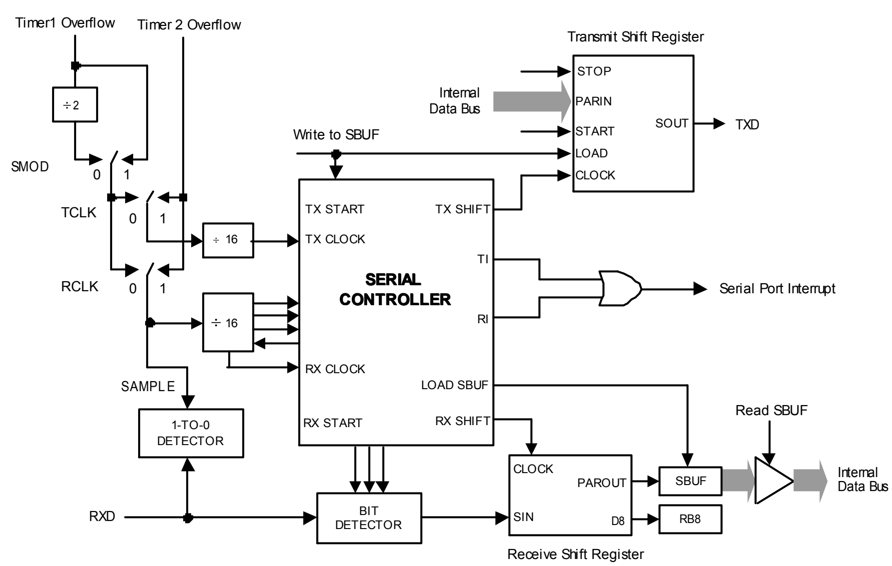
Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivates RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.



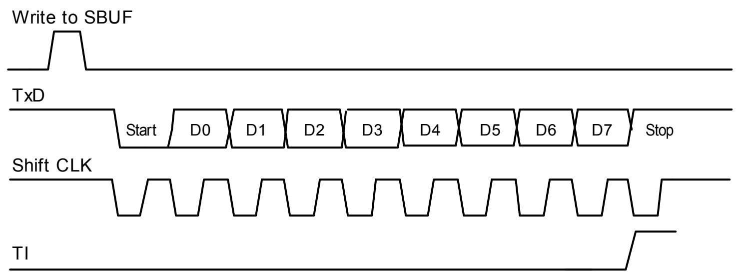
Receive Timing of Mode 0

Mode1: 8-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The baud rate in this mode is variable. The serial receive and transmit baud rate can be programmed to be 1/16 or 1/32 of the Timer1 overflow or 1/16 of Timer 2 overflow (Refer to **Baud Rate** Section for details). The functional block diagram is shown below.



Transmission begins with a "write to SBUF" signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SUBF" signal. The start bit is firstly put out on TxD pin, then are the 8 bits of data. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time that the stop is send.



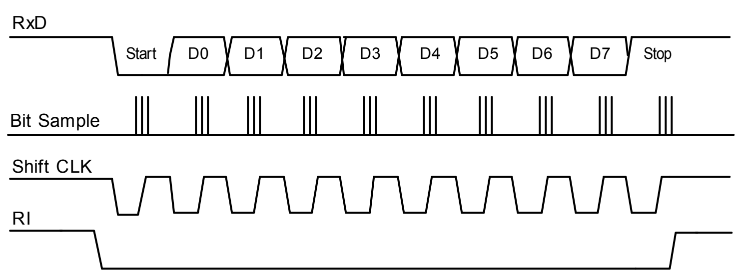
Send Timing of Mode 1

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7^{th}, 8^{th} and 9^{th} counter states of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI are set if the following conditions are met:

1. RI must be 0
2. Either SM2 = 0, or the received stop bit = 1

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

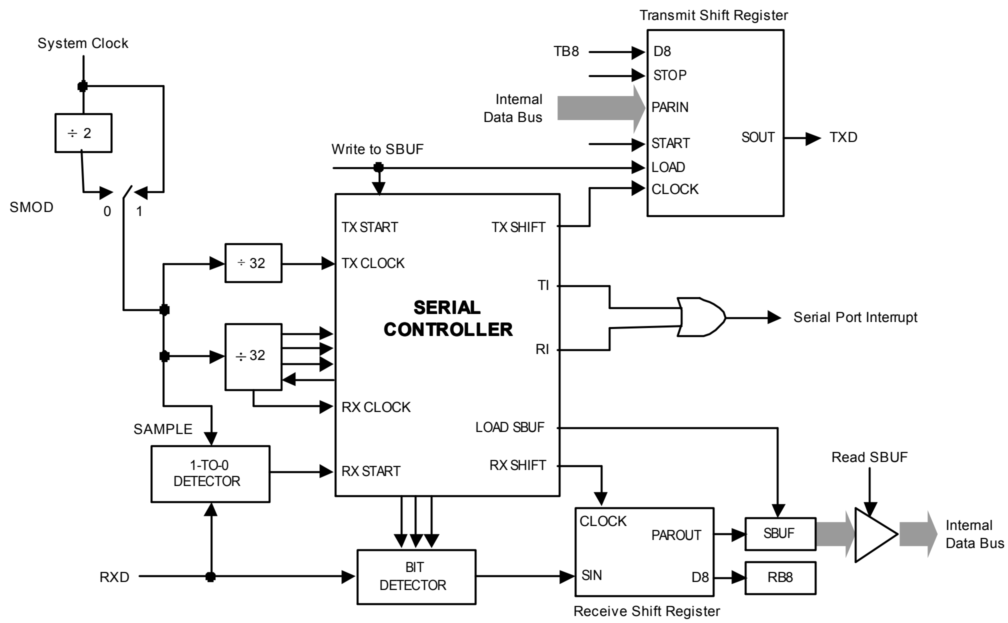
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



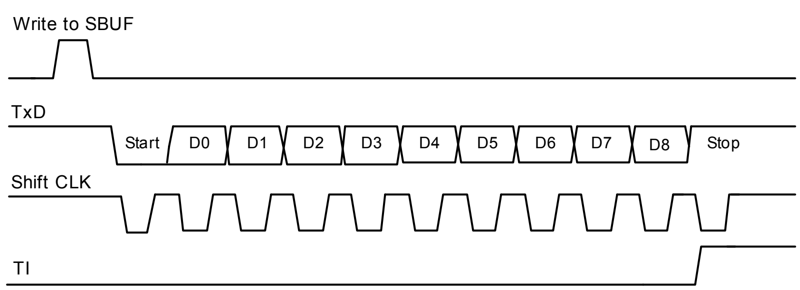
Receive Timing of Mode 1

Mode2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

This mode provides the 11 bits full duplex asynchronous communication. The 11 bit consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition **(**Refer to **Multiprocessor Communication** Section for details**)**. When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below.



Transmission begins with a "write to SBUF" signal, the "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SUBF" signal). The start bit is firstly put out on TxD pin, then are the 9 bits of data. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time, this will be at the 11th rollover of the divide-by-16 counter after a write to SBUF.



Send Timing of Mode 2

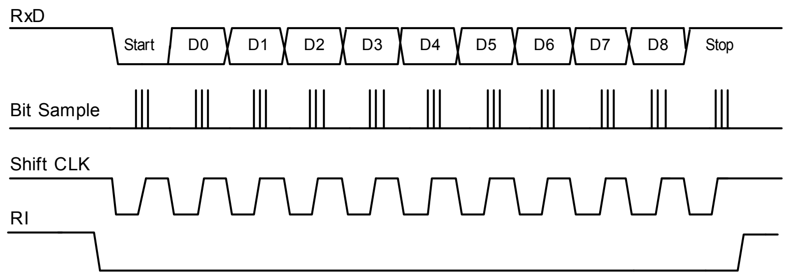
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter. The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7th, 8th and 9th counter state of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit detected after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register.

After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set if the following conditions are met:

1. RI must be 0
2. Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

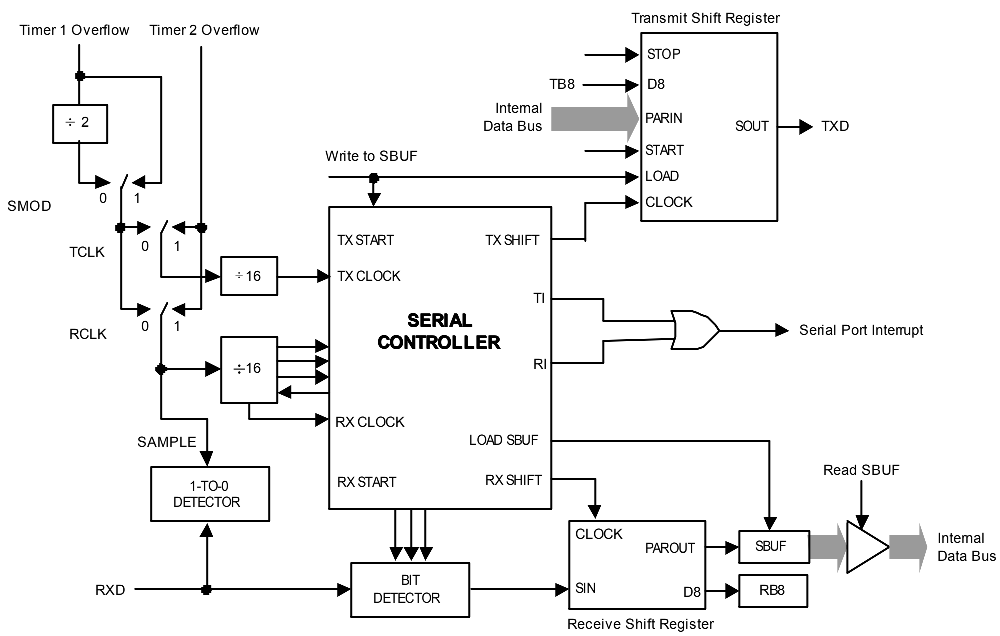
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

Mode3: 9-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

Mode3 uses transmission protocol of the Mode2 and baud rate generation of the Mode1.



8.2.3 Baud Rate Generate

In Mode0, the baud rate is programmable to either 1/12 or 1/4 of the system frequency. This baud rate is determined by SM2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

In Mode1 & Mode3, the baud rate can be selected from Timer1/2 overflow rate.

Timer2 can be selected as TX and/or RX baud rate clock source by setting the TCLK (T2CON.4) and/or RCLK (T2CON.5) bits, respectively (Refer to Timer2 Section for details). When either TCLK or RCLK is set to logic 1, Timer2 is forced into Baud Rate Generator Mode. If TCLK and/or RCLK is logic 0, Timer1 acts as the baud rate clock source for the Tx and/or Rx circuits, respectively.

The Mode1 & 3 baud rate equations are shown below, where TH1 is the 8-bit reload register for Timer 1, SMOD is the EUART baud rate doubler (PCON.7)， [RCAP2H, RCAP2L] is the 16-bit reload register for Timer2. T1CLK is the clock source of Timer 1, T2CLK is the clock source of Timer2.

$\text{BaudRate} = \frac{2^{SMOD}}{32} \times \frac{f_{T1}}{256 - TH1}$, Baud Rate using Timer1, Mode2

$\text{BaudRate} = \frac{1}{2 \times 16} \times \frac{f_{T2}}{65536 - [RCAP2H, RCAP2L]}$, Baud Rate using Timer 2, with system clock

$\text{BaudRate} = \frac{1}{16} \times \frac{f_{T2}}{65536 - [RCAP2H, RCAP2L]}$, Baud Rate using Timer 2, with T2 clock input

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, the serial port runs at 1/64 of the clock. When set to 1, the serial port runs at 1/32 of the clock.

$$\text{BaudRate} = 2^{SMOD} \times \left(\frac{f_{SYS}}{64}\right)$$

8.2.4 Multi-processor Communication

Software Address Recognition

Modes2 and 3 of the EUART have a special provision for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the EUART interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte.

With SM2 = 1, no other slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed leave their SM2 set and go on with their business, ignoring the incoming data bytes.

Note:

In mode 0, SM2 is used to select baud rate doubling. In mode 1, SM2 can be used to check the validity of the stop bit. If SM2 = 1 in mode 1, the receive interrupt will not be activated unless a valid stop bit is received.

Automatic (Hardware) Address Recognition

In Mode 2 & 3, setting the SM2 bit will configure EUART act as following: when a stop bit is received, EUART will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts on the reception of the following data byte(s).

The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the addressed slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the addressed slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, as they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all transmissions until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. The slave address is an 8-bit value specified in the SADDR register. The SADEN register is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR. Use of the Given Address allows multiple slaves to be recognized while excluding others.

	Slave 1	Slave 2
SADDR	10100100	10100111
SADEN (0 mask)	11111010	11111001
Given Address	10100x0x	10100xx1
Broadcast Address (OR)	1111111x	11111111

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as don't cares. In most cases, the Broadcast Address is FFh, this address will be acknowledged by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXXXXXX (all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUART 0 will reply to any address, which it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor by software address recognition mentioned above.

8.2.5 Error Detection

Error detection is available when the SSTAT bit in register PCON is set to logic 1.The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).All the 3 bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Transmit Collision

The Transmit Collision bit (TXCOL bit in register SCON) reads '1' if RI is set 0 and user software writes data to the SBUF register while a transmission is still in progress. If this occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overrun

The Receive Overrun bit (RXOV in register SCON) reads '1' if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happen.

Frame Error

The Frame Error bit (FE in register SCON) reads '1' if an invalid (low) STOP bit is detected.

Break Detection

A break is detected when any 11 consecutive bits are sensed low. Since a break condition also satisfies the requirements for a framing error, a break condition will also result in reporting a framing error. Once a break condition has been detected, the EUART will go into an idle state and remain in this idle state until a valid stop bit (rising edge on RxD line) has been received.

8.2.6 Register

Table 8.2 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SMOD	**Baud rate doubler** If set in mode1 & 3, the baud-rate of EUART is doubled if using timer1 as baud-rate generator If set in mode2, the baud-rate of EUART is doubled
6	SSTAT	**SCON[7:5] function select bit** 0: SCON[7:5] operates as SM0, SM1, SM2 1: SCON[7:5] operates as FE, RXOV, TXCOL
4-0	-	**Other bits Refer to Power Section for details**
3-2	GF[1:0]	**General purpose flags for software use**
1	PD	**Power-Down mode control bit**
0	IDL	**Idle mode control bit**

EUART related SFR

Table 8.3 EUART Control & Status Register

98H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0 /FE	SM1 /RXOV	SM2 /TXCOL	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**SM[0:1]**	**EUART Serial mode control bit, when SSTAT = 0** 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8 bit Asynchronous Mode, variable baud rate 10: mode 2, 9 bit Asynchronous Mode, fixed baud rate 11: mode 3, 9 bit Asynchronous Mode, variable baud rate
7	**FE**	**EUART Frame Error flag, when FE bit is read, SSTAT bit must be set 1** 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware
6	**RXOV**	**EUART Receive Over flag, when RXOV bit is read, SSTAT bit must be set 1** 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware
5	**SM2**	**EUART Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0** 0: In mode 0, baud-rate is 1/12 of system clock In mode 1, disable stop bit validation check, any stop bit will set RI to generate interrupt In mode 2 & 3, any byte will set RI to generate interrupt 1: In mode 0, baud-rate is 1/4 of system clock In mode 1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In mode 2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	**TXCOL**	**EUART Transmit Collision flag, when TXCOL bit is read, SSTAT bit must be set 1** 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware
4	**REN**	**EUART Receiver enable bit** 0: Receive Disable 1: Receive Enable
3	**TB8**	**The 9th bit to be transmitted in mode2 & 3 of EUART, set or clear by software**
2	**RB8**	**The 9th bit to be received in mode1,2 & 3 of EUART** In mode 0, RB8 is not used In mode 1, if receive interrupt occurs, RB8 is the stop bit that was received In modes 2 & 3 it is the 9th bit that was received
1	**TI**	**Transmit interrupt flag of EUART** 0: Cleared by software 1: Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in other modes
0	**RI**	**Receive interrupt flag of EUART** 0: cleared by software 1: Set by hardware at the end of the 8th bit time in mode 0, or during the stop bit time in other modes

Table 8.4 EUART Data Buffer Register

99H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SBUF.7-0**	This SFR accesses two registers; a transmit shift register and a receive latch register. A write of SBUF will send the byte to the transmit shift register and then initiate a transmission. A read of SBUF returns the contents of the receive latch.

Table 8.5 EUART Slave Address & Address Mask Register

9AH-9BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SADDR.7-0**	**SFR SADDR defines the EUART's slave address**
7-0	**SADEN.7-0**	**SFR SADEN is a bit mask to determine which bits of SADDR are checked against a received address** 0: Corresponding bit in SADDR is a "don't care" 1: Corresponding bit in SADDR is checked against a received address

8.3 Analog to Digital Converter (ADC)

8.3.1 Feature

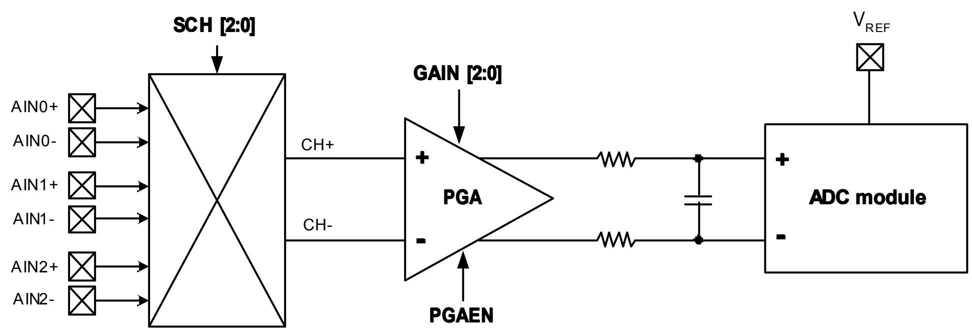
- 20-bit data output
- 16-bit resolution
- Internal reference voltage
- Internal or external reference voltage can be selected by user
- SH79F085: 2 differential input
- SH79F165: 3 differential input

The SH79F085/SH79F165 include a full-differential 20-bit Σ-Δ analog to digital converter. This ADC built-in reference voltage. User can also select external reference voltage. The analog input will be amplified by the PGA (Programmable Gain Amplifier) before being input to ADC module. There are two kinds of analog input, differential input and calibration input.

When set ADON bit in ADCON register, the conversion is always doing. When one conversion is complete, the data in ADC data register will be updated and ADIF bit in ADCON register will be set. If ADC interrupt is enabled, the ADC interrupt will generate.

The ADC module can also work in IDLE mode and the ADC interrupt will wake up the IDLE mode. But the module is disabled in Power-Down mode.

8.3.2 ADC Diagram



8.3.3 Register

Table 8.6 ADC Control Register

93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	-	REFC	-	SCH2	SCH1	SCH0
R/W	R/W	R/W	-	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	0	-	0	0	0

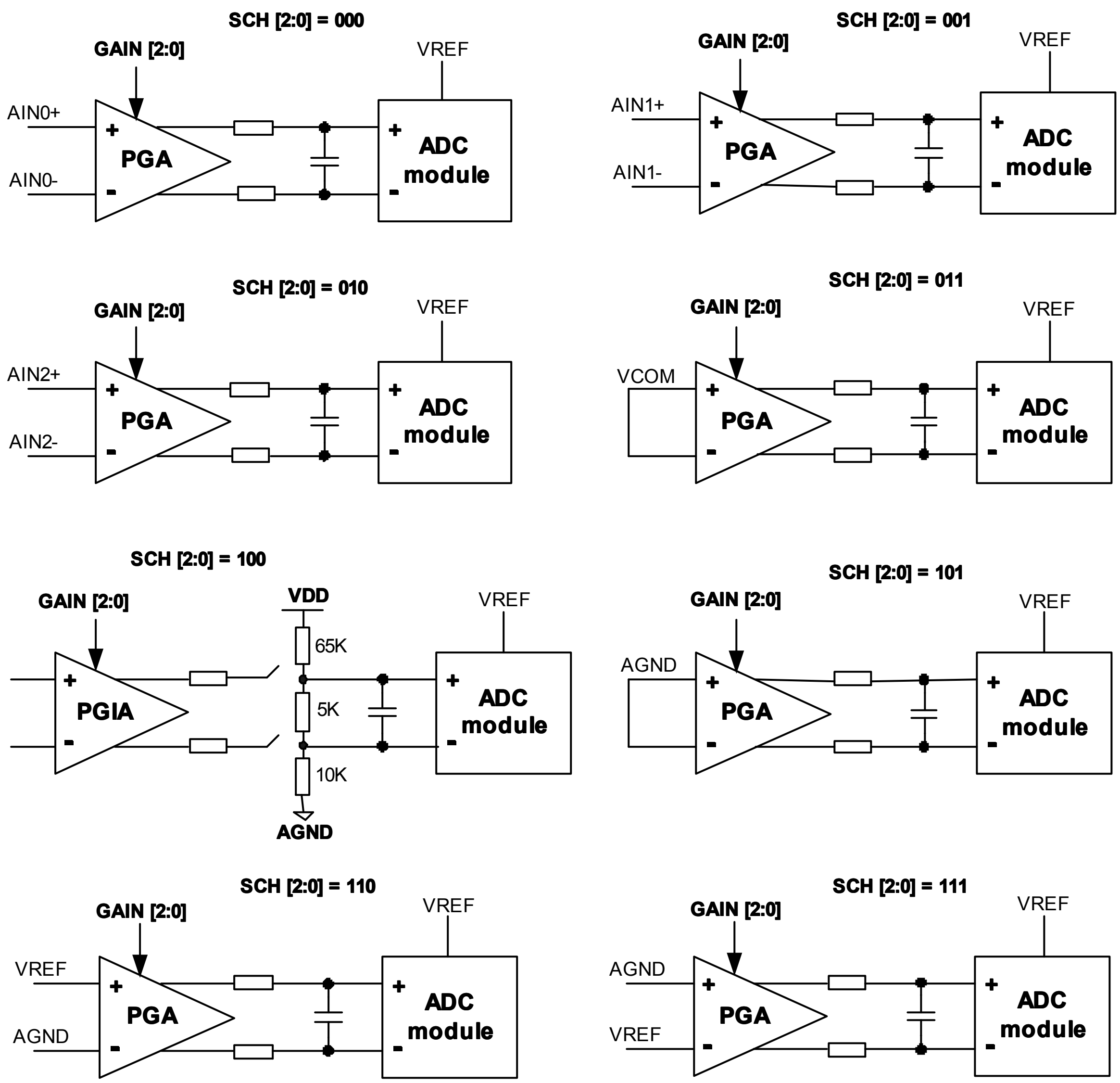
Bit Number	Bit Mnemonic	Description
7	**ADON**	**ADC Control bit** 0: Disable ADC module 1: Enable ADC module, set to start AD convert
6	**ADCIF**	**ADC Interrupt Flag bit** 0: No ADC interrupt generate, must be cleared by software 1: Set by hardware, one conversion complete
4	**REFC**	**ADC Reference Control bit** 0: Select internal reference voltage, P27OS bit in ADCH register must write "1" 1: Select external reference voltage in VREF pin, P27OS bit in ADCH register must write "1"
2-0	**SCH[2:0]**	**ADC Channel Select bit** 000: ADC differential input AIN0+, AIN0- 001: ADC differential input AIN1+, AIN1- 010: ADC differential input AIN2+, AIN2- 011: PGA internal short, connect with VCOM 100: Measure voltage of V_{DD}, internal differential input: 1/16 V_{DD} 101: PGA internal short, connect with AGND 110: PGA Positive connect with V_{REF}, PGA Negative connect with AGND 111: PGA Positive connect with AGND, PGA Negative connect with V_{REF}

Notes:

(1) Clearing ADON bit during converting time will stop current AD conversion.

(2) The first two-conversion result is not use, because Σ-Δ analog to digital converter need setup time.

ADC Channel Diagram:



Note:

If SCH[2:0] = 100, it used to measure voltage value of V_{DD}. An internal 80kΩ resistor will connect V_{DD} to GND to provide sample point. If SCH[2:0] ≠ 100. This resistor will be disconnected.

Table 8.7 ADC Clock Register

94H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	TADC7	TADC6	TADC5	TADC4	TADC3	TADC2	TADC1	TADC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TADC[7:0]**	**ADC Clock Register** ADC Clock = $f_{SYS}/2/(256\text{-}TADC[7:0])$

Note:

(1) The f_{SYS} is system Clock, it will affect ADC clock when system clock prescaler is changed;
(2) ADT register sets ADC working clock, 100kHz is recommended as ADC clock;
(3) The relation between ADC clock and ADT: ADC clock = $f_{SYS}/2/(256\text{-}TADC[7:0])$;
(4) ADC conversion rate: ADC clock/4000;
(5) AC power 50Hz noise will be filtered out when ADC conversion rate is 25Hz;
(6) AC power 60Hz noise will be filtered out when ADC conversion rate is 20Hz;
(7) Both AC power 50Hz and 60Hz noise will be filtered out when ADC conversion rate is 10Hz;
*(8) ADC precision will affect when conversion rate more than 50Hz.(Refer to **electrical characteristics** section for details).*

Table 8.8 ADC Random Clock Register

B7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADRAND	RANDEN	-	-	-	RAND3	RANDC2	RAND1	RAND0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**RANDEN**	**ADC Random Clock Enable bit** 0: Disable random clock 1: Enable random clock
3-0	**RAND[3:0]**	**ADC Random Clock Control bit** 0000: Random clock rang 0-F 0001: Random clock rang 0-F 0010: Random clock rang 0-F 0011: Random clock rang 0-F 0100: Random clock rang 0-1 0101: Random clock rang 0-3 0110: Random clock rang 0-7 0111: Random clock rang 0, 1, 2, 3, 8, 9, a, b 1000: Random clock rang 0, 1, 8, 9 1001: Random clock rang 0, 1, 4, 5 1010: Random clock rang 0, 8 1011: Random clock rang 0, 4, 8, c 1100: Random clock rang 0, 2, 8, a 1101: Random clock rang 0, 2, 4, 6, 8, a, c, e 1110: Random clock rang 0, 2, 4, 6 1111: Random clock rang 0, 4 ADC actual clock = ADC clock ± ADC random clock

Table 8.9 ADC Channel Configuration Register

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH	VREF2	VREF1	VREF0	-	P27OS	CH2	CH1	CH0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-5	**VREF[2:0]**	**Internal Reference Voltage Select bit** 000: V_{REF} = 0.1V 001: V_{REF} = 0.2V 010: V_{REF} = 0.3V 011: V_{REF} = 0.4V 100: V_{REF} = 0.5V 101: V_{REF} = 0.6V 110: V_{REF} = 0.7V 111: V_{REF} = 0.8V
3	**P27OS**	**V_{REF} pin Configuration bit** 0: P2.7 as I/O Ports 1: P2.7 as ADC reference voltage input/output pin
2	**CH2**	**AIN2 Channel Configuration bit** 0: P2.1-P2.2 as I/O Ports 1: P2.1-P2.2 as ADC analog input (AIN2+, AIN2-)
1	**CH1**	**AIN1 Channel Configuration bit** 0: P1.5-P1.6 as I/O Ports 1: P1.5-P1.6 as ADC analog input (AIN1+, AIN1-)
0	**CH0**	**AIN0 Channel Configuration bit** 0: P2.5-P2.6 as I/O Ports 1: P2.5-P2.6 as ADC analog input (AIN0+, AIN0-)

Table 8.10 AD Converter Data Register

91H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDL	-	-	-	-	A3	A2	A1	A0
R/W	-	-	-	-	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0
96H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDM	A11	A10	A9	A8	A7	A6	A5	A4
R/W	R	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0
97H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDH	A19	A18	A17	A16	A15	A14	A13	A12
R/W	R	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
19-0	**A19-A0**	**20-bit ADC data register**

Note:

(1) ADC conversion result is stored in A19-A0. The A19 is the sign bit of ADC data. Refer to the following formula to calculate ADC conversion data value:

ADC data = ((VIN+) - (VIN-)) / V_{REF} X 500000

When (VIN+) > (VIN-) is positive, A19 is 0 which means the ADC data is positive. The ADC value is A19-A0;

When (VIN+) < (VIN-) is negative, A19 is 1 which means the ADC data is negative. The ADC value is 100000H minus A19-A0.

*(2) To obtain maximum range of ADC output, the maximum absolute of ADC input voltage of ((AINx+) - (AINx-))*Gain should be close to reference voltage value, bit can't over the reference voltage value.*

ADC Conversion Data Value refer to following:

ADC Data	7A120H	40000H	00001H	00000H	FFFF FH	C0000H	85EE0
Decimal Value	500000	262144	1	0	-1	-262144	-500000

Start ADC Conversion Step:

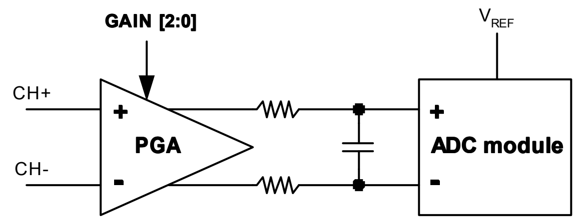
- Set REGEN bit in REGCON register to start regulator.
- Set or clear REFC bit in ADCON register and set P27OS bit in ADCH register to select reference voltage.
- Set SCH[2:0] bits in ADCON register and set CH0~2 bit in ADCH register to select ADC channel.
- Set GAIN[2:0] bits in PGAM register to select PGA gain.
- Set register PGAM to select PGA chopper function and choose chop clock.
- Set PGAEN bit in PGAM register to enable PGA function.
- Set register ADT to choose ADC clock.
- Set ADON bit in ADCON register to start ADC conversion
- ADCIF of register ADCON will be set when ADC conversion is finished, the new ADC data will be stored in ADC data register.If ADC interrupt is enabled, an interrupt will generate.
- Obtain ADC conversion data by ADDH/ADDM/ADDL.
- Clear ADCIF bit in ADCON register for next ADC conversion.

8.4 Programmable Gain Amplifier (PGA)

8.4.1 Feature

- Low noise programmable gain amplifier
- Programmable gain range 12.5 - 200
- Chopper

The SH79F085/SH79F165 provides a low noise programmable gain amplifier. This PGA provides amplification setting of 12.5, 25, 50, 75, 100, 125, 150 and 200 for ADC analog input. The PGA gain setting is controlled by Gain[2:0] bits in PGAM register. A chopper is included, which can be used for eliminate PGA offset. Chopper work clock can select 1kHz, 2kHz, 3kHz, or 4kHz.



8.4.2 Register

Table 8.11 PGA Mode Control Register

A3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGAM	PGAEN	GAIN2	GAIN1	GAIN0	-	CHOPEN	CHOPC1	CHOPC0
R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	**PGAEN**	**PGA Enable bit** 0: Disable PGA function, PGA Gain = 1 1: Enable PGA function
6-4	**GAIN[2:0]**	**PGA Gain select bit** 000: Gain = 12.5 001: Gain = 25 010: Gain = 50 011: Gain = 75 100: Gain = 100 101: Gain = 125 110: Gain = 150 111: Gain = 200
2	**CHOPEN**	**Chopper Enable bit** 0: Disable chopper function 1: Enable chopper function
1-0	**CHOPC[1:0]**	**Chopper Work Clock Select bit** 00: 1kHz 01: 2kHz 10: 3kHz 11: 4kHz Work clock of 1kHz is recommended

8.5 Buzzer

8.5.1 Feature

- Output a signal (square wave) used for tones such as a confirmation tone
- Selectable whether to output one of 10 output frequencies or to disable the output

8.5.2 Register

Table 8.12 Buzzer Output Control Register

BDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUZCON	-	-	-	BCA3	BCA2	BCA1	BCA0	BZEN
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
4-1	**BCA[3:0]**	**Buzzer output carrier frequency control bits** 0000: system clock/8192 0001: system clock/4096 0010: system clock/2048 0011: system clock/1024 0100: system clock/512 0101: system clock/32 0110: system clock/16 0111: system clock/8 1000: system clock/16384 1001: system clock/32768 others: system clock/8192
0	**BZEN**	**Enable buzzer output control bit** 0: P1.0 is I/O port 1: P1.0 is buzzer output port

8.6 Low Voltage Reset (LVR)

8.6.1 Feature

- Enabled by the code option and V_{LVR} is 3.1V or 4.3V
- LVR de-bounce timer T_{LVR} is about 30-60µs
- An internal reset flag indicates low voltage reset generates

The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage below the specified value V_{LVR}. The LVR de-bounce timer T_{LVR} is about 30-60µs.

The LVR circuit has the following functions when the LVR function is enabled: (t means the time of the supply voltage below V_{LVR})

Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq T_{LVR}$;

Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$, but $t < T_{LVR}$.

The LVR function is enabled by the code option.

It is typically used in AC line or large battery supplier applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage. This feature can protect system from working under bad power supply environment.

8.7 Watchdog Timer (WDT) and Reset State

8.7.1 Feature

- Auto detect Program Counter (PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH79F085/SH79F165built in Program Counter(PC)over range detect circuit, if program counter value is larger than flash romsize, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash rom with A5H.

Watchdog Timer

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled permanently by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow frequency. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

There are also some reset flags in this register as below:

8.7.2 Register

Table 8.13 Reset Control Register

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Mnemonic	Description
7	**WDOF**	**Watch Dog Timer Overflow or OVL Reset Flag** Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows and no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	**PORF**	**Power On Reset Flag** Set only by Power On Reset, cleared only by software 0: No Power On Reset 1: Power On Reset occurred
4	**LVRF**	**Low Voltage Reset Flag** Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	**CLRF**	**Pin Reset Flag** Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred
2-0	**WDT[2:0]**	**WDT Overflow period control bit** 000: Overflow period minimal value = 4096ms 001: Overflow period minimal value = 1024ms 010: Overflow period minimal value = 256ms 011: Overflow period minimal value = 128ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms ***Notes:*** *If WDT_opt is enable in application, you must clear WatchDog periodically, and the interval must be less than the value list above.*

8.8 Power Management

8.8.1 Feature

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH79F085/SH79F165 supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

8.8.2 Idle Mode

In this mode, the clock to CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH79F085/SH79F165 enter Idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter Idle mode. The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

(1) An interrupt generated. After warm-up time, the clock to the CPU will be restored, and the hardware will clear SUSLO register and IDL bit in PCON register. Then the program will execute the interrupt service routine first, and then jumps to the instruction immediately following the instruction that activated Idle mode.

(2) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled), this will restore the clock to the CPU, the SUSLO register and the IDL bit in PCON register will be cleared by hardware, finally the SH79F085/SH79F165 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

8.8.3 Power-Down Mode

The Power-Down mode places the SH79F085/SH79F165 in a very low power state. Power-Down mode will stop all the clocks including CPU and peripherals. If WDT is enabled, WDT block will keep on working. When entering Power-Down mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79F085/SH79F165 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

The setting of PD bit will be the last instruction that CPU executed. If PLL is enabled before CPU enters Power-Down mode, it will be also stopped, then will be restarted after Power-Down mode exit.

Note: *If IDL bit and PD bit are set simultaneously, the SH79F085/SH79F165 enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit form Power-Down mode.*

There are three ways to exit the Power-Down mode:

(1) An active external Interrupt such as INT0, INT1 & INT2 will make SH79F085/SH79F165 exit Power-Down mode. The oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) If system clock is external crystal (400kHz - 16MHz) or internal RC 16.6MHz, Timer3 clock is external crystal 32.768kHz or internal RC 128kHz, Timer3 interrupt will make SH79F085/SH79F165 exit Power-Down mode. The high frequency crystal will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(3) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled). This will restore the clock to the CPU after warm-up time, the SUSLO register and the PD bit in PCON register will be cleared by hardware, finally the SH79F085/SH79F165 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note:

(1) In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.

(2) In order to entering Idle/Power-Down, all ports should be set as output, or set as input and pull-high is opened to avoid floating.

(3) In power saving mode: SOP24 packaging need software set the address of bit 0 to bit 3 in P0CR as 1, or set as 0 and set bit 0 to bit3 in P0PCR;SOP20 packaging need software set bit 0 to bit 3 in P0CR, bit 7 in P2CR and bit 0 to bit 2 in P2CR as 1,or set as 0 and set corresponding bit in PxPCR(x=0,1,2) as 1, so as to avoid leakage current.

8.8.4 Register

Table 8.14 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SMOD	**Baud rate double bit**
6	SSTAT	**SCON[7:5] function selection bit**
3-2	GF[1:0]	**General purpose flags for software use**
1	PD	**Power-Down mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode
0	IDL	**Idle mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode

Table 8.15 Suspend Mode Control Register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SUSLO[7:0]	This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise the either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle.

```
IDLE_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #01H
        NOP
        NOP
        NOP
```

```
POWERDOWN_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #02H
        NOP
        NOP
        NOP
```

8.9 Warm-up Timer

8.9.1 Feature

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation startup

SH79F085/SH79F165 has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read customer option etc.

SH79F085/SH79F165 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from Power-down mode.

After power-on, SH79F085/SH79F165 will start power warm-up procedure first, and then oscillator warm-up procedure.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		WDT Reset (Not in Power-Down Mode)		WDT Reset (Wakeup from Power-Down Mode)		Wakeup from Power-Down Mode (Only for interrupt)	
TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*
11ms	YES	1000CKs	NO	1000CKs	YES	64CKs	YES

OSC Warm-up Time

Option: OP_WMT / Oscillator Type	00	01	10	11
Crystal (400kHz-16MHz)	2^{17} X T_{OSC}	2^{14} X T_{OSC}	2^{11} X T_{OSC}	2^{8} X T_{OSC}
32kHz Crystal	2^{13} X T_{OSC}			
Internal RC	2^{7} X T_{OSC}			

8.10 Code Option

OP_CERAMIC:
0: Ceramic Oscillator > 2MHz (default)
1: Ceramic Oscillator < 2MHz

OP_WDT:
0: Disable WDT function (default)
1: Enable WDT function

OP_WDTPD:
0: Disable WDT function in the Power-Down mode (Default)
1: Enable WDT function in the Power-Down mode

OP_RST:
0: P0.4 used as RST pin (Default)
1: P0.4 used as I/O pin

OP_WMT[1:0]: (High frequency crystal)
00: longest warm up time (Default)
01: longer warm up time
10: shorter warm up time
11: shortest warm up time

OP_OSC[3:0]:
0011: Internal 128kHz RC oscillator, Internal 16.6MHz RC oscillator, OSC and OSCX shared with IO (Default)
0110: Internal 128kHz RC oscillator, 400k - 16.6M crystal oscillator at OSC
1010: 32.768kHz crystal oscillator at OSC, Internal 16.6MHz RC oscillator

OP_ISP:
0: Enable ISP function (Default)
1: Disable ISP function

OP_ISPPIN:
0: Enter ISP mode only when P1.5 and P1.6 are connected to GND, simultaneously (Default)
1: Enter ISP mode directly regardless the condition of P1.5 and P1.6
Note: *When OP_ISP = 0, OP_ISPIN is available*

OP_LVREN:
0: Disable LVR function (Default)
1: Enable LVR function

OP_LVRLEVEL:
0: 3.1V LVR Level1 (Default)
1: 4.3V LVR Level2

OP_SCM:
0: SCM is invalid in warm up period (default)
1: SCM is valid in warm up period

9. Instruction Set

ARITHMETIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ADD A, Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A, direct	Add direct byte to accumulator	0x25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data	Add immediate data to accumulator	0x24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data	Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	2	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	1	3
INC DPTR	Increment data pointer	0xA3	1	4
MUL AB 8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB 8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A	Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16	Long subroutine call	0x12	3	7
RET	Return from subroutine	0x22	1	8
RETI	Return from interrupt	0x32	1	8
AJMP addr11	Absolute jump	0x01-0xE1	2	4
LJMP addr16	Long jump	0x02	3	5
SJMP rel	Short jump (relative address)	0x80	2	4
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	6
JZ rel (not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel (not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel (not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel (not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit, rel (not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit, rel (not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel (not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A, direct, rel (not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A, #data, rel (not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn, #data, rel (not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel (not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn, rel (not taken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel (not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP	No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

10. Electrical Characteristics

Absolute Maximum Ratings

DC Supply Voltage. . . . .-0.3V to +6.0V

Input/Output Voltage. . . . . .GND-0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . . . -40℃ to +85℃

Flash Operating Temperature. . . . . .0℃ to +85℃

Storage Temperature. . . . . -55℃ to +125℃

Comments

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Operating Voltage	V_{DD}	3.0	5.0	5.5	V	f_{OSC} = 16.6MHz
Operating Current	I_{OP1}	-	4	8	mA	f_{OSC} = 16.6MHz, V_{DD} = 5.0V All output pins unload, all digital input pins un-floating CPU on (execute NOP instruction), LVR on, WDT on All other function block off
	I_{OP2}	-	35	80	μA	f_{OSC} = 128kHz, V_{DD} = 5.0V All output pins unload, All digital input pins un-floating CPU on (execute NOP instruction), LVR on, WDT on All other function block off
Stand by Current (IDLE)	I_{SB1}	-	2	5	mA	f_{OSC} = 16.6MHz, V_{DD} = 5.0V All output pins unload, All digital input pins un-floating CPU off (IDLE mode), LVR on, WDT on All other function block off
	I_{SB2}	-	20	40	μA	f_{OSC} = 128kHz, V_{DD} = 5.0V All output pins unload, All digital input pins un-floating CPU off (IDLE mode), LVR on, WDT on All other function block off
Stand by Current (Power-Down)	I_{SB3}	-	10	18	μA	f_{OSC} = 128kHz, V_{DD} = 5.0V All output pins unload, All digital input pins un-floating CPU off (Power-Down mode), LVR on, WDT on, Time3 on All other function block off
	I_{SB4}	-	5	10	μA	f_{OSC} off, V_{DD} = 5.0V All output pins unload, All digital input pins un-floating CPU off (Power-Down mode), LVR off, WDT off, Timer3 off All other function block off

(to be continued)

(continue)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
WDT Current	I_{WDT}	-	1	3	μA	V_{DD} = 5.0V, WDT on
Input Low Voltage1	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input High Voltage1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input Low Voltage2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{RESET}$, T0, T1, T2, INT0/1/2, T2EX, RXD (Schmitt trigger)
Input High Voltage2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{RESET}$, T0, T1, T2, INT0/1/2, T2EX, RXD (Schmitt trigger)
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN} = V_{DD} or GND
Pull-high Resistor	R_{PH}	-	30	-	kΩ	V_{DD} = 5.0V, V_{IN} = GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O port, I_{OH} = -10mA, V_{DD} = 5.0V
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O port, I_{OL} = 10mA, V_{DD} = 5.0V

Notes:

1. ∗: Data in "Typ." Column is at 5.0V, 25°C, unless otherwise specified.
2. Maximum value of the supply current from V_{DD} is 100mA.
3. Maximum value of the output current to GND is 150mA.

ADC Electrical Characteristics (V_{DD} =3.0 - 5.5V, V_{DDR} = 2.7V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Operating Voltage	V_{DDR}	-	2.7	-	V	
Resolution	N_R	-	16	-	bit	$0.4 \le V_{AIN} \le 1.6$
Reference Voltage	V_{REF}	0.1	-	1.2	V	
Common-mode input range	V_{AIN}	0.4	-	1.6	V	
Integral Nonlinearity	D_{LE}	-	±0.5	±1.0	LSB	0.1V < V_{REF} ≤ 0.6V, F_{AD} = 10Hz
Differential Nonlinearity	I_{LE}	-	±0.010	±0.015	%FS	0.1V < V_{REF} ≤ 0.6V, F_{AD} = 10Hz
A/D Conversion Current	I_{AD}	-	1	1.5	mA	ADC module on
ADC Clock	F_{ADCLK}	50	-	200	kHz	
ADC Conversion Rate	F_{AD}	-	10	50	Hz	

Programmable Gain Amplifier (PGA) Electrical Characteristics
(V_{DD} = 3.0 - 5.5V, V_{DDR} = 2.7V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Operating Voltage	V_{DDR}	-	2.7	-	V	
Input Offset Voltage1	V_{IO1}	-	±20	±50	uV	Chopper on
Input Offset Voltage2	V_{IO2}	-	±1	±2.5	mV	Chopper off
Common-mode Output range	V_{O_PGA}	0.4	-	1.6	V	
Common-mode Input Range	V_{ICR}	0.4	-	2.0	V	

Regulator Electrical Characteristics (V_{DD} = 3.0 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Operating Voltage	V_{DD}	3.0	-	5.5	V	
Output Voltage	V_{DDR}	2.6	2.7	2.8	V	I_{VDDR} = 0 - 15mA
Output Current	I_{DRV}	-	15	-	mA	
Supply Current	I_{SS}	-	50	100	uA	

AC Electrical Characteristics (V_{DD} = 3.0 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Oscillator start time	T_{OSC1}	-	1	2	ms	16MHz Crystal Oscillator
	T_{OSC2}	-	1	2	s	32.768 kHz Crystal Oscillator
RESET pulse width	t_{RESET}	10	-	-	μs	Low Active
RESET pin Pull-high Resistor	R_{RPH}	-	30	-	kΩ	V_{DD} = 3.0V, V_{IN} = GND
WDT RC Period	F_{WDT}	1	2	3	KHz	
High frequence RC	F_{RC1}	16.423	16.589	16.755	MHz	16.6MHz Internal RC Oscillator (V_{DD} = 3.0 - 5.5V, T_A = 25°C)
Low frequence RC	F_{RC2}	125.4	128	130.6	KHz	128KHz Internal RC Oscillator (V_{DD} = 3.0 - 5.5V, T_A = 25°C)

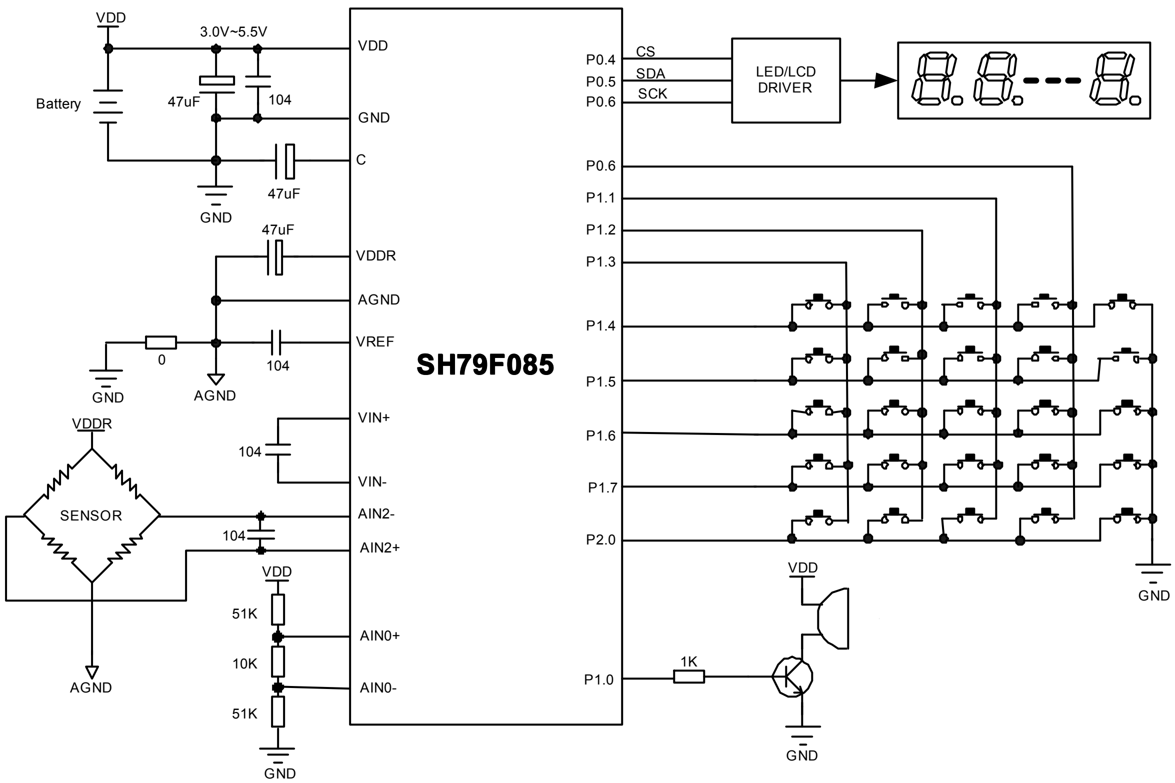
Low Voltage Reset Electrical Characteristics (V_{DD} = 3.0 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
LVR Voltage1	V_{LVR1}	3.0	3.1	3.2	V	LVR on V_{DD} = V_{LVR1} - 5.5V, f_{OSC} = 16.6MHz
LVR Voltage2	V_{LVR2}	4.2	4.3	4.4	V	LVR on V_{DD} = V_{LVR2} - 5.5V, f_{OSC} = 16.6MHz
Low LVR Voltage	T_{LVR}	-	30	-	μs	f_{OSC} = 16.6MHz

11. Application Circuit

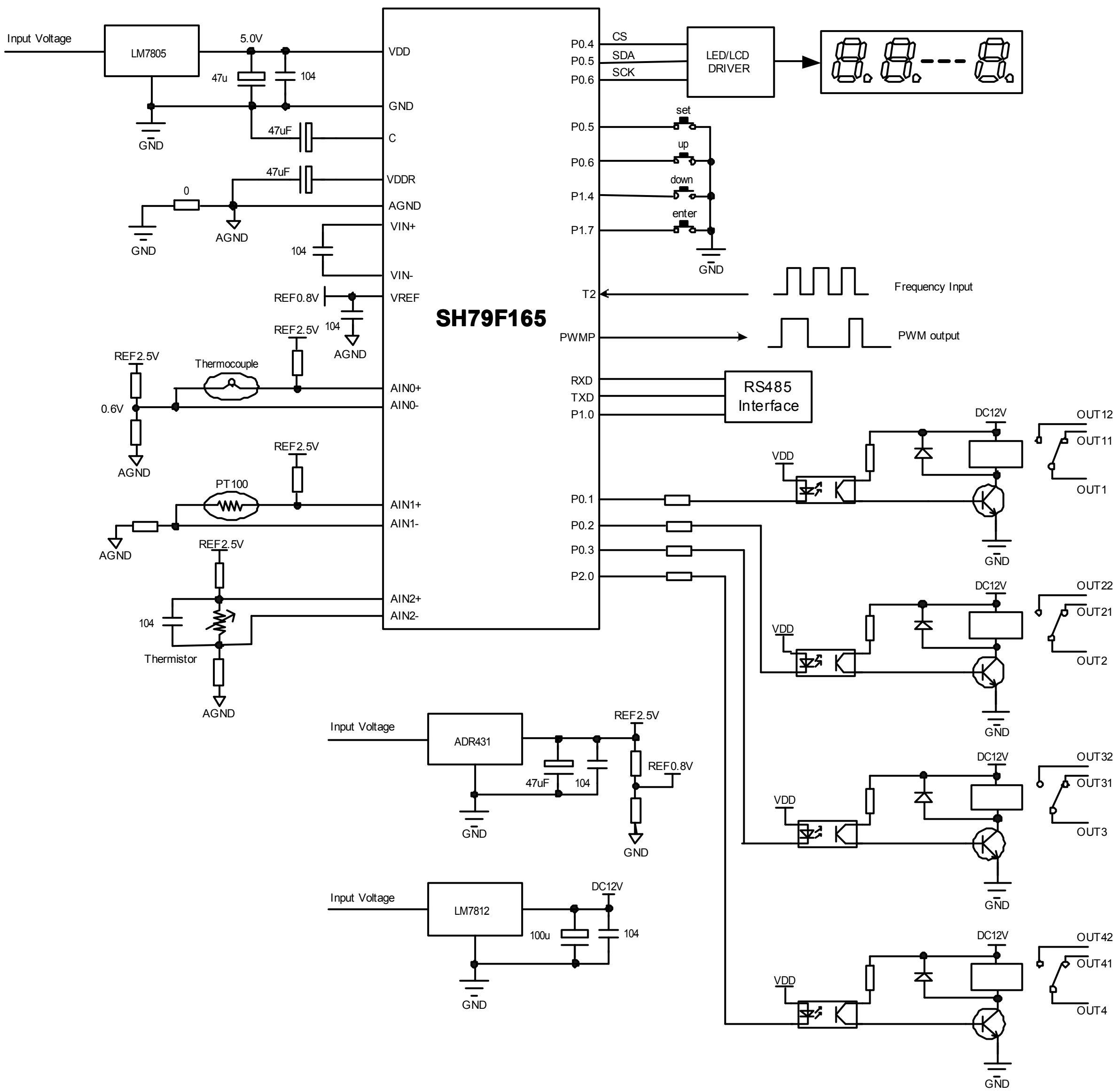
11.1 Electronic Weighing Scale

- VIN+/VIN-/VREF as ADC pin.
- SH79F085 built-in digital circuit regulator. It can output stable voltage of 1.8V for core and peripherals.
- SH79F085 built-in analog circuit regulator. It can output stable voltage of 2.7V for analog devices.
- SH79F085 built-in measure voltage of V_{DD} channel, An internal 80kΩ resistor will connect V_{DD} to GND to provide sample point. If SCH[2:0]≠100, this resistor will be disconnected.



11.2 Industry Temperature Controller

- VIN+/VIN-/VREF as ADC pin.
- SH79F165 built-in digital circuit regulator. It can output stable voltage of 1.8V for core and peripherals.
- SH79F165 built-in analog circuit regulator. It can output stable voltage of 2.7V for analog devices.
- SH79F165 built-in measure voltage of V_{DD} channel, An internal 80kΩ resistor will connect V_{DD} to GND to provide sample point. If SCH[2:0]≠100, this resistor will be disconnected.

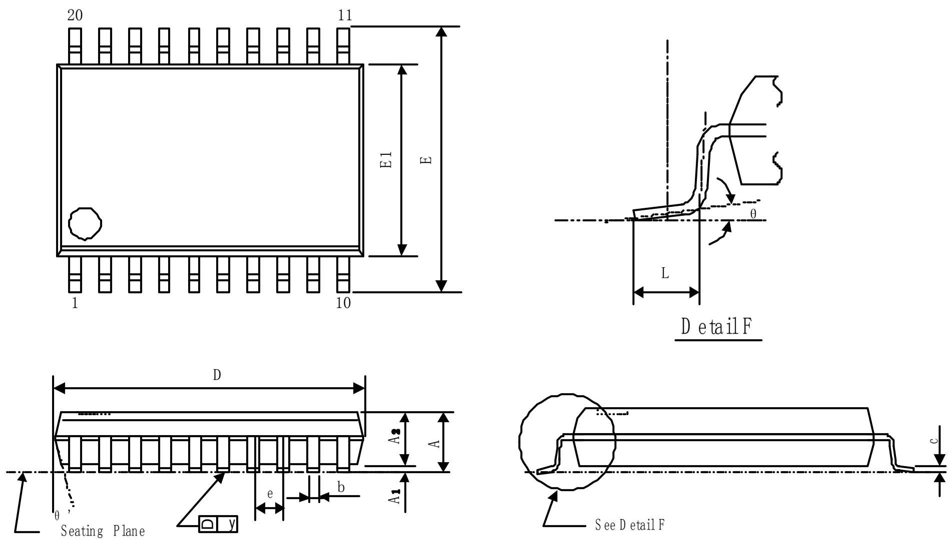


12. Ordering Information

Part No.	Package
SH79F085X/020XU	TSSOP20
SH79F085M/024MU	SOP24
SH79F165M/024MU	SOP24

13. Package Information

TSSOP (N.B.) 20L Outline Dimensions unit: inches/mm



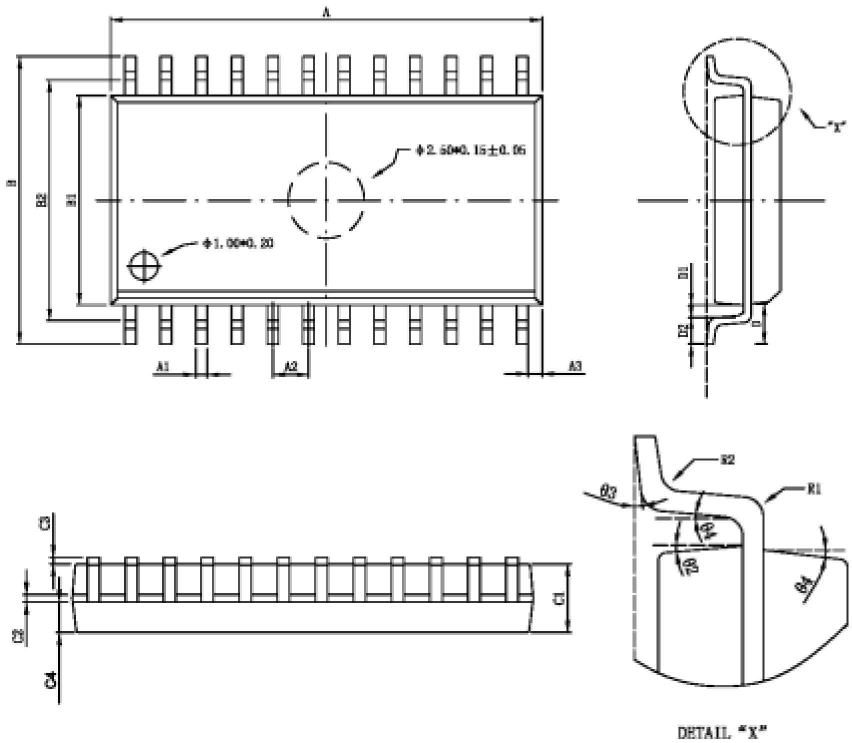
Symbol	Dimensions in inch			Dimensions in mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.048	---	---	1.20
A_1	0.002	---	0.006	0.05	---	0.15
A_2	0.031	0.039	0.041	0.80	1.00	1.05
b	0.007	---	0.012	0.19	---	0.30
C	0.004	---	0.008	0.09	---	0.20
D	0.252	0.256	0.260	6.40	6.50	6.60
E	---	0.252	---	---	6.40	---
E_1	0.169	0.173	0.177	4.30	4.40	4.50
e		0.026	---	---	0.65	---
L	0.018	0.024	0.030	0.45	0.60	0.75
y	---	---	0.004	---	---	0.10
θ	0°	---	8°	0°	---	8°
θ'	---	12°	---	---	12°	---

Notes:

1. Package body sizes exclude mold flash protrusions or gate burrs.
2. Tolerance±0.1mm unless otherwise specified.
3. Coplanarity: 0.1mm.
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

SOP (N.B.) 24L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inch		Dimension in mm	
	Min.	Max.	Min.	Max.
A	0.602	0.609	15.28	15.48
A1	0.016 Typ.		0.406 Typ.	
A2	0.050 Typ.		1.27 Typ.	
A3	0.020 Typ.		0.50 Typ.	
B	0.390	0.413	9.90	10.50
B1	0.292	0.30	7.42	7.62
B2	0.343 Typ.		8.7 Typ.	
C1	0.084	0.092	2.13	2.33
C2	0.008	0.013	0.204	0.33
C3	0.004	0.010	0.10	0.25
C4	0.034 Typ.		0.86 Typ.	
D	0.053 Typ.		1.34 Typ.	
D1	0.013 Typ.		0.33 Typ.	
D2	0.027	0.035	0.686	0.90
R1	0.010 Typ.		0.25 Typ.	
R2	0.010 Typ.		0.25 Typ.	
θ1	7° Typ.		7° Typ.	
θ2	7° Typ.		7° Typ.	
θ3	4° Typ.		4° Typ.	
θ4	10° Typ.		10° Typ.	

14. Product SPEC. Change Notice

Version	Content	Date
2.1	SH79F085 add SOP24 package SH79F165 cancle SOP28 package Modify clerical error Add the description about using High frequency oscillator	Jan. 2014
2.0	Original	Aug. 2011

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