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SINO WEALTH

SH79F329 Enhanced 8051 Microprocessor with Analog Front End

1. Features

8-bit MCU based on 8051 compatible pipeline instructions ÿ Flash ROM: 32K bytes ÿ RAM: internal 256 bytes, external 1024 bytes ÿ Operating voltage: VVPACK/VBAT = 4.5V - 25V

ÿ Oscillator: - Internal RC oscillator: 64KHz - Multiplied to 1MHz, 2MHz, 4MHz, 8MHz

ÿ 13 CMOS bidirectional I/O pins ÿ I/O built-in pull-up resistor ÿ 2 open-drain structure I/O pins ÿ 2 8-bit timers T0, T1 ÿ Interrupt sources: - Timer 0, Timer 1 - External interrupts INT1-2 - CADC, VADC, SMBus, SCI, AFE ÿ SMBus interface (master/slave mode) ÿ 2 16-bit ÿ-ÿ analog-to-digital converters (ADCs) - CADC: 1 differential input - VADC: 2 single-ended inputs

ÿ Built-in low voltage reset function LVR voltage: 2.3V (VDD) ÿ CPU machine cycle: 1 oscillation cycle

ÿ Watchdog Timer (WDT) (Code Option) ÿ Built-in oscillator warm-up counter ÿ High-voltage analog front end - Built-in 3V, 25mA power regulator (LDO) - 3 high-voltage output ports - Analog comparator with programmable threshold and delay time - 40mA maximum conduction circuit between VC1-VC5 Low power working mode: - Idle mode - Power down mode Flash type Package: TQFP48, TSSOP38

2. Overview

SH79F329 is a high-speed and high-efficiency 8051 compatible microcontroller. Under the same oscillation frequency, it has the characteristics of faster operation and better performance than the traditional 8051 chip.

SH79F329 retains most of the features of the standard 8051 chip, including built-in 256 bytes of RAM and two 8-bit timers and external interrupts INT1 and INT2. In addition, The SH79F329 also integrates 1024 bytes of RAM. The SH79F329 microcontroller also includes 32K bytes of Flash suitable for programs and data.

SH79F329 not only integrates the SMBus standard communication module, but also integrates two 16-bit ÿ-ÿ analog-to-digital converter modules (ADC) and an internal communication module (SCI). To achieve high reliability and low power consumption, the SH79F329 integrates a watchdog timer, has a low voltage reset function, and provides two low power saving modes.

The SH79F329 integrates a high-voltage analog front end (AFE), including 1 AFE interrupt, 1 power regulator, 3 high-voltage output ports that can be used for MOSFET control, 3 analog comparators, 4-way voltage differential input conversion and 4-way internal conduction circuits.

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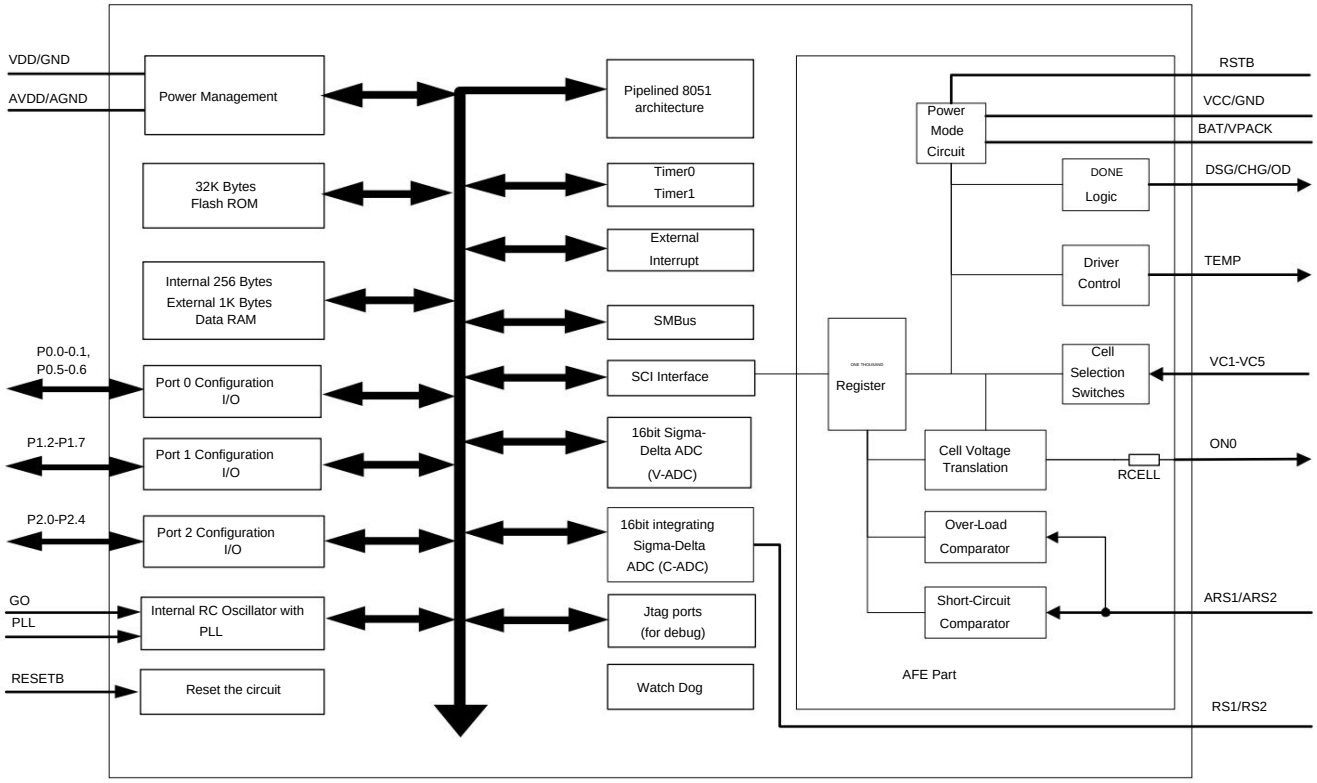
3. Block Diagram



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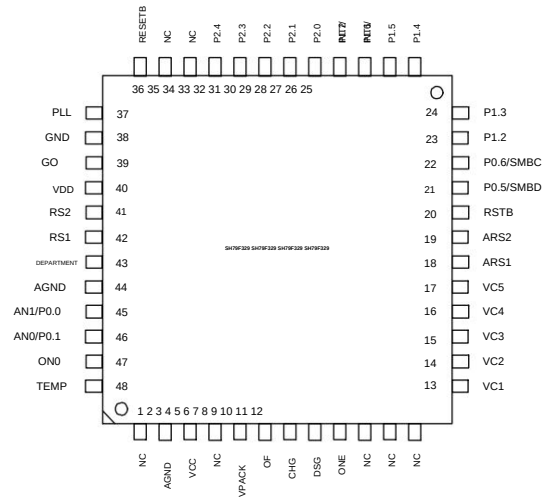
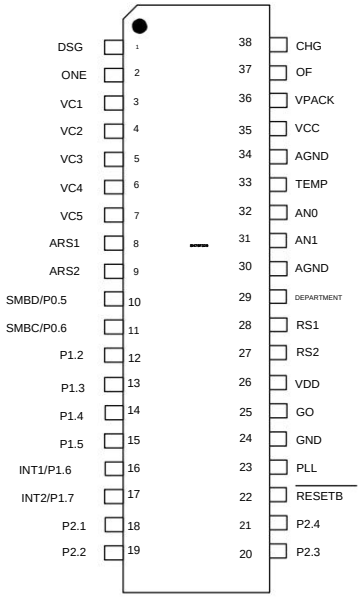
4. Pin configuration

TQFP48 (Total: 48 pins)



TQFP48 pin configuration diagram

TSSOP38 TSSOP38 TSSOP38 TSSOP38 (Total: 38 pins)



TSSOP38 TSSOP38 TSSOP38 TSSOP38 Pin Configuration Diagram

Notice:

In pin naming, the function written on the outermost side has the highest priority, and the function written on the innermost side has the lowest priority. When a pin is occupied by a high-priority function, it cannot be used as a pin for a low-priority function even if a low-priority function is allowed. Only when the software prohibits the high-priority function of the pin can the corresponding pin be released for use as a low-priority port.

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Table 4.1 TQFP48 pin functions

Pin number	Pin Name	Default function pin number	Pin Name	Default functionality
2	AGND	AGND	27	P1.6/INT1	P1.6
3	VCC	VCC	28	P1.7/INT2	P1.7
5	VPACK	VPACK	29	P2.0	P2.0
6	OF	OF	30	P2.1	P2.1
7	CHG	CHG	31	P2.2	P2.2
8	DSG	DSG	32	P2.3	P2.3
9	ONE	ONE	33	P2.4	P2.4
13	VC1	VC1	36	RESETB	RESETB
14	VC2	VC2	37	PLL	PLL
15	VC3	VC3	38	GND	GND
16	VC4	VC4	39	GO	GO
17	VC5	VC5	40	VDD	VDD
18	ARS1	ARS1	41	RS2	RS1
19	ARS2	ARS2	42	RS1	RS1
20	RSTB	RSTB	43	DEPARTMENT	DEPARTMENT
21	P0.5/SMBD	P0.5	44	AGND	AGND
22	P0.6/SMBC	P0.6	45	P0.0/AN1	P0.0
23	P1.2	P1.2	46	P0.1/AN0	P0.1
24	P1.3	P1.3	47	ON0	ON0
25	P1.4	P1.4	48	TEMP	TEMP
26	P1.5	P1.5	1,4,10-12, 34-35	NC	NC

Table 4.2 TSSOP38 TSSOP38 TSSOP38 TSSOP38 Pin Function

Pin number	Pin Name	Default function pin number	Pin Name	Default functionality
1	DSG	DSG	20	P2.2	P2.3
2	ONE	ONE	21	P2.3	P2.4
3	VC1	VC1	22	RESETB	RESETB
4	VC2	VC2	23	PLL	PLL
5	VC3	VC3	24	GND	GND
6	VC4	VC4	25	GO	GO
7	VC5	VC5	26	VDD	VDD
8	ARS1	ARS1	27	RS2	RS1
9	ARS2	ARS2	28	RS1	RS1
10	P0.5/SMBD	P0.5	29	DEPARTMENT	DEPARTMENT
11	P0.6/SMBC	P0.6	30	AGND	AGND
12	P1.2	P1.2	31	P0.0/AN1	P0.0
13	P1.3	P1.3	32	P0.1/AN0	P0.1
14	P1.4	P1.4	33	TEMP	TEMP
15	P1.5	P1.5	34	AGND	AGND
16	P1.6/INT1	P1.6	35	VCC	VCC
17	P1.7/INT2	P1.7	36	VPACK	VPACK
18	P2.1	P2.0	37	OF	OF
19	P2.2	P2.1	38	CHG	CHG

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5. Pin Description

Pin Number	type	illustrate
I/O Ports		
P0.0-P0.1, P0.5-P0.6 P1.2	I/O	4-bit bidirectional I/O port
- P1.7	I/O	6-bit bidirectional I/O port
P2.0 - P2.4	I/O	5-bit bidirectional I/O port
SMBus Port		
SMBD	I/O	SMBus communication data line
SMBC	I/O	SMBus communication clock line
ADC		
AN0	I	VADC single-ended input 0 pin
AN1	I	VADC single-ended input 1 pin
RS1	I	CADC differential input positive pin
RS2	I	CADC differential input negative pin
Interrupt/Reset/Power Port		
INT1	I	External interrupt 1 input pin
INT2	I	External interrupt 2 input pin
RESETB	I	Reset pin
GO	I	Internal oscillation circuit pin
PLL	I	frequency multiplication circuit pin
VDD	P	Digital power pin
GND	P	Digital ground pin
DEPARTMENT	P	Analog power pin
AGND	P	Analog ground pin
AFE Port		
VPACK	P	AFE power input pin
ONE	P	AFE power input pin
VCC	P	AFE power regulator output pin
AGND	P	AFE analog ground pin
CHG	O	AFE high voltage output pin
DSG	O	AFE high voltage output pin
OF	O	AFE high voltage open drain output pin
RSTB	O	AFE reset output, it is recommended to connect to RESETB
VC1	I	AFE voltage conversion highest input pin
VC2	I	AFE voltage conversion second high input pin
VC3	I	AFE voltage conversion third high input pin
VC4	I	AFE voltage conversion fourth high input pin
VC5	I	AFE voltage conversion lowest input pin
ON0	O	AFE voltage conversion output pin
TEMP	O	AFE output pin
ARS1	I	AFE comparator input pin
ARS2	I	AFE comparator input pin

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Continued from the table above

Pin Number	type	illustrate
Programmer		
TDOÿP1.2ÿ	O	Debug interface: test data output
TMSÿP1.3ÿ	I	debug interface: test mode selection
TDIÿP1.4ÿ	I	Debug interface: test data input
TCKÿP1.5ÿ	I	debug interface: test clock input
Notice: When P1.2-1.5 is used as a debugging interface, the original function of P1.2-1.5 is disabled.		

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6. SFR footage

SH79F329 has built-in 256 bytes of direct addressing registers, including general data memory and special function registers (SFR). The SFRs of SH79F329 are as follows :

CPU core registers: ACC, B, PSW, SP, DPL, DPH

CPU core enhanced registers: AUXC, DPL1, DPH1, INSCON, XPAGE

Power clock control register: PCON, SUSLO

Flash registers: IB_CLK0ÿIB_CLK1ÿIB_OFFSETÿIB_DATAÿIB_CON1ÿIB_CON2ÿIB_CON3ÿIB_CON4ÿ IB_CON5

Data Page Control Register: XPAGE

Watchdog Timer Register: RSTSTAT

System clock control register: CLKCON

Interrupt registers: IEN0ÿIEN1ÿIPH0ÿIPL0ÿIPH1ÿIPL1

I/O port registers: P0ÿP1ÿP2ÿP0CRÿP1CRÿP2CRÿP0PCRÿP1PCRÿP2PCRÿP2SELÿP0OS

Timer register: TCONÿBTCONÿBT0ÿBT1

SMBus Registers: SMBCONÿSMBSTAÿSMBDATÿSMBADR

SCI Registers: SCICON,SCIDAT,SCIADR

ADC Registers: ADCPÿOPDYÿVADCONÿVADC1ÿVADD0ÿCADCONÿCADC1ÿCADD0ÿCAD2ÿCAD1ÿ CAD0ÿDAD2ÿDAD1ÿDAD0ÿV0OR1ÿV0OR0ÿV0FSR1ÿV0FSR0ÿCOR1ÿCOR0ÿCFSR1ÿCFSR0

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Table 6.1 C51 core SFRs

Symbolic Address		name	POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
ACC	E0H	accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC F1H		C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW D0H		Program status word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data pointer low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
VAT	83H	Data pointer high byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data pointer 1 low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data pointer 1 high byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON 86H		Data pointer selection	----00-0	·	·	·	·	DIV	I have	·	DPS

Table 6.2 Power Clock Control SFRs

Symbolic Address		name	POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
PCON 87H		Power Control	----0000	·	·	·	·	GF1	GF0	PD	IDL
SUSLO 8EH		Power control protection word	00000000	SUSLO.7 SUSLO.6 SUSLO.5 SUSLO.4 SUSLO.3 SUSLO.2 SUSLO.1 SUSLO.0							

Table 6.3 Flash Control SFRs

Symbolic Address		name	POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
IB_CLK0 F9H		Flash Programming Clock Register 0	00000000	IB_CLK0.7 IB_CLK0.6 IB_CLK0.5 IB_CLK0.4 IB_CLK0.3 IB_CLK0.2 IB_CLK0.1 IB_CLK0.0							
IB_CLK1 FAH		Flash programming clock register 1	00000000	IB_CLK1.7 IB_CLK1.6 IB_CLK1.5 IB_CLK1.4 IB_CLK1.3 IB_CLK1.2 IB_CLK1.1 IB_CLK1.0							
IB_OFF SET	FBH	Programmable flash low byte offset	00000000	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
IB_DATA FCH		Programmable flash data register	00000000	IB_DATA.7 IB_DATA.6 IB_DATA.5 IB_DATA.4 IB_DATA.3 IB_DATA.2 IB_DATA.1 IB_DATA.0							
IB_CON1 F2H		Flash control register 1	00000000	IB_CON1.7 IB_CON1.6 IB_CON1.5 IB_CON1.4 IB_CON1.3 IB_CON1.2 IB_CON1.1 IB_CON1.0							
IB_CON2 F3H		flash control register 2	---00000	·	·	·	IB_CON2.4 IB_CON2.3 IB_CON2.2 IB_CON2.1 IB_CON2.0				
IB_CON3 F4H		flash control register 3	----0000	·	·	·	·	IB_CON3.3 IB_CON3.2 IB_CON3.1 IB_CON3.0			
IB_CON4 F5H		Flash control register 4	----0000	·	·	·	·	IB_CON4.3 IB_CON4.2 IB_CON4.1 IB_CON4.0			
IB_CON5 F6H		Flash control register 5	----0000	·	·	·	·	IB_CON5.3 IB_CON5.2 IB_CON5.1 IB_CON5.0			
XPAGE F7H		flash page register	00000000	XPAGE.7 XPAGE.6 XPAGE.5 XPAGE.4 XPAGE.3 XPAGE.2 XPAGE.1 XPAGE.0							

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Table 6.4 WDT SFR

Symbolic Address	name	POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
RSTSTAT B1H	Watchdog timer control register	*-***000	WDOF	·	PORF	LVRF	CLRF	WDT2	WDT.1	WDT.0

*Note: * indicates the reset value in the RSTSTAT register for different reset situations. For details, see the WDT section.*

Table 6.5 Clock Control SFR

Symbolic Address		name	POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
CLKCON B2H		System clock selection	----0000	·	·	·	·	PLLCON	FS2	FS1	FS0

Table 6.6 Interrupt SFRs

Symbolic Address		name	POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
IEN0 A8H		Interrupt Enable Control 0	00000000	EA	EVADC	ECADC	ESMB	ET1	EX1	ET0	EAFE
IEN1	A9H	Interrupt Enable Control 1	------00	·	·	·	·	·	·	YOU GO OUT	EX2
IPH0	B4H	Interrupt priority control high bit 0	-0000000	·	PVADCH PCADCH PSMBH			PT1H	PX1H	PT0H	PAFEH
IPL0	B8H	Interrupt priority control low bit 0	-0000000	·	PVADCL PCADCH PSMBL			PT1L	PX1L	PT0L	PAFEL
IPH1	B5H	Interrupt priority control high bit 1	------00	·	·	·	·	·	·	PSCIH	PX2H
IPL1	B9H	Interrupt priority control low bit 1	------00	·	·	·	·	·	·	PSCIL	PX2L

Table 6.7 Port SFRs

Symbolic Address		name	POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
P0	80H	8-bit port 0	-00---00	·	P0.6	P0.5	·	·	·	P0.1	P0.0
P1	90H	8-bit port 1	000000--	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	·	·
P2	AH	8-bit port 2	---00000	·	·	·	P2.4	P2.3	P2.2	P2.1	P2.0
P0CR E1H		Port 0 input/output direction control	-00---00	·	P0CR.6	P0CR.5	·	·	·	P0CR.1	P0CR.0
P1CR E2H		Port 1 input/output direction control	000000--	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	·	·
P2CR E3H		Port 2 input/output direction control	---00000	·	·	·	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P0PCR E9H		Port 0 internal pull-up enables	------00	·	·	·	·	·	·	P0PCR.1 P0PCR.0	
P1PCR EAH		Port 1 internal pull-up enables	000000--	P1PCR.7 P1PCR.6 P1PCR.5 P1PCR.4 P1PCR.3 P1PCR.2						·	·
P2PCR EBH		Port 2 internal pull-up allows	---00000	·	·	·	P2PCR.4 P2PCR.3 P2PCR.2 P2PCR.1 P2PCR.0				
P2SEL EEH		Port 2 output function selection	---00000	·	·	·	P2SEL.4	P2SEL.3 P2SEL.2		P2SEL.1	P2SEL.0
P0OS EFH		Port 0 output function selection	----0000	·	·	·	·	SDAP	CLKP	SMBDP SMBCP	

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Table 6.8 Timer SFRs

Symbolic Address		name	POR/WDTILVR POR/WDTILVR POR/WDTILVR POR/WDTILVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
TCON 88H		Timer Interrupt Control Register	00000000	IBT1	IBT0	IE2	IT2	IE1	IT1	AFEIF	AFEM
BTCON A2H		Timer Mode Register	00000000	ENBT1	BT1M.2	BT1M.1	BT1M.0	ENBT0	BT0M.2	BT0M.1	BT0M.0
BT1	A3H	Timer 1 Control Register	00000000	BT1.7	BT1.6	BT1.5	BT1.4	BT1.3	BT1.2	BT1.1	BT1.0
BT0	A4H	Timer 0 Control Register	00000000	BT0.7	BT0.6	BT0.5	BT0.4	BT0.3	BT0.2	BT0.1	BT0.0

Table 6.9 SMBus SFRs

Symbolic Address	name	POR/WDTILVR POR/WDTILVR POR/WDTILVR POR/WDTILVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
SMBCON C1H	SMBus Control Registers	00000000	ALL	ENSMB	STA	WHAT	AND	AA	TFREE	FREE
SMBSTA C2H	SMBus Status Register	11111000 SMBSTA.7 SMBSTA.6 SMBSTA.5 SMBSTA.4 SMBSTA.3						CR.1	CR.0	THIS IS IT
SMBADR C3H	SMBus Data Register	00000000	SLAVE.6	SLAVE.5	SLAVE.4	SLAVE.3	SLAVE.2	SLAVE.1	SLAVE.0	GC
SMRDAT C4H	SMBus Address Register	00000000 SMBDAT.7 SMBDAT.6 SMBDAT .5 SMBDAT.4 SMBDAT.3 SMBDAT.2 SMBDAT.1 SMBDAT.0								

Table 6.10 SCI SFRs

Symbolic Address	name	POR/WDTILVR POR/WDTILVR POR/WDTILVR POR/WDTILVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
SCICON C5H	SCI Control Register	00--0000	SCIEN	SCIF			SCIRW	SCISTA.2	SCISTA.1	SCISTA.0
SCIADR C6H	SCI Address Register	00000000	SCIA.6	SCIA.5	SCIA.4	SCIA.3	SCIA.2	SCIA.1	SCIA.0	Read/Write
SCIDAT C7H	SCI Data Register	00000000	SCID.7	SCID.6	SCID.5	SCID.4	SCID.3	SCID.2	SCID.1	SCID.0

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Table 6.11 ADC SFRs

Symbolic Address	name	POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
ADCP E7H	VADC Channel Configuration Register	------00	·	·	·	·	·	·	AN0P	AN1P
OPDY E6H	ADC clock delay control register	----0000	·	·	·	·	OPDY.3	OPDY.2	OPDY.1	OPDY.0
VADCON D9H	VADC Control Register	00000000	VADCEN VADCIF		SCH	VOF	VCE	VCR1	VCR0	NCH
VADC1 IS DONE	VADC High Byte Register	00000000	VADC.15 VADC.14 VADC.13 VADC.12 VADC.11 VADC.10 VADC.9 VADC.8							
VADC0 DBH	VADC Low Byte Register	00000000	VADC.7 VADC.6		GUIDE.5	GUIDE.4	GUIDE.3	GUIDE.2	GUIDE.1	DRIVER.0
CADCON DCH	CADC Control Register	000-0000	CADCEN CADCIF		MODE	·	COF	CCE	CCR1	CCR0
CADC1DDH	CADC High Byte Register	00000000	CADC.15 CADC.14 CADC.13 CADC.12 CADC.11 CADC.10 CADC.9							CADC.8
CADC0 DEH	CADC Low Byte Register	00000000	CADC.7	CADC.6	CADC.5	CADC.4	CADC.3 CADC.2		CADC.1	CADC.0
UAD2 D1H	CADC positive accumulation register high byte	----0000	·	·	·	·	UAD.19	UAD.18	UAD.17	UAD.16
UAD1	D2H CADC positive accumulation register second high byte 00000000		UAD.15	UAD.14	UAD.13	UAD.12	UAD.11	UAD.10	UAD.9	UAD.8
UAD0 D3H	CADC positive accumulation register low byte 00000000		UAD.7	UAD.6	UAD.5	UAD.4	UAD.3	UAD.2	UAD.1	UAD.0
DAD2 D4H	CADC negative accumulation register high byte	----0000	·	·	·	·	DAD.19	DAD.18	DAD.17	DAD.16
DAD1	D5H CADC negative accumulation register second high byte 00000000		DAD.15	DAD.14	DAD.13	DAD.12	DAD.11	DAD.10	DAD.9	DAD.8
DAD0 D6H	CADC negative accumulation register low byte 00000000		DAD.7	DAD.6	DAD.5	DAD.4	DAD.3	DAD.2	DAD.1	DAD.0
V0OR1 CDH	VADC offset register high byte	00000000	V0OR.15 V0OR.14 V0OR.13 V0OR.12 V0OR.11 V0OR.10						V0OR.9	V0OR.8
V0OR0 CEH	VADC offset register low byte	00000000	V0OR.7	V0OR.6	V0OR.5	V0OR.4	V0OR.3	V0OR.2	V0OR.1	V0OR.0
V0FSR1 CFH	VADC full scale calibration register high byte 00000000		V0FSR.15 V0FSR.14 V0FSR.13 V0FSR.12 V0FSR.11 V0FSR.10 V0FSR.9 V0FSR.8							
V0FSR0 D7H	VADC full scale calibration register low byte 00000000		V0FSR.7 V0FSR.6 V0FSR.5 V0FSR.4 V0FSR.3 V0FSR.2 V0FSR.1							V0FSR.0
COR1 BCH	CADC Offset Register High Byte	00000000	COR.15	COR.14	COR.13	COR.12	COR.11	COR.10	COR.9	COR.8
COR0 BDH	CADC Offset Register Low Byte	00000000	COR.7	COR.6	COR.5	COR.4	COR.3	COR.2	COR.1	COR.0
CFSR1 BEH	CADC full scale calibration register high byte 00000000		CFSR.15 CFSR.14 CFSR.13 CFSR.12 CFSR.11 CFSR.10						CFSR.9	CFSR.8
CFSR0 BFH	CADC full scale calibration register low byte 00000000		CFSR.7	CFSR.6	CFSR.5	CFSR.4	CFSR.3	CFSR.2	CFSR.1	CFSR.0

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Table 6.12 AFE Regs

Symbolic Address		name	POR/WDTILVR POR/WDTILVR POR/WDTILVR POR/WDTILVR /PIN reset value	No. 7	No. 6	No. 5	No. 4	No. 3	No. 2	No. 1	No. 0
STATED 00H		AFE Status Register	----0000	·	·	·	·	WDF	OL	SCCHG SCDSG	
AOUTPUT CTL	01H	AFE Output Control Register	-0000000	·	WDDIS	APD	AIDL	OF	CHG	DSG	LTCLR
AFUNCCTL 02H		AFE Function Control Register	--000000	·	·	TEMP	XSCD	XSCC	SCORE	PACKOUT VMEN	
ACELL_SEL 03H		AFE conversion and balance conduction register	00000000	CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0
AOLV 04H		AFE inverse comparator 2 voltage register	---00000	·	·	·	READ 4	OLV3	READ2	READ 1	OLV0
AOLT 05H		AFE reverse comparator 2 time register	----0000	·	·	·	·	OLT3	OLT2	OLT1	OLT0
ASCC 06H		AFE positive comparator 1 voltage and time register 00000000		SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
ASCD 07H		AFE reverse comparator 1 voltage and time register 00000000		SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0

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SFR video

	Bit addressable	Not bit addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H		IB_CLK0	IB_CLK1	IB_OFFSET	IB_DATA				FFH
F0H	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7H
E8H		P0PCR	P1PCR	P2PCR			P2SEL	P0OS	EFH
E0H	ACC	P0CR	P1CR	P2CR			OPDY	ADCP	E7H
D8H		VADCON	VADC1	VADC0	CADCON	CADC1	CAD0		DFH
D0H	PSW	UAD2	UAD1	UAD0	DAD2	DAD1	DAD0	V0FSR0	D7H
C8H						V0OR1	V0OR0	V0FSR1	CFH
COH		SMBCON	SMBSTA	SMBADR	SMBDAT	SCICON	SCIADR	SCIDAT	C7H
B8H	IPL0	IPL1			COR1	COR0	CFSR1	CFSR0	BFH
B0H		RSTSTAT	CLKCON		IPH0	IPH1			B7H
A8H	IEN0	IEN1							AFH
AH	P2		BTCON	BT1	BT0				A7H
98H									9FH
90H	P1								97H
88H	TCON						SUSLO		8FH
80H	P0	SP	DPL	VAT	DPL1	DPH1	INSCON	PCON	87H
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Note: Unused SFR addresses cannot be read or written.

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7. Standard Features

7.1 CPU

7.1.1 CPU Core Special Function Registers

characteristic

ÿ CPU core registers: ACC, B, PSW, SP, DPL, DPH

accumulator

The accumulator ACC is a commonly used special register, and A is used as the mnemonic of the accumulator in the instruction system.

B Register

In multiplication and division instructions, register B is used. In other instructions, register B can be used as a temporary register.

Stack Pointer (SP)

The stack pointer SP is an 8-bit special register. When executing PUSH, various subroutine calls, interrupt response and other instructions, SP first increases by 1 and then pushes the data onto the stack; when executing POP, When RET, RETI and other instructions are executed, SP is decremented by 1 after the data is removed from the stack. The top of the stack can be any address of the on-chip internal RAM (00H-FFH). After the system is reset, SP Initialized to 07H, the stack actually starts at address 08H.

Program Status Word (PSW) Register

The Program Status Word (PSW) register contains program status information.

Table 7.1 PSW Register

D0H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
PSW	C	AC	F0	RS1	RS0	OV	F1	P
Read/	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	read
write reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7	**C**	Carry flag 0: No carry or borrow occurs in an arithmetic or logical operation. 1: A carry or borrow occurs during an arithmetic or logical operation.
6	**AC**	Auxiliary carry flag 0: No auxiliary carry or borrow occurs in arithmetic logic operations. 1: During arithmetic logic operation, an auxiliary carry or borrow occurs
5	**F0**	F0 flag User-defined flags
4-3	RS[1:0] RS[1:0] RS[1:0] RS[1:0]	R0-R7 register page select bits 00: Page 0 (mapped to 00H-07H) 01: Page 1 (mapped to 08H-0FH) 10: Page 2 (mapped to 10H-17H) 11: Page 3 (mapped to 18H-1FH)
2	**OV**	Overflow flag 0: No overflow occurred 1: Overflow occurs
1	**F1**	F1 flag User-defined flags
0	**P**	Parity bit 0: The number of digits with the value 1 in accumulator A is even 1: The number of digits with the value 1 in accumulator A is an odd number

Data Pointer (DPTR)

The data pointer DPTR is a 16-bit special register. The high-order byte register is represented by DPH and the low-order byte register is represented by DPL. They can be used as a It can be processed as a 16-bit register DPTR or as two independent 8-bit registers DPH and DPL.

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7.1.2 CPU Enhanced Core Special Function Registers

ÿ Extended 'MUL' and 'DIV' instructions: 16 bits * 8 bits, 16 bits / 8 bits

ÿ Dual data pointer

ÿ CPU enhanced core registers: AUXC, DPL1, DPH1, INSCON

SH79F329 extends the 'MUL' and 'DIV' instructions and uses a new register - AUXC register to store the upper 8 bits of the operation data to achieve 16-bit operation.

The AUXC register is used in multiplication and division instructions. In other instructions, the AUXC register can be used as a temporary register.

The CPU enters standard mode after reset, and the 'MUL' and 'DIV' instruction operations are consistent with the standard 8051 instruction operations. When the corresponding bit of the INSCON register is 1, 'MUL'

And the 16-bit operation function of the 'DIV' instruction is turned on.

	operate		result		
			A	**B**	**AUXC**
I have	INSCON.2 = 0; 8-bit mode	(A)*(B)	low byte	high byte	...
	INSCON.2 = 1; 16-bit mode (AUXC A)*(B) low byte			middle byte	High Byte
DIV	INSCON.3 = 0; 8-bit mode	(A)/(B)	Quotient low byte	Remainder	...
	INSCON.3 = 1; 16-bit mode (AUXC A)/(B) quotient low byte			Remainder	Quotient high byte

Dual data pointer

Using dual data pointers can speed up data storage movement. The standard data pointer is named DPTR and the new data pointer is named DPTR1.

The data pointer DPTR1 is similar to DPTR and is a 16-bit dedicated register. Its high-order byte register is represented by DPH1 and its low-order byte register is represented by DPL1 .

They can be processed as a 16-bit register DPTR1 or as two independent 8-bit registers DPH1 and DPL1.

One of the two data pointers is selected by setting the DPS bit in the INSCON register to 1 or 0. All instructions related to reading or manipulating the DPTR will select the most recent data pointer.

The data pointer for the next selection.

7.1.3 Registers

Table 7.2 Data Pointer Selection Register

86H	**7th 6th 5th 4th**	**3rd 2nd 1st 0th**						
INSCON	.	.	.	.	DIV	I have	.	DPS
Read/Write	.	.	.	.	Read/Write	Read/Write	.	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	.	.	.	.	0	0	.	0

Bit number	Bit Notation	illustrate
3	**DIV**	16-bit/8-bit division selection bit 0: 8-bit division 1: 16-bit division
2	**I have**	16-bit/8-bit multiplication select bit 0: 8-bit multiplication 1: 16-bit multiplication
0	**DPS**	Data pointer select bit 0: Data pointer 1: Data pointer 1

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7.2 RAM

7.2.1 Features

SH79F329 provides internal RAM and external RAM for data storage. The following is the memory space allocation:

ÿ The lower 128 bytes of RAM (address from 00H to 7FH) can be addressed directly or indirectly

ÿ The upper 128 bytes of RAM (address from 80H to FFH) can only be addressed indirectly

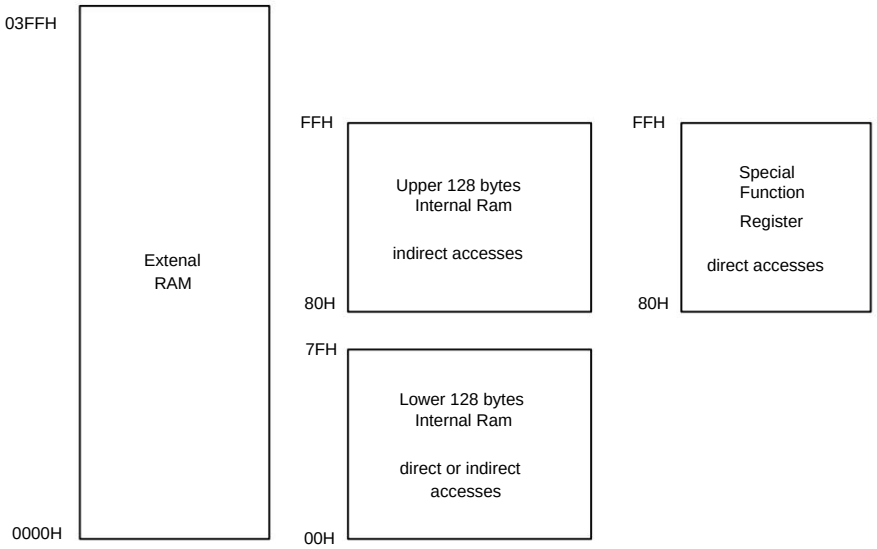
ÿ Special function registers (SFR, address from 80H to FFH) can only be directly addressed

ÿ External RAM bytes can be indirectly addressed via MOVX instructions

The upper 128 bytes of RAM occupy the same address space as the SFR, but are physically separated from the SFR space.

When the CPU is in the same position as the SFR, it can distinguish whether the high 128 bytes of data RAM or SFR is accessed according to the type of instruction being accessed.

Note: Unused SFR addresses are prohibited from reading and writing



Internal Configuration

SH79F329 supports the traditional method of accessing external RAM. Use MOVXA, @Ri or MOVX@Ri, A to access the external low 256 bytes RAM; use MOVX A, @DPTR or MOVX@DPTR, A to access external 1024 bytes of RAM.

Users can also use the XPAGE register to access external RAM, using the MOVX A, @Ri or MOVX @Ri, A instructions. XPAGE is used to represent a register higher than 256. byte RAM address.

In Flash SSP mode, XPAGE can also be used as a segment selector (see SSP chapter for details).

7.2.2 Registers

Table 7.3 Data Storage Page Register

F7H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
XPAGE	XPAGE.7 XPAGE.6 XPAGE.5 XPAGE.4 XPAGE.3 XPAGE.2 XPAGE.1 XPAGE.0							
Read/	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
write reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**XPAGE[7:0]**	RAM page select control bits When executing MOVX A, @Ri or MOVX@Ri, A, access beyond the range of 0-3FFH is invalid.

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7.3 Flash memory SH79F329

has a built-in 32K programmable Flash for storing program code and provides self-programming function.

Note: The last 64 bytes ($7FC0-$7FFF) are reserved and cannot be used as programmable memory.

In ICP (In-Circuit Programming) mode, the program can operate all Flash, such as erasing or writing. Flash read or write operations are in bytes, but erase can only be in sectors (2k) or overall erase. In ICP mode, the sector erase operation can erase any block except sector 15. In self-programming

mode (SSP), except for sector 15, all other sectors can be erased.

The erase code sectors cannot be erased either.

In ICP mode, you can also perform a global erase, which will erase the entire Flash memory (including sector 15).

7.3.1 Features ÿ

Programmable memory includes 16 x 2KB blocks, totaling 32KB ÿ Programming and erasing

operations can be performed within the operating voltage range ÿ ICP operation

supports write, read and erase operations ÿ Fast overall/sector erase and

programming ÿ Minimum program/erase times: 10,000

times ÿ Minimum data retention period: 10 years ÿ Low power

consumption **7.3.2 Flash operation in ICP mode**

ICP mode is the online programming mode, which means that programming can be done after the CPU is soldered on the user board. In ICP mode, the user system must be shut down before the programmer can refresh the Flash memory through the ICP programming interface. The ICP programming interface includes 6 wires (VDD, GND, TDO, TDI, TCK, TMS). First use 4 JTAG pins (TDO, TDI, TCK, TMS)

to enter the programming mode. Only when these 4 pins specify the waveform input, the CPU can enter the programming mode .

ICP mode supports the following

operations: **(1)** Code protection control mode programming

The code protection function of SH79F329 provides high-performance security protection for user code. Two modes are available for each partition: Code protection mode 0: Allow/

disable write/read operations by any programmer (excluding overall erase). Code protection mode 1: Allow/disable read operations through

MOVC instructions in other partitions, or erase/write operations through SSP functions. The user must set the corresponding protection bits using the Flash programmer to enter the desired protection mode.

(2) Mass Erase

Regardless of the status of the code protection control mode, the mass erase operation will erase all programmed code, code options, code protection bits, and custom ID code contents.

(The Flash programmer provides users with a custom ID code setting function to distinguish their products).

Mass erase can only be performed by a Flash programmer.

(3) Sector Erase

The sector erase operation will erase the contents of the selected sector except for sector 15. Both the user program and the Flash programming can perform this operation. If the

user program needs to perform this operation, the code protection control mode 1 of the selected sector must be disabled. If the

programmer needs to perform this operation, the code protection control mode 0 of the selected sector must be disabled.

Note: The last sector (sector 15) cannot perform the sector erase function.

(4) Write/read code

The read/write code operation can write customer data to the Flash programming memory or read data from the Flash memory. The programmer or the user program can perform this operation. If the user program needs

to perform this operation, the code protection control mode 1 of the selected sector must be disabled. Regardless of whether the security bit is set or not, the user program can read/write the sector where the program itself is located . If the

programmer needs to perform this operation, the code protection control mode 0 of the selected sector must be disabled.

Programming clock control register

Operation	**ICP**	**SSP**
Code Protection	support	Not supported
Sector Erase	Support (no security bit)	Support (no security bit)
Mass Erase	support	Not supported
Write/Read	Support (no security bit)	Supported (no security bit or native sectors)

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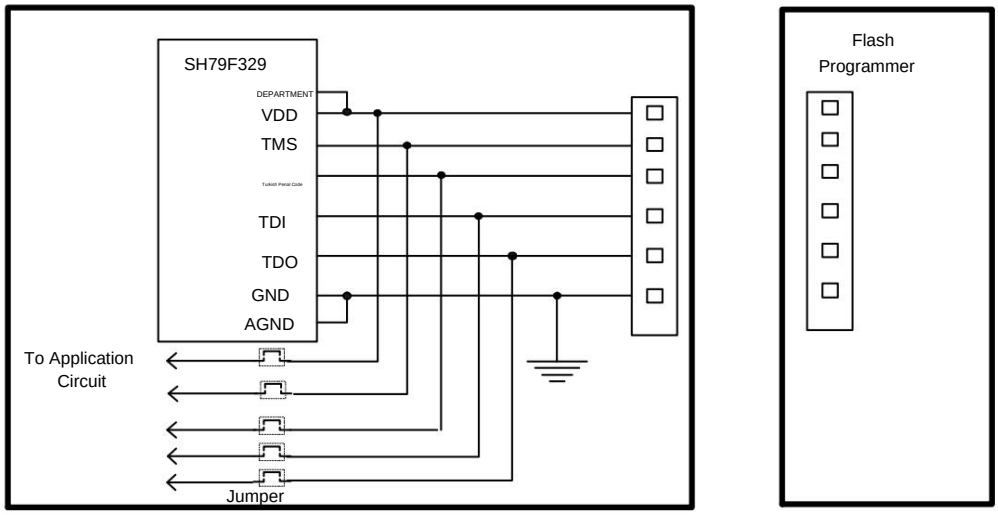
In ICP mode, all Flash operations can be completed through the 6-wire interface programmer. Because the programming signal is very sensitive, the user needs to use 5 jumpers to connect the programming pins (VDD, TDO, TDI, TCK, TMS) are separated from the application circuit. As shown in the figure below.



It is recommended to follow the following steps: (1) Before connecting the programming interface, you must disconnect the jumper and separate the programming pins from the application circuit before programming can begin. (2) After the programmer is connected to the programming interface, start programming. (3) After programming is completed, disconnect the programmer and connect the jumper.

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7.4 Sector Self-Programming (SSP) Function

SH79F329 provides SSP (Sector Self Programming) function, if the selected sector is not protected, user code can erase all sectors except sector 15 or any sector Execute the burn operation. Once the sector is burned, it cannot be burned again before the sector is erased.

SH79F329 has a built-in complex control flow to prevent the code from being modified by mistake. If the specified conditions (IB_CON2-5) are not met, the SSP will be terminated.

7.4.1 Registers

Table 7.4 Timing control register for programming

F9H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
IB_CLK0 IB_CLK0 IB_CLK0 IB_CLK0	IB_CLK0.7 IB_CLK0.6 IB_CLK0.5 IB_CLK0.4 IB_CLK0.3 IB_CLK0.2 IB_CLK0.1 IB_CLK0.0							
FAH	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
IB_CLK1 IB_CLK1	IB_CLK1.7 IB_CLK1.6 IB_CLK1.5 IB_CLK1.4 IB_CLK1.3 IB_CLK1.2 IB_CLK1.1 IB_CLK1.0							
IB_CLK1	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
IB_CLK1 **read/write** reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	IB_CLKx[7-0] IB_CLKx[7-0] IB_CLKx[7-0] IB_CLKx[7-0] IB_CLKx[7-0] **x = 0, 1**	Flash programming clock selection The values in B_CLK1:IB_CLK0 are calculated as follows. programming: 65536 $\frac{T_{prog}}{8 \times T_{sysck}}$ 20 *us* ÿ T_{prog} ÿ 40 *us* *Fsys* ÿ 1 *MHz* 65536ÿ $\frac{T_{prog}}{T_{sysck}}$ 20 ÿs T_{prog} ÿ 40 *us* *Fsys* ÿ 1 *MHz* Typical value Tprog = 30us Sector Erase: 65536 $\frac{T_{erase}}{8 \times T_{sysck}}$ 50 *ms* ÿ T_{erase} ÿ 90 *ms* *Fsys* ÿ 1 *MHz* 65536 ÿ $\frac{T_{erase}}{T_{sysck}}$ 50 ÿs T_{erase} ÿ 90 *ms* *Fsys* <1 *MHz* Typical value Terase = 60ms Note: When using sector erase, the system clock must be less than or equal to 8MHz. If the oscillator frequency is greater than 8MHz, the user must use system clock division to ensure that the system clock is less than or equal to 8MHz

fSYS	***Programming Programming Programming Programming***	***Erase***
8M	*FFE2H*	*15A0H*
4M	*FFF1H*	*8AD0H*
2M	*FFF8H*	*C568H*
1M	*FFFBH*	*E2B4H*
32K	*FFFFH*	*F880H*

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Table 7.5 Programming offset register

F7H	7th 6th 5th 4th 3rd 2nd 1st 0th							
XPAGE	XPAGE.7 XPAGE.6 XPAGE.5 XPAGE.4 XPAGE.3 XPAGE.2 XPAGE.1 XPAGE.0							
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-3	**XPAGE[7:3]** The sector number of the memory cell being programmed, 00000 represents sector 0	
2-0	**XPAGE[2:0]** The upper 3 bits of the memory cell to be programmed	

Table 7.6 Flash memory offset register for programming

FBH	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_OFFSET IB_OFFSET IB_OFFSET IB_OFFSET	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
Read/	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
write reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**IB_OFFSET[7 IB_OFFSET[7 IB_OFFSET[7 IB_OFFSET[7:0]** The lower 8 bits of the memory cell to be programmed	

Table 7.7 Data registers for programming

FCH	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_DATA IB_DATA IB_DATA	IB_DATA.7 IB_DATA.6 IB_DATA.5 IB_DATA.4 IB_DATA.3 IB_DATA.2 IB_DATA.1 IB_DATA.0							
IB_DATA read/write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**IB_DATA[7 IB_DATA[7 IB_DATA[7 IB_DATA[7:0]** programming data	

Table 7.8 SSP type selection register

F2H	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_CON1 IB_CON1	IB_CON1.7 IB_CON1.6 IB_CON1.5 IB_CON1.4 IB_CON1.3 IB_CON1.2 IB_CON1.1 IB_CON1.0							
IB_CON1	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
IB_CON1 read/write reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	IB_CON1[7 IB_CON1[7 IB_CON1[7 IB_CON1[7:0]	SSP Operation Selection 0xE6: Sector Erase 0x6E: Burn storage unit

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Table 7.9 SSP flow control register 1

F3H	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_CON2 IB_CON2 IB_CON2	.	.	.	IB_CON2.4 IB_CON2.3 IB_CON2.2 IB_CON2.1 IB_CON2.0				
IB_CON2 Read/Write	.	.	.	Read/Write	Read/Write Read/Write Read/Write			Read/Write
Reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	.	.	.	0	0	0	0	0

Bit number	Bit Notation	illustrate
4	IB_CON2.4 IB_CON2.4 IB_CON2.4 IB_CON2.4	System clock selection 0ÿfSYS > 1MHz 1ÿfSYS < 1MHz
3-0	**IB_CON2[3 IB_CON2[3 IB_CON2[3 IB_CON2[3 IB_CON2[3:0]** must be 05H, otherwise the Flash programming will terminate.	

Table 7.10 SSP flow control register 2

F4H	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_CON3 IB_CON3 IB_CON3	.	.	.	.	IB_CON3.3 IB_CON3.2 IB_CON3.1 IB_CON3.0			
IB_CON3 Read/Write	.	.	.	.	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	.	.	.	.	0	0	0	0

Bit number	Bit Notation	illustrate
3-0	**IB_CON3[3 IB_CON3[3 IB_CON3[3 IB_CON3[3 IB_CON3[3:0]** must be 0AH, otherwise the Flash programming will terminate.	

Table 7.11 SSP flow control register 3

F5H	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_CON4 IB_CON4 IB_CON4	.	.	.	.	IB_CON4.3 IB_CON4.2 IB_CON4.1 IB_CON4.0			
IB_CON4 Read/Write	.	.	.	.	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	.	.	.	.	0	0	0	0

Bit number	Bit Notation	illustrate
3-0	**IB_CON4[3:0]** must be 09H, otherwise Flash programming will terminate.	

Table 7.12 SSP flow control register 4

F6H	7th 6th 5th 4th 3rd 2nd 1st 0th							
IB_CON5 IB_CON5 IB_CON5	.	.	.	.	IB_CON5.3 IB_CON5.2 IB_CON5.1 IB_CON5.0			
IB_CON5 Read/Write	.	.	.	.	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	.	.	.	.	0	0	0	0

Bit number	Bit Notation	illustrate
3-0	**IB_CON5[3:0]** must be 06H, otherwise Flash programming will terminate.	

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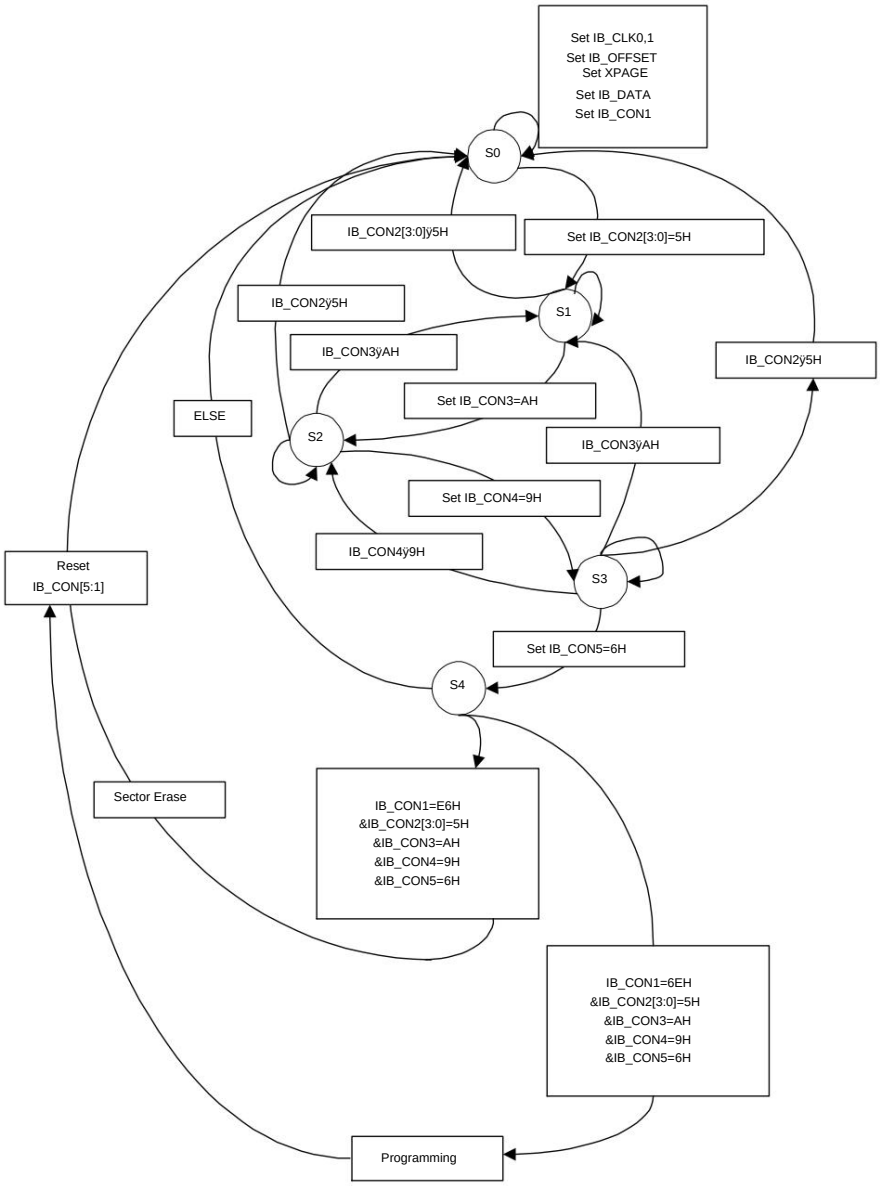
7.4.2 Flash Control Flowchart



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7.4.3 Notes on SSP Programming

To ensure that SSP programming is completed successfully, the user software must be set up according to the following steps: **(1)** Burning: 1. Disable interrupts; 2. Set IB_CLK1, IB_CLK0; 3. Set XPAGE, IB_OFFSET according to the corresponding sector number to be programmed; 4. Set IB_DATA according to programming requirements; 5. Set IB_CON1-5 in sequence 6. Add 4 NOP instructions; 7. Start burning, the CPU will enter IDLE mode; automatically exit IDLE mode after burning is completed; 8. If you need to continue writing data, jump to step 3; 9. Clear XPAGE; 10. Restore interrupt and system frequency division settings. **(2)** Erase: 1. Disable interrupts; 2. Set IB_CLK1, IB_CLK0; 3. Set XPAGE according to the corresponding sectors; 4. Set IB_CON1-5 in order; 5. Add 4 NOP instructions; 6. Start erasing, the CPU will enter IDLE mode; automatically exit IDLE mode after erasing is completed; 7. If more sectors need to be erased, jump to step 3 to continue; 8. Clear XPAGE; 9. Restore interrupts and system frequency division settings. **(3)** Read: Use "MOVC A, @A + DPTR" or "MOVC A, @A + PC" to read.

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7.5 System Clock and Oscillator

7.5.1 Features

ÿ Built-in 64KHz RC oscillator

ÿ Built-in system clock X128 multiplier

ÿ Built-in 1/1, 1/2, 1/4, 1/8 divider

7.5.2 Overview

SH79F329 uses an internal 64KHz RC oscillator, providing a x128 multiplier and 1/1, 1/2, 1/4, 1/8 dividers. There are 32.768kHz, 1048kHz, 2097kHz, 4194kHz, 8338kHz five frequencies as system clock options.

7.5.3 Registers

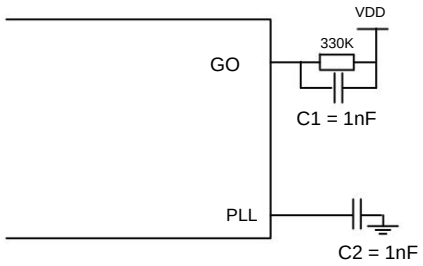
Table 7.13 System clock control register

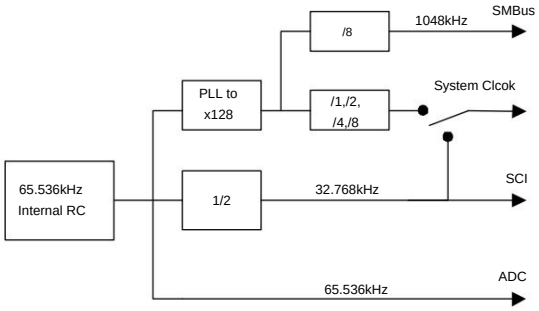
B2H	7th 6th 5th 4th 3rd 2nd 1st 0th							
CLKCON	.	.	.	.	PLLCON	FS2	FS1	FS0
Read/Write	.	.	.	.	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	.	.	.	.	0	0	0	0

Bit number	Bit Notation	illustrate
3	**PLLCON**	System clock frequency multiplier 0: Disable the internal clock multiplier 1: Enable the internal clock multiplier
2-0	FS[2:0] FS[2:0] FS[2:0] FS[2:0]	System clock control register 0xx: Select 32.768kHz as the system clock 100: Select 1048kHz as the system clock 101: Select 2097kHz as the system clock 110: Select 4194kHz as the system clock 111: Select 8338kHz as the system clock

7.5.4 Oscillator Types

Internal 64KHz RC oscillator and system frequency division circuit





7.5.5 System Clock Selection

When selecting the multiplier clock, follow the steps below to set

1. Set FS[1:0] to the desired frequency
2. Set PLLCON
3. Wait for no less than 2ms
4. Set FS2

7.5.6 AFE Communication Clock

When CLKP in register P0OS is set to 1, an internal 32.768kHz clock is provided to the AFE and is not affected by the internal system clock.

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7.6 I/O Ports

7.6.1 Features

- ÿ 13 bidirectional I/O ports
- ÿ 2 bidirectional open-drain I/O ports
- ÿ I/O ports can be shared with other functions

SH79F329 provides 15-bit programmable bidirectional I/O ports. The port data is in register Px. The port control register (PxCRy) controls whether the port is used as input or Output. Each I/O port has an internal pull-up resistor controlled by PxPCRy (x = 0-2, y = 0-7) when the port is used as an input .

Some I/O pins of the SH79F329 can be shared with selected functions. When all functions are enabled, there is a priority in the CPU to avoid function conflicts. (See Port Sharing for details.) Sharing chapter).

7.6.2 Registers

Table 7.14 Port Control Register

E1H - E3H	**7th**	**6th**	**5th**	**4th**	**3rd**	**2nd**	**1st**	**0th**
P0CR (E1H)	·	·	P0CR.6	P0CR.5	·	·	P0CR.1	P0CR.0
P1CR (E2H)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	·	·
P2CR (E3H)	·	·	·	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**PxCRy** **x = 0-2, y = 0-7**	Port input/output control register 0: Input mode 1: Output mode

Special note: Unused bits must remain at 0

Table 7.15 Port pull-up resistor control register

E9H - EBH	**7th**	**6th**	**5th**	**4th**	**3rd**	**2nd**	**1st**	**0th**
P0PCR (E9H)	·	·	·	·	·	·	P0PCR.1	P0PCR.0
P1PCR (EAH)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	·	·
P2PCR (EBH) read/	·	·	·	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (ENG/WDT/LVR (ENG/WD/T/LVR (ENG/WD/T/LVR (ENG/WD/T/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**PxPCRy** **x = 0-2, y = 0-7**	Internal pull-up resistor control for input ports 0: Internal pull-up resistor is disabled 1: Internal pull-up resistor is on

Special note: unused bits must remain 1

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Table 7.16 Port Data Register

80H, 90H, A0H	7th 6th 5th 4th 3rd 2nd 1st 0th							
P0 (80H)	·	P0.6	P0.5	·	·	·	P0.1	P0.0
P1 (90H)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	·	·
P2 (A0H)	·	·	·	P2.4	P2.3	P2.2	P2.1	P2.0
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit symbol	illustrate
7-0	Px.y x = 0-2, y = 0-7	Port Data Register

Special note: Unused bits must remain at 0

Table 7.17 Port multiplexing selection register

B2H	7th 6th 5th 4th 3rd 2nd 1st 0th							
P0OS	·	·	·	·	SDAP	CLKP SMBDP SMBCP		
Read/Write	·	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	·	·	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
3	SDAP	AFE communication data line multiplexing control bit 0: Close the AFE communication data line 1: Open the AFE communication data line
2	CLKP	AFE communication clock line multiplexing control bit 0: Disable the AFE communication clock line 1: Enable the AFE communication clock line
1	SMBDP	P0.5 multiplexing control bit 0: P0.5 is used as a normal open-drain IO 1: P0.5 is used as SMBus communication data line
0	SMBCP	P0.6 multiplexing control bit 0: P0.6 is used as a normal open-drain IO 1: P0.6 is used as the SMBus communication clock line

Table 7.18 Port 2 driver enhancement register

B2H	7th 6th 5th 4th 3rd 2nd 1st 0th							
P2SEL	·	·	·	P2SEL.4 P2SEL.3 P2SEL.2 P2SEL.1 P2SEL.0				
Read/Write	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	·	·	·	0	0	0	0	0

Bit number	Bit Notation	illustrate
4-0	P2SEL[4:0] P2SEL[4:0] P2SEL[4:0] P2SEL[4:0]	Port 2 Driver Enhancement Register 0: Used as normal IO 1: A 250 ohm resistor is connected in series internally, providing a maximum pull-down capability of 4mA

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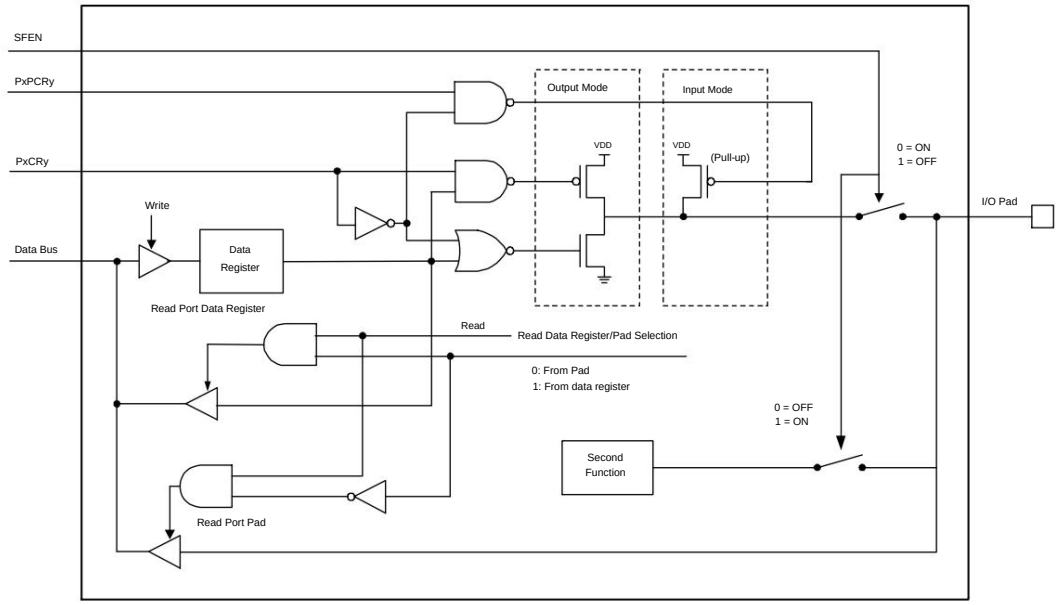
7.6.3 Port Module Diagram



Notice:

(1) The input port read operation directly reads the pin level.

(2) There are two input sources for output port read operations: one is to read from the port data register, and the other is to read the pin level directly. Use the read instruction to distinguish between read-modify-Write instructions read registers, while other instructions read pin levels.

(3) Regardless of whether the port is shared for other functions, write operations to the port are all for the port data register.

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7.6.4 Port Sharing

The 6 bidirectional I/O ports can also be shared as a second special function. The sharing priority follows the rule of highest external and lowest internal:

In the pinout diagram, the outermost pin has the highest priority, and the innermost pin has the lowest priority.

The priority function (if enabled) cannot be used as a lower priority function, even if the lower priority function is enabled. Only the higher priority function is enabled by hardware or software.

After the device is turned off, the corresponding pin can be used for lower priority functions. Pull-up resistors are also controlled by the same rules.

When the port is allowed to be reused for other functions, the user can modify PxCR and PxPCR (x = 0-2), but these operations will not be effective until the other reused functions are disabled. Affects the port status.

When the port is allowed to be multiplexed for other functions, any read and write operations on the port will only affect the value of the data register, and the port pin value remains unchanged until the multiplexed other functions are reset. It is functionally disabled.

PORT0:

- AN1 (P0.0): VADC channel 1 input
- AN0 (P0.1): VADC channel 0 input
- SMBD (P0.5): SMBus communication data line
- SMBC (P0.6): SMBus communication clock line

Table 7.19 PORT0 shared function list

Pin number priority function			Enable bit
45	1	AN1 VADC channel 1 input	
	2	P0.0 None of the above	
46	1	AN0 VADC channel 0 input	
	2	P0.1 None of the above	
21	1	SMBD SMBus communication data cable	
	2	P0.5 None of the above	
22	1	SMBC SMBus communication clock line	
	2	P0.6 None of the above	

PORT1:

- INT1 (P1.6): External interrupt 1 input
- INT2 (P1.7): External interrupt 2 input

Table 7.20 PORT1 shared function list

Pin number priority function			Enable bit
27	1	INT1 Set the EX1 bit in the IEN0 register to 1, and P1.6 to input mode	
	2	P1.6 None of the above	
28	1	INT2 Set the EX2 bit in the IEN0 register to 1, and P1.7 to input mode	
	2	P1.7 None of the above	

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7.7 Interruptions

7.7.1 Features

ÿ 9 interrupt sources

ÿ 4-level interrupt priority

SH79F329 has 9 interrupt sources: 2 external interrupts (INT1, INT2), 2 timer interrupts (Timer 0, 1), 1 SMBus interrupt, 2 ADC interrupts, 1 SCI interrupt, 1 AFE interrupt.

7.7.2 Interrupt Enable

Any interrupt source can be enabled or disabled individually by setting the corresponding bit in registers IEN0 and IEN1 to 1 or clearing it to 0. The IEN0 register also contains a full The local enable bit EA is the master switch for all interrupts. Generally, after reset, all interrupt enable bits are set to 0 and all interrupts are disabled.

7.7.3 Registers

Table 7.21 Primary Interrupt Enable Register

A8H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
IEN0	EA	EVADC ECADC ESMB			ET1	EX1	ET0	EAFE
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

v

Bit number	Bit Notation	illustrate
7	**EA**	All interrupt enable bits 0: Disable all interrupts 1: Enable all interrupts
6	**EVADC**	VADC interrupt enable bit 0: Disable VADC interrupt 1: Enable VADC interrupt
5	**ECADC**	CADC interrupt enable bit 0: Disable CADC interrupt 1: Enable CADC interrupt
4	**ESMB**	SMBus Interrupt Enable bit 0: Disable SMBus interrupt 1: Enable SMBus interrupt
3	**ET1**	Timer 1 overflow interrupt enable bit 0: Disable timer 1 overflow interrupt 1: Enable timer 1 overflow interrupt
2	**EX1**	**External interrupt 1 enable bit** 0: Disable external interrupt 1 1: Enable external interrupt 1
1	**ET0**	Timer 0 overflow interrupt enable bit 0: Disable timer 0 overflow interrupt 1: Enable timer 0 overflow interrupt
0	**EAFE**	AFE interrupt enable bit 0: Disable AFE interruption 1: Enable AFE interrupt

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Table 7.22 Secondary interrupt enable register

A9H	7th 6th 5th 4th 3rd 2nd 1st 0th							
IEN1	.	.	.	.	.	.	YOU GO OUT	EX2
Read/Write	.	.	.	.	.	.	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	.	.	.	.	.	.	0	0

Bit number	Bit Notation	illustrate
1	YOU GO OUT	SCI interrupt enable bit 0: Disable SCI interrupt 1: Enable SCI interrupt
0	**EX2**	**External interrupt 2 enable bit** 0: Disable external interrupt 2 1: Enable external interrupt 2

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7.7.4 Interrupt Flag

Each interrupt source has its own interrupt flag. When an interrupt occurs, the hardware will set the corresponding flag bit, and the interrupt flag bit will be listed in the interrupt summary table.

When an external interrupt source generates an external interrupt IN Tx (x = 1/2), if the interrupt is edge-triggered, the CPU responds to the interrupt and the interrupt flag bits (IE1/2 of the TCON register) are set to bit) is cleared to 0 by hardware; if the interrupt is low-level triggered, the external interrupt source pin level directly controls the interrupt flag instead of being controlled by on-chip hardware.

Note: When external interrupts are disabled and the pins are not multiplexed for other functions, the external interrupt flag will change with the interrupt pin status.

When the counter of timer 0/1 overflows, the interrupt flag position TFx (x = 0, 1) of the TCON register is set to 1, generating a timer 0/1 interrupt. After the CPU responds to the interrupt, the flag

The flag is automatically cleared to 0 by hardware.

The AFEIF interrupt in the TCON register can be set to edge trigger or level trigger. If it is edge triggered, AFEIF is cleared by hardware after the CPU responds to the interrupt.
The interrupt cannot be cleared until the AFE status returns to normal.

An SMBus interrupt is generated when SI, TFREE, and TOUT in the SMBCON register are set to 1. The interrupt flag must be cleared by software.

When VADCIF in the VADCON register is set to 1, a VADC interrupt is generated. If an interrupt occurs, the result in VADC1/VADC0 is valid.

The flag must be cleared by software.

When CADCIF in the CADCON register is set to 1, a CADC interrupt is generated. If an interrupt is generated, CADC1/CADC0, UAD2/UAD1/UAD0,
The result of DAD2/DAD1/DAD0 is valid. The CADCIF interrupt flag must be cleared by software.

An SCI interrupt is generated when the SCIF bit in the SCICON register is set to 1. The interrupt flag must be cleared by software.

Table 7.23 Timer Control Register (x = 0, 1)

88H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
TCON	IBT1	IBT0	IE2	IT2	IE1	IT1	AFEIF	AFEM
Read/	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
write reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7, 6	**IBTx** **(x = 0, 1)**	Timer x overflow flag 0: Timer x has no overflow and can be cleared to 0 by software 1: Timer x overflows, set to 1 by hardware
5, 3	**Ex** **(x = 1, 2)**	External interrupt x request flag 0: Suspend without interruption 1: External interrupt pending
4, 2	**ITx** **(x = 1, 2)**	External interrupt x trigger mode bit 0: Low level trigger 1: Falling edge trigger
1	**AFEIF**	AFE interrupt trigger flag 0: No AFE interrupt 1: Trigger AFE interrupt
0	**AFEM**	AFE trigger mode bits 0: Continuous trigger mode 1: Single trigger mode

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7.7.5 Interrupt Vector

When an interrupt occurs, the contents of the program counter are pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The address of the interrupt vector is detailed in the interrupt summary table.

List in detail.

7.7.6 Interrupt Priority

Each interrupt source can be individually set to one of the four interrupt priority levels by clearing or setting the corresponding bits in IPL0, IPH0, IPL1, and IPH1.

The advanced service program is described as follows:

When responding to an interrupt service routine, you can respond to an interrupt with a higher priority, but you cannot respond to another interrupt with the same or lower priority.

When responding to the highest-level interrupt service routine, no other interrupts will be responded to. If interrupt sources with different interrupt priorities request interrupts at the same time, the one with the higher priority will be responded to.

Discontinue application.

If interrupt sources of the same priority level request interrupts at the same time at the beginning of an instruction cycle, the internal query sequence determines the interrupt request response order.

Interrupt Priority		
Priority		Interrupt Priority
IPHx	**IPLx**	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.24 Interrupt priority control register

B8H, B4H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
IPL0	·	PVADCL PCADCL	PSMBL PT1L			PX1L	PT0L	PAFEL
IPH0	·	PVADCH PCADCH	PSMBH PT1H			PX1H	PT0H	PAFEH
Read/Write	·	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	·	0	0	0	0	0	0	0
B9H,B5H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
IPL1	·	·	·	·	·	·	PSCIL	PX2L
IPH1	·	·	·	·	·	·	PSCIH	PX2H
Read/Write	·	·	·	·	·	·	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	·	·			·	·	0	0

Bit number	Bit Notation	illustrate
7-0	**PxxxL/H PxxxL/H PxxxL/H PxxxL/H** Corresponding interrupt source xxx priority selection	

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7.7.7 Interrupt Processing

The interrupt flags are sampled in every machine cycle. All interrupts are sampled on the rising edge of the clock. If a flag is set, the CPU captures the interrupt flag.
The interrupt system calls a long branch instruction (LCALL) to call its interrupt service routine, but the LCALL generated by the hardware can be blocked by any of the following conditions:

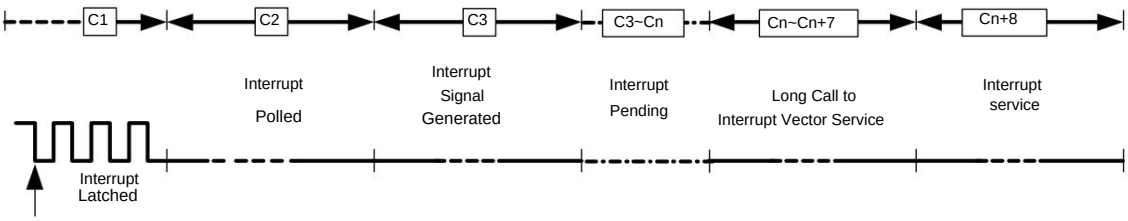
An interrupt of the same or higher priority is in progress. The current cycle

is not the last cycle of the instruction being executed. In other words, no interrupt request can be responded to before the instruction being executed is completed. The instruction being executed is a RETI or an

instruction that accesses the special register IEN0\1 or IPL\H. In other words, after RETI or reading or writing IEN0\1 or IPL\H, the interrupt request will not be responded to immediately, but will be responded to after at least one other instruction is executed.

Note: Because changing the priority usually requires 2 instructions, during this period, it is recommended to turn off the corresponding interrupt to avoid interrupts during the priority modification process. If the interrupt flag is no longer valid when the module status changes, the interrupt will not be responded to. Each polling cycle only queries the valid interrupt request.

The polling cycle/LCALL sequence is shown in the following figure:



Interrupt response time

The LCALL generated by the hardware pushes the contents of the program counter into the stack (but does not save the PSW), and then stores the vector address of the corresponding interrupt source (refer to the interrupt vector table) into the program counter. The interrupt

service program starts from the specified address and ends with the RETI instruction. The RETI instruction notifies the processor that the interrupt service program has ended, and then pops the top two bytes of the stack and reloads them into the program counter. After executing the interrupt service program, the program returns to where it stopped. The RET instruction can also return to the original address to continue execution, but the interrupt priority control system still considers an interrupt of the same priority to be responded to. In this case, interrupts of the same priority or lower priority will not be responded to.

7.7.8 Interrupt Response Time If an

interrupt is detected, the request flag for this interrupt will be set in each machine cycle after it is detected. The internal circuit will maintain this value until the next machine cycle, and the CPU will generate an interrupt in the third machine cycle. If the response is valid and conditions permit, the hardware LCALL instruction will call the service routine for the requested interrupt when the next instruction is executed, otherwise the interrupt is suspended. The LCALL instruction calls the routine in 7 machine cycles. Therefore, it takes at least 3+7 complete machine cycles from the external interrupt request to the start of the interrupt routine execution.

When a request is blocked due to the three conditions mentioned above, the interrupt response time will be longer. If an interrupt of the same or higher priority is executing, the additional waiting time depends on
The length of the interrupt service routine being executed.

If the instruction being executed has not reached the last cycle, if the RETI instruction is being executed, it takes 8 cycles to complete the RETI instruction being executed, plus the maximum time of 20 machine cycles required to complete the next instruction (if the instruction is a DIV or MUL instruction with a 16-bit operand). If there is only one interrupt source in the system, plus 7 machine cycles for the LCALL call instruction, the longest response time is 2+8+20+7 machine cycles. Therefore, the interrupt response time is generally greater than 10 machine cycles and less than 37 machine cycles.

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7.7.9 External interrupt input

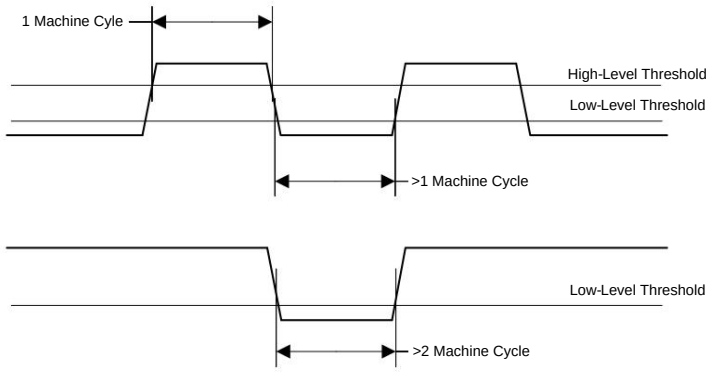
SH79F329 has 2 external interrupt inputs. External interrupt 1-2 has an independent interrupt source. External interrupt 1/2 can be set by setting IT2, IT1 in TCON register.
When ITx = 0 (x = 1, 2), the external interrupt INTx (x = 1, 2) pin is low level triggered; when ITx (x = 1, 2) = 1,
The external interrupt INTx (x = 1, 2) is edge triggered. In this mode, the INTx (x = 1, 2) pin is continuously sampled as high level in one cycle and low level in the next cycle.
The interrupt request flag of the TCON register is set to 1, and an interrupt request is issued. Since the external interrupt pin is sampled once per machine cycle, the input high or low level should be
Maintain at least 1 machine cycle to ensure that it can be sampled correctly.

If the external interrupt is triggered by a falling edge, the external interrupt source should keep the interrupt pin at a high level for at least 1 machine cycle and then keep it at a low level for at least 1 machine cycle.
This ensures that the edge can be detected to set IEx to 1. When the interrupt service routine is called, the CPU automatically clears IEx to 0.

If the external interrupt is triggered by a low level, the external interrupt source must keep the request valid until the requested interrupt is generated. This process requires 2 system clock cycles.
If the interrupt service is completed and the external interrupt is still maintained, the next interrupt will be generated. When the interrupt is level-triggered, it is not necessary to clear the interrupt flag IEx (x = 1, 2).
Because the interrupt is only related to the input port level.

When SH79F329 enters idle or power-down mode, the interrupt will wake up the processor to continue working. See the Power Management section for details.

Note: The interrupt flags of external interrupts 1-2 are automatically cleared to 0 by hardware when the interrupt service routine is executed.



External interrupt detection

7.7.10 Interrupt Summary

Interrupt Sources	Vector Address	Enable bit	Flags	Polling priority
Reset	0000H	·	·	0 (highest level)
ONE THOUSAND	0003H	EAFE	AFEIF	2
Timer0	000BH	ET0	IBT0	3
INT1	0013H	EX1	IE1	4
Timer1	001BH	ET1	IBT1	5
SMBus	0023H	ESMB	YES, ALL, TFREE	6
C-ADC	002BH	ECADC	CADCIF	7
V-ADC	0033H	EVADC	VADCIF	8
INT2	003BH	EX2	IE2	9
SCI	0043H	YOU GO OUT	SCIF	10

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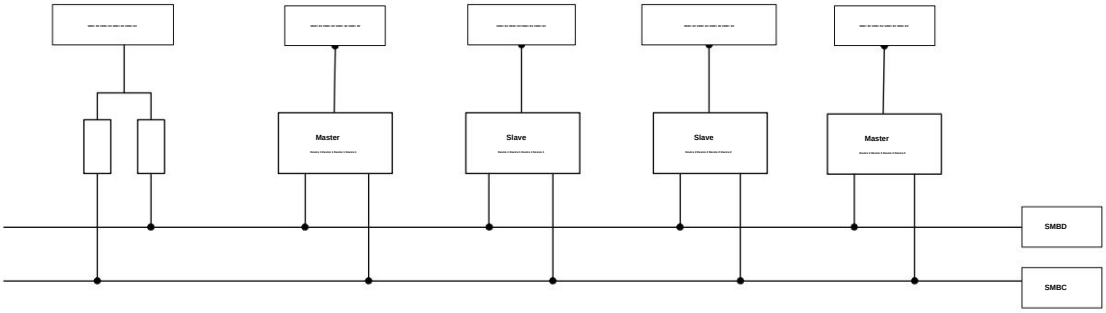
8. Enhanced Functionality

8.1 SMBus Serial Communication Interface

The SMBus serial bus uses two wires (SMBD and SMBC) to transfer information between the bus and the device. SH79F329 fully complies with the SMBus bus specification and automatically Process the bytes transferred and keep track of the serial communication.

Typical SMBus communication is shown in the figure below, which supports up to 128 different devices to communicate.



8.1.1 Features

ÿ Two-line mode, simple and fast

Communication level is not limited by VDD and will not affect VDD ÿ Supports master

mode (Master) and slave mode (Slave)

ÿ Allows sending data (Transmitter) and receiving data (Receiver)

ÿ Support arbitration function for multi-host communication

ÿ With low-level bus timeout judgment (Timeout)

ÿ System can be woken up in idle mode

ÿ Address programmable

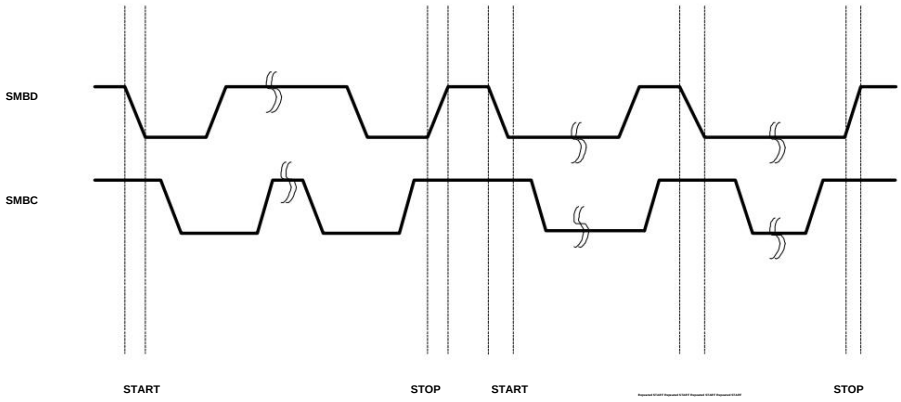
8.1.2 Data transmission format

Data transmission format

Each bit of data transmission on the data line requires a pulse on the clock line. The data line should remain stable when the clock is high. However, the start condition and the end condition are This rule does not need to be followed when conditions are met.

Similar to the I2C communication protocol, SMBus defines two special waveforms: start condition and stop condition. The falling edge of the data line when the clock line is high is defined as the start condition. The rising edge of the data line when the clock line is high is defined as the end condition. Both the start condition and the end condition are sent by the host. After sending the start condition, the The bus is in the "busy" state. The bus returns to "idle" after the termination condition or the data line and clock line remain at high level for more than 50us.

The host can initiate and terminate a transfer. When the host sends a start condition, a transfer begins, and when it sends a stop condition, the current transfer ends. The bus is defined as "busy" between the start condition and the stop condition. Other hosts should not try to initiate a transfer. In the "busy" state, if the host sends a start condition again, The condition is defined as a "repeated start condition", indicating that the host wants to start a new transmission without giving up the bus. After sending the repeated start condition, the bus is still in Since the nature of the repeated start condition and the start condition are exactly the same, this article will use the start condition unless otherwise stated. to replace both.



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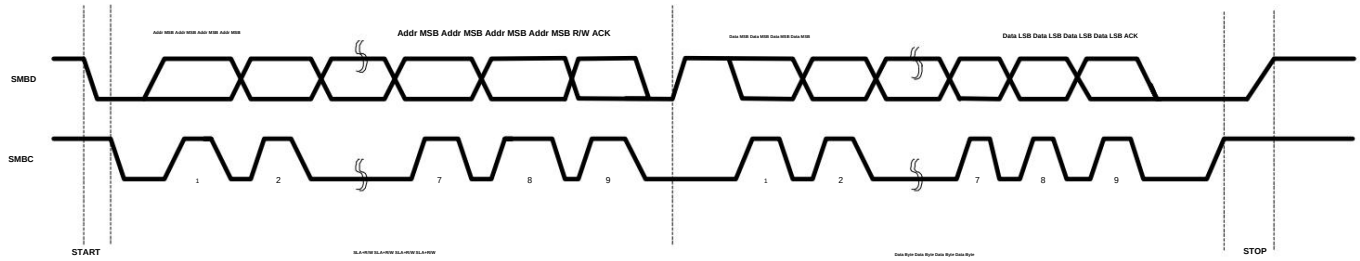
All data packets (including address packets) consist of 9 bits, including 1 byte and an acknowledge bit. The host is responsible for sending the clock and the start and end conditions, and the receiver is responsible for
The receiver sends an "acknowledge" signal by pulling the data line low at the ninth clock pulse; or maintaining a high level at the ninth pulse indicates "no response".
When the receiver receives the last byte or cannot continue to receive data for some reason, it should respond with a "no response" signal. The SMBus uses a high-to-low
The transmission is performed bit by bit.

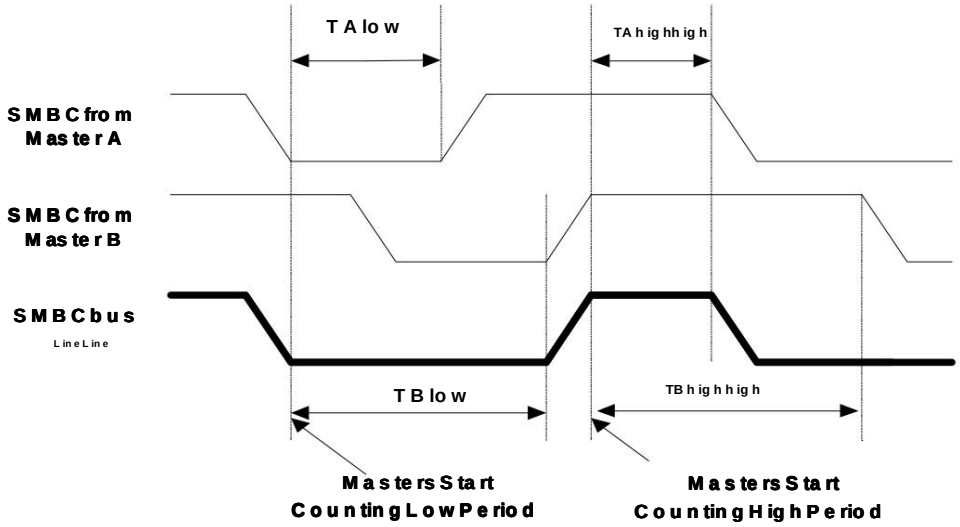
A transfer usually includes a start condition, address + read/write, one or more data packets and a stop condition. The data format that only contains the start condition and the stop condition
It is not in accordance with the communication rules. It is worth noting that the "wired AND" structure provides convenience for the handshake signal between the host and the slave.
When it is doing business, the slave can extend the low level time of the clock line by pulling down the clock line, thereby reducing the communication frequency. The slave can extend the low level period of the clock line but will not
Affects the high level period of the clock line.



Clock synchronization

When multiple hosts want to control the bus at the same time, the bus will determine the high and low levels of the clock line based on the "wired AND" principle.
It is very important to know the start of each clock pulse.

The high-to-low transition of the clock line level will cause all devices involved in the transmission to start low-level timing. Each device releases the clock when the timing reaches its own low-level requirement.
The clock line enters a high level waiting period before the clock line becomes high level; when all devices count the full low level period, the clock line becomes high level. After that, all devices start
The high level is timed, and the first device to count the full high level period will pull the clock line low and enter the next clock cycle.



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The data

arbitration master can only start a transfer when the bus is in the "idle" state. Two or more masters may send a start signal at the same time within the minimum hold time (tHOLD:STA).
condition so that only one start condition is seen on the bus.

Since the host sending the start condition cannot know whether there are other hosts competing for the bus, it can only rely on arbitration of the data line when the clock is high to determine which host occupies the total bus. When a host transmits a low level, the host transmitting a high level will lose arbitration and must give up the bus.

The master that loses arbitration will continue to send clocks until the current transmission byte is sent. When two masters access a slave at the same time, the address stage may be successfully passed.
This mechanism requires all SMBus devices to detect the true state of the data line when transmitting data.

If the host has also turned on the slave mode, it should check whether the address on the line matches its own after losing arbitration during the address sending phase; if it is an access to itself, it should immediately switch to the slave mode to receive information.

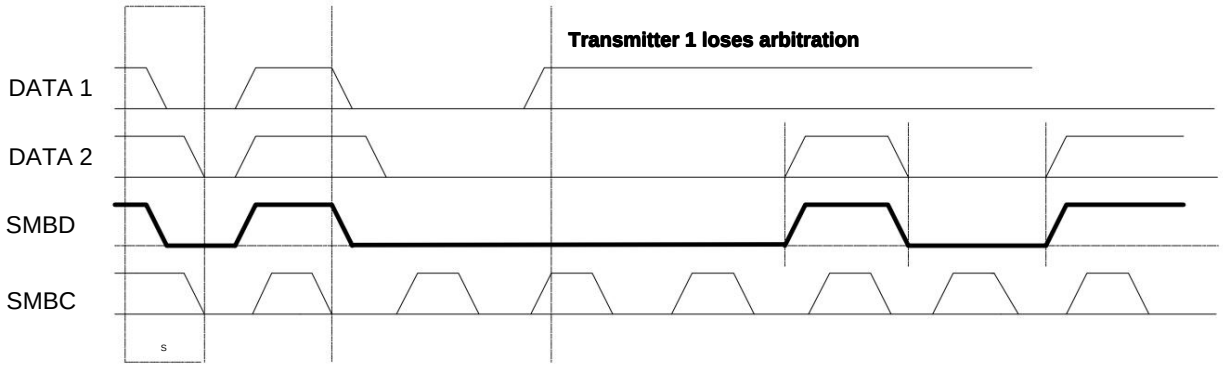
During each transmission, the "repeated start condition" on the line must still be detected. When a "repeated start condition" that is not issued by itself is detected, the current transmission should be exited immediately.

Arbitration will not occur in the following

situations: 1. Repeated start condition

and data 2. Stop condition and

data 3. Repeated start condition and stop condition



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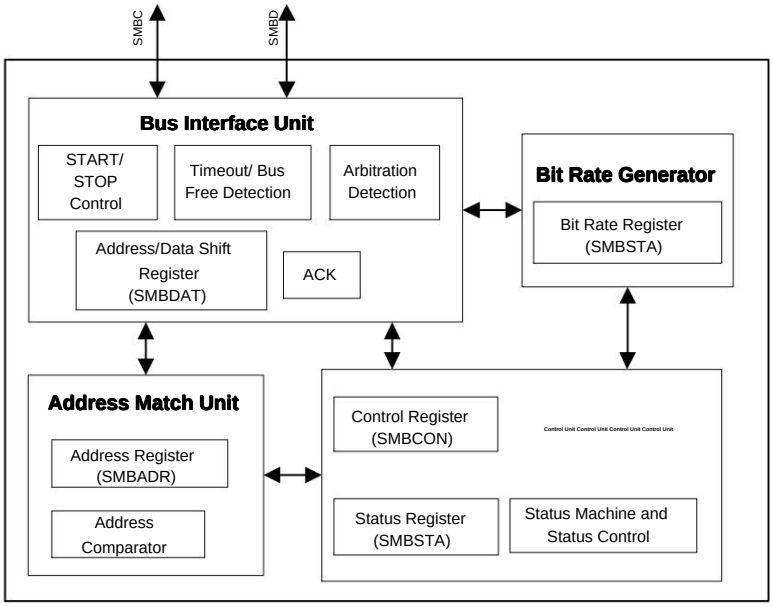
8.1.3 Functional Description

The figure below describes the detailed structure of the SMBus communication module.



The bus interface unit

consists of a data and address shift register (SMBDAT), a start/stop condition controller, an arbitration and bus timeout detection unit. The SMBDAT register stores the data or

address to be sent and the data and address received. The start/stop condition controller is responsible for sending

and detecting start conditions, repeated start conditions and stop conditions on the bus. If the SH79F329 has started a transmission as a host,

the arbitration unit will always detect whether an arbitration has occurred. When arbitration is lost, the control unit can make appropriate

action and generate the corresponding status code.

SH79F329 stipulates that the bus is in "idle" state when it maintains a high level for more than 50us. TFREE in register SMBCON will be set (if the control bit EFREE is set). If the clock line is pulled low by the slave, the

communication will be temporarily suspended; and the host has no way to pull the clock line high. To solve this problem, the SMBus protocol stipulates that the slaves involved in the transmission

All devices define "bus timeout" when the clock line is low for more than 25ms. The software should reset the SMBus module within 10ms to release the bus. In the host mode, the

frequency generation

unit can set the communication frequency through the CR[1:0] of the SMBCON register. There are three communication frequencies: 16KHz, 32KHz, and 64KHz.

Address Matching Unit

The address matching unit checks whether the received address matches the 7-bit address in register SMBADR. If the general address enable bit GC is set, it will also check whether it matches the general address 00H. When the address matches, the control unit will take appropriate actions and generate corresponding status codes. Control unit The control unit

monitors the

SMBus bus and responds accordingly according to the settings of the control register SMBCON. When there is an event on the SMBus bus that requires the attention of the application layer , the SMBus interrupt flag is set. The status code indicating the current event will be written to the status register SMBSTA. The status register SMBSTA only indicates the communication status information when the SMBus communication interrupt occurs; in other cases, the status register contains a status code used to indicate that there is no valid status code. The clock line will remain at a low level until the interrupt is cleared. The application software can allow SMBus communication to continue after completing the task.

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8.1.4 Transfer Mode

SMBus communication is a byte-based and interrupt-driven communication bus. All bus events such as receiving a byte or sending a start condition will generate an interrupt. So during the byte transfer, the application software can perform other operations. It should be noted that the SMBus enable bit ENSMB in the control register SMBCON and all interrupt control bits EA and SMBus interrupt control bits ESMB in the interrupt control register IE0 will jointly determine whether an interrupt will be generated when the SMBus interrupt flag SI is set. If ESMB or EA is not set, the application software must enumerate the SI flag to know whether an SMBus event has occurred.

When the SI bit is set, it indicates that an SMBus transfer has been completed and is waiting for a response from the application software. The status register SMBSTA contains the current status. Application software

The registers SMBCON and SMBSTA can be used to determine which type of

communication is performed on the SMBus. The following will introduce the four main modes of SMBus communication and describe all possible

status codes. The following

abbreviations are used in the figure

below: S: Start condition Rs:

Repeated start condition R:

Read control

bit W: Write control bit:

Acknowledge bit A ÿ: No acknowledge bit DATA: 8-bit data

P: Termination condition SLA: Slave

address The circle is used to indicate

that the interrupt flag has been set. The number represents the status code of the current status register SMBSTA with the lower three bits masked. Before SI is cleared, SMBus communication will be suspended and the application software must decide whether to continue communication or terminate the current transmission. For each status code, the required software action and subsequent transmission details are described.

Host sending mode

In the master transmission mode, a series of data is sent to the slave. To enter the master transmission mode, a start condition is followed by a slave address + write control word (SLA+W).

The address packet indicates entry into the host transmit mode (MT).

By setting ENSMB and STA in the control register SMBCON, clearing STO and SI, the SMBus logic will detect the SMBus bus and issue a start condition (STA) when allowed. When the start condition (STA) is transmitted, the communication interrupt (SI) is set, the status register (SMBSTA) is 08H, and the interrupt service routine should write the slave address and write control word (SLA+W) to the data register SMBDAT. Clear the SI flag before starting the next transmission.

When the slave address and write control word are transmitted and an "acknowledge" bit is received, the interrupt (SI) is set and there are several possible states in the status register SMBSTA: 18H, 20H and 38H for the host mode and 68H, 78H and B0H for the slave mode.

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Host sends mode status code

Status Code	The **SMBus** bus and Hardware interface status	Application software response						The next action performed by **SMBus**
		Read/write data register **SMBDAT**	**THIS**	**IS**	**THIS**	**YES**	**AA**	
08H	Start condition sent	Write SLA+W	X	0	0	X		Send SLA+W, receive ACK
10H	Repeated start condition sent	Write SLA+W or	X	0	0	X		Same as above
		Write SLA+R	X	0	0	X		Send SLA+R, SMBus will switch to host receiving mode
18H	SLA+W sent; ACK received	Write data byte or no	0	0	0	X		Send data, receive ACK
		SMBDAT action or no	1	0	0	X		Send repeated start condition
		SMBDAT action or 0 1				0	X	Send termination condition; clear STO flag
		No SMBDAT Action 1			1	0	X	Send a stop condition followed by a start condition; STO is cleared
20H	SLA+W sent; non-ACK received	Write data byte or	0	0	0	X		Send data, receive ACK
		No SMBDAT action or	1	0	0	X		Send repeated start condition
		No SMBDAT action or 0 1				0	X	Send termination condition; clear STO flag
		No SMBDAT Action 1			1	0	X	Send a stop condition followed by a start condition; STO is cleared
28H	Data in SMBDAT has been sent ;	write data byte or	0	0	0	X		Send data, receive ACK
	ACK received	No SMBDAT action or	1	0	0	X		Send repeated start condition
		No SMBDAT action or 0 1				0	X	Send termination condition; clear STO flag
		No SMBDAT action 1			1	0	X	Send a stop condition followed by a start condition; STO is cleared
30H	Data in SMBDAT has been sent; data byte has been written or	non-ACK has been received	0	0	0	X		Send data, receive ACK
		No SMBDAT action or No	1	0	0	X		Send repeated start condition
		SMBDAT action or 0 1				0	X	Send termination condition; clear STO flag
		No SMBDAT action 1			1	0	X	Send a stop condition followed by a start condition; STO is cleared
38H	In SLA+W or data transmission Lost arbitration bit	No SMBDAT action or	0	0	0	X		SMBus bus is released; enters non-addressed slave mode
		No SMBDAT action	1	0	0	X		Send a start condition when the bus is idle

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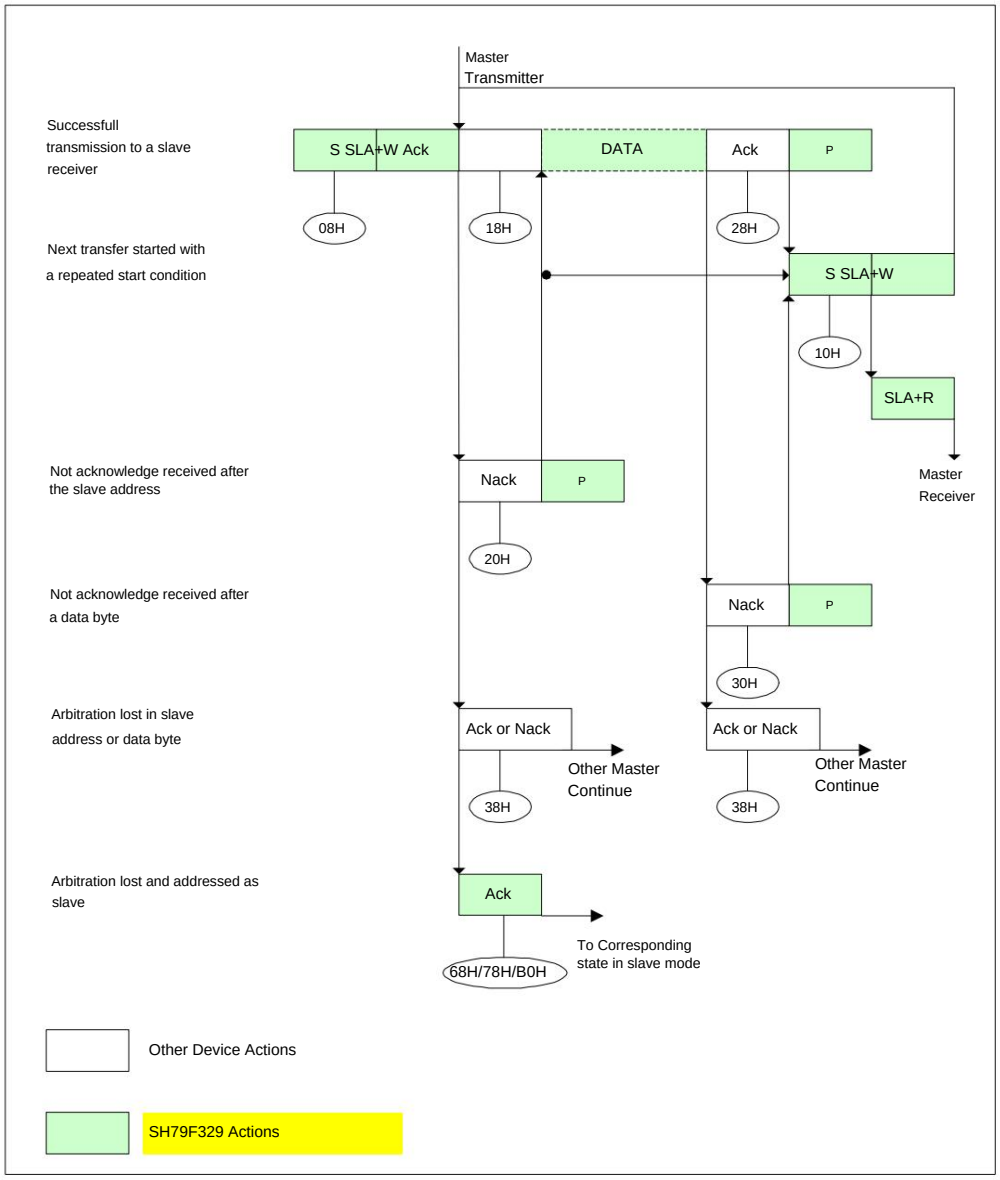

Master Receive Mode

In the master receive mode, a series of data is received from the slave. To enter the master receive mode, a start condition is followed by a slave address + read control word (SLA+R). The address packet indicates entry into the host transmit mode (MR).

By setting ENSMB and STA in the control register SMBCON, clearing STO and SI, the SMBus logic will detect the SMBus bus and issue a start condition (STA) when allowed. When the start condition (STA) is transmitted, the communication interrupt (SI) is set, the status register (SMBSTA) is 08H, and the interrupt service routine should write the slave address and read control word (SLA+R) to the data register SMBDAT. Clear the SI flag before starting the next transmission.

When the slave address and write control word are transmitted and an "acknowledge" bit is received, the interrupt (SI) is set and there are several possible states in the status register SMBSTA: 40H, 48H and 38H for the host mode and 68H, 78H and B0H for the slave mode.

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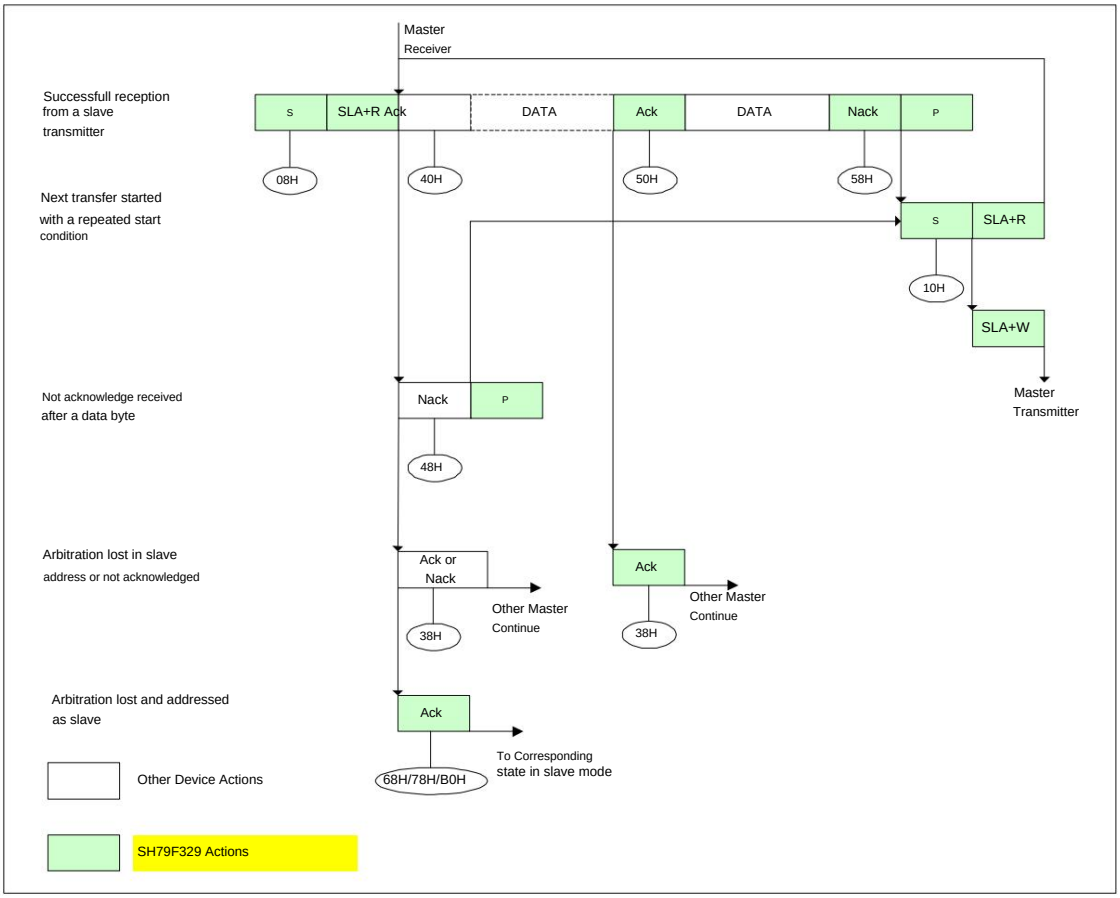
Host receiving mode status code

Status Code	The **SMBus** bus and Hardware interface status	Application software response						The next action performed by **SMBus**
		Read/write data register **SMBDAT**	**THIS IS**	**THIS**	**YES**	**AA**		
08H	Start condition sent	Write SLA+R	X	0	0	X	Send SLA+R, receive ACK	
10H	Repeated start condition sent	Write SLA+R or	X	0	0	X	Same as above	
		Write SLA+W No	X	0	0	X	Send SLA+W, SMBus will switch to host sending mode	
38H	When sending SLA+R or non-ACK Losing Arbitration	SMBDAT action or	0	0	0	X	SMBus bus is released; enter non-addressed slave mode	
		No SMBDAT action	1	0	0	X	Send a start condition when the bus is idle	
40H	SLA+R sent; ACK	No SMBDAT action or	0	0	0	No SMBDAT action	0	0 Receive data and return non-ACK
	received SLA+R	0 0 No SMBDAT action or	No SMBDAT action or					1 Receive data and return ACK
48H	sent; non-ACK	0 1 No SMBDAT action	1	0	0	X	Send repeated start condition	
	received	Read data or Read data	Read data or				0	X Send termination condition; clear STO flag
		Read data or Read data			1		0	X Send a stop condition followed by a start condition; STO is cleared
50H	Data received;		0	0	0			0 Receive data and return non-ACK
	ACK responded		0	0	0			1 Receive data and return ACK
58H	Data received;		1	0	0	X	Send repeated start condition	
	Non-ACK responded		0	1				0 X Send termination condition; clear STO flag
			1	1				0 X Send a stop condition followed by a start condition; STO is cleared



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Slave Transmit Mode

In the slave transmit mode, a series of data is sent to the master. To initialize the slave transmit mode, the control register SMBCON and the address register SMBADR must be

Initialize the line: Set ENSMB and AA in the control register SMBCON, clear STA, STO and SI; the high 7 bits in the address register SMBADR are ready for SH79F329

If GC is set, SH79F329 will also respond to the general address (00H); otherwise, it will not respond to the general address.

After SMBADR and SMBCON are initialized, the SH79F329 will wait for the bus to respond to its own address or the general address (if GC is set).

If the address and read flag are 'read', the SMBus enters the slave transmit mode, otherwise it enters the slave receive mode. After the address and read flag are received, the interrupt flag (SI) is set.

Status register SMBSTA is valid.

During the transmission, if the Acknowledge Enable bit 'AA' is cleared, the SMBus will transmit the last byte and enter C0H according to the Acknowledge or Not Acknowledge bit sent by the host receiver.

or C8H state. The bus will switch to non-address slave mode and no longer respond to master transmission. As a result, the host receiver will receive a string of '1'. The last byte is sent.

After that, if the host still needs additional data (transmission 'acknowledge' signal), it enters the C8H state.

Slave send mode status code

Status Code	The **SMBus** bus and Hardware interface status	Application software response					The next action performed by **SMBus**
		Read/write data register **SMBDAT**	**THIS IS**	**THIS**	**YES**	**AA**	
A8H	Received own SLA+R; Write data or Response ACK Write data		X	0	0	0	Send the last data; wait for ACK response
			X	0	0	1	Send data; wait for ACK response
B0H	Send SLA+R/W as host When the arbitration is lost, the host receives SLA+Rÿ ACK has been responded to write data	Write data or SMBDAT	X	0	0	0	Send the last data; wait for ACK response
			X	0	0	1	Send data; wait for ACK response
B8H	data has been sent; write data or receive ACK response to write data		X	0	0	0	Send the last data; wait for ACK response
			X	0	0	1	Send data; wait for ACK response
COH	SMBDAT data has been sent; Received NACK response	No SMBDAT action or 0 0 0	1	0	0	0	Switch to non-addressed slave mode; do not respond to own address and general address
		No SMBDAT action or 0 0 0	1	0	0	1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR
		No SMBDAT action or	1	0	0	0	Switch to non-addressed slave mode; do not respond to own address and general Address; send 'start condition' when bus is idle
		No SMBDAT action 1 0 0	1	0	0	1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR. Set; send 'start condition' when the bus is idle
C8H	Last SMBDAT sent Receive ACK response	No SMBDAT action or 0 0 0	data (AA = 0);			0	Switch to non-addressed slave mode; do not respond to own address and general address
		No SMBDAT action or 0 0 0				1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR
		No SMBDAT action or	1	0	0	0	Switch to non-addressed slave mode; do not respond to own address and general Address; send 'start condition' when bus is idle
		No SMBDAT action 1 0 0				1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR. Set; send 'start condition' when the bus is idle

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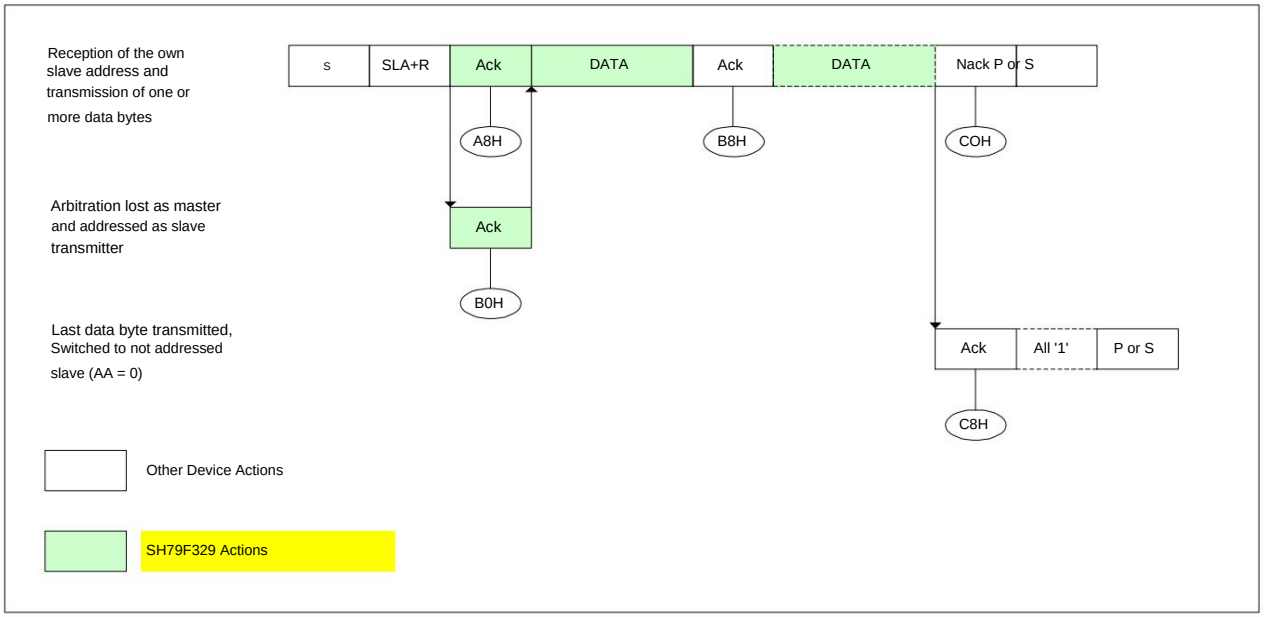

Slave Receive Mode

In slave receiving mode, a series of data is received from the master. To initialize the slave receiving mode, the control register SMBCON and the address register SMBADR must be

Initialize the line: Set ENSMB and AA in the control register SMBCON, clear STA, STO, and SI; the upper 7 bits in the address register SMBADR are ready for SH79F329

If GC is set, SH79F329 will also respond to the general address (00H); otherwise, it will not respond to the general address.

After SMBADR and SMBCON are initialized, the SH79F329 will wait for the bus to respond to its own address or the general address (if GC is set).

If the address and write flag are 'write', the SMBus enters the slave receive mode, otherwise it enters the slave transmit mode. After the address and write flag are received, the interrupt flag (SI) is set.

Status register SMBSTA is valid.

During the transmission, if the acknowledgment enable bit 'AA' is cleared, the SMBus will receive the last byte and respond with a non-acknowledgment. Responding with a non-acknowledgment can indicate the current

The slave cannot receive more bytes. When 'AA = 0', the SH79F329 cannot respond to access to its own address; but it still monitors the bus status and can respond to the access through AA = 1

Restore response to own address. SH79F329 can be temporarily isolated from the bus by AA = 0.

Slave receiving mode status code

Status Code	The **SMBus** bus and Hardware interface status	Application software response				The next action performed by **SMBus**
		Read/write data register **SMBDAT**	**THIS IS**	**THIS YES**	**AA**	
60H	Received own SLA+W; No SMBDAT action	or X 0 0 Responsed ACK	No SMBDAT action	X 0 0		0 Receive data; send NACK response 1 Receive data; send ACK response
68H	Send SLA+R/W as host When the arbitration is lost, the host receives SLA+Wÿ ACK has been responded	No SMBDAT action or X 0 0 No SMBDAT action X 0 0 Received the general address sent by the				0 Receive data; send NACK response 1 Receive data; send ACK response
70H	host; No SMBDAT action or X 0 0	No SMBDAT action X 0 0 ACK has been responded				0 Receive data; send NACK response 1 Receive data; send ACK response
78H	Send SLA+R/W as host When the arbitration is lost, the host receives Send general address; ACK has been responded	No SMBDAT action or X 0 0 No SMBDAT action X 0 0				0 Receive data; send NACK response 1 Receive data; send ACK response

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Continued from the table above

80H	In the addressed state; Data received; ACK has been responded	Read data or	X 0 0		0	Receive data; send NACK response
		Reading Data	X 0 0		1	Receive data; send ACK response
88H	In the addressed state; Data received; Responded to NACK	Read data or	0 0 0		0	Switch to non-addressed slave mode; do not respond to own address and general address
		Read data or	0 0 0		1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR
		Read data or	1 0 0		0	Switch to non-addressed slave mode; do not respond to own address and general Address; send 'start condition' when bus is idle
		Reading Data	1 0 0		1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR. Set; send 'start condition' when the bus is idle
90H	In the universal address addressed state; received data; ACK has been responded	Read data or	X 0 0		0	Receive data; send NACK response
		Reading Data	X 0 0		1	Receive data; send ACK response
98H	In the universal address addressed state; received data; Responded to NACK	Read data or	0 0 0		0	Switch to non-addressed slave mode; do not respond to own address and general address
		Read data or	0 0 0		1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR
		Read data or	1 0 0		0	Switch to non-addressed slave mode; do not respond to own address and general Address; send 'start condition' when bus is idle
		Reading Data	1 0 0		1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR. Set; send 'start condition' when the bus is idle
AH	As a slave, a termination condition is received condition	No SMBDAT action or 0 0 0 or repeated start			0	Switch to non-addressed slave mode; do not respond to own address and general address
		No SMBDAT action or 0 0 0			1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR
		No SMBDAT action or	1 0 0		0	Switch to non-addressed slave mode; do not respond to own address and general Address; send 'start condition' when bus is idle
		No SMBDAT action 1 0 0			1	Switch to non-addressed slave mode; respond to own address, whether to respond The general address depends on the setting of GC in register SMBADR. Set; send 'start condition' when the bus is idle

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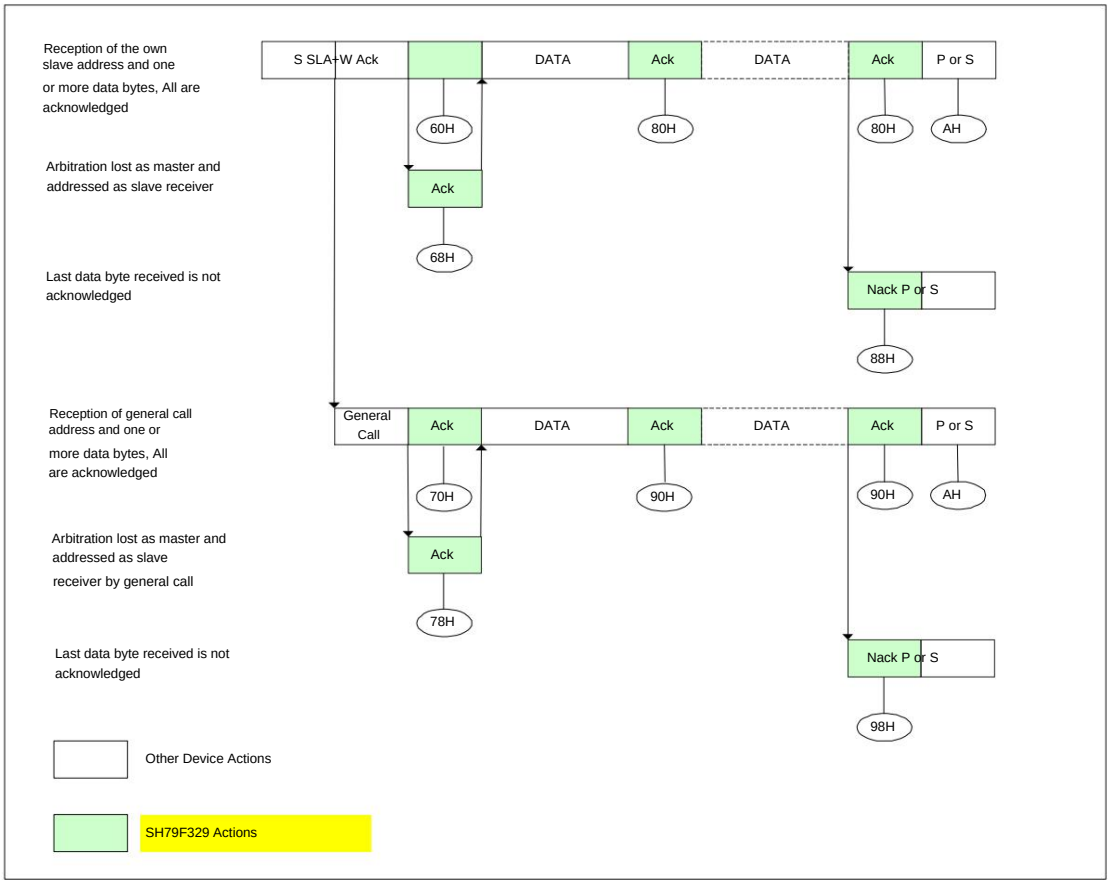

In addition to

the above status codes, there are two status codes in other modes that do not have clear SMBus status. Status 0F8H means that there is no corresponding status information because the interrupt flag SI is not set.

Interrupt SI is not set, that is, it is filled with 0F8H after clearing a state and before a new state is established.

Status 00H indicates that an error has occurred in the SMBus bus communication, that is, an illegal start condition or end condition has occurred in the transmission. For example, a start condition or end condition has occurred when transmitting an address, data, or responding to an ACK response. Status 00H will also occur when the bus disrupts the internal logic. When an illegal state occurs, the interrupt flag SI will be set. Normal communication can be restored by setting STO and clearing the SI flag. The SH79F329 will enter the non-addressed slave mode and automatically clear the STO flag. The data line and clock line will be released, and no end condition will be transmitted

on the line. Other modes

Status Code	**SMBus** bus and hardware interface status	Application software responds to read/write data registers **SMBDAT**	**THIS IS**	**THIS**	**YES**	**AA**	The next action performed by **SMBus**
F8H No valid status code; SI=0 No SMBDAT action No SMBCON Action Waiting for or processing the current transmission An illegal start							
00H	condition or stop condition is sent in the master or addressed slave mode; The interface causes confusion in the SMBus internal logic	No SMBDAT action	0	1	0	X	Only internal hardware is affected; release the bus; switch to non-addressed slave mode; clear STO

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8.1.5 Registers

Table 8.1 SMBus Control Register

C1H	7th 6th 5th 4th 3rd 2nd 1st 0th							
SMBCON	ALL TOGETHER		STA	WHAT	AND	AA	FREE TFREE	
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7	**ALL**	Bus timeout flag 0: No timeout occurs 1: Set when the SMBus is low for more than 25ms. Must be cleared by software
6	**ENSMB**	**SMBus enable bit** 0: Disable SMBus function 1: Enable SMBus function
5	**STA**	Start bit 0: No start condition will be sent 1: Send a start condition when the bus is idle
4	**WHAT**	Stop bit 0: No termination condition will be sent 1: Send a stop condition when acting as a master; do not send a stop condition to the bus when acting as a slave, but the state is restored To the non-addressed slave state. The hardware will automatically clear this flag
3	**AND**	SMBus serial interrupt flag 0: No SMBus serial interrupt occurred 1: Set when a status other than 0xF8 is generated in the SMBus communication status, must be cleared by software
2	**AA**	Declaration reply flag 0: Reply to non-'answer' signal (SMBD high level) 1: Reply 'answer' signal (SMBD low level)
1	**TFREE**	Bus high level timeout flag 0: No timeout occurs 1: Set when the clock line is high for more than 50us while participating in bus transmission. Must be cleared by hardware
0	**FREE**	Bus high level timeout enable bit 0: Disable bus high level timeout judgment 1: Allow bus high level timeout judgment

Special note: TOUT, SI, and TFREE will all trigger SMBus interrupts, and the three share one interrupt vector

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Table 8.2 SMBus Status Register

C2H	7th 6th 5th 4th 3rd 2nd 1st 0th							
SMBSTA	SMBSTA.7 SMBSTA.6 SMBSTA.5 SMBSTA.4 SMBSTA.3 CR.1						CR.0	THIS IS IT
Read/Write	read	read	read	read	read	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-3	SMBSTA[7: SMBSTA[7: SMBSTA[7: SMBSTA[7:3]	SMBus serial communication status bits See the corresponding status description
2:1	CR[1:0] CR[1:0] CR[1:0] CR[1:0]	**SMBus Transmit Frequency** 00:16KHz 01ÿ32KHz 10ÿ64KHz 11ÿ64KHz
0	**THIS IS IT**	Bus timeout enable bit 0: Disable bus timeout judgment 1: Enable bus timeout detection

Table 8.3 SMBus Address Register

C3H	7th 6th 5th 4th 3rd 2nd 1st 0th							
SMBADR	SLVA.6 SLVA.5 SLVA.4 SLVA.3 SLVA.2 SLVA.1						SLAVE.0	GC
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-1	**SLAVE[6:0]**	SMBus address configuration bits Address when configuring SH79F329 as a slave
0	**GC**	General address enable bit 0: Disable response to general address 1: Allow responses to general addresses

Table 8.4 SMBus Data Register

C4H	7th 6th 5th 4th 3rd 2nd 1st 0th							
SMBDAT	SMBDAT.7 SMBDAT.6 SMBDAT.5 SMBDAT.4 SMBDAT.3 SMBDAT.2 SMBDAT.1 SMBDAT.0							
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**SMBDAT** SMBus communication data register	

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8.2 Analog/Digital Converter (ADC)

8.2.1 Features

ÿ SH79F329 has two 16-bit high-precision ÿ-ÿ analog-to-digital converters (CADC, VADC)

ÿ CADC is a dual-ended differential input

ÿ VADC is 2-way single-ended input

ÿ Provide zero-scale input and full-scale input calibration

ÿ CADC provides forward and reverse automatic accumulation functions

ADC interrupt in idle mode can wake up the system (if interrupt is enabled)

ADC is disabled in power-down mode

8.2.2 VADC

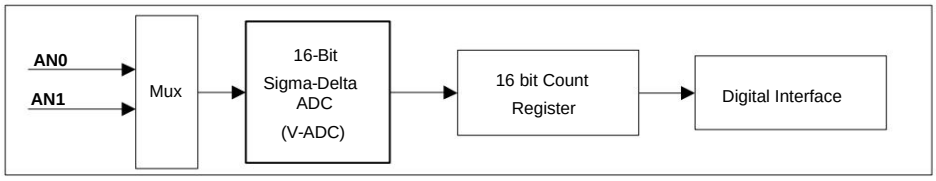
VADC is a 16-bit ÿ-ÿ analog-to-digital converter. The reference voltage VREF is generated by AVDD. Two ADC channels share one ADC module, but only one channel can be used at a time. The VADCEN signal controls the start of conversion, and VADCIF indicates the end of conversion. When the conversion is completed, the VADC data register is updated and an interrupt is generated (if VADC If VADCEN is not cleared, the next conversion starts automatically.

VADC provides zero-scale and full-scale input calibration. When VCE = 1 and VOF = 0, zero-scale input calibration is performed; when VCE = 1 and VOF = 1, full-scale input calibration is performed.

VADC provides a channel switching control bit NCH. When switching to a new channel or when a large change in the input signal is expected, set this bit so that VADC uses a longer settling time. Time to ensure the validity of the conversion results.

VADC provides three conversion frequency options: 32Hz, 64Hz, and 128Hz.

Before using VADC, the corresponding control bits in the ADCP register must be set.



VADC Setup Sequence

1. Set the corresponding IO port as ADC application port through register ADCP
2. Select channel 0 or channel 1
3. Set NCH/VCE/VOF
4. Set VADCEN
5. Wait for VADCIF to be set or interrupted, and query the conversion result

For VADC, VADC Data = (VAN0(VAN1) - AGND) / (VREF+ - VREF-) X 32768. The zero input conversion result is 0x0000, and the full-scale input conversion result is 0x7FFF. Normally, no value greater than 0x7FFF appears.

VADC data	8000H	C000H	FFFFH	0000H	0001H	4000H	7FFFH
Decimal Value	·	·	-1	0	1	16384	32767

8.2.3 VADC Register

Table 8.5 ADC clock delay control register

E6H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
OPDY	·	·	·	·	OPDY.3 OPDY.2	OPDY.1 OPDY.0		
Read/Write	·	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR/PIN)	·	·	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
3-0	**OPDY[3:0]** internal storage bit, must be set to 0	

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Table 8.6 VADC pin multiplexing selection register

E7H	7th 6th 5th 4th 3rd 2nd 1st 0th							
ADCP	·	·	·	·	·	·	AN0P	AN1P
Read/Write	·	·	·	·	·	·	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	·	·	·	·	·	·	0	0

Bit number	Bit Notation	illustrate
1	**AN1P**	P0.0 function selection control bit 0: P0.0 is used as a normal IO 1: P0.0 is used as VADC channel 1
0	**AN0P**	P0.1 function selection control bit 0: P0.1 is used as a normal IO 1: P0.1 is used as VADC channel 0

Table 8.7 VADC Control Register

D9H	7th 6th 5th 4th 3rd 2nd 1st 0th							
VADCON	VADCEN VADCIF		SCH	VOF	VCE	VCR1	VCR0	NCH
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7	**THE WATER**	**VADC control bits** 0: Disable ADC module 1: Turn on the ADC module
6	**VADCIF**	VADC interrupt flag 0: No ADC interrupt, cleared by software 1: Set to 1 by hardware, indicating that the AD conversion has been completed
5	**SCH**	Channel selection bits 0: Convert channel 0 1: Convert channel 1
4	**VOF**	Calibration function selection bit 0: Zero-amplitude input calibration 1: Full-scale input calibration
3	**VCE**	Calibration function enable bit 0: Disable the calibration function 1: Enable the calibration function
2-1	VCR[1:0] VCR[1:0] VCR[1:0] VCR[1:0]	VADC conversion frequency selection 00ÿ32Hz 01ÿ64Hz 10ÿ128Hz 11ÿ128Hz
0	**NCH**	Channel switching control bit 0: No channel switching 1: There is a channel switching action, and VADC needs 4 conversion cycles to complete the conversion

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Table 8.8 VADC conversion result register

YES, DBH	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
VADC1 (DAH)	VADC.15 VADC.14 VADC.13 VADC.12 VADC.11 VADC.10 VADC.9 VADC.8							
VADC0 (DBH) read/	VADC.7 VADC.6 VADC.5 VADC.4 VADC.3 VADC.2 VADC.1 VADC.0							
write	read	read	read	read	read	read	read	read
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0 **7-0**	**VADC[15:0]** When the conversion is completed, the data is updated to the digital value corresponding to the analog voltage	

Table 8.9 VADC zero-scale calibration result register

CDH, CEH	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
V0OR1 (CDH)	V0OR.15 V0OR.14 V0OR.13 V0OR.12 V0OR.11 V0OR.10 V0OR.9 V0OR.8							
V0OR0 (CEH) read/	V0OR.7 V0OR.6 V0OR.5 V0OR.4 V0OR.3 V0OR.2 V0OR.1 V0OR.0							
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0 **7-0**	**V0OR[15:0]** When the conversion is completed, the data is updated to the digital value corresponding to the analog voltage	

Table 8.10 VADC Full-Scale Calibration Register

CFHÿD7H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
V0FSR1 (CFH)	V0FSR.15 V0FSR.14 V0FSR.13 V0FSR.12 V0FSR.11 V0FSR.10 V0FSR.9 V0FSR.8							
V0FSR0 (D7H) read/	V0FSR.7 V0FSR.6 V0FSR.5 V0FSR.4 V0FSR.3 V0FSR.2 V0FSR.1 V0FSR.0							
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0 **7-0**	**V0FSR[15:0]** When the conversion is completed, the data is updated to the digital value corresponding to the analog voltage	

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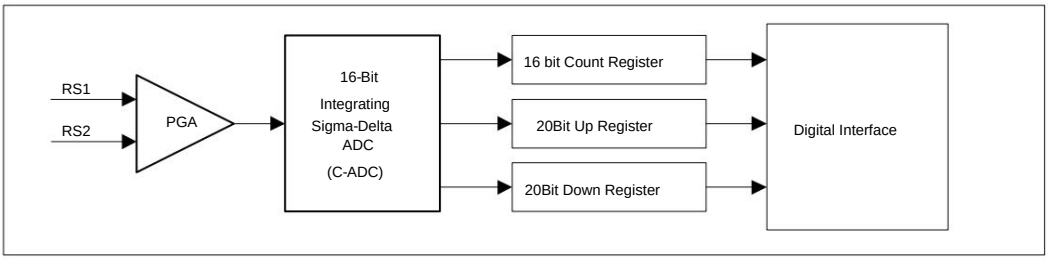
8.2.4 CADC

CADC is a 16-bit ÿ-ÿ analog-to-digital converter. The reference voltage VREF is 1/4 of VADC and uses differential input. The CADCEN signal controls the start of conversion, and CADCIF prompts the conversion.
When the conversion is complete, the VADC data register is updated and an interrupt is generated (if the CADC interrupt is enabled). If MODE is set, the CADCEN
It will not be cleared and the next conversion will start automatically; if MODE is cleared, CADCEN will be cleared and the next conversion will not start.

CADC provides zero-scale and full-scale input calibration. CCE = 1, COF = 0 performs zero-scale input calibration; CCE = 1, COF = 1 performs full-scale input calibration.

CADC provides three conversion frequency options: 4Hz, 8Hz, 16Hz, and 32Hz.

When VRS1 > VRS2, the conversion result is subtracted from the Offset and added to the positive accumulator; when VRS1 < VRS2, the conversion result is subtracted from the Offset and added to the negative accumulator.



CADC Setup Sequence

1. Set MODE/CCE/COF
2. Set CADCEN
3. Wait for CADCIF to be set or interrupted, and query the conversion result

For CADC, CADC Data = (VRS1-VRS2) / (VREF+ - VREF-) X 32768. The conversion result of zero input is 0x0000, and the conversion result of full-scale input is 0x7FFF.
The negative full-scale input conversion result is 0x8000.

CADC data	8000H	C000H	FFFFH	0000H	0001H	4000H	7FFFH
Decimal Value	-32768	-16384	-1	0	1	16384	32767

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8.2.5 CADC Register

Table 8.11 CADC Control Register

DCH	7th 6th 5th 4th 3rd 2nd 1st 0th							
CADCON	CADCEN CADCIF MODE				COF	CCE	CCR1	CCR0
Read/	Read/Write	Read/Write	Read/Write		Read/Write	Read/Write	Read/Write	Read/Write
write reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0		0	0	0	0

Bit number	Bit Notation	illustrate
7	**CADCEN**	**CADC Control Bits** 0: Disable CADC module 1: Open the CADC module
6	**CADCIF**	CADC interrupt flag 0: No CADC interrupt, cleared by software 1: Set to 1 by hardware, indicating that the AD conversion has been completed
5	**MODE**	Conversion mode selection bits 0: Perform a single conversion and clear CADCEN after the conversion is completed. 1: Perform multiple conversions. After the conversion is completed, CADCEN is not cleared and the next conversion begins.
3	**COF**	Calibration function selection bit 0: Zero-amplitude input calibration 1: Full-scale input calibration
2	**CCE**	Calibration function enable bit 0: Disable the calibration function 1: Enable the calibration function
1-0	CCR[1:0] CR[1:0] CR[1:0] CR[1:0]	CADC conversion frequency selection 00ÿ4Hz 01ÿ8Hz 10ÿ16Hz 11ÿ32Hz

Table 8.12 CADC conversion result register

DDHÿDEH	7th 6th 5th 4th 3rd 2nd 1st 0th							
CADC1 (DDH)	CADC.15 CADC.14 CADC.13 CADC.12 CADC.11 CADC.10 CADC.9 CADC.8							
CADC0 (DEH) read/	CADC.7 CADC.6 CADC.5 CADC.4 CADC.3 CADC.2 CADC.1 CADC.0							
write	read	read	read	read	read	read	read	read
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0 **7-0**	**CADC[15:0]** When the conversion is completed, the data is updated to the digital value corresponding to the analog voltage	

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Table 8.13 CADC zero-scale calibration result register

BCHýBDH	7th 6th 5th 4th 3rd 2nd 1st 0th							
COR1 (BCH)	COLOR.15 COLOR.14 COLOR.13 COLOR.12 COLOR.11 COLOR.10 COLOR.9							COR.8
COR0 (BDH) read/	COR.7	COR.6	COR.5	COR.4	COR.3	COR.2	COR.1	COR.0
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0 **7-0**	**COR[15:0]** When the conversion is completed, the data is updated to the digital value corresponding to the analog voltage	

Table 8.14 CADC Full-Scale Calibration Register

BEHýBFH	7th 6th 5th 4th 3rd 2nd 1st 0th							
CFSR1 (BEH)	CFSR.15 CFSR.14 CFSR.13 CFSR.12 CFSR.11 CFSR.10 CFSR.9 CFSR.8							
CFSR0 (BFH) read/	CFSR.7 CFSR.6 CFSR.5 CFSR.4 CFSR.3 CFSR.2 CFSR.1 CFSR.0							
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0 **7-0**	**CFSR[15:0]** When the conversion is completed, the data is updated to the digital value corresponding to the analog voltage	

Table 8.15 CADC forward accumulation register

D1H , D2H , D3H7th6th5th4th3rd2nd1st0th								
UAD2 (D1H)	.	.	.	.	UAD.19 UAD.18 UAD.17 UAD.16			
UAD1 (D2H)	UAD.15 UAD.14 UAD.13 UAD.12 UAD.11 UAD.10						UAD.9	UAD.8
UAD0 (D3H) read/	UAD.7	UAD.6	UAD.5	UAD.4	UAD.3	UAD.2	UAD.1	UAD.0
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
3-0 **7-0** **7-0**	When **UAD[19:0]** is converted to positive, data accumulation is performed	

Table 8.16 CADC negative accumulation register

D4H , D5H , D6H7th6th5th4th3rd2nd1st0th								
DAD2 (D4H)	.	.	.	.	DAD.19 DAD.18 DAD.17 DAD.16			
DAD1 (D5H)	DAD.15 DAD.14 DAD.13 DAD.12 DAD.11 DAD.10						DAD.9	DAD.8
DAD0 (D6H) read/	DAD.7	DAD.6	DAD.5	DAD.4	DAD.3	DAD.2	DAD.1	DAD.0
write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVR POR/WDT/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
3-0 **7-0** **7-0**	When **DAD[19:0]** is converted to negative, data accumulation is performed	

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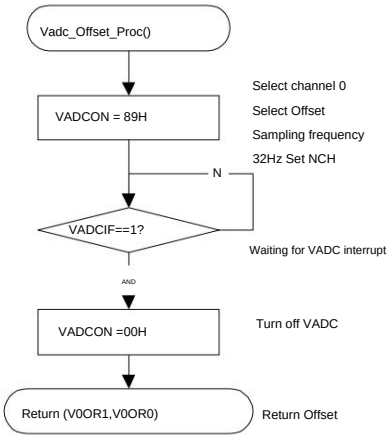
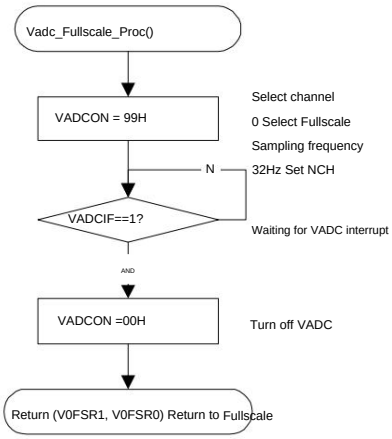
8.2.6 Program Examples

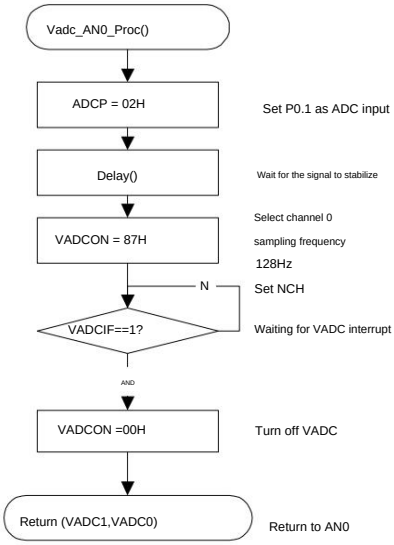
VADC Measurement Offset



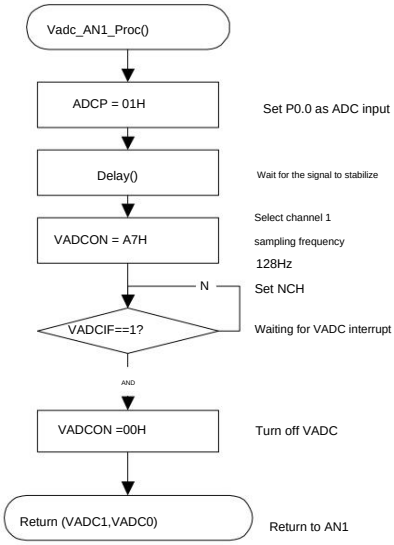
VADCÿÿFullscale Fullscale Fullscale Fullscale



VADC measures the AN0 input voltage



VADC measures the AN1 input voltage



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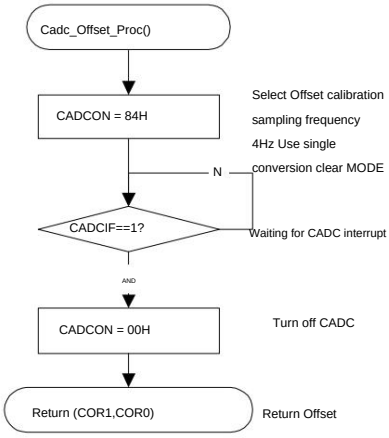
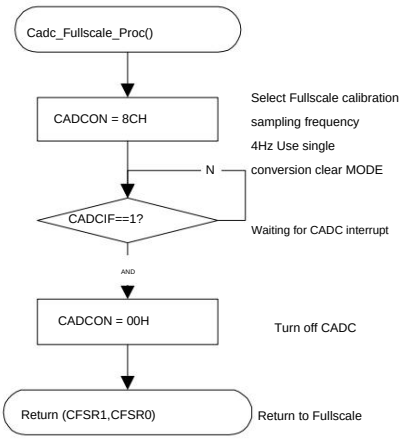
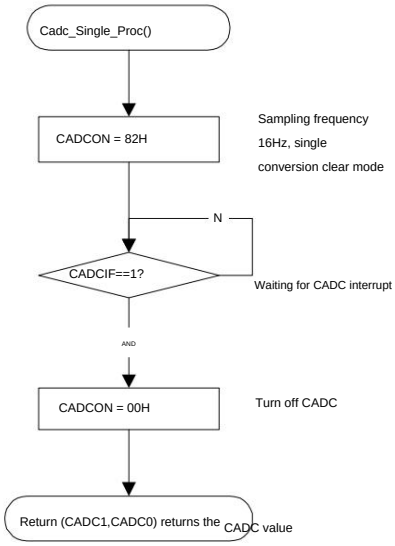
CADC Measurement Offset



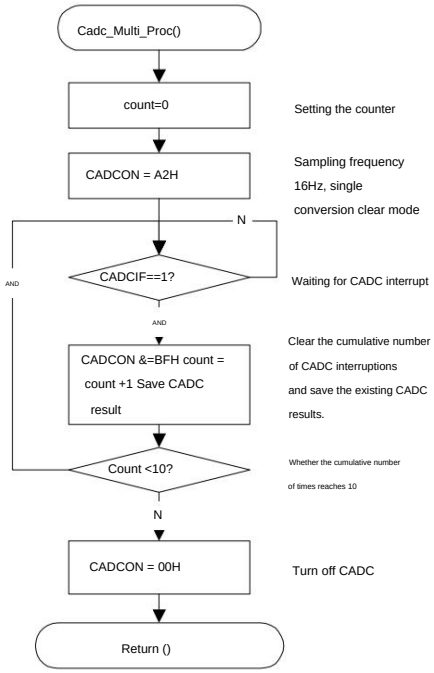
CADCÿÿFullscale Fullscale Fullscale Fullscale



CADC measures single input voltage



CADC measures the input voltage 10 times



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8.3 AFE Communication (SCI)

8.3.1 Features ÿ

Provides communication interface with analog front end (AFE) **ÿ**

Can detect AFE working status

8.3.2 AFE Communication (SCI) Protocol

The SCI interface controls and monitors the communication with the analog front end. The SCI communication consists of three parts: address, data, and response. SCIADR sets the AFE sub-address and Read/write type, SCIEN starts the transmission, SCIF indicates the end of the transmission. SCISTA saves the communication status.

Communication with AFE must be performed according to the

following steps: 1. Set SDAP and CLKP in register P0OS 2. Set AFE sub-

address and read/write operation in SCIADR 3. If it is a write action, fill

in the corresponding content to SCIDAT 4. If it is a write action, set whether

to perform automatic reading 5. Enable SCI function and start

transmission 6. Wait for SCIF to be set 7.

Check whether the SCISTA

status is 0. If so, the transmission is correct, otherwise the transmission is wrong 8. If it is a read action, read

the SCIDAT content

Note:

When writing, please confirm that the read result is consistent with the original written data, otherwise please

to rewrite it. *1.* When reading, it is recommended to read three times in a row and use the three-choice method

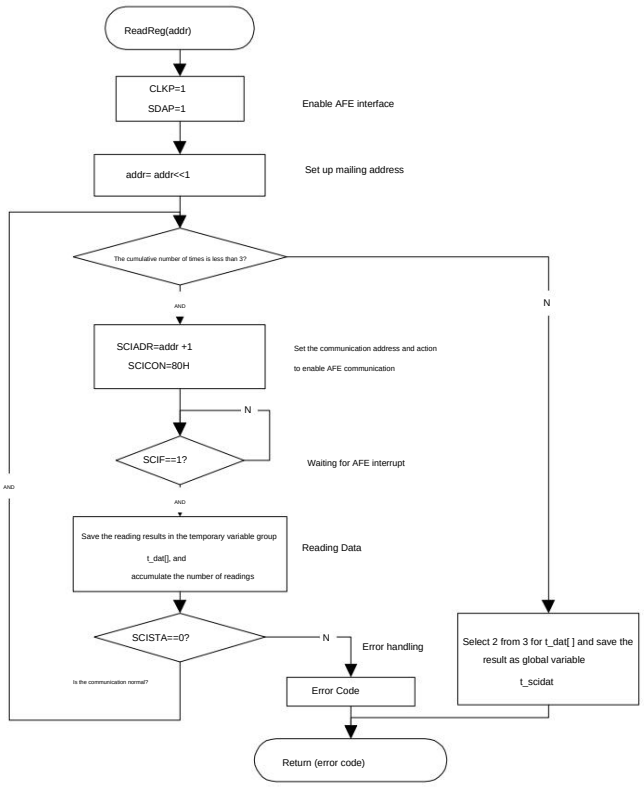
determine the read value. *2.* Please read the SCIDAT content within 32us

after SCIF is set. *3.* When performing a read-modify-write operation, please save it in RAM after reading SCIDAT In, yes Modify the RAM content and then write it into SCIDAT , do not use *it tears*

Perform a read-modify-write operation on the register.

8.3.3 AFE Communication Example

Read AFE status register (subregister 00H)



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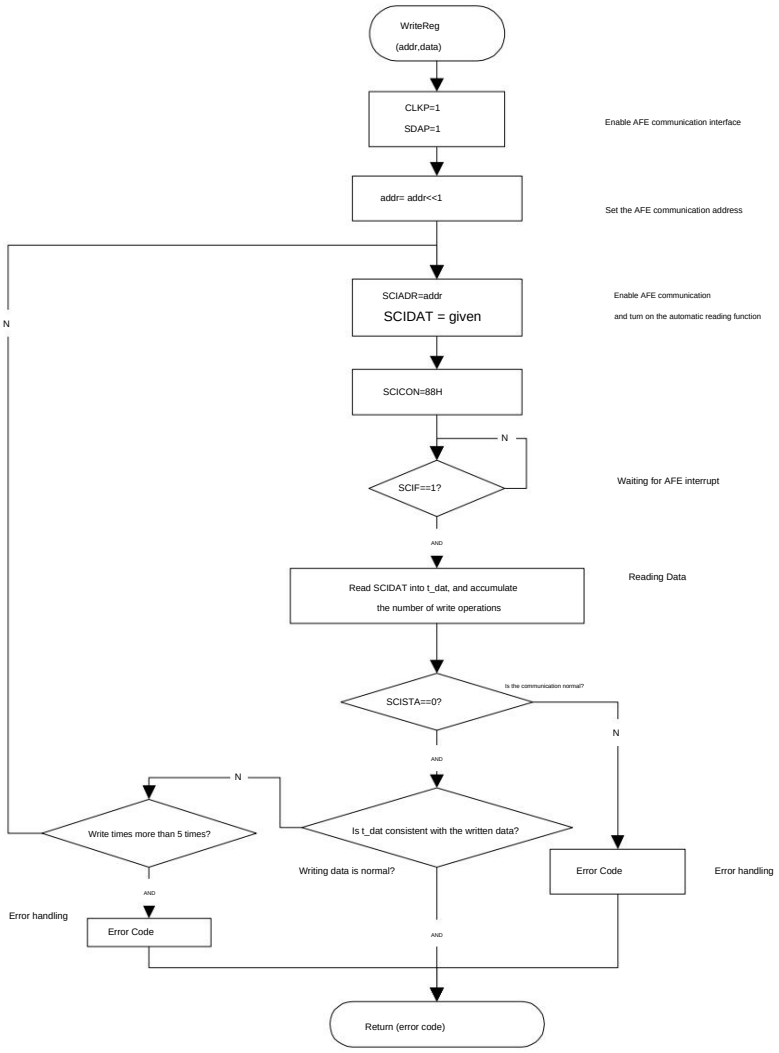
Write AFE function control register (sub-register 02H)



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8.3.4 SCI Registers

Table 8.17 SCI Control Register

C5H	7th 6th 5th 4th	3rd 2nd 1st 0th						
SCICON	SCIEN	SCIF	·	·	SCIRW	SCISTA.2	SCISTA.1	SCISTA.0
Read/Write	Read/Write	Read/Write	·	·	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN)	0	0	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
7	**SCIEN**	SCI control bits 0: Disable SCI module 1: Open the SCI module
6	**SCIF**	SCI interrupt flag 0: No SCI interrupt, cleared by software 1: Set to 1 by hardware, indicating that the transfer is complete
3	**SCIRW**	Automatic read control bit 0: Normal read/write operation 1: After the write action is completed, the read action is automatically executed and an interrupt is generated afterwards
2-0	**SCISTA[2:0]**	Transfer status bit 000: Transmission is correct Else: Transfer failed

Table 8.18 SCI address register

C6H	7th 6th 5th 4th	3rd 2nd 1st 0th						
SCIADR	·	·	·	·	SCIA.2	SCIA.1	SCIA.0	Read/Write
Read/Write	·	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN)	·	·	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
3-1	**SCIA[2:0]** AFE sub-address	
0	Read/Write Read/Write Read/Write Read/Write	Read and write control bits 0: Perform a write operation 1: Perform a read operation

Table 8.19 SCI data register

C7H	7th 6th 5th 4th	3rd 2nd 1st 0th						
it tears	SCID7	SCID6	SCID5	SCID4	SCID3	SCID2	SCID1	SCID0
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**SCID[7:0]** AFE data register	

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8.4 Timer

8.4.1 Features

ÿ SH79F329 has 2 timers (Timer 0, 1)

ÿ 8 clock division modes

ÿ 8-bit accumulative timer

ÿ Overflow from 0FFH to 00H, an interrupt is generated

ÿ With automatic reload function

8.4.2 Timer Operation

By default, the timer is in reset state. The timer is started by writing '1' to ENBTx in register BTCON. If BTx is updated during the counting process,
The counter then re-reads BTx and starts counting from this number. When the BT0/BT1 count reaches 00H, an interrupt is generated (if the timer interrupt is enabled). Timer BT0/BT1
The timer will be automatically reloaded and start counting from BT0/BT1 again. Setting the ET0 and ET1 bits of the IEN0 register to 1 enables timer 0 and timer 1 interrupts. (See the Interrupts section for details).

Timer 0 and Timer 1 should operate in the following order:

1. Set the starting count value through BT0/BT1

2. Select the frequency division coefficient BTxM[2:0]

3. Enable ENBTx

8.4.3 Timer Registers

Table 8.20 Timer x control register (x = 0,1)

A2H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
BTCON	ENBT1	BT1M.2	BT1M.1	BT1M.0	ENBT0	BT0M.2	BT0M.1	BT0M.0
Read/	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
write reset value (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7, 3	**ENBTx** **x = 0, 1**	Timer x start, stop control bit 0: Stop timer x 1: Start timer x
6-4, 2-0	**BTxM** **x = 0, 1**	Timer x frequency division coefficient control bit 000ÿfSYS/20 001ÿfSYS/21 010ÿfSYS/22 011ÿfSYS/23 100ÿfSYS/24 101ÿfSYS/26 110ÿfSYS/28 111ÿfSYS/210

Table 8.21 Timer/Counter x Mode Register (x = 0,1)

A4H,A3H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
BT0	BT0.7	BT0.6	BT0.5	BT0.4	BT0.3	BT0.2	BT0.1	BT0.0
BT1	BT1.7	BT1.6	BT1.5	BT1.4	BT1.3	BT1.2	BT1.1	BT1.0
Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Reset value (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN) (ENG/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**BTx[7:0]** **x = 0, 1**	Timer initial value

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8.5 Low Voltage Reset **(LVR) 8.5.1**

Features ÿ LVR

voltage VLVR is 2.3V ÿ LVR debounce time

TLVR is 30-60µs ÿ When the supply voltage is lower than the set

voltage VLVR , an internal reset will be generated The low voltage reset (LVR) function is to monitor

the supply voltage. When the supply voltage is lower than the set voltage VLVR , the MCU will generate an internal reset. The LVR debounce time TLVR is about 30µs-60µs.

After the LVR function is turned on, it has the following characteristics (t represents the time when the voltage is lower than the set

voltage VLVR): When VDD ÿ VLVR and t ÿ T LVR, a system reset is

generated. When VDD > VLVR or VDD < VLVR, but t < T LVR, no system reset is generated. The LVR

function can be turned on or off through code options. In AC or large-capacity battery

applications, it is easy to cause the MCU power supply to temporarily be lower than the defined operating voltage after connecting a large load. Low voltage reset can be applied here to ensure that the MCU power supply is stable and stable.

The protection system generates an effective reset when the voltage is lower than the set voltage.

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8.6 Watchdog Timer (WDT) and Reset Status

8.6.1 Features

ÿ Watchdog can work in power-down mode (set by code option)

ÿ Watchdog overflow frequency selectable

The watchdog timer is a down counter with a 32KHz internal oscillator as its clock source. Through code options, the WDT can be set to continue in power-down mode.
Run. When the timer overflows, the chip is reset. The WDT function can be turned on or off through code options.

The WDT control bits (bits 2 - 0) are used to select different overflow times. After the timer overflows, the WDT overflow flag (WDOF) will be automatically set to 1 by hardware.

Write to the RSTSTAT RSTSTAT RSTSTAT RSTSTAT register and the watchdog timer starts counting again before overflowing.

Some other reset flags are listed below:

8.6.2 Registers

Table 8.22 RSTSTAT Control Register

B1H	7th 6th 5th 4th	3rd 2nd 1st 0th						
RSTSTAT RSTSTAT RSTSTAT RSTSTAT	WDOF	·	PORF	LVRF	CLRF	WDT2	WDT.1	WDT.0
Read/	Read/Write	·	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
write reset value **(POR)**	0	·	1	0	0	0	0	0
Reset value **(WDT)**	1	·	in	in	in	0	0	0
Reset value **(LVR)**	in	·	in	1	in	0	0	0
Reset value **(PIN)**	in	·	in	in	1	0	0	0

Bit number	Bit Notation	illustrate
7	**WDOF**	Watchdog overflow flag Set to 1 by hardware when overflow occurs, and cleared to 0 by software or power-on reset 0: No WDT overflow occurred 1: WDT overflow occurs
5	**PORF**	Power-on reset flag Set to 1 by hardware after power-on reset, can only be cleared to 0 by software 0: No power-on reset occurred 1: A power-on reset has occurred
4	**LVRF**	Low voltage reset flag Set to 1 after low voltage reset, can be cleared to 0 by software or power-on reset 0: No low voltage reset occurred 1: A low voltage reset occurred
3	**CLRF**	Reset pin reset flag The pin is set to 1 after reset and cleared to 0 by software or power-on reset. 0: No pin reset occurred 1: A pin reset has occurred
2-0	WDT[2:0] WDT[2:0] WDT[2:0] WDT[2:0]	WDT overflow period control bit 000: WDT RC Clock/217 (Typ. = 4096ms) 001: WDT RC Clock/215 (typical value = 1024ms) 010: WDT RC Clock/213 (typical value = 256ms) 011: WDT RC Clock/212 (typical value = 128ms) 100: WDT RC Clock/211 (typical value = 64ms) 101: WDT RC Clock/29 (typical value = 16ms) 110: WDT RC Clock/27 (typical value = 4ms) 111: WDT RC Clock/25 (typical value = 1ms)

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8.7 Power Management

8.7.1 Features ÿ

Idle mode and Power-Down mode ÿ Interrupt and reset can exit Idle

and Power-Down modes To reduce power consumption, SH79F329 provides two low-power saving modes: Idle mode and

Power-Down mode. Both modes are controlled by PCON

8.7.2 Idle Mode Idle mode can reduce system

power consumption. In this mode, the

program stops running, the CPU clock stops, but the external device clock continues to run.

Stop in a certain state, and all CPU states are saved before entering idle mode, such as PC, PSW, SFR, RAM, etc.

Two consecutive instructions: first set the SUSLO register to 55H, then set the IDL bit in the PCON register to 1, making the SH79F329 enter the idle mode.

If the two consecutive instructions mentioned above are completed, the CPU will clear the SUSLO register or the IDL bit in the next machine cycle and the CPU will not enter the idle mode.

The IDL position is set to 1 when the CPU enters the idle mode. There are two ways to exit the idle

mode: (1) Interrupt generation. After the warm-up

timer is over, the CPU clock is restored, and the hardware clears the SUSLO register and the IDL bit in the PCON register. The interrupt service routine is then executed, followed by a jump to the instruction following the instruction that entered the idle mode. (2) After the reset signal is generated (a low

level appears on the reset pin, WDT resets, and LVR resets). After the warm-up timer is over, the CPU clock is restored, the SUSLO register and the IDL bit in the PCON register are cleared by hardware, and finally the SH79F329 is reset and the program starts executing from address 0000H. At this time, the RAM remains unchanged and the SFR values change according to different functional modules.

8.7.3 ÿÿÿÿÿPower-Down Power-Down Power-Down Power-Downÿ

Power-down mode can make SH79F329 enter a very low power consumption state. Power-down mode will stop all clock signals of CPU and peripherals. If WDT is enabled, WDT module will continue to work. All CPU states are saved before entering power-down mode, such as PC, PSW, SFR, RAM, etc.

Two consecutive instructions: first set the SUSLO register to 55H, then set the PD position in the PCON register to 1, so that the SH79F329 enters power-down mode.

The above two consecutive instructions will cause the CPU to clear the SUSLO register or the PD bit in the next machine cycle, and the CPU will not enter the power-down mode.

The PD bit is set to 1 when the last instruction executed before the CPU enters Power-down mode.

Note: If IDL and PD are set at the same time, SH79F329 enters power-down mode. After exiting power-down mode, the CPU will not enter idle mode. After exiting power-down mode, the hardware clears *IDL and PD bits.*

There are two ways to exit the power-down mode: (1)

A valid external interrupt (such as INT1, INT2) causes the SH79F329 to exit the power-down mode. After the interrupt occurs, the oscillator starts, and after the warm-up timer ends, the CPU clock and the external device clock are restored. The PD bit in the SUSLO register and the PCON register will be cleared by hardware, and then the program runs the interrupt service routine. After completing the interrupt service routine, it jumps to the instruction after entering the power-down mode and continues to run.

(2) Reset signal (low level on reset pin, WDT reset if enabled, LVR reset if enabled). After warm-up time, CPU clock will be restored , SUSLO register and PD bit in PCON register will be cleared by hardware, and finally SH79F329 will be reset, and program will start to run from address 0000H. RAM will remain unchanged, while SFR value may change according to different functional modules.

Note: To enter these two low-power modes, you must add three no-operation instructions (NOP) after setting the IDL/PD bit in PCON.

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8.7.4 Registers

Table 8.23 Power Control Register

87H	7th 6th 5th 4th 3rd 2nd 1st 0th							
PCON	·	·	·	·	GF1	GF0	PD	IDL
Read/	·	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write
write reset value (POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVRPIN)	·	·	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
3-2	**GF[1:0] GF[1:0] GF[1:0] GF[1:0]** General flag for software	
1	**PD**	Power-down mode control bits 0: Cleared by hardware when an interrupt or reset occurs 1: Enter power-down mode by software setting
0	**IDL**	Idle mode control bit 0: Cleared by hardware when an interrupt or reset occurs 1: Enter idle mode by software setting

Table 8.24 Power saving mode control register

8EH	7th 6th 5th 4th 3rd 2nd 1st 0th							
SUSLO	SUSLO.7 SUSLO.6 SUSLO.5 SUSLO.4 SUSLO.3 SUSLO.2 SUSLO.1 SUSLO.0							
Read/	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
write reset value (POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVR POR/WDTI/LVRPIN)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-0	**SUSLO[7:0]**	This register is used to control the CPU to enter power saving mode (idle or power down). Only continuous instructions like the following can Make the CPU enter power saving mode, otherwise the SUSLO, IDL or PD bit will be cleared to 0 by hardware in the next cycle.

Program example:

```
IDLE_MODE:
        MOV SUSLO, #55H
        ORL     PCON, #01H
        NOP
        NOP
        NOP

POWERDOWN_MODE:
        MOV SUSLO, #55H
        ORL     PCON, #02H
        NOP
        NOP
        NOP
```

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8.8 Warm-up counter

8.8.1 Features

ÿ Built-in power preheat counter eliminates unstable power-on state

ÿ Built-in oscillator warm-up counter eliminates unstable state when oscillator starts oscillation

SH79F329 has a built-in power-on preheating counter, which is mainly used to eliminate the unstable state when the power-on voltage is established, and to complete some internal initialization sequences, such as reading Get internal customer code options, etc.

The SH79F329 has a built-in oscillator warm-up counter, which can eliminate the unstable state of the oscillator when it starts oscillating in the following situations: power-on reset, pin reset, from low power mode The types include wake-up, watchdog reset and LVR reset.

After power-on, SH79F329 will first go through the power-on preheating counting process, wait for overflow, and then go through the oscillator preheating counting process, and start running the program after overflow .

Power on preheating count time

Power-on reset/ Pin reset/low voltage reset power on		Watchdog reset (in non-power-down mode) Interrupt wake-up in power-down mode Watchdog reset (in power-down mode)					
Warm-up count time	Oscillator Power-up Warm-up count time	Power on Warm-up count time	Oscillator Power-up Warm-up count time	Power on Warm-up count time	Oscillator Power-up Warm-up count time	Power on Warm-up count time	Oscillator Power-up Warm-up count time
11ms	have	0.5ms	none	0.008ms	have	0.5ms	have

Oscillator power-on warm-up count time

Oscillator Type	state	Warm-up count time
32.768kHzRC	Power-on reset/pin reset/low voltage reset	27 X COARSE
32.768kHzRC	Interrupt wake-up in power-down mode	27 X COARSE
32.768kHzRC	Watchdog reset (in power-down mode)	27 X COARSE

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8.9 Code Options

OP_EWDT[2]

OP_EWDT[2] OP_EWDT[2] OP_EWDT[2]: 0: In power-down mode, the watchdog timer (WDT) is invalid (default) 1: In power-down mode, the watchdog timer (WDT) is still valid **OP_LVREN[1] OP_LVREN[1]**

OP_LVREN[1]

OP_LVREN[1]: 0: Disable the low voltage reset (LVR) function (default)

1: Enable the low voltage reset (LVR) function

OP_WDT[0]

OP_WDT[0] OP_WDT[0] OP_WDT[0]: 0: Disable the watchdog (WDT) function (default) 1: Enable the watchdog (WDT) function

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9. Analog Front End (AFE)

9.1 Features

25mA, 3V output LDO 2 high-voltage

output ports, 1 open-drain high-voltage output port 4 differential voltage conversions,

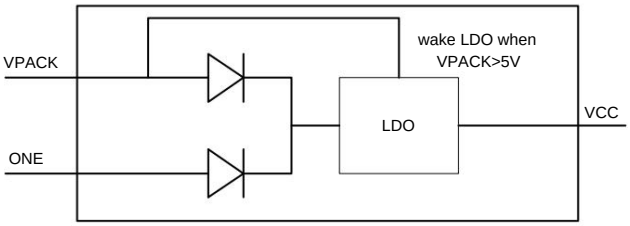
4 internal conduction circuits 3 differential comparators AFE internal

idle and power-down modes

9.2 Power regulator LDO SH79F329 has a built-

in 3V, 25mA power regulator

LDO. When the VPACK voltage is greater than 5V, the LDO is started; when VCC is greater than 2.5V, it enters the normal working mode, using BAT and VPACK dual-end power supply; VCC is less than 2.1V or the PD bit of the AFE internal register output control register (01H) is written 1 to turn off the LDO (if the VPACK voltage is less than 5V).



9.3 AFE Digital Output Ports AFE

has 5 digital output ports: CHG, DSG, OD, TEMP, RSTB. CHG, DSG, OD are high voltage output ports. TEMP, RSTB are low voltage output ports.

CHG, DSG, OD, and TEMP are all controlled by the AFE output register control bit and the AFE status register. When the AFE status register is not 0, or AIDL or APD in the AFE output control register is 1, CHG, DSG, and OD output high level, and TEMP outputs low level. To use it as a normal high-voltage output port, you need to turn off the 4 status detections and clear AIDL and APD.

Pin number name		Output '0'	Output '1'	Remark
10 CHG		The AFE status register (00H) is 0 and AFE output control register CHG (bit 2) = 1 and AFE output control register APD (bit 5) = 0 and AFE output control register AIDL (bit 4) = 0	Any of the left conditions does not hold	High level depends on VPACK
11	DSG	The AFE status register (00H) is 0 and AFE output control register DSG (bit 1) = 1 and AFE output control register APD (bit 5) = 0 and AFE output control register AIDL (bit 4) = 0	Any of the left conditions does not hold	High level depends on BAT
9	OF	The AFE status register (00H) is 0 and AFE output control register OD (bit 3) = 1 and AFE output control register APD (bit 5) = 0 and AFE output control register AIDL (bit 4) = 0	Any of the left conditions does not hold	The output high level needs a pull-up resistor, and the high level is not higher than VPACK
48 TEMP	Any of the conditions on the right is not true		WDF=0 in the AFE status register (00H) and AFE function control register TEMP (bit 5) = 1 and AFE output control register APD (bit 5) = 0 and AFE output control register AIDL (bit 4) = 0	The output low level needs a pull-down resistor, and the low level should not be lower than GND
20 RSTB	LDO is not turned on or is turned off		LDO output is normal	

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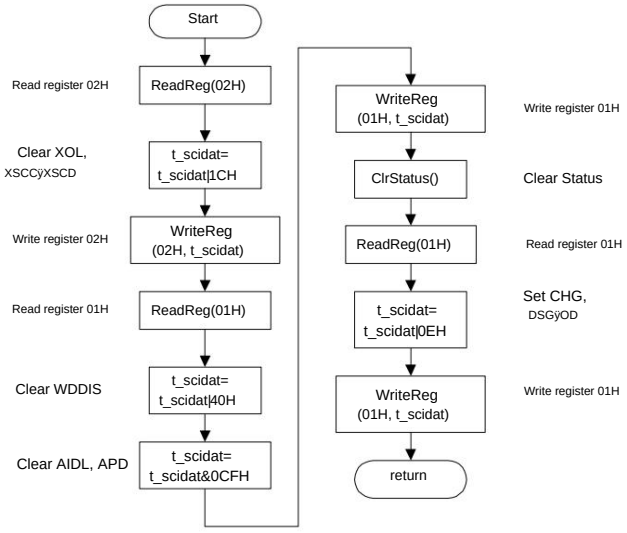
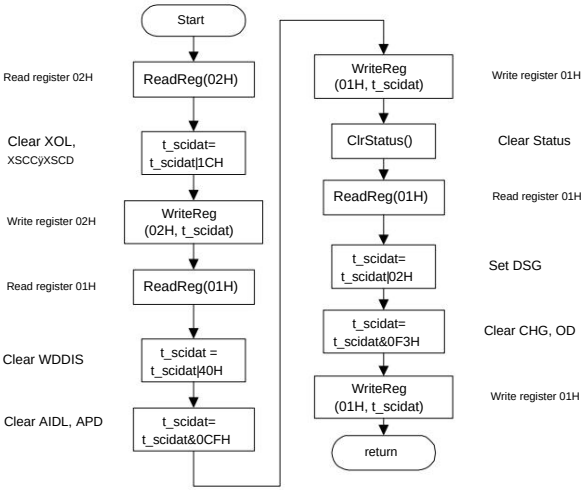
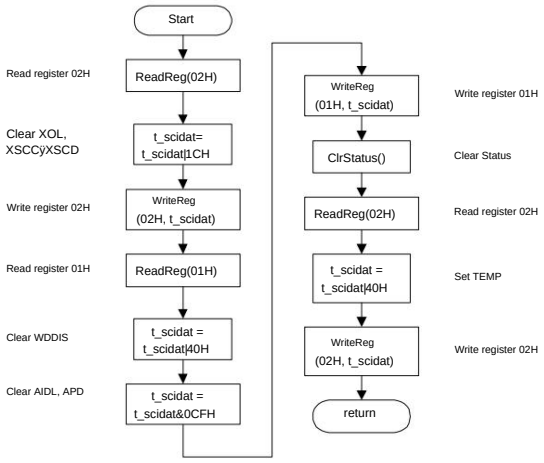
Example: PINCHG = 0, PINDSG = 0, PINOD = 0



Example: PINCHG = 1, PINDSG = 0, PINOD = 1



Example: PINTEMP = 3V



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9.4 AFE Voltage Conversion

The AFE provides VPACK voltage conversion, 4-way differential voltage conversion and internal calibration functions.

AFE can provide VPACK voltage conversion output: Vout = VVPACK/25

AFE can select 4-way differential voltage conversion output (VC1-VC2, VC2-VC3, VC3-VC4, VC4-VC5): VOUT = VREF - 0.15 X (VVCn-VVCn+1)

AFE can output internal voltage reference REF and other internal offset calibration.

The control list is shown in the following table:

VMEN	PACK	CAL	THE	ON0	Remark
0	X	XX	XX	0	
1	1	XX	XX	PACK	VVPACK/25
1	0	11	XX	V3 or VREF	Built-in reference power supply
1	0	10	XX	V2	Measure the built-in reference power supply through the conversion circuit
1	0	01	00	V01	VC5 output zero drift
1	0	01	01	V11	VC4 output zero drift
1	0	01	10	V21	VC3 output zero drift
1	0	01	11	V31	VC2 output zero drift
1	0	00	00	V00	VREF - 0.15 X (VC4-VC5)
1	0	00	01	V10	VREF - 0.15 X (VC3-VC4)
1	0	00	10	V20	VREF - 0.15 X (VC2-VC3)
1	0	00	11	V30	VREF - 0.15 X (VC1-VC2)

Special note: To ensure the accuracy of voltage conversion, please make sure that the internal conduction circuit is not enabled.

From the above formula: VC4-VC5 = (V01-V00)/(V01-V2) X V3

VC3-VC4 = (V11-V10)/(V01-V2) X V3

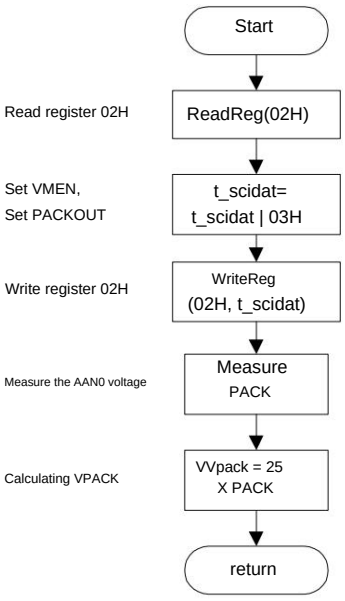
VC2-VC3 = (V21-V20)/(V01-V2) X V3

VC1-VC2 = (V31-V30)/(V01-V2) X V3

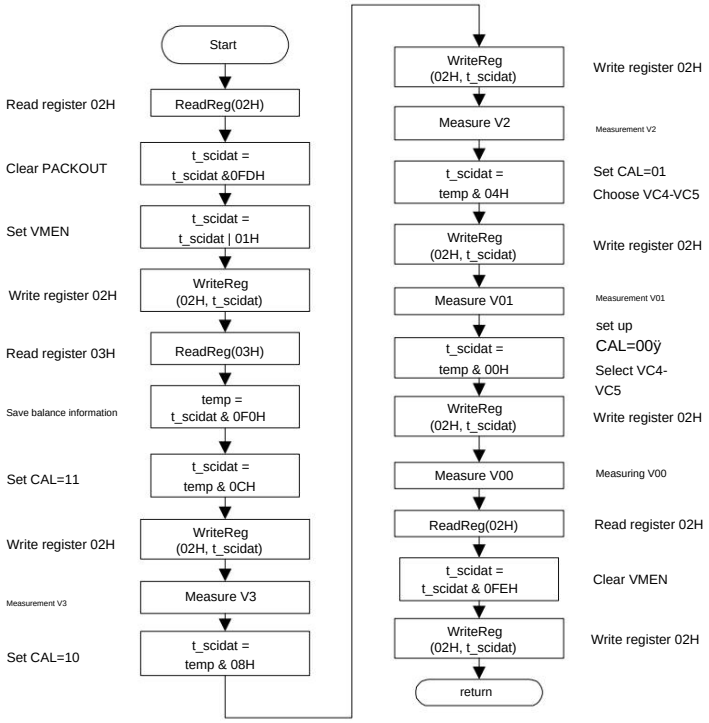
VVPACK = PACK X 25

Among them, VREF is the built-in reference voltage of AFE.

Example: Measuring VPACK Voltage



Measure VC4-VC5 VC4-VC5 VC4-VC5 VC4-VC5 voltage variables



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9.5 AFE Internal Conductive Circuit

AFE provides an internal conduction loop for 4 sets of differential voltages. When the input voltage is 2V, the on-resistance is about 150 ohms.

Special note: To ensure the accuracy of voltage conversion, please make sure that the internal conduction circuit is not enabled.

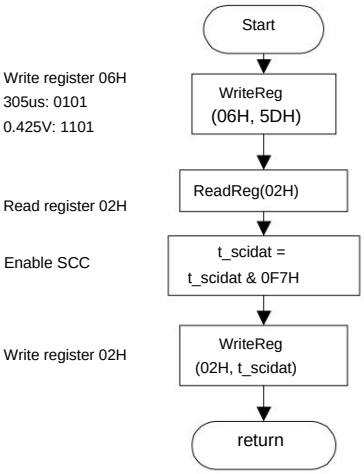
9.6 AFE Communication Monitor

When an AFE communication error occurs, WDF (bit 3) of the AFE Status subregister is set, and AFEIF is set, triggering an AFE interrupt (if EAFE is enabled).

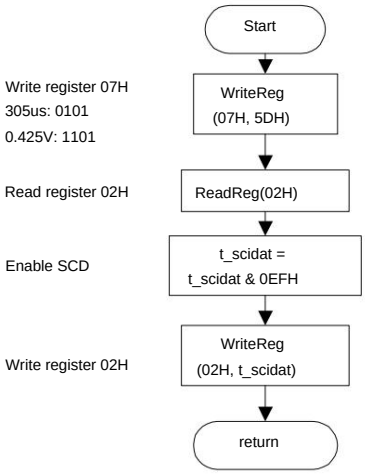
9.7 AFE Analog Comparators AFE

has three analog comparators. Forward comparator 1 is used to detect the voltage difference between ARS1 and ARS2; reverse comparator 1 and reverse comparator 2 are used to detect the voltage difference between ARS2 and ARS1. When the ARS1 and ARS2 voltages meet the conditions, the AFE status subregister is set, and AFEIF is set to trigger the AFE interrupt (if EAFE is enabled). **Set the reverse comparator 1 voltage threshold to**

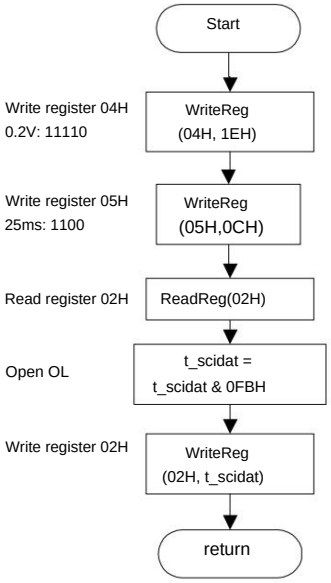
Example: Set the positive comparator 1 voltage threshold to 0.425V and the time delay to 305us



0.425V and the time delay to 305us



Example: Set the voltage threshold of reverse comparator 2 to 0.2V and the time delay to 25ms



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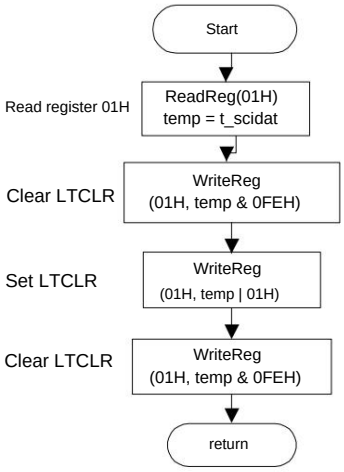
9.8 AFE Status Clear

When the AFE status register is set, the status register and AFE interrupt trigger source can be cleared by writing 0->1->0 to LTCLR in the output control register.

Example: Clear the Status Register



9.9 AFE States and Modes

SH79F329 AFE has 4 abnormal working states or modes: AFE communication error state, AFE analog comparator trigger state, AFE idle low power mode and AFE Power-down low-power mode.

When AFE communication fails or the comparator is triggered, the AFE status register sets the flag bit and triggers the SH79F329 AFE interrupt. Writing '1' to the LTCLR bit and then writing '0' to it clears the AFE status register and the AFE interrupt trigger source.

AFE has two low power modes: AFE idle mode and AFE power-down mode. In AFE idle mode, the comparator and communication detection functions are turned off, and CHG, DSG, and OD Output high level, TEMP output low level, voltage conversion and internal path are closed.

When AFE is in power-down mode, the LDO output is turned off (if VPACK is less than 5V), and the rest is the same as idle mode.

	AFE communication error triggers analog comparator AFE idle mode AFE power-down mode				normal
CHG	1	1	1	1	By register setting
DSG	1	1	1	1	By register setting
OF	1	1	1	1	By register setting
TEMP	0	0	0	0	By register setting
ON0	0	0	0	0	By register setting
Internal access	closure	closure	closure	closure	By register setting
LDO	normal	normal	normal	closure	By register setting
Communication detection	normal	normal	closure	closure	By register setting
Analog comparator normal		normal	closure	closure	By register setting

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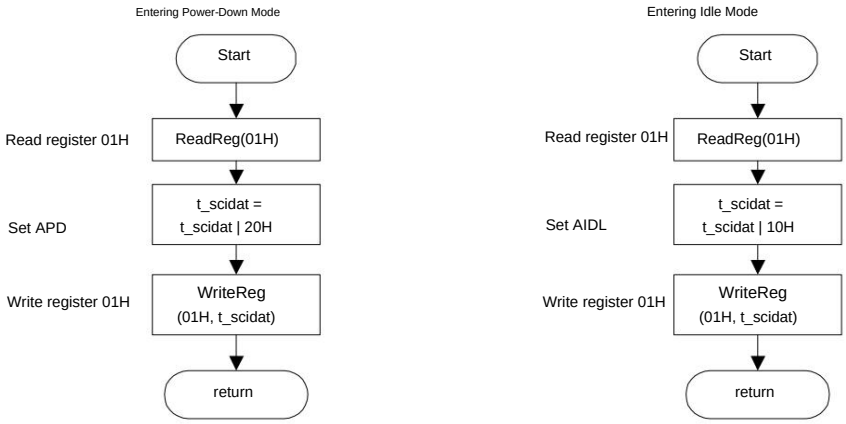
Example:



9.10 AFE Internal Registers

Table 9.1 Analog Front End Status Register

AFE - 00H	**7th 6th 5th 4th 3rd 2nd 1st 0th**							
AFE Status	·	·	·	·	WDF	OL	SCCHG SCDSG	
Read/Write	·	·	·	·	read	read	read	read
ÿÿÿ(BY/LVR BY/LVR BY/LVR BY/LVR)	·	·	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
3	**WDF**	AFE communication flag 0: AFE communication is normal 1: AFE communication error
2	**OL**	**Reverse comparator 2 trigger flag** 0: Inverting comparator 2 is not triggered 1: VARS2-VARS1 is greater than the reverse comparator 2 voltage threshold, and the time exceeds the time threshold
1	**SCCHG**	**Positive comparator 1 trigger flag** 0: Positive comparator 1 is not triggered 1: VARS1-VARS2 is greater than the positive comparator 1 voltage threshold, and the time exceeds the time threshold
0	**SCDSG**	**Reverse comparator 1 trigger flag** 0: Inverting comparator 1 is not triggered 1: VARS2-VARS1 is greater than the reverse comparator 1 voltage threshold, and the time exceeds the time threshold

Special note: When any bit of the AFE status register is set to '1', the SH79F329 AFE interrupt will be triggered (if enabled).

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Table 9.2 Analog front end output control register

AFE - 01H	7th 6th 5th 4th 3rd 2nd 1st 0th							
AFE Output CTL read/write reset	·	WDDIS	APD	AIDL	OF	CHG	DSG	LTCLR
value	·	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
(POR/LVR POR/LVR POR/LVR POR/LVR)	·	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
6	**WDDIS**	AFE communication monitoring control bit 0: Monitor AFE communication 1: Do not monitor AFE communication
5	**APD**	AFE power-down mode control bit 0: Software clearing required 1: AFE enters power-down mode controlled by software
4	**AIDL**	AFE idle mode control bit 0: Software clearing required 1: AFE enters idle mode controlled by software
3	**OF**	OD output control bit 0: OD output high level (external pull-up resistor required) 1: OD output low level
2	**CHG**	CHG output control bit 0: CHG outputs high level (depends on VPACK level) 1: CHG outputs low level
1	**DSG**	DSG output control bit 0: DSG outputs high level (depends on BAT level) 1: DSG output low level
0	**LTCLR**	AFE status reset control bit 0: Normal state 0->1->0: Clear AFE status register

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Table 9.3 Analog front end function control register

AFE - 02H	7th 6th 5th 4th 3rd 2nd 1st 0th							
AFE Func CTL	·	·	TEMP XSCD XSCC			XOL PACKOUT VMEN		
Read/write	·	·	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/LVR POR/LVR POR/LVR POR/LVR)	·	·	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
5	**TEMP**	TEMP output control bit 0: TEMP outputs low level (pull-down resistor required) 1: Output high level (depending on VCC level)
4	**XSCD**	Inverting comparator 1 control bit 0: Enable reverse comparator 1 1: Turn off reverse comparator 1
3	**XSCC**	Positive comparator 1 control bit 0: Enable positive comparator 1 1: Turn off positive comparator 1
2	**SCORE**	Inverting comparator 2 control bit 0: Enable reverse comparator 2 1: Turn off reverse comparator 2
1	PACKOUT PACKOUT PACKOUT PACKOUT	VPACK voltage conversion control bit 0: Disable VPACK voltage conversion 1: AAN0 outputs VPACK/25 (if VMEN = 1)
0	**VMEN**	AAN0 output control bit 0: AAN0 output 0 1: AAN0 outputs VPACK/25 (PACKOUT = 1) or 4-way differential voltage conversion result (PACKOUT = 0)

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Table 9.4 Analog front-end voltage conversion control register

AFE - 03H	7th 6th 5th 4th	3rd 2nd 1st 0th						
AFE CELL_SEL CELL_SEL CELL_SEL	CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0
CELL_SEL	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
read/write reset value (POR/LVR POR/LVR POR/LVR POR/LVR)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7	CB3	VC1-VC2 VC1-VC2 VC1-VC2 VC1-VC2 internal path control bit 0: Close the internal path 1: Open the internal path
6	CB2	VC2-VC3 VC2-VC3 VC2-VC3 VC2-VC3 internal path control bit 0: Close the internal path 1: Open the internal path
5	CB1	VC3-VC4 VC3-VC4 VC3-VC4 VC3-VC4 internal path control bit 0: Close the internal path 1: Open the internal path
4	CB0	VC4-VC5 VC4-VC5 VC4-VC5 VC4-VC5 internal path control bit 0: Close the internal path 1: Open the internal path
3-2	CAL[1:0]	AAN0 differential voltage conversion function control bit 00: Output CELL1-0 selected differential input VOUT = VREF - 0.15 X VCn-VCn+1 01: Output CELL1-0 selects differential input low voltage end zero drift 10: Output built-in REF through conversion circuit 11: Directly output built-in REF
1-0	CELL[1:0]	AAN0 differential voltage conversion selection bit 00: Output VC4-VC5 conversion voltage 01: Output VC3-VC4 conversion voltage 10: Output VC2-VC3 conversion voltage 11: Output VC1-VC2 conversion voltage

Special note: To ensure the accuracy of voltage conversion, please make sure that the internal conduction circuit is not turned on.

Table 9.5 Analog front end reverse comparator 2 voltage control register

AFE - 04H	7th 6th 5th 4th	3rd 2nd 1st 0th						
AFE OLV	·	·	·	READ 4	OLV3	READ2	READ 1	OLV0
Read/Write	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
ÿÿÿ(BY/LVR BY/LVR BY/LVR BY/LVR)	·	·	·	0	0	0	0	0

Bit number	Bit Notation	illustrate
4-0	OLV[4:0]	Inverting Comparator 2 Voltage Threshold Control Register 00000: 0.050V 00001: 0.055V 00010: 0.060V 00011: 0.065V 00100: 0.070V 00101: 0.075V 00110: 0.080V 00111: 0.085V 01000: 0.090V 01001: 0.095V 01010: 0.100V 01011: 0.105V 01100: 0.110V 01101: 0.115V 01110: 0.120V 01111: 0.125V 10000: 0.130V 10001: 0.135V 10010: 0.140V 10011: 0.145V 10100: 0.150V 10101: 0.155V 10110: 0.160V 10111: 0.165V 11000: 0.170V 11001: 0.175V 11010: 0.180V 11011: 0.185V 11100: 0.190V 11101: 0.195V 11110: 0.200V 11111: 0.205V

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Table 9.6 Analog front end reverse comparator 2 delay time control register

AFE - 05H	7th 6th 5th 4th	3rd	2nd	1st	0th			
AFE OLT	·	·	·	·	OLT3	OLT2	OLT1	OLT0
Read/write	·	·	·	·	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/LVR POR/LVR POR/LVR POR/LVR)	·	·	·	·	0	0	0	0

Bit number	Bit Notation	illustrate
3-0	OLT[3:0]	Reverse Comparator 2 Time Threshold Control Register 0000: 1ms 0001: 3ms 0010: 5ms 0011: 7ms 0100: 9ms 0101: 11ms 0110: 13ms 0111: 15ms 1000: 17ms 1001: 19ms 1010: 21ms 1011: 23ms 1100: 25ms 1101: 27ms 1110: 29ms 1111: 31ms

Table 9.7 Analog front end positive comparator 1 delay time control register

AFE - 06H	7th	6th	5th	4th	3rd	2nd	1st	0th
AFE SCC	SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
Read/write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/LVR POR/LVR POR/LVR POR/LVR)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-4	SCCT[3:0]	Positive Comparator 1 Time Threshold Control Register 0000: 0ÿs 0001: 61ÿs 0100: 244ÿs 0101: 305ÿs 1000: 488ÿs 1001: 549ÿs 1100: 732ÿs 1101: 791ÿs 0010: 122ÿs 0011: 183ÿs 0110: 366ÿs 0111: 427ÿs 1010: 610ÿs 1011: 671ÿs 1110: 854ÿs 1111: 915ÿs
3-0	SCCV[3:0]	Positive Comparator 1 Voltage Threshold Control Register 0000: 0.100V 0001: 0.125V 0100: 0.200V 0101: 0.225V 1000: 0.300V 1001: 0.325V 1100: 0.400V 1101: 0.425V 0010: 0.150V 0011: 0.175V 0110: 0.250V 0111: 0.275V 1010: 0.350V 1011: 0.375V 1110: 0.450V 1111: 0.475V

Table 9.8 Analog front end reverse comparator 1 delay time control register

AFE - 07H	7th	6th	5th	4th	3rd	2nd	1st	0th
AFE SCD	SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0
Read/write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
reset value (POR/LVR POR/LVR POR/LVR POR/LVR)	0	0	0	0	0	0	0	0

Bit number	Bit Notation	illustrate
7-4	SCDT[3:0]	Reverse Comparator 1 Time Threshold Control Register 0000: 0ÿs 0001: 61ÿs 0100: 244ÿs 0101: 305ÿs 1000: 488ÿs 1001: 549ÿs 1100: 732ÿs 1101: 791ÿs 0010: 122ÿs 0011: 183ÿs 0110: 366ÿs 0111: 427ÿs 1010: 610ÿs 1011: 671ÿs 1110: 854ÿs 1111: 915ÿs
3-0	SCDV[3:0]	Inverting Comparator 1 Voltage Threshold Control Register 0000: 0.100V 0001: 0.125V 0010: 0.150V 0011: 0.175V 0100: 0.200V 0101: 0.225V 0110: 0.250V 0111: 0.275V 1000: 0.300V 1001: 0.325V 1010: 0.350V 1011: 0.375V 1100: 0.400V 1101: 0.425V 1110: 0.450V 1111: 0.475V

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10. Instruction Set

Arithmetic operation instructions					
instruction		Functional Description	Code	Byte cycle	
ADD A, Rn		Accumulator plus register	0x28-0x2F	1	1
ADD A, direct		Accumulator plus directly addressed byte	0x25	2	2
ADD A, @Ri		Accumulator plus internal RAM	0x26-0x27	1	2
ADD A, #data		Accumulator plus immediate value	0x24	2	2
ADDC A, Rn		Accumulator adds register and carry bit	0x38-0x3F	1	1
ADDC A, direct		Accumulator adds directly addressed byte and carry bit	0x35	2	2
ADDC A, @Ri		Accumulator adds internal RAM and carry bit	0x36-0x37	1	2
ADDC A, #data		Accumulator adds immediate value and carry	0x34	2	2
SUBB A, Rn		bit Accumulator subtracts register and borrow	0x98-0x9F	1	1
SUBB A, direct		bit Accumulator subtracts directly addressed byte and	0x95	2	2
SUBB A, @Ri		borrow bit Accumulator subtracts internal RAM and	0x96-0x97	1	2
SUBB A, #data		borrow bit Accumulator subtracts immediate	0x94	2	2
INC A		value and borrow bit Accumulator adds 1	0x04	1	1
INC Rn		Register plus 1	0x08-0x0F	1	2
INC direct		Directly addressed byte plus 1	0x05	2	3
INC @Ri		Internal RAM plus 1	0x06-0x07	1	3
DEC A		Accumulator	0x14	1	1
DEC Rn		minus 1 Register	0x18-0x1F	1	2
DEC direct		minus 1 Directly addressed	0x15	2	3
DEC @Ri		byte minus 1 Internal RAM minus 1	0x16-0x17	1	3
INC DPTR		Data pointer incremented by 1	0xA3	1	4
MUL AB	8 X 8 16 X 8	Accumulator multiply register B	0xA4	1	11 20
DIV AB	8 / 8 16 / 8	Divide the accumulator by register B	0x84	1	11 20
And A		Decimal Adjustment	0xD4	1	1

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Logical operation instructions

instruction	Functional Description	Code	Byte cycle	
ANL A, Rn	Accumulator and register	0x58-0x5F	1	1
ANL A, direct	Accumulator and direct addressing byte	0x55	2	2
ANL A, @Ri	Accumulator and internal RAM	0x56-0x57	1	2
ANL A, #data	Accumulator and immediate value	0x54	2	2
ANL direct, A	Directly address byte and accumulator	0x52	2	3
ANL direct, #data	Directly address byte and immediate	0x53	3	3
ORL A, Rn	accumulator or register	0x48-0x4F	1	1
ORL A, direct	accumulator or directly address byte	0x45	2	2
ORL A, @Ri	accumulator or internal RAM	0x46-0x47	1	2
ORL A, #data	Accumulator or immediate	0x44	2	2
ORL direct, A	data Direct addressable byte or	0x42	2	3
ORL direct, #data	accumulator Direct addressable byte or	0x43	3	3
XRL A, Rn	immediate data Accumulator	0x68-0x6F	1	1
XRL A, direct	XOR register Accumulator XOR Direct	0x65	2	2
XRL A, @Ri	addressable byte Accumulator XOR	0x66-0x67	1	2
XRL A, #data	internal RAM Accumulator XOR immediate data	0x64	2	2
XRL direct, A	Directly address byte XOR accumulator	0x62	2	3
XRL direct, #data	Directly address byte XOR immediate	0x63	3	3
CLR A	accumulator clear	0xE4	1	1
CPL A	accumulator invert	0xF4	1	1
RL A	Accumulator left ring shift	0x23	1	1
RLC A	accumulator with carry flag left ring shift	0x33	1	1
RR A	accumulator right ring shift	0x03	1	1
RRC A	accumulator with carry flag right ring shift	0x13	1	1
SWAP A	accumulator high 4 bits and low 4 bits exchanged	0xC4	1	4

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Data transfer instructions				
instruction	Functional Description	Code	Byte cycle	
MOV A, Rn	Register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Direct addressing byte to accumulator	0xE5	2	2
MOVE A, @Ri	Internal RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Immediate data to	0x74	2	2
MOV Rn, A	accumulator Accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Directly addressed byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Immediate value to register	0x78-0x7F	2	2
MOV direct, A	Accumulator to direct addressed byte	0xF5	2	2
MOV direct, Rn	Register to direct addressed byte	0x88-0x8F	2	2
MOV direct1, direct2	Directly addressed byte to direct addressed byte	0x85	3	3
MOV direct, @Ri	Internal RAM to direct addressed byte	0x86-0x87	2	3
MOV direct, #data	Immediate value to direct addressed	0x75	3	3
MOV @Ri, A	byte Accumulator to internal RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Direct addressing byte is sent to internal	0xA6-0xA7	2	3
MOV @Ri, #data	RAM. Immediate data is sent	0x76-0x77	2	2
MOV DPTR, #data16	to internal RAM. 16-bit immediate data	0x90	3	3
MOVC A, @A+DPTR	is sent to data pointer. Program code is sent to accumulator (relative data		1	7
MOVC A, @A+PC	pointer). 0x93. Program code is sent to accumulator (relative program counter). 0x83.		1	8
MOVX A, @Ri	External RAM to accumulator (8-bit address)	0xE2-0xE3	1	5
MOVX A, @DPTR	External RAM to accumulator (16-bit address)	0xE0	1	6
MOVX @Ri, A	Accumulator to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	The accumulator is sent to the external RAM (16-bit address). The directly	0xF0	1	5
PUSH direct	addressed byte is pushed to the top of the stack. The	0xC0	2	5
POP direct	top of the stack is popped to the directly addressed	0xD0	2	4
XCH A, Rn	byte. The accumulator is exchanged with the register.	0xC8-0xCF	1	3
XCH A, direct	The accumulator is swapped with the directly addressed byte.	0xC5	2	4
XCH A, @Ri	The accumulator is swapped with the internal RAM.	0xC6-0xC7	1	4
XCHD A, @Ri	The lower 4 bits of the accumulator are swapped with the lower 4 bits of the internal RAM.	0xD6-0xD7	1	4

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Control program transfer instruction

instruction	Functional Description	Code	Byte cycle	
ACALL addr11	Absolute call within 2KB	0x11-0xF1	2	7
LCALL addr16	64KB internal length call	0x12	3	7
RIGHT	subroutine return	0x22	1	8
RARELY	interrupt return	0x32	1	8
AJMP addr11	Absolute transfer within 2KB	0x01-0xE1	2	4
LJMP addr16	64KB long transfer	0x02	3	5
SJMP rel	relatively short	0x80	2	4
JMP @A+DPTR (no jump	transfer relatively long transfer	0x73	1	6
JZ rel occurs) (Transfer occurs)	Branch if accumulator is zero	0x60	2	3 5
JNZ rel (No transfer occurs) (transfer occurs)	Branch if accumulator is non-zero	0x70	2	3 5
JC rel (No transfer occurs) (transfer occurred)	C set transfer	0x40	2	2 4
JNC rel (No transfer occurs) (transfer occurred)	C clear transfer	0x50	2	2 4
JB bit, rel (no transfer occurs) (Transfer occurs)	Direct addressing bit position transfer	0x20	3	4 6
JNB bit, rel (no transfer occurs) (Transfer occurs)	Directly address bits cleared to branch	0x30	3	4 6
JBC bit, rel (no transfer occurs) (Transfer occurs)	Direct addressing sets the bit to transfer and clear the bit	0x10	3	4 6
CJNE A, direct, rel (no transfer occurs) (Transfer occurs)	If the accumulator is not equal to the directly addressed byte, the	0xB5	3	4 6
CJNE A, #data, rel (no transfer occurs) (Transfer occurs)	If the accumulator and the immediate value are not equal, jump	0xB4	3	4 6
CJNE Rn, #data, rel (no transfer occurs) (Transfer occurs)	Transfer when register and immediate value are not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel (no transfer occurs) (Transfer occurs)	Internal RAM and immediate data are not equal to transfer	0xB6-0xB7	3	4 6
DJNZ Rn, rel (no transfer occurs) (Transfer occurs)	Register decremented by 1, jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel (no transfer occurs) (Transfer occurs)	Directly addressed byte minus 1, transfer if not zero	0xD5	3	4 6
NOP	No operation	0	1	1

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Bit operation instructions

instruction	Functional Description	Code	Byte cycle	
CLR C	C is cleared	0xC3	1	1
CLR bit	to clear the directly addressed bit	0xC2	2	3
SETB C	C sets the	0xD3	1	1
SETB bit	direct addressing bit	0xD2	2	3
CPL C	C inverts	0xB3	1	1
CPL bit	the directly addressed bit.	0xB2	2	3
ANL C, bit	C logical AND direct addressing bit	0x82	2	2
ANL C, /bit	C logical inversion of the direct addressing bit	0xB0	2	2
ORL C, bit	C logical or direct addressing bit	0x72	2	2
ORL C, /bit	C logical or direct addressing bit inverse	0xA0	2	2
MOV C, bit	direct addressing bit sent to C	0xA2	2	2
MOV bit, C	C sends direct addressing bit	0x92	2	3

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11. Electrical characteristics

Limit parameters*

BAT/VPACK DC supply voltage . . . . . -0.3V to +34V

DSG, CHG, OD output voltage . . . . . -0.3V to BAT/PACK

VC1-4 input voltage . . . . . -0.3 to +34V

VC5 input voltage . . . . . -0.3 to +4V

VC1-VC2, VC2-VC3, VC3-VC4 input voltage . . . . -0.3 to +8.5V

VDD supply voltage. . . . . -0.3V to +7.0V

Open Drain I/O Voltage . . . . . -0.3 to 6V

ADC Input Pins . . . . . -1 to 1V

GPIO Input/Output Voltage . . . Operating . . . . . GND-0.3V to VDD+0.3V

Ambient Temperature . . . . . -40°C to +85°C

Storage . . . . . -55°C to +125°C

Temperature . . . *Notes

If the device's operating conditions exceed the range of the "Maximum Parameters" on the left, the device will Permanent damage. The device will function only when it is operating within the specified range. Working under the conditions listed in the extreme parameters will affect the Reliability of device operation.

DC Electrical Characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20 - 85°C, fSYS = 8.338MHz, unless otherwise specified)

parameter	Symbol	Min.	Typ.ÿ	Max.	Unit	condition
Operating voltage	VDD		3.0		V	VDD input voltage
Operating Current (VDD + AVDD)	IOP1		4.5	8	mA	All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 8.338MHz, no Flash operation
	IOP2		2.5	4.5 mA		All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 4.194MHz, no Flash operation
	IOP3		1.5	2.5 mA		All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 2.097MHz, no Flash operation
	IOP4		0.8	1.5 mA		All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 1.048MHz, no Flash operation
	IOP5		0.2	0.5 mA		All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 32.768KHz, no Flash operation
Standby Current (VDD + AVDD) (Idle mode: Idle)	ISB1		0.6	0.8 mA		All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 32.768KHz, no Flash operation, all functional modules enabled
	ISB2		100	200	µA	All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 32.768KHz, no Flash operation, all functional modules enabled, CADC and VADC disabled
Standby Current (VDD + AVDD) Power-Down Mode	IPD1		15	25	µA	All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 32.768KHz, PLL off, no Flash operation, watchdog on, all functional modules off
	IPD2			5	µA	All output pins are unloaded, AVDD = VDD = VCC = 3V, internal RC oscillator circuit, fSYS = 32.768KHz, PLL off, no Flash operation, watchdog off, all functional modules off
Operating current (AFE part only)	IAOP1		60	90	µA	VCC, TEMP have no external load, SCI module is turned on VMEN = 1, VC5 = VC4 = 0V, CHG/DSG output low voltage Balance, turn off the balance circuit, AWDT detection, turn on the comparator detection
	IAOP2		25	50	µA	VCC, TEMP have no external load, SCI module is turned on VMEN = 0, VC5 = VC4 = 0V, CHG/DSG output low voltage Balance, turn off the balance circuit, AWDT detection, turn on the comparator detection TA = -25°C to 85°C

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Continued from the table above

parameter	Symbol	Min.	Typ.ÿ	Max.	Unit	condition
Standby current (AFE part only) (AFE Idle Mode: AIDL)	IASB	·	20	40	µA	VCC has no external load, SCI module is enabled, AIDL = 1 TA = -25°C to 85°C
Standby current (AFE part only) (AFE power-down mode: APD)	IAPD	·	0.1	1.0	µA	AVDD/VDD has no external power supply, PACK has no external power supply, APD = 1 TA = -25°C to 85°C
Output high voltage	VOH	0.9VDD	·	VDD	V	P0, P1, P2 ports (except SMBD and SMBC) IOH = 1mA @ VDD = 3V
Output low voltage	VOL1	0	·	0.1VDD	V	P0, P1, P2 ports (except SMBD and SMBC) IOL1 = -1mA @ VDD = 3V
	VOL2	0	·	0.4	V	SMBD and SMBC, IOL2 = -7mA @ VDD = 3V
	VOL3	0.8		1.2	V	P2 port, P2SEL set, IOL3 = -4mA@ VDD = 3V
Input high voltage	V1	0.7VDD		-	V	VDD + 0.3 V P0, P1, P2 ports (Schmitt trigger)
	HIV2	2	·	6	V	SMBD, SMBC
Input low voltage	WILL1	-0.3	·	0.3VDD	V	P0, P1, P2 ports (Schmitt trigger)
	VIL2	-0.3	·	0.8	V	SMBD, SMBC
Pull-up resistor	RUPULUP	·	30	·	kÿ	
Series resistance	RSERIES	200	250	300	ÿ	P2 port internal series resistor (P2SEL is set)

Notice:

1. "ÿ" indicates typical values. Data are at 3.0V, 25° C unless otherwise specified. Measurements at C
2. The system power consumption consists of two parts: the main part (AVDD+VDD) and AFE. Choosing different combinations will result in different final system power consumption.

Low Voltage Reset Electrical Characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20~85°C, fSYS = 8.338MHz, unless otherwise specified.)

parameter	Symbol	Min	Typ	Max	Unit	condition
LVR voltage	VLVRL	2.2	2.3	2.4	V	LVR allows
LVR low voltage reset width TLVR		·	30	·	µs	

VADC Analog/Digital Converter Electrical Characteristics

parameter	Symbol	Min	Typ	Max	Unit	condition
Supply voltage	DEPARTMENT	·	3.0	·	V	
Reference voltage source	VREF	·	1.2	·	V	
Accuracy	No.	·	16	·	bit	GND ÿ VAIN ÿ VREF
A/D input voltage	VVAIN	GND	·	1.23	V	
A/D input resistance	RVAIN	·	8	·	Mÿ	
Integral nonlinearity error	WITH	·	±1	±3	LSB	fOSC = 8.338MHz, AVDD = 3.0V
Offset Error	NO	·	2		mV	fOSC = 8.338MHz, AVDD = 3.0V

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CADC Analog/Digital Converter Electrical Characteristics

	Symbol	Min	Typ	Max	Unit	condition
Parameters Supply	DEPARTMENT	·	3.0	·	V	
voltage Reference	CREF	·	0.3	·	V	
voltage source accuracy	No.	·	16	·	bit	GND ÿ VAIN ÿ VREF
A/D input voltage	ONLY	-0.3	·	0.3		In VRS1, VRS2
A/D differential input voltage	VCAIN	-0.3	·	0.3		In VRS1 - VRS2
A/D input resistance	RCAIN	·	2.5	·	Mÿ	
integral nonlinearity	WITH	·	±1	±3		LSB fOSC = 8.338MHz, AVDD = 3.0V
error offset error	NO	·		200		µV fOSC = 8.338MHz, AVDD = 3.0V

Power Regulator Electrical Characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20 - 85°C, fSYS = 8.338MHz, unless otherwise noted.)

parameter	Symbol	Min	Typ	Max	Unit	condition
LDO startup voltage VSTARTUP 5			·	- V	for VPACK	
VCC start voltage VSTART		2.4	2.5	2.6 V	VVPACK > VSTARTUP	
VCC shutdown voltage VEND regulator		·	2.1	2.3 V	VVPACK > VSTARTUP	
output	VCC	·	3.0	- V		
Regulator Output	VCC	-4%	3 2% V	8.0V < VBAT or VVPACK < 25V, ILOAD < 25mA, TA = -25°C to 85°C		
	VCC	-9%	3 2% V	6.5V < VBAT or VVPACK < 8V, ILOAD < 25mA, TA = -25°C to 85°C		
	VCC	-9%	3 2% V	5.4V < VBAT or VVPACK < 6.5V, ILOAD < 16mA, TA = -25°C to 85°C		
	VCC	-2%	3 2% V	4.5V < VBAT or VVPACK < 25V, ILOAD < 2mA, TA = -25°C to 85°C		
Temperature Drift	ÿVTEMP	·	±0.2	- %	Iout = 2mA, TA = -25°C to 85°C	
Load Regulation	ÿVVCCLOAD	·	7	15 mV	0.1mA < ILOAD < 2mA	
	ÿVVCCLOAD	·	40	100 mV	0.1mA < ILOAD < 25mA	
Linearity	ÿILINE	·	3	10 mV	5.4V <VBAT < 25V, ILOAD = 2mA	

Voltage Converter Electrical Characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20 - 85°C, fSYS = 8.338MHz, unless otherwise noted.)

parameter	Symbol	Min	Typ	Max	Unit	condition
Convert output voltage	VCELL_OUT	·	0.975	±1%	V	VCn - VCn+1 = 0V, 8.0V < VBAT or VVPACK < 25V
	VCELL_OUT	·	0.3	±1%	V	VCn - VCn+1 = 4.5V, 8.0V < VBAT or VVPACK < 25V
Reference voltage output	REF	·	0.975	±1%	V	8.0V < VBAT or VVPACK < 25V
VPACK voltage divider output	VPACK - VPACK/25	±5%	V	5.0V < VVPACK < 25V		
Conversion Factor	K	0.147	0.150	0.153	·	K = (AAN0 output (VC5 = VC4 = 0.0V) - AAN0 output (VC5 = 0.0V, VC4 = 4.5V) / 4.5
	K	0.147	0.150	0.153	·	K = (AAN0 output (VC2 = VC1 = 13.5V) - AAN0 output (VC2 = 13.5V, VC1 = 18V) / 4.5
AAN0 setup time tAAN0		·	5	8	mS	AAN0 outputs VPack voltage conversion result
AAN0 setup time tAAN0		·	5	8	mS	AAN0 outputs CELL voltage conversion result

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Analog Comparator Electrical Characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20 - 85°C, fSYS = 8.338MHz, unless otherwise noted.)

parameter	Symbol	Min	Typ	Max	Unit	condition
Reverse comparator 2 threshold range	VOL	-50	·	-205	mV	
Reverse comparator 2 threshold spacing	ÿVOL	·	5	·	mV	
Reverse comparator 2 threshold hysteresis	VHYS(OL)	7	10	13	mV	
Forward comparator 1 threshold range	VSC	100	·	475	mV	
Reverse comparator 1 threshold range	VSC	-100	·	-475	mV	
Forward comparator 1 threshold spacing	ÿVSC	·	25	·	mV	
Reverse comparator 1 threshold spacing	ÿVSC	·	-25	·	mV	fOSC = 8.338MHz, AVDD = 3.0V
Forward and reverse comparator 1 threshold		40	50	60	mV	fOSC = 8.338MHz, AVDD = 3.0V
hysteresis VHYS(SC) Reverse comparator 2 threshold		40	50	60	mV	VOL = 50mV(min)
accuracy VOL_ACR Reverse comparator 2 threshold		90	100	110	mV	VOL = 100mV
accuracy VOL_ACR Reverse comparator 2 threshold accuracy			205	226	mV	VOL = 205mV(max)
VOL_ACR 184 Forward and reverse comparator 1		80	100	120	mV	forward and reverse VSC = 100 (min)
threshold accuracy VSC_ACR Forward and reverse comparator 1			200	220	mV	forward and reverse VSC = 200
threshold accuracy VSC_ACR 180 Forward and reverse comparator 1 threshold accuracy VSC_ACR 426			475	523	mV	forward and reverse VSC = 475(max)

AFE output pin electrical characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20 - 85°C, fSYS = 8.338MHz, unless otherwise stated bright.)

parameter	Symbol	Min	Typ	Max	Unit	condition
TEMP internal series resistance RDS(on)		·	50	100	ÿ	Rdson = (VVCC - VTEMP)/1mA
DSG output low level	VDSGON	·	·	1	V	VBAT = 5 - 20V, IO = -0.5mA
CHG output low level	VCHGON	·	·	1	V	VVPACK = 5 - 20V, IO = -0.5mA
DSG output high level	VDSGOFF	VBAT-1	·	·	V	VBAT = 5 - 20V, IO = 0.5mA
CHG output high level	VCHGOFF	VPACK-1	·	·	V	VVPACK = 5 - 20V, IO = 0.5mA
DSG rising edge time	tR	·	40	200	µs	CL = 4700pF, VDSG: 10% - 90%
CHG rising edge time	tR	·	40	200	µs	CL = 4700pF, VCHG: 10% - 90%
DSG falling edge time	tF	·	40	200	µs	CL = 4700pF, VDSG: 90% - 10%
CHG falling edge time	tF	·	40	200	µs	CL = 4700pF, VCHG: 90% - 10%
OD low level drive	IOD	6	10	·	mA	external 5V voltage
VCn~VCn+1 on-resistance	RBAL		150 ±50%	ÿ		VCn-VCn+1=2V

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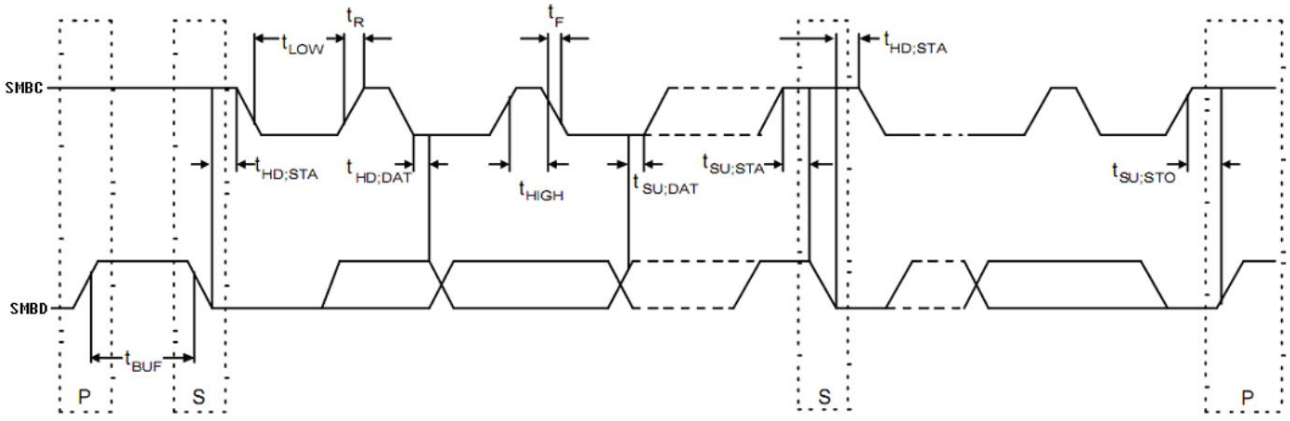
AC Electrical Characteristics (BAT = 14V, VDD = AVDD = VCC, AGND = GND = 0V, TA = -20 - 85°C, fSYS = 8.338MHz, unless otherwise specified.)

parameter	Symbol	Min	Typ	Max	Unit	condition
RC Oscillator Frequency	fRC	·	32.768	·	kHz	VDD = 3.0V, 330Kÿ resistor accuracy -0.1~0.1%, temperature drift 50ppm
Frequency Error	ugly	·	0.5	±2 %		
Frequency Drift	fDIO	·	·	±1 % According to TA = 0-50°C		
Start-up time	fSIO	·	·	200	ms	Frequency Output in ±1%
Frequency Multiplier Power Consumption	IPLL	·	60	·	µA	VDD = 3.0V
Frequency doubler start-up time	tSP	·	2	5	ms	±0.5% Frequency Error
Reset pulse width tPW(RSTB) Low voltage reset pulse		10	·	·	µs	Low level active
width tPW(LVR) Oscillator resistance		·	20	·	µs	LVR allows
	ROSC	·	330 ±0.1% Kÿ Temperature drift 50ppm			
PLL load capacitance	CL	·	1	·	nF	
SMBus Frequency Range	fSMB	10	·	100	kHz	
Bus idle interval low	tBUF	4.7	·	·	µs	
period	tLOW	4.7	·	·	µs	
High level period	tHIGH	4.0	·	50	µs	
Data retention time	tHD: THAT	300	·	·	ns	
Data creation time	tSU: DAT 250		·	·	ns	
STA hold time	tHD: STA	4.0	·	·	µs	
STA establishment time	tSU:STA	4.7	·	·	µs	
STO establishment time	tSU: STO	4.0	·	·	µs	
Rise time	tR	·	·	1000	ns	(VILMAX - 0.15V) to (VIHMIN + 0.15V)
Fall time	tF	·	·	300	ns	0.9VDD to (VILMAX - 0.15)
Timeout period	tTIMEOUT	·	25	·	ms	



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12. Application Circuit

- 4 LED displays - 2

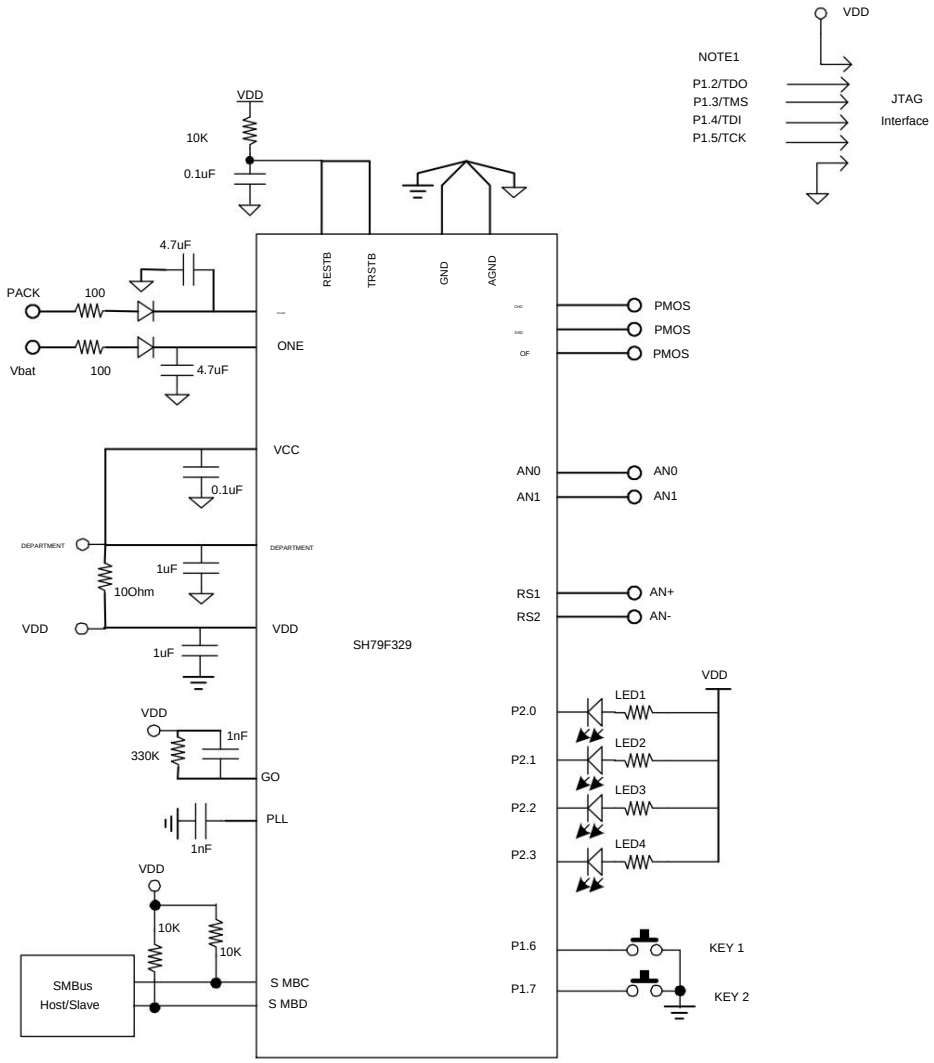
buttons

- SMBus communication

- 2 single-ended voltage

measurements - 1 differential

voltage measurement - 3 PMOS controls



Note: Refer to the JTAG pin connection diagram

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13. Ordering Information

Product Number	Encapsulation
SH79F329U/048UR	TQFP48
SH79F329X/038XU	TSSOP38

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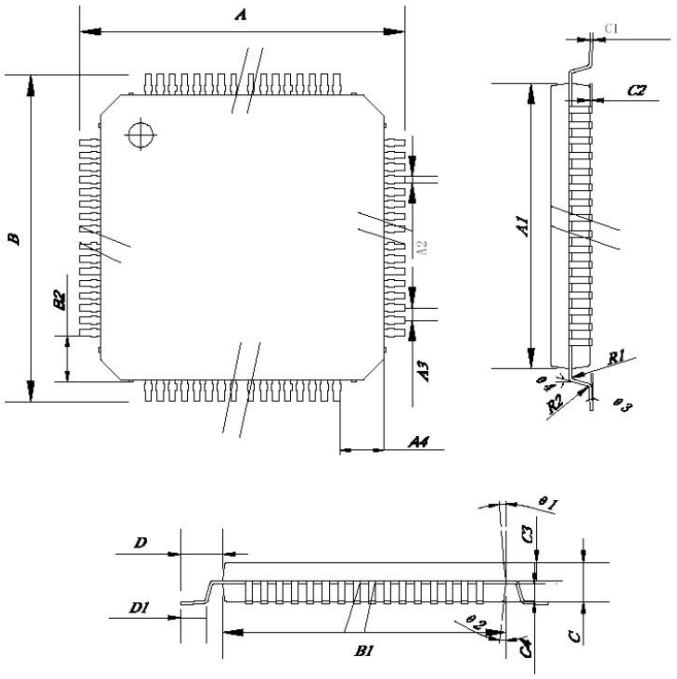
14. Packaging information

TQFP 48 dimensions **(BODY SIZE: 10*10)**

Unit: inches/millimeters



symbol	Dimensions in inchesDimensions in millimeters			
	Min Max Min Max			
A	0.346	0.362	8.80	9.20
A1	0.270	0.278	6.85	7.05
A2	0.006	0.010	0.15	0.25
A3	0.020 Typ.		0.5 Type.	
A4	0.026 Type.		0.65 Type.	
B	0.346 0.362		8.80 9.20	
B1	0.270	0.278	6.85	7.05
B2	0.026 Type.		0.65 Type.	
C	0.035	0.041	0.90	1.05
C1	0.004	0.008	0.09	0.20
C2	0.002	0.006	0.05	0.15
C3	0.017 Type.		0.4365 Type.	
C4	0.017 Type.		0.4365 Type.	
D	0.033 0.045		0.85 1.15	
D1	0.018	0.030	0.45	0.75
R1	0.006 Type.		0.15 Type.	
R2	0.006 Typ.		0.15 Type.	
i1	12° Typ.		12° Type.	
i2	12° Typ.		12° Type.	
i3	0° - 7°		0° - 7°	
i4	7° Type.		7° Type.	

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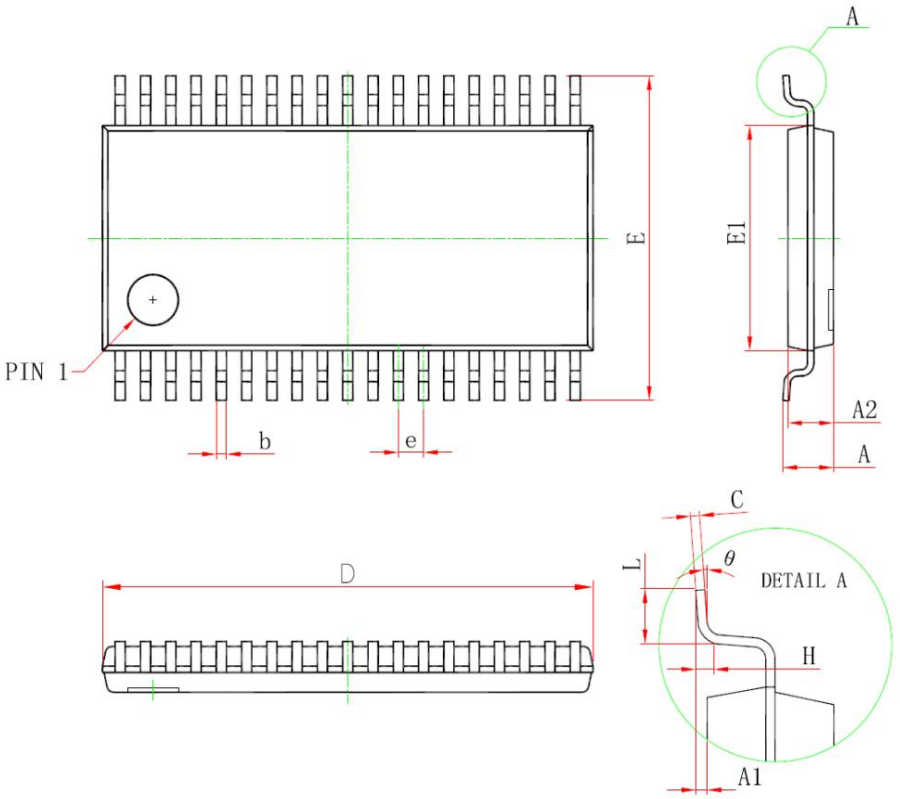
TSSOP 38 form factor

TSSOP38 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177
e	0.50 (BSC)		0.020(BSC)	
H	0.25(TYP)		0.01(TYP)	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

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15. Specification Change Record

Version	Record	date
2.0	Add TSSOP38 package	October 2011
1.0	Initial release	January 2011

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Table of contents

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