SH79F6488/SH79F6489

Enhanced 8051 Microcontroller with 20bit Σ-ΔADC and LCD Driver

1. Features

- 8-bit micro-controller with Pipe-line structured 8051 compatible instruction set
- Flash ROM: 64K Bytes
- RAM: internal 256 Bytes, external 2304 Bytes
- EEPROM-like: build-in 2048 Bytes
- Operation Voltage: V_{DD} = 3V - 5.5V
- Oscillator (code option)
  - Crystal oscillator: 400kHz - 16MHz
  - Crystal oscillator: 32.768kHz
  - Internal RC: 12MHz
  - PLL: 48MHz
- 72 CMOS bi-directional I/O pins
- Built-in pull-up resistor for input pin
- 3 16-bit timer/counters T2, T3, T4
- Base timer (BT)
- Powerful interrupt sources:
  - Timer2, 3, 4, BT
  - INT0, 1, 2, 3, 4
  - PWM0-2, ADC, EUART, SCM, SPI
  - USB (for SH79F6489)
- Enhanced UART (EUART)
- 3 12-bit PWM timer
- LCD driver:
  - 4 X 36 dots (1/4 duty 1/3 bias)
  - 5 X 35 dots (1/5 duty 1/3 bias)
  - 6 X 34 dots (1/6 duty 1/3 bias)
  - Low power LCD
- Built-in regulator
  - Output: 2.7V or 3.3V
- 20-bit Σ-Δ Analog Digital Converter (ADC)
  - 20-bit data output, 16-bit resolution
  - 3 differential input/4 Single-ended inputs
- Built-in Programmable Gain Amplifier (PGA)
  - Gain: 1X-128X
- Built-in Operational Amplifier (OP)
- SH79F6489: The Universal Serial Bus (USB)
  - Compatible with USB2.0 (Full speed 12Mbps)
  - Support control, interrupt and buck data transfer
  - Support 3 endpoints: (EP0, EP1, EP2)
- SPI (Master/Slave Mode)
- Built-in Low Voltage Reset (LVR) function (code option)
  - LVR voltage: 3.1V
  - LVR voltage: 4.0V
- CPU Machine cycle: 1 oscillator clock
- Built-in Watch Dog Timer (WDT) (code option)
- Built-in oscillator Warm-up timer
- Support Low power operation modes:
  - Idle Mode
  - Power-Down Mode
- Flash Type
- Package:
  - LQFP64
  - LQFP80
  - CHIP (90 Pads)

2. General Description

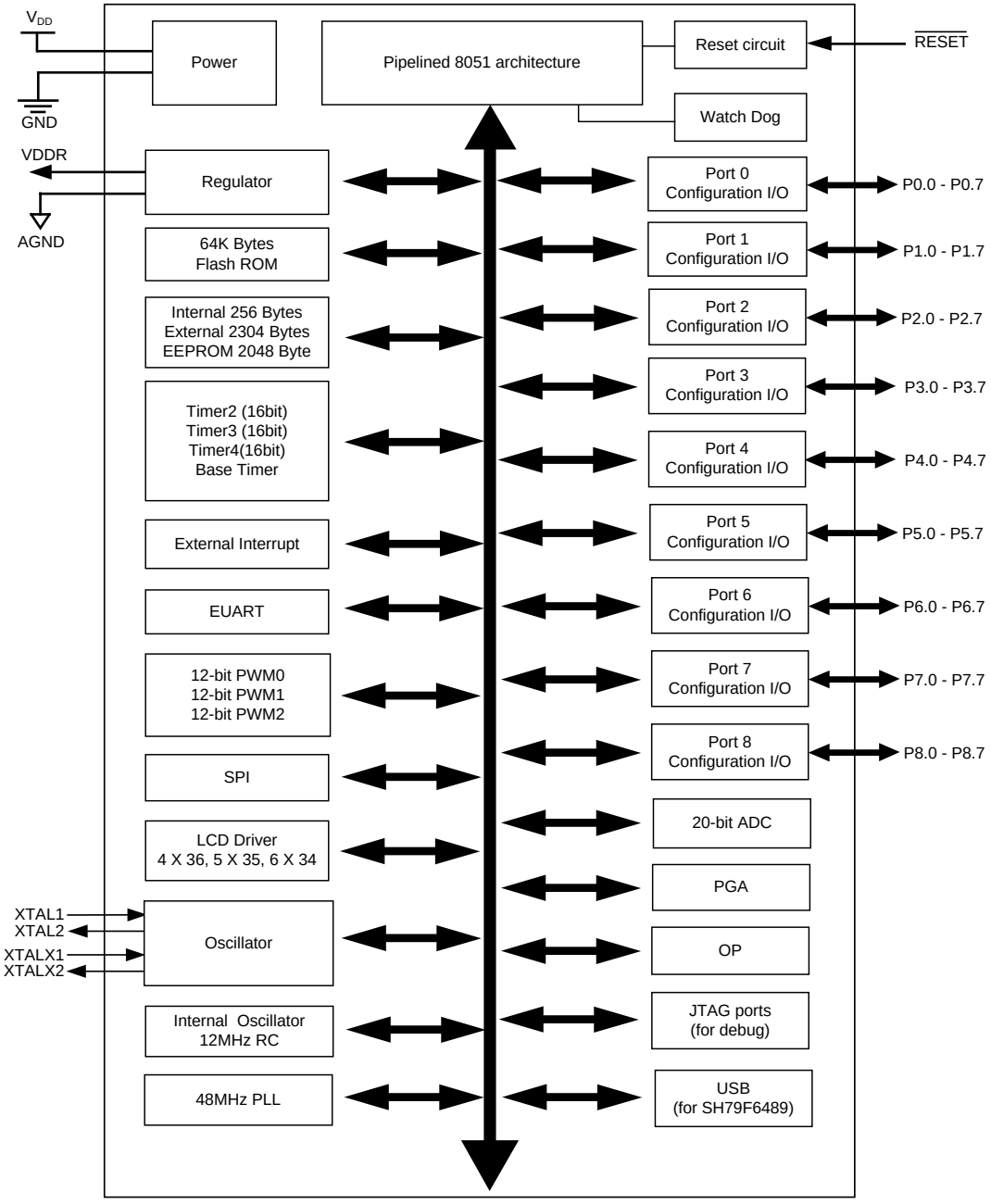
The SH79F6488/SH79F6489 is a high performance 8051 compatible micro-controller, regard to its build-in Pipe-line instruction fetch structure, that helps the SH79F6488/SH79F6489 can perform more fast operation speed and higher calculation performance, if compare SH79F6488/SH79F6489 with standard 8051 at same clock speed.

The SH79F6488/SH79F6489 retains most features of the standard 8051. These features include internal 256 bytes RAM, UART and INT0-2. In addition, the SH79F6488/SH79F6489 provides external 2304 bytes RAM, It also contains 64K bytes Flash memory block both for program and data.

Some standard communication modes such as EUART and SPI are supported in the SH79F6488/SH79F6489. Also the Low power LCD driver, 20-bit Σ-ΔADC, PGA, OP and PWM are incorporated in SH79F6488/SH79F6489. In additation, the Universal Serial Bus (USB) interface is integrated into SH79F6489.

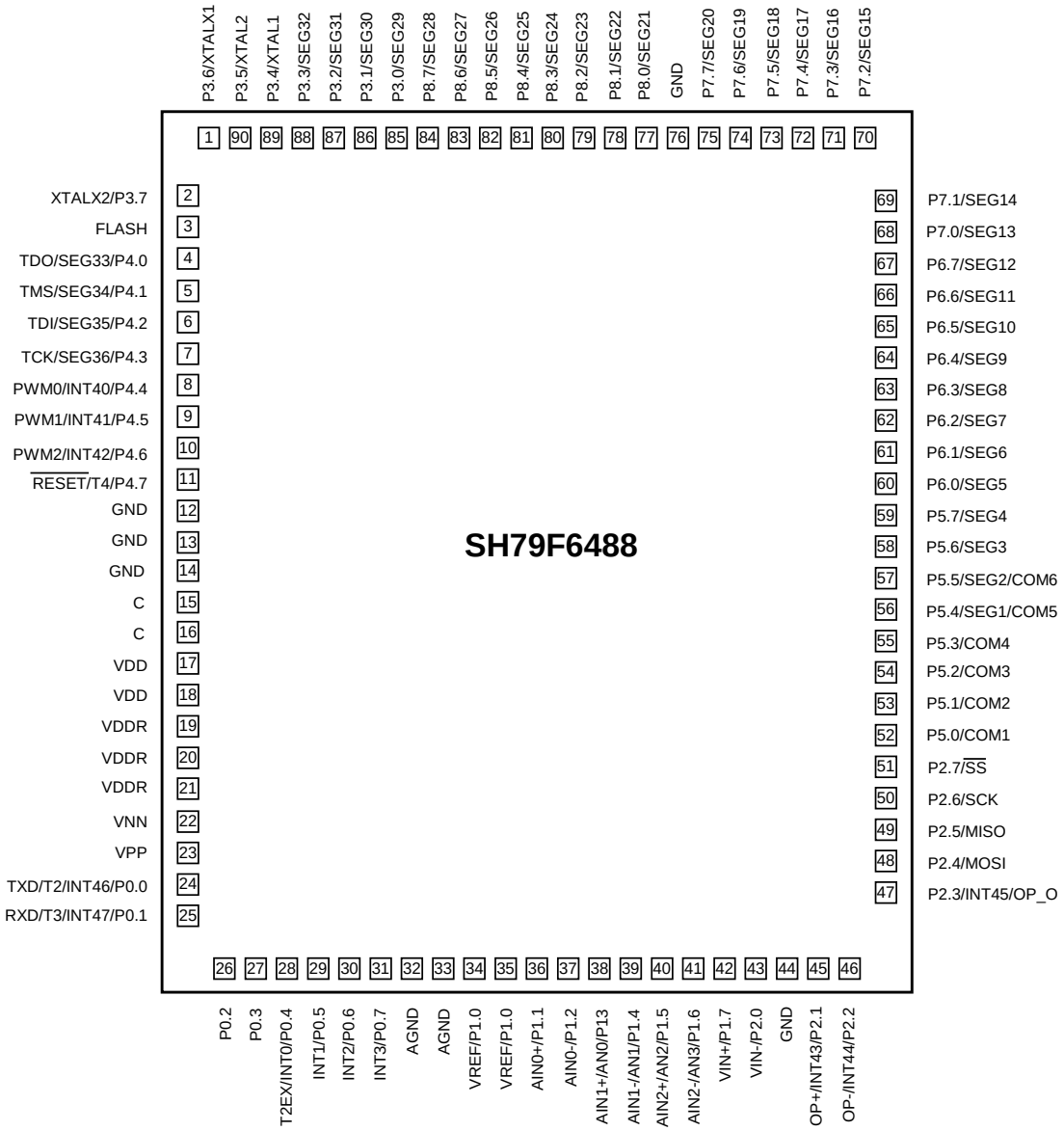
For high reliability and low cost issues, the SH79F6488/SH79F6489 builds in Watchdog Timer, Low Voltage Reset and System Clock Monitor function. And SH79F6488/SH79F6489 also supports two power saving modes to reduce power consumption.

3. Block Diagram

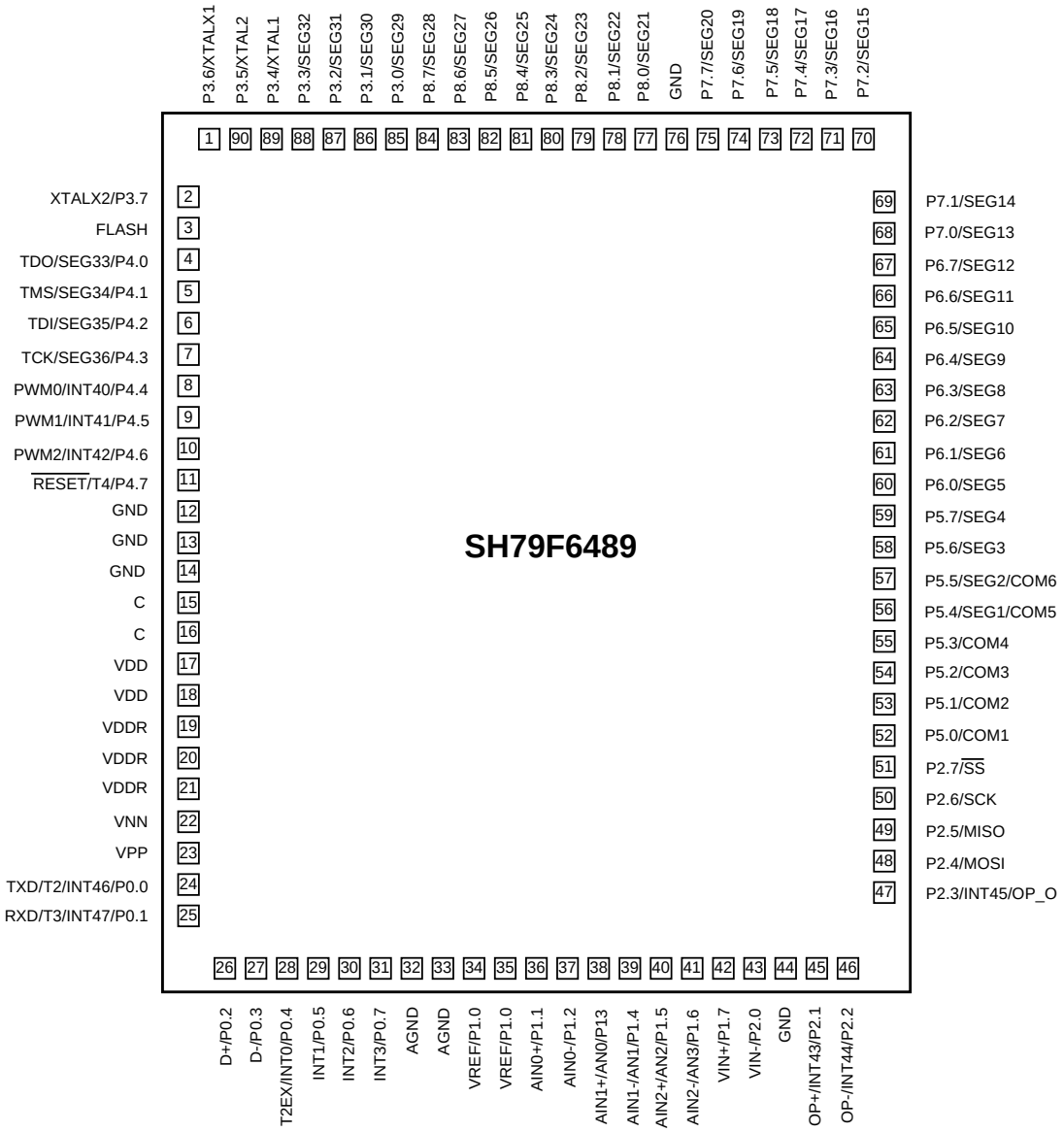


4. Pin Configuration

4.1 Pad Configuration

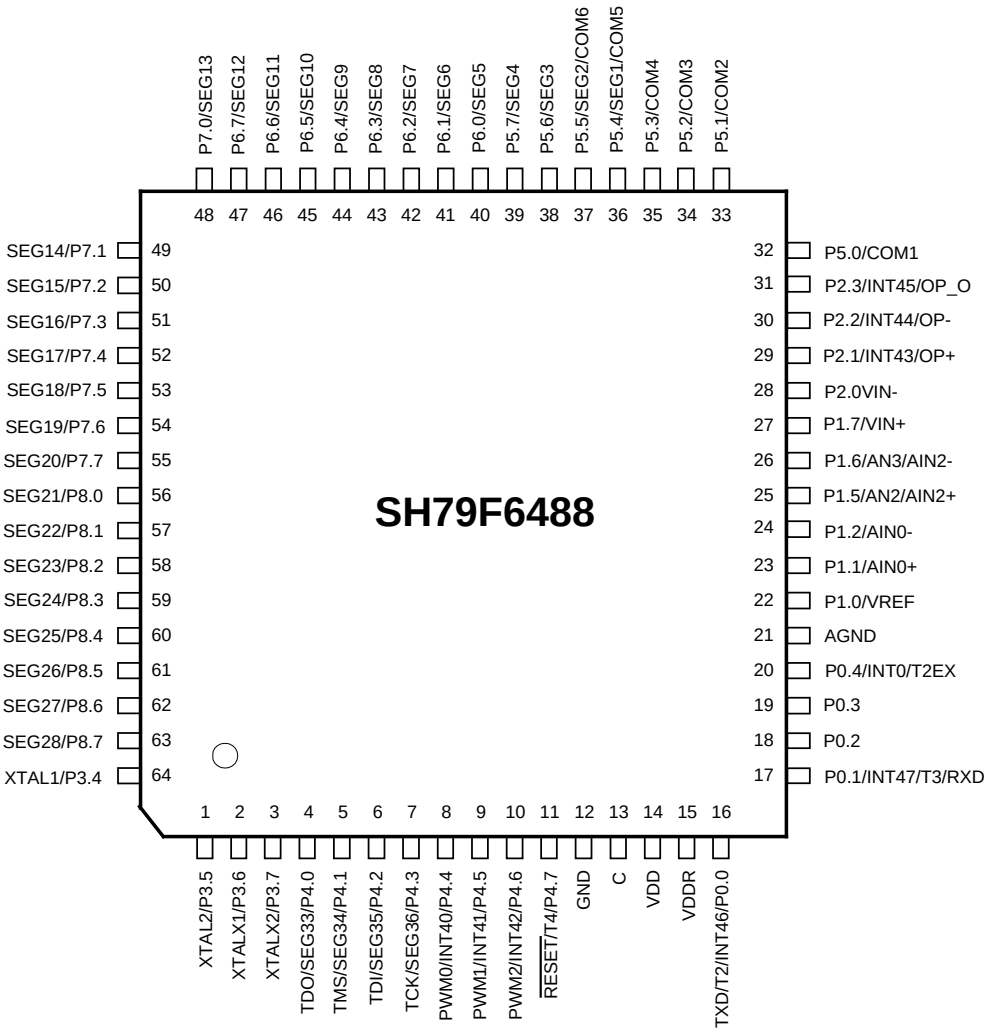


SH79F6488 Pad Configuration Diagram

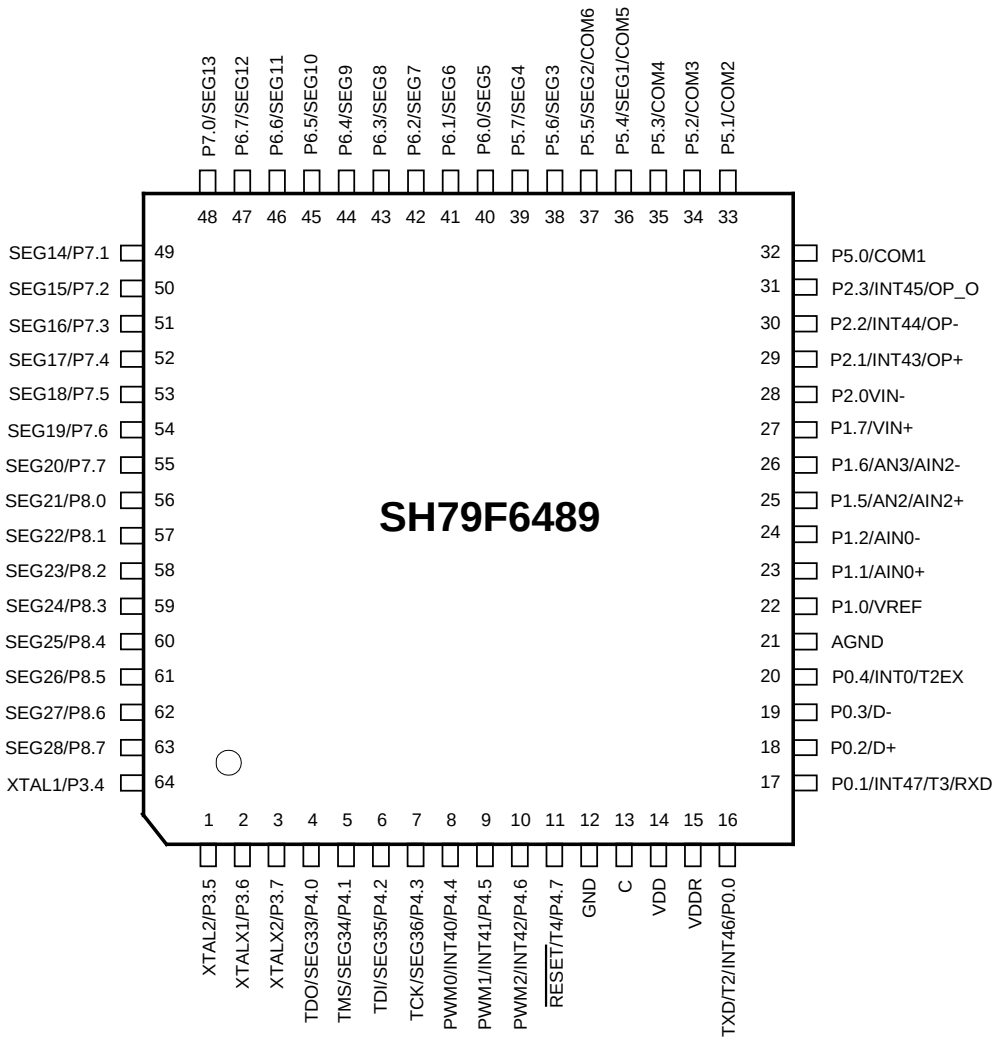


SH79F6489 Pad Configuration Diagram

4.2 Package: LQFP64

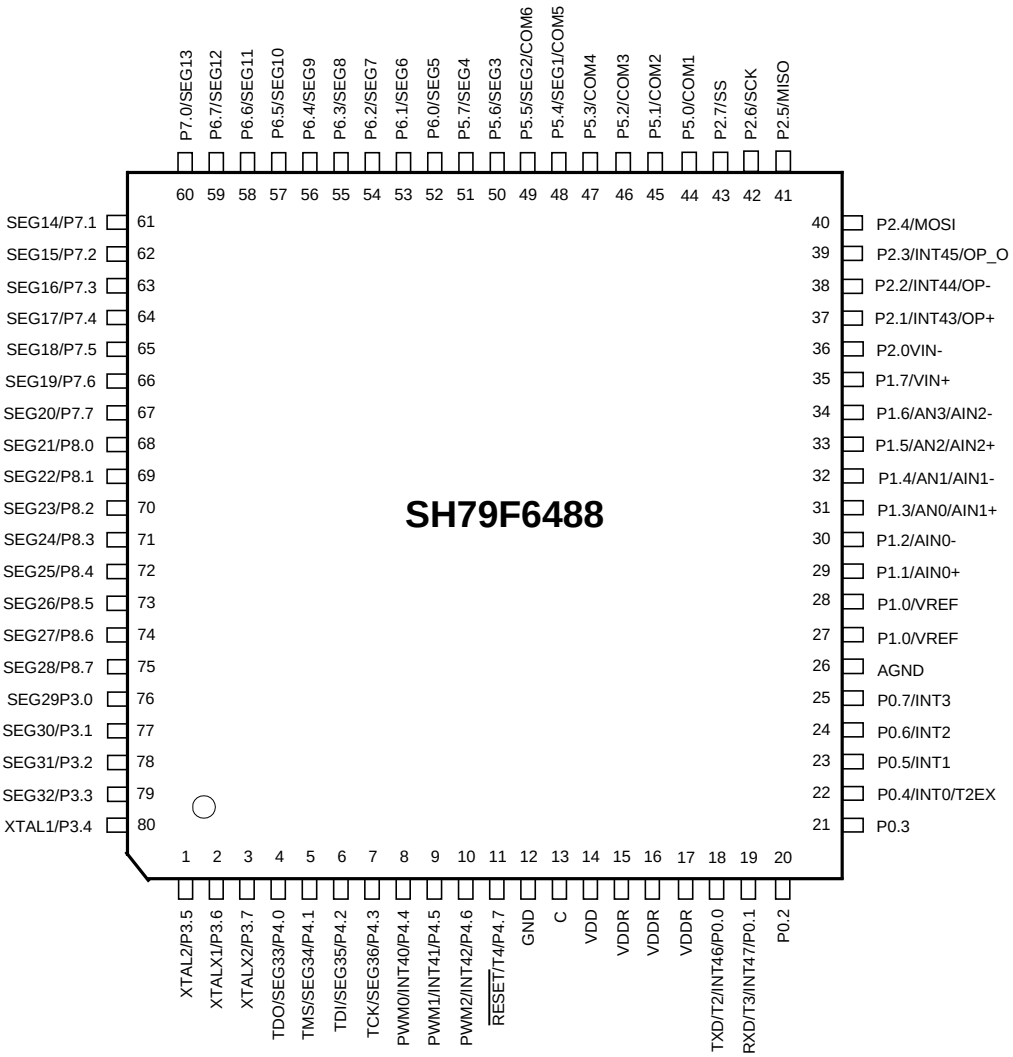


SH79F6488 Pin Configuration Diagram

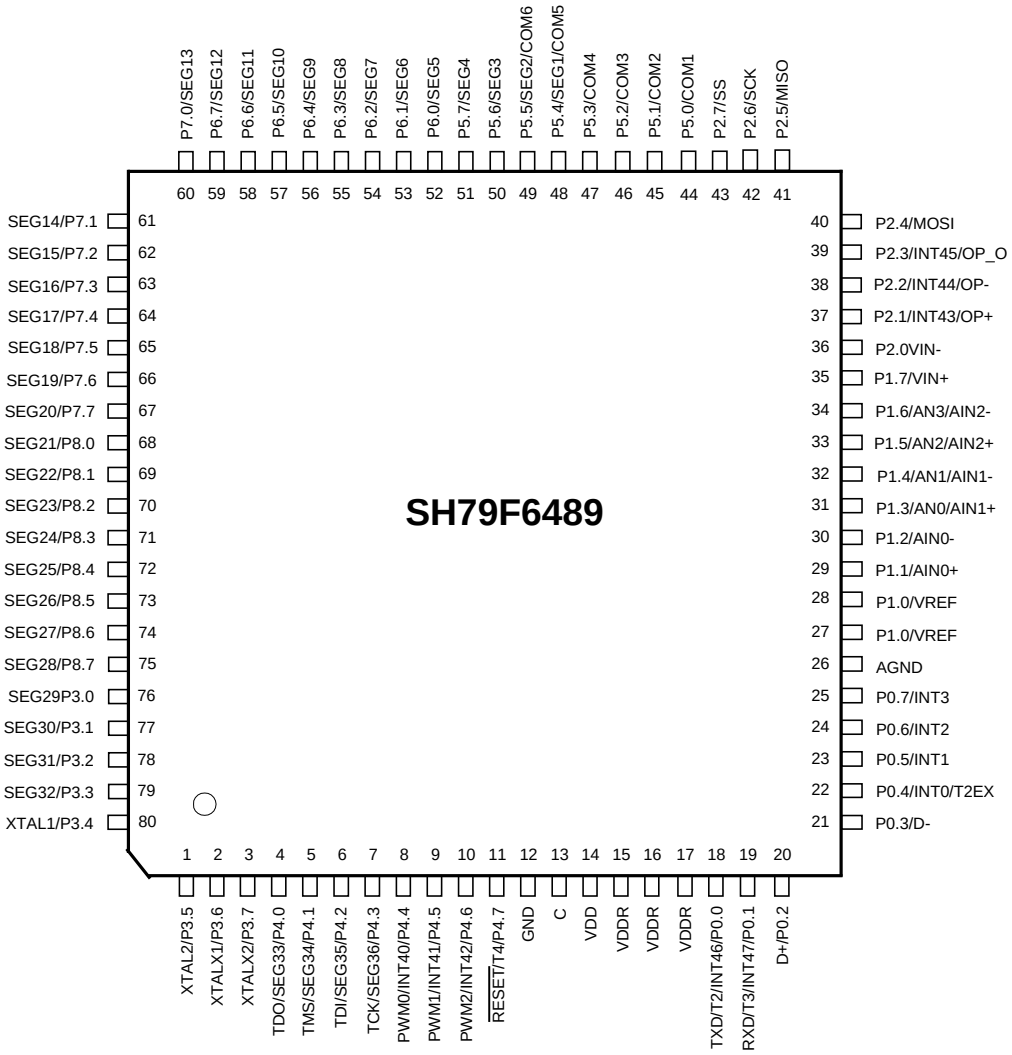


SH79F6489 Pin Configuration Diagram

4.3 Package: LQFP80



SH79F6488 Pin Configuration Diagram



SH79F6489 Pin Configuration Diagram

Table 4.1 Pin Function

Pad No.	LQFP64 Pin No.	LQFP80 Pin No.	Pin Name	Default Function	Pad No.	LQFP64 Pin No.	LQFP80 Pin No.	Pin Name	Default Function
1	2	2	XTALX1/P3.6	XTALX1 or P3.6, by code option	46	30	38	OP-/INT44/P2.2	OP-
2	3	3	XTALX2/P3.7	XTALX2 or P3.7, by code option	47	31	39	OP_O/INT45/P2.3	OP_O
3	/	/	FLASH	FLASH	48	/	40	MOSI/P2.4	P2.4
4	4	4	TDO/SEG33/P4.0	P4.0	49	/	41	MISO/P2.5	P2.5
5	5	5	TMS/SEG34/P4.1	P4.1	50	/	42	SCK/P2.6	P2.6
6	6	6	TDI/SEG35/P4.2	P4.2	51	/	43	$\overline{SS}$/P2.7	P2.7
7	7	7	TCK/SEG36/P4.3	P4.3	52	32	44	COM1/P5.0	P5.0
8	8	8	PWM0/INT40/P4.4	P4.4	53	33	45	COM2/P5.1	P5.1
9	9	9	PWM1/INT41/P4.5	P4.5	54	34	46	COM3/P5.2	P5.2
10	10	10	PWM2/INT42/P4.6	P4.6	55	35	47	COM4/P5.3	P5.3
11	11	11	$\overline{RESET}$ /T4/P4.7	$\overline{RESET}$ or P4.7, by code option	56	36	48	COM5/SEG1/P5.4	P5.4
12	12	12	GND	GND	57	37	49	COM6/SEG2/P5.5	P5.5
13			GND	GND	58	38	50	SEG3/P5.6	P5.6
14			GND	GND	59	39	51	SEG4/P5.7	P5.7
15	13	13	C	C	60	40	52	SEG5/P6.0	P6.0
16			C	C	61	41	53	SEG6/P6.1	P6.1
17	14	14	VDD	VDD	62	42	54	SEG7/P6.2	P6.2
18			VDD	VDD	63	43	55	SEG8/P6.3	P6.3
19	15	15	VDDR	VDDR	64	44	56	SEG9/P6.4	P6.4
20		16	VDDR	VDDR	65	45	57	SEG10/P6.5	P6.5
21		17	VDDR	VDDR	66	46	58	SEG11/P6.6	P6.6
22	/	/	VNN	VNN	67	47	59	SEG12/P6.7	P6.7
23	/	/	VPP	VPP	68	48	60	SEG13/P7.0	P7.0
24	16	18	TXD/T2/INT46/P0.0	P0.0	69	49	61	SEG14/P7.1	P7.1
25	17	19	RXD/T3/INT47/P0.1	P0.1	70	50	62	SEG15/P7.2	P7.2
26	18	20	SH79F6488: P0.2 SH79F6489: D+/P0.2	P0.2	71	51	63	SEG16/P7.3	P7.3
27	19	21	SH79F6488: P0.3 SH79F6489: D-/P0.3	P0.3	72	52	64	SEG17/P7.4	P7.4
28	20	22	T2EX/INT0/P0.4	P0.4	73	53	65	SEG18/P7.5	P7.5
29	/	23	INT1/P0.5	P0.5	74	54	66	SEG19/P7.6	P7.6
30	/	24	INT2/P0.6	P0.6	75	55	67	SEG20/P7.7	P7.7

(to be continued)

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Pad No.	LQFP64 Pin No.	LQFP80 Pin No.	Pin Name	Default Function	Pad No.	LQFP64 Pin No.	LQFP80 Pin No.	Pin Name	Default Function
31	/	25	INT3/P0.7	P0.7	76	/	/	GND	GND
32	21	26	AGND	AGND	77	56	68	SEG21/P8.0	P8.0
33			AGND	AGND	78	57	69	SEG22/P8.1	P8.1
34	22	27	VREF/P1.0	VREF	79	58	70	SEG23/P8.2	P8.2
35		28	VREF/P1.0	VREF	80	59	71	SEG24/P8.3	P8.3
36	23	29	AIN0+/P1.1	AIN0+	81	60	72	SEG25/P8.4	P8.4
37	24	30	AIN0-/P1.2	AIN0-	82	61	73	SEG26/P8.5	P8.5
38	/	31	AIN1+/AN0/P1.3	AIN1+/AN0	83	62	74	SEG27/P8.6	P8.6
39	/	32	AIN1-/AN1/P1.4	AIN1-/AN1	84	63	75	SEG28/P8.7	P8.7
40	25	33	AIN2+/AN2/P1.5	AIN2+/AN2	85	/	76	SEG29/P3.0	P3.0
41	26	34	AIN2-/AN3/P1.6	AIN2-/AN3	86	/	77	SEG30/P3.1	P3.1
42	27	35	VIN+/P1.7	VIN+	87	/	78	SEG31/P3.2	P3.2
43	28	36	VIN-/P2.0	VIN-	88	/	79	SEG32/P3.3	P3.3
44	/	/	GND	GND	89	64	80	XTAL1/P3.4	XTAL1 or P3.4, by code option
45	29	37	OP+/INT43/P2.1	OP+	90	1	1	XTAL2/P3.5	XTAL2 or P3.5, by code option

90 pads

Note:

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram. This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function use.

5. Pin Description

Pin No.	Type	Description
I/O PORT		
P0.0 - P0.7	I/O	8-bit bi-directional I/O port
P1.0 - P1.7	I/O	8-bit bi-directional I/O port
P2.0 - P2.7	I/O	8-bit bi-directional I/O port
P3.0 - P3.7	I/O	8-bit bi-directional I/O port
P4.0 - P4.7	I/O	8-bit bi-directional I/O port
P5.0 - P5.7	I/O	8-bit bi-directional I/O port
P6.0 - P6.7	I/O	8-bit bi-directional I/O port
P7.0 - P7.7	I/O	8-bit bi-directional I/O port
P8.0 - P8.7	I/O	8-bit bi-directional I/O port
Timer/Counter		
T2	I/O	Timer2 external input/output
T3	I	Timer3 external input
T4	I/O	Timer4 external input/output
T2EX	I	Timer2 Reload/Capture/Direction Control
PWM		
PWM0	O	Output pin for 12-bit PWM0 timer
PWM1	O	Output pin for 12-bit PWM1 timer
PWM2	O	Output pin for 12-bit PWM2 timer
EUART		
RXD	I	EUART data input
TXD	O	EUART data output
ADC		
AIN0-	I	Negative differential input ADC pin 0
AIN0+	I	Positive differential input ADC pin 0
AIN1-	I	Negative differential input ADC pin 1
AIN1+	I	Positive differential input ADC pin 1
AIN2-	I	Negative differential input ADC pin 2
AIN2+	I	Positive differential input ADC pin 2
AN0	I	ADC single-ended input pin 0
AN1	I	ADC single-ended input pin 1
AN2	I	ADC single-ended input pin 2
AN3	I	ADC single-ended input pin 3 for battery voltage monitor
VREF	I/O	ADC reference voltage input/output pin, connect 0.1μF capacitor to AGND
VIN+	I/O	PGA positive input/output pin, connect 0.1μF capacitor to VIN-
VIN-	I/O	PGA negative input/output pin, connect 0.1μF capacitor to VIN+
OP		
OP+	I	OP positive input pin
OP-	I	OP negative input pin
OP_O	O	OP Output pin

(to be continued)

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Pin No.	Type	Description
LCD		
COM1 - COM4	O	Common signal output for LCD display
SEG1/COM5	O	Segment 1 signal output or COM5 for LCD display
SEG2/COM6	O	Segment 2 signal output or COM6 for LCD display
SEG3 - SEG36	O	Segment signal output for LCD display
SPI		
MOSI	I/O	SPI master output slave input
MISO	I/O	SPI master input slave output
SCK	I/O	SPI serial clock
$\overline{SS}$	I	SPI Slave Select
SH79F6489: USB		
D+	I/O	USB data positive pin terminal
D-	I/O	USB data negative pin terminal
Interrupt & Reset & Clock & Power		
INT0 - INT3	I	External interrupt 0-3 input source
INT40 - INT47	I	External interrupt 40-47 input source
$\overline{RESET}$	I	The device will be reset by A low voltage on this pin longer than 10us, an internal resistor about 30kΩ to V_{DD}, So using only an external capacitor to GND can cause a PIN reset.
XTAL1	I	Oscillator input
XTAL2	O	Oscillator output
XTALX1	I	OscillatorX input
XTALX2	O	OscillatorX output
GND	P	Ground
AGND	P	Analog Power Ground
VDD	P	Power source (3.0 - 5.5V)
VDDR	P	Power regulator output (2.7V or 3.3V), connect 47μF capacitor to AGND
C	P	Built-in regulator output for core (1.8V), connect 0.47μF capacitor
Programmer		
TDO (SEG33)	O	Debug interface: Test data out
TMS (SEG34)	I	Debug interface: Test mode select
TDI (SEG35)	I	Debug interface: Test data in
TCK (SEG36)	I	Debug interface: Test clock in
FLASH Testing		
FLASH	I	FLASH testing interface, the application of this pin floating
VPP	P	FLASH testing interface, the application of this pin floating
VNN	P	FLASH testing interface, the application of this pin floating

Note:
When SEG33-SEG36 used as debug interface, functions of SEG33-SEG36 are blocked.

6. SFR Mapping

The SH79F6488/SH79F6489 provides 256 bytes of internal RAM to contain general-purpose data memory and Special Function Register (SFR). The SFR of the SH79F6488/SH79F6489 fall into the following categories:

CPU Core Registers:	ACC, B, PSW, SP, DPL, DPH
Enhanced CPU Core Registers:	AUXC, DPL1, DPH1, INSCON, XPAGE
Power and Clock Control Registers:	PCON, SUSLO
Flash Registers:	IB_OFFSET, IB_DATA, IB_CON1, IB_CON2, IB_CON3, IB_CON4, IB_CON5, FLASHCON
Data Memory Register:	XPAGE
Hardware Watchdog Timer Register:	RSTSTAT
System Clock Control Registers:	CLKCON, LCKLO, CLKRC0, CLKRC1
PLL Register:	PLLCON
Interrupt System Registers:	IEN0, IEN1, IENC, IPH0, IPL0, IPH1, IPL1, EXF0, EXF1, TCON
I/O Port Registers:	P0, P1, P2, P3, P4, P5, P6, P7, P8, P0CR, P1CR, P2CR, P3CR, P4CR, P5CR, P6CR, P7CR, P8CR, P0PCR, P1PCR, P2PCR, P3PCR, P4PCR, P5PCR, P6PCR, P7PCR, P8PCR
Timer Registers:	T2CON, T2MOD, TH2, TL2, RCAP2L, RCAP2H, TCON1, T3CON, TL3, TH3, T4CON, TL4, TH4
Base Timer Registers:	BTCON, SEC, MIN
LCD Registers:	LCDCON, LCDCON1, P5SS, P6SS, P7SS, P8SS, PXSS, SPLCON
EUART Registers:	SCON, SBUF, SADEN, SADDR, PCON, SBRTL, SBRTH, SFINE
Regulator Register:	REGCON
PGA Register:	PGAM
OP Register:	OPCON
ADC Registers:	ADCON, ADT, ADCH, ADCDS, ADDL, ADDM, ADDH
SPI Registers:	SPCON, SPSTA, SPDAT
PWM Registers:	PWM0CON, PWM1CON, PWM2CON, PWM0PL, PWM0PH, PWM1PL, PWM1PH, PWM2PL, PWM2PH, PWM0DL, PWM0DH, PWM1DL, PWM1DH, PWM2DL, PWM2DH
USB Registers: (for SH79F6489)	USBCON, USBIF1 ,USBIF2, USBIE1, USBIE2, USBADDR, EP0CON, EP1CON, EP2CON, IEP0CNT, IEP1CNT, IEP2CNT, OEP0CNT, OEP1CNT OEP2CNT

Table 6.1 C51 Core SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	-0--00-0	-	BKS0	-	-	DIV	MUL	-	DPS

Table 6.2 Power and Clock control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 6.3 Flash control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFF SET	FBH	Offset Register for Programming	00000000	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
IB_DATA	FCH	Data Register for Programming	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1	F2H	Flash Memory Control Register 1	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2	F3H	Flash Memory Control Register 2	----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3	F4H	Flash Memory Control Register 3	----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4	F5H	Flash Memory Control Register 4	----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5	F6H	Flash Memory Control Register 5	----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
XPAGE	F7H	Memory Page	00000000	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
FLASHCON	A7H	Flash access control	-------0	-	-	-	-	-	-	-	FAC

Table 6.4 WDT SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H	Watchdog Timer Control	*-***000	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

Note: * : *RSTSTAT initial value is determined by different RESET.*

Table 6.5 CLKCON SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	B2H	System Clock Control Register	111000--	32k_SPDUP	CLKS1	CLKS0	SCMIF	OSC2ON	FS	-	-
PLLCON	B3H	PLL Clock Control Register	------00	-	-	-	-	-	-	PLLON	PLLFS
CLKLO	BDH	Internal RC adjust Contro Register	0---0000	CLKRCEN	-	-	-	CLKLO.3	CLKLO.2	CLKLO.1	CLKLO.0
CLKRC0	BEH	Internal RC adjust Register	uuuuuuuu	CLKRC0.7	CLKRC0.6	CLKRC0.5	CLKRC0.4	CLKRC0.3	CLKRC0.2	CLKRC0.1	CLKRC0.0
CLKRC1	BFH	Internal RC initial adjust Register	uuuuuuuu	CLKRC1.7	CLKRC1.6	CLKRC1.5	CLKRC1.4	CLKRC1.3	CLKRC1.2	CLKRC1.1	CLKRC1.0

Table 6.6 Interrupt SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H	Interrupt Enable Control 0	00000000	EA	EADC	ET2	ES	ET3	EX1	ET4	EX0
IEN1	A9H	Interrupt Enable Control 1	00000000	ESCM	EBT	EPWM	EUSB (for 6489)	EX4	EX3	EX2	ESPI
IPH0	B4H	Interrupt Priority Control High 0	-0000000	-	PADCH	PT2H	PS0H	PT3H	PX1H	PT4H	PX0H
IPL0	B8H	Interrupt Priority Control Low 0	-0000000	-	PADCL	PT2L	PS0L	PT3L	PX1L	PT4L	PX0L
IPH1	B5H	Interrupt Priority Control High 1	00000000	PSCM	PBTH	PPWMH	PUSBL (for 6489)	PX4H	PX3H	PX2H	PSPIH
IPL1	B9H	Interrupt Priority Control Low 1	00000000	PSCM	PBTL	PPWML	PUSBH (for 6489)	PX4L	PX3L	PX2L	PSPIL
EXF0	E8H	External interrupt Control 0	00000000	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
EXF1	D8H	External interrupt Control 1	00000000	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
IENC	BAH	Interrupt 4channel enable control	00000000	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
TCON	88H	External interrupt0/1 Control	----0000	-	-	-	-	IE1	IT1	IE0	IT0

Table 6.7 Port SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	80H (Bank0)	8-bit Port0	00000000	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1	90H (Bank0)	8-bit Port1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2	A0H (Bank0)	8-bit Port2	00000000	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3	B0H (Bank0)	8-bit Port3	00000000	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4	C0H (Bank0)	8-bit Port4	00000000	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5	80H (Bank1)	8-bit Port5	00000000	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
P6	90H (Bank1)	8-bit Port6	00000000	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
P7	A0H (Bank1)	8-bit Port7	00000000	P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
P8	B0H (Bank1)	8-bit Port8	00000000	P8.7	P8.6	P8.5	P8.4	P8.3	P8.2	P8.1	P8.0
P0CR	E1H (Bank0)	Port0 input/output direction control	00000000	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR	E2H (Bank0)	Port1 input/output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR	E3H (Bank0)	Port2 input/output direction control	00000000	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR	E4H (Bank0)	Port3 input/output direction control	00000000	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR	E5H (Bank0)	Port4 input/output direction control	00000000	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR	E1H (Bank1)	Port5 input/output direction control	00000000	P5CR.7	P5CR.6	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P6CR	E2H (Bank1)	Port6 input/output direction control	00000000	P6CR.7	P6CR.6	P6CR.5	P6CR.4	P6CR.3	P6CR.2	P6CR.1	P6CR.0
P7CR	E3H (Bank1)	Port7 input/output direction control	00000000	P7CR.7	P7CR.6	P7CR.5	P7CR.4	P7CR.3	P7CR.2	P7CR.1	P7CR.0
P8CR	E4H (Bank1)	Port8 input/output direction control	00000000	P8CR.7	P8CR.6	P8CR.5	P8CR.4	P8CR.3	P8CR.2	P8CR.1	P8CR.0
P0PCR	E9H (Bank0)	Internal pull-high enable for Port0	00000000	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR	EAH (Bank0)	Internal pull-high enable for Port1	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR	EBH (Bank0)	Internal pull-high enable for Port2	00000000	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR	ECH (Bank0)	Internal pull-high enable for Port3	00000000	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR	EDH (Bank0)	Internal pull-high enable for Port4	00000000	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR	E9H (Bank1)	Internal pull-high enable for Port5	00000000	P5PCR.7	P5PCR.6	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
P6PCR	EAH (Bank1)	Internal pull-high enable for Port6	00000000	P6PCR.7	P6PCR.6	P6PCR.5	P6PCR.4	P6PCR.3	P6PCR.2	P6PCR.1	P6PCR.0
P7PCR	EBH (Bank1)	Internal pull-high enable for Por7	00000000	P7PCR.7	P7PCR.6	P7PCR.5	P7PCR.4	P7PCR.3	P7PCR.2	P7PCR.1	P7PCR.0
P8PCR	ECH (Bank1)	Internal pull-high enable for Port8	00000000	P8PCR.7	P8PCR.6	P8PCR.5	P8PCR.4	P8PCR.3	P8PCR.2	P8PCR.1	P8PCR.0

Table 6.8 Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	C8H Bank0	Timer/Counter2 Control	00--0000	TF2	EXF2	-	-	EXEN2	TR2	C/T2	CP/RL2
T2MOD	C9H Bank0	Timer/Counter2 Mode	0-----00	TCLKP2	-	-	-	-	-	T2OE	DCEN
RCAP2L	CAH Bank0	Timer/Counter2 Reload /Caprure Low Byte	00000000	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	CBH Bank0	Timer/Counter2 Reload /Caprure High Byte	00000000	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH Bank0	Timer/Counter2 Low Byte	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH Bank0	Timer/Counter2 High Byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
T3CON	88H Bank1	Timer/Counter3 Control	0-00-000	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
TL3	8CH Bank1	Timer/Counter3 Low Byte	00000000	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	8DH Bank1	Timer/Counter3 High Byte	00000000	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
T4CON	C8H Bank1	Timer/Counter4 Control	00000000	TF4	TC4	T4PS1	T4PS0	T4M1	T4M0	TR4	T4CLKS
TL4	CCH Bank1	Timer/Counter4 Low Byte	00000000	TL4.7	TL4.6	TL4.5	TL4.4	TL4.3	TL4.2	TL4.1	TL4.0
TH4	CDH Bank1	Timer/Counter4 High Byte	00000000	TH4.7	TH4.6	TH4.5	TH4.4	TH4.3	TH4.2	TH4.1	TH4.0

Table 6.9 Base Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BTCON	C1H	Base Timer Control	0000----	BTEN	BTIF	BTS1	BTS0	-	-	-	-
SEC	C2H	Second and half second	00000000	HSEC	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
MIN	C3H	Minutes Register	-0000000	-	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0

Table 6.10 Regulator SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REGCON	A1H	Regulator Control	------00	-	-	-	-	-	-	REGS	REGEN

Table 6.11 LCD SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON	ABH	LCD Control	000-00--	LCDON	MOD1	MOD0	-	DUTY1	DUTY0	-	-
LCDCON1	AAH	LCD Control1	0-00-000	FCMOD	-	FCCTL1	FCCTL0	-	CONTR2	CONTR1	CONTR0
P5SS	9EH	P0 mode Select	00000000	P5S7	P5S6	P5S5	P5S4	P5S3	P5S2	P5S1	P5S0
P6SS	9FH	P1 mode Select	00000000	P6S7	P6S6	P6S5	P6S4	P6S3	P6S2	P6S1	P6S0
P7SS	ACH	P2 mode Select	00000000	P7S7	P7S6	P7S5	P7S4	P7S3	P7S2	P7S1	P7S0
P8SS	ADH	P3 mode Select	00000000	P8S7	P8S6	P8S5	P8S4	P8S3	P8S2	P8S1	P8S0
PXSS	AEH	PX mode Select	00000000	P4S3	P4S2	P4S1	P4S0	P3S3	P3S2	P3S1	P3S0
SLPCON	AFH	SLP mode Select	-0000000	-	SLPDUTY1	SLPDUTY0	SLPD4	SLPD3	SLPD2	SLPD1	SLPD0

Table 6.12 PWM SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0CON	C5H	PWM0 Control	0000-000	PWM0EN	PWM0S	PWM0CK1	PWM0CK0	-	PWM0IE	PWM0IF	PWM0SS
PWM1CON	C6H	PWM1 Control	0000-000	PWM1EN	PWM1S	PWM1CK1	PWM1CK0	-	PWM1IE	PWM1IF	PWM1SS
PWM2CON	C7H	PWM2 Control	0000-000	PWM2EN	PWM2S	PWM2CK1	PWM2CK0	-	PWM2IE	PWM2IF	PWM2SS
PWM0PH	D2H	PWM0 Period Control high	----0000	-	-	-	-	PWM0P.11	PWM0P.10	PWM0P.9	PWM0P.8
PWM0PL	D1H	PWM0 Period Control low	00000000	PWM0P.7	PWM0P.6	PWM0P.5	PWM0P.4	PWM0P.3	PWM0P.2	PWM0P.1	PWM0P.0
PWM1PH	D4H	PWM1 Period Control high	----0000	-	-	-	-	PWM1P.11	PWM1P.10	PWM1P.9	PWM1P.8
PWM1PL	D3H	PWM1 Period Control low	00000000	PWM1P.7	PWM1P.6	PWM1P.5	PWM1P.4	PWM1P.3	PWM1P.2	PWM1P.1	PWM1P.0
PWM2PH	D6H	PWM2 Period Control high	----0000	-	-	-	-	PWM2P.11	PWM2P.10	PWM2P.9	PWM2P.8
PWM2PL	D5H	PWM2 Period Control low	00000000	PWM2P.7	PWM2P.6	PWM2P.5	PWM2P.4	PWM2P.3	PWM2P.2	PWM2P.1	PWM2P.0
PWM0DH	DAH	PWM0 Duty Control high	----0000	-	-	-	-	PWM0D.11	PWM0D.10	PWM0D.9	PWM0D.8
PWM0DL	D9H	PWM0 Duty Control low	00000000	PWM0D.7	PWM0D.6	PWM0D.5	PWM0D.4	PWM0D.3	PWM0D.2	PWM0D.1	PWM0D.0
PWM1DH	DCH	PWM1 Duty Control high	----0000	-	-	-	-	PWM1D.11	PWM1D.10	PWM1D.9	PWM1D.8
PWM1DL	DBH	PWM1 Duty Control low	00000000	PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
PWM2DH	DEH	PWM2 Duty Control high	----0000	-	-	-	-	PWM2D.11	PWM2D.10	PWM2D.9	PWM2D.8
PWM2DL	DDH	PWM2 Duty Control low	00000000	PWM2D.7	PWM2D.6	PWM2D.5	PWM2D.4	PWM2D.3	PWM2D.2	PWM2D.1	PWM2D.0

Table 6.13 SPI SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPCON	A4H	SPI Control	00000000	DIR	MSTR	CPHA	CPOL	SSDIS	SPR2	SPR1	SPR0
SPSTA	A5H	SPI Status	00000---	SPEN	SPIF	MODF	WCOL	RXOV	-	-	-
SPDAT	A6H	SPI Data	00000000	SPDAT7	SPDAT6	SPDAT5	SPDAT4	SPDAT3	SPDAT2	SPDAT1	SPDAT0

Table 6.14 EUART SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	98H	Serial Control	00000000	SM0/FE	SM1/RXOV	SM2/TXCOL	REN	TB8	RB8	TI	RI
SBUF	99H	Serial Data Buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADEN	9BH	Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
SADDR	9AH	Slave Address	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
PCON	87H	Power & serial Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SBRTH	9CH	Baudrate Generator	00000000	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL	9DH	Baudrate Generator	00000000	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
SFINE	B6H	Baudrate Generator	----0000	-	-	-	-	SFINE.3	SFINE.2	SFINE.1	SFINE.0

Table 6.15 PGA SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGAM	A3H	PGA mode Control	00000000	GAIN3	GAIN2	GAIN1	GAIN0	VINON	CHOP	CHOPC1	CHOPC0

Table 6.16 ADC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	93H	ADC Control	00000000	ADON	ADCIF	VREFIN	VREFS	SCH3	SCH2	SCH1	SCH0
ADT	94H	ADC Time Configuration	00000000	TADC7	TADC6	TADC5	TADC4	TADC3	TADC2	TADC1	TADC0
ADCH	95H	ADC Channel Configuration	00111111	VREF1	VREF0	VREFOS	CH2N	CH2P	CH1N	CH1P	CH0
ADCDS	92H	ADC output mode	-----010	-	-	-	-	-	ADCRATE	VINOS	ADCDF
ADDL	91H	ADC Data Low Byte	----0000	-	-	-	-	A3	A2	A1	A0
ADDM	96H	ADC Data Middle Byte	00000000	A11	A10	A9	A8	A7	A6	A5	A4
ADDH	97H	ADC Data High Byte	00000000	A19	A18	A17	A16	A15	A14	A13	A12

Table 6.17 OP SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPCON	A2H	OP Control	-------10	-	-	-	-	-	-	OPOS	OPEN

Table 6.18 USB SFRs (for SH79F6489)

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBCON	99H Bank1	USB Control	00000--0	ENUSB	SW1CON	SWRST	DPSTA	DMSTA	-	-	GOSUSP
USBIF1	E8H Bank1	USB Interrupt Vector1	00000000	PUPIF	OVERIF	OW	SETUPIF	SOFIF	RESMIF	SUSPIF	USBRSTIF
USBIF2	F8H Bank1	USB Interrupt Vector2	-000-000	-	OEP2IF	OEP1IF	OEP0IF	-	IEP2IF	IEP1IF	IEP0IF
USBIE1	9AH Bank1	USB Interrupt Enable1	00-00000	PUPIE	OVERIE	-	SETUPIE	SOFIE	RESMIE	SUSPIE	PBRSTIE
USBIE2	9BH Bank1	USB Interrupt Enable2	-000-000	-	OEP2IE	OEP1IE	OEP0IE	-	IEP2IE	IEP1IE	IEP0IE
USBADDR	9CH Bank1	USB Device Address	-0000000	-	USBADDR6	USBADDR5	USBADDR4	USBADDR3	USBADDR2	USBADDR1	USBADDR0
EP0CON	98H Bank1	USB Endpoint0 Control	00--0000	IEP0DTG	OEP0DTG	-	-	IEP0STL	IEP0RDY	OEP0STL	OEP0RDY
EP1CON	C0H Bank1	USB Endpoint1 Control	00--0000	IEP1DTG	OEP1DTG	-	-	IEP1STL	IEP1RDY	OEP1STL	OEP1RDY
EP2CON	D8H Bank1	USB Endpoint2 Control	00--0000	IEP2DTG	OEP2DTG	-	-	IEP2STL	IEP2RDY	OEP2STL	OEP2RDY
IEP0CNT	9DH Bank1	USB Endpoint0 input data buffer	----0000	-	-	-	-	IEP0CNT3	IEP0CNT2	IEP0CNT1	IEP0CNT0
IEP1CNT	9EH Bank1	USB Endpoint1 input data buffer	---00000	-	-	-	IEP1CNT4	IEP1CNT3	IEP1CNT2	IEP1CNT1	IEP1CNT0
IEP2CNT	9FH Bank1	USB Endpoint2 input data buffer	-0000000	-	IEP2CNT6	IEP2CNT5	IEP2CNT4	IEP2CNT3	IEP2CNT2	IEP2CNT1	IEP2CNT0
OEP0CNT	A5H Bank1	USB Endpoint0 output data buffer	----0000	-	-	-	-	OEP0CNT3	OEP0CNT2	OEP0CNT1	OEP0CNT0
OEP1CNT	A6H Bank1	USB Endpoint1 output data buffer	---00000	-	-	-	OEP1CNT4	OEP1CNT3	OEP1CNT2	OEP1CNT1	OEP1CNT0
OEP2CNT	A7H Bank1	USB Endpoint2 output data buffer	-0000000	-	OEP2CNT6	OEP2CNT5	OEP2CNT4	OEP2CNT3	OEP2CNT2	OEP2CNT1	OEP2CNT0

***Note**: - :Unimplemented*

SFR Map

Bank0

	Bit addressable	**Non Bit addressable**							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H				IB_OFFSET	IB_DATA				FFH
F0H	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7H
E8H	EXF0	P0PCR	P1PCR	P2PCR	P3PCR	P4PCR			EFH
E0H	ACC	P0CR	P1CR	P2CR	P3CR	P4CR			E7H
D8H	EXF1	PWM0DL	PWM0DH	PWM1DL	PWM1DH	PWM2DL	PWM2DH		DFH
D0H	PSW	PWM0PL	PWM0PH	PWM1PL	PWM1PH	PWM2PL	PWM2PH		D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	TCON1		CFH
C0H	P4	BTCON	SEC	MIN		PWM0CON	PWM1CON	PWM2CON	C7H
B8H	IPL0	IPL1	IENC			CLKLO	CLKRC0	CLKRC1	BFH
B0H	P3	RSTSTAT	CLKCON	PLLCON	IPH0	IPH1	SFINE		B7H
A8H	IEN0	IEN1	LCDCON1	LCDCON	P7SS	P8SS	PXSS	SLPCON	AFH
A0H	P2	REGCON	OPCON	PGAM	SPCON	SPSTA	SPDAT	FLASHCON	A7H
98H	SCON	SBUF	SADDR	SADEN	SBRTH	SBRTL	P5SS	P6SS	9FH
90H	P1	ADDL	ADCDS	ADCON	ADT	ADCH	ADDM	ADDH	97H
88H	TCON						SUSLO		8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	7/F	

Bank1

	Bit addressable	Non Bit addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H	USBIF2 (for 6489)								FFH
F0H	B	AUXC						XPAGE	F7H
E8H	USBIF1 (for 6489)	P5PCR	P6PCR	P7PCR	P8PCR				EFH
E0H	ACC	P5CR	P6CR	P7CR	P8CR				E7H
D8H	EP2CON (for 6489)								DFH
D0H	PSW								D7H
C8H	T4CON				TL4	TH4			CFH
C0H	EP1CON (for 6489)								C7H
B8H	IPL0	IPL1							BFH
B0H	P8				IPH0	IPH1			B7H
A8H	IEN0	IEN1							AFH
A0H	P7					OEP0CNT (for 6489)	OEP1CNT (for 6489)	OEP2CNT (for 6489)	A7H
98H	EP0CON (for 6489)	USBCON (for 6489)	USBIE1 (for 6489)	USBIE2 (for 6489)	USBADDR (for 6489)	IEP0CNT (for 6489)	IEP1CNT (for 6489)	IEP2CNT (for 6489)	9FH
90H	P6								97H
88H	T3CON				TL3	TH3	SUSLO		8FH
80H	P5	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	

Note:

(1) The unused addresses of SFR are not available.

(2) The BKS1 and BKS0 bits in INSTCON register is used to choose the bank0 or bank1. For more detail description please refers to the table 7.2 Data Pointer Select Register.

7. Normal Function

7.1 CPU

7.1.1 CPU Core SFR

Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Table 7.1 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**CY**	**Carry flag bit** 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	**AC**	**Auxiliary Carry flag bit** 0: an auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	**F0**	**F0 flag bit** Available to the user for general purposes
4-3	**RS[1:0]**	**R0-R7 Register bank select bits** 00: Bank0 (Address to 00H-07H) 01: Bank1 (Address to 08H-0FH) 10: Bank2 (Address to 10H-17H) 11: Bank3 (Address to 18H-1FH)
2	**OV**	**Overflow flag bit** 0: no overflow happen 1: an overflow happen
1	**F1**	**F1 flag bit** Available to the user for general purposes
0	**P**	**Parity flag bit** 0: an even number of “one” bits in the Accumulator 1: an odd number of “one” bits in the Accumulator

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

7.1.2 Enhanced CPU core SFRs

- Extended 'MUL' and 'DIV' instructions: 16bits*8bits, 16bits/8bits
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH79F6488/SH79F6489 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bits operand. A new register - the register is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bits operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bits mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8-bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16-bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8-bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16-bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is the same with DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

7.1.3 Registers

Table 7.2 Data Pointer Select Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	BKS1	BKS0	-	-	DIV	MUL	-	DPS
R/W	R/W	R/W	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	-	0

Bit Number	Bit Mnemonic	Description
7-6	**BKS[1:0]**	**SFR Bank Selection Bit** 00: SFR Bank0 selected 01: SFR Bank1 selected 1x: reserved
3	**DIV**	**16-bit/8-bit Divide Selection Bit** 0: 8-bit Divide 1: 16-bit Divide
2	**MUL**	**16-bit/8-bit Multiply Selection Bit** 0: 8-bit Multiply 1: 16-bit Multiply
0	**DPS**	**Data Pointer Selection Bit** 0: Data pointer 1: Data pointer1

7.2 RAM

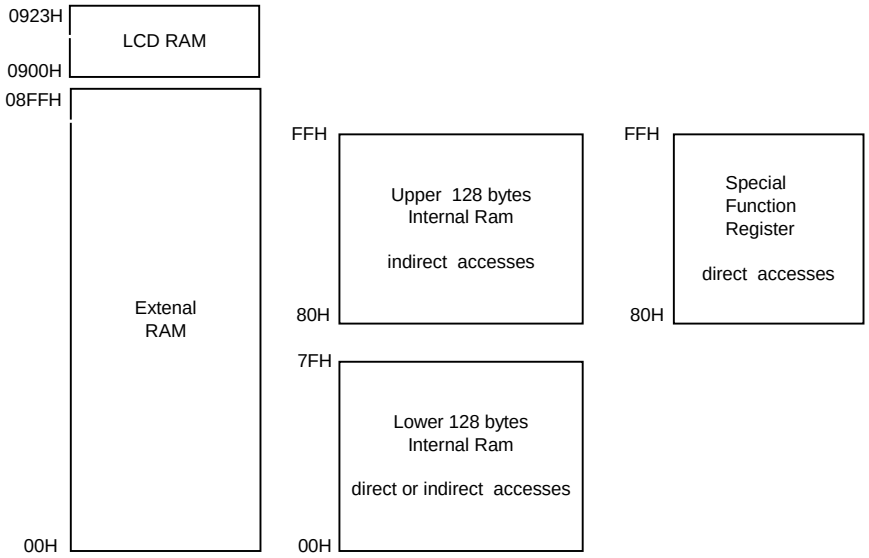
7.2.1 Features

SH79F6488/SH79F6489 provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:

- The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.
- The 2304 bytes of external RAM(addresses 00H to 8FFH) are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.

Note: *the unused address is unavailable in SFR.*



The Internal and External RAM Configuration

The SH79F6488/SH79F6489 provides traditional method for accessing of external RAM. Use *MOVXA, @Ri* or *MOVX @Ri, A;* to access external low 256 bytes RAM; *MOVX A, @DPTR* or *MOVX @DPTR, A* also to access external 256 bytes RAM.

In SH79F6488/SH79F6489 the user can also use XPAGE register to access external RAM only with *MOVX A, @Ri* or *MOVX @Ri, A* instructions. The user can use XPAGE to represent the high byte address of RAM above 256 Bytes.

But SH79F6488/SH79F6489 only has 256 bytes external RAM, XPAGE must be set as 0.

In Flash SSP mode, the XPAGE can also be used as sector selector (Refer to SSP Function).

7.2.2 Registers

Table 7.3 Data Memory Page Register

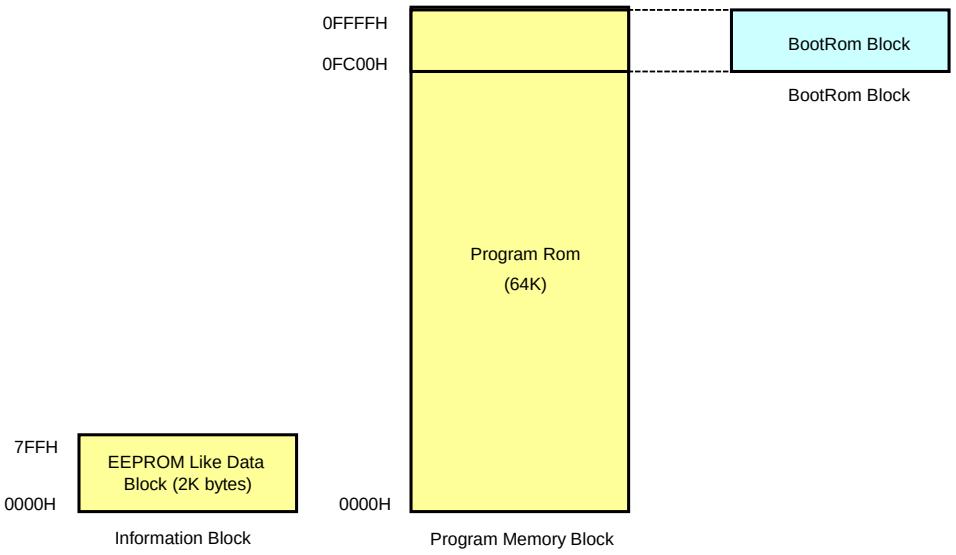
F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**XPAGE[7:0]**	RAM Page Selector

7.3 Flash Program Memory

7.3.1 Features

- The program memory consists 64 X 1KB sectors, total 64KB
- Programming and erase can be done over the full operation voltage range
- Write, read and erase operation are all supported by In-Circuit Programming (ICP)
- Fast mass/sector erase and programming
- Minimum program/erase cycles: 100000
- Minimum years data retention: 10
- Low power consumption



The SH79F6488/SH79F6489 embeds 64K flash program memory for program code. The flash program memory provides electrical erasure and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode.

7.3.2 Flash Operation in ICP Mode

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 wires (V_{DD}, GND, TCK, TDI, TMS, TDO).

At first the four JTAG pins (TDO, TDI, TCK, TMS) are used to enter the programming mode. Only after the three pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the FLASH Programmer's user guide.

The ICP mode supports the following operations:

(1) Code-Protect Control mode Programming

SH79F6488/SH79F6489 implements code-protect function to offer high safeguard for customer code. Two modes are available for each sector.

Code-protect control mode 0: Used to enable/disable the write/read operation (except mass erase) from any programmer.

Code-protect control mode 1: Used to enable/disable the read operation through MOVC instruction from other sectors; or the sector erase/write operation through **SSP** Function.

To enable the wanted protect mode, the user must use the Flash Programmer to set the corresponding protect bit.

(2) Mass Erase

The mass erase operation will erase all the contents of program code, code option, code protect bit and customer code ID, regardless the status of code-protect control mode. (The Flash Programmer supplies customer code ID setting function for customer to distinguish their product.)

Mass erase is only available in Flash Programmer.

(3) Sector Erase

The sector erase operation will erase the contents of program code of selected sector . This operation can be done by Flash Programmer or the user's program.

If done by the Flash Programmer, the code-protect control mode 0 of the selected sector must be disabled.

(4) EEPROM-Like Erase

The EEPROM-Like erase operation will erase the contents of program code of EEPROM-Like. This operation can be done by Flash Programmer or the user's program.

(5) Write/Read Code

The Write/Read Code operation will write the customer code into the Flash Programming Memory or read the customer code from the Flash Programming Memory. This operation can be done by Flash Programmer or the user's program.

If done by the user's program, the code-protect control mode 1 of the selected sector must be disabled. But the program can read/write its own sector regardless of its security bit.

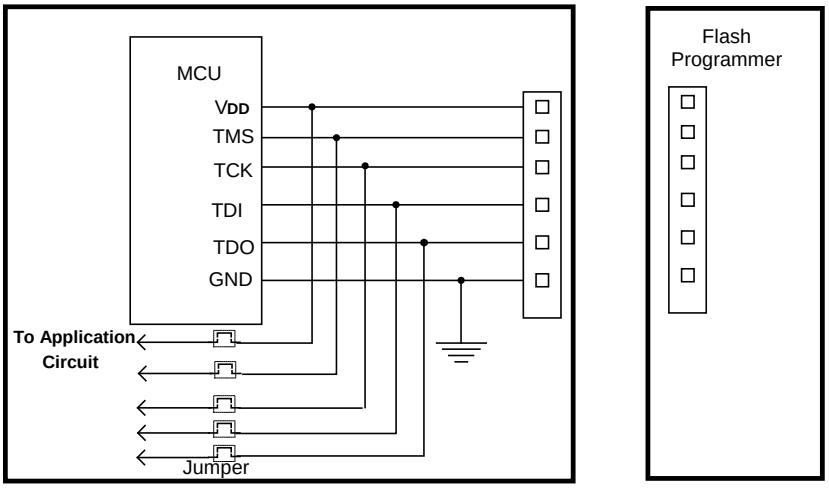
If done by the Flash Programmer, the code-protect control mode 0 of the selected sector must be disabled.

(6) Write/Read EEPROM-Like

The Write/Read EEPROM-Like operation will write the customer data into the EEPROM-Like or read the customer data from the EEPROM-Like. This operation can be done by Flash Programmer or the user's program.

Operation	ICP	SSP
Code Protection	Yes	No
Sector Erase	Yes (without security bit)	Yes (without security bit)
Mass Erase	Yes	No
EEPROM-like Erase	Yes	Yes
Write/Read	Yes (without security bit)	Yes (without security bit or its own sector)
EEPROM-like Write/Read	Yes	Yes

In ICP mode, all the flash operations are completed by the programmer through 6-wire interface. Since the program timing is very sensitive, five jumpers are needed (V_{DD}, TDO, TDI, TCK, TMS) to separate the program pins from the application circuit as the following diagram.



The recommended steps are as following:

(1) The jumpers must be open to separate the programming pins from the application circuit before programming.
(2) Connect the programming interface with programmer and begin programming.
(3) Disconnect programmer and short these jumpers after programming is complete.

7.4 SSP Function

The SH79F6488/SH79F6489 provides SSP (Self Sector Programming) function, each sector can be sector erased or programmed by the user's code if the selected sector is not be protected. But once sector has been programmed, it cannot be reprogrammed before sector erase.

The SH79F6488/SH79F6489 builds in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON1-5), the SSP will be terminated.

7.4.1 SSP Registers

(1) Offset Register for Programming

For Flash memory, one sector is 1024 bytes, register defined as below:

Table 7.4 Offset Register for Programming

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-2	**XPAGE[7:2]**	Sector of the flash memory to be programmed, 000000---means sector 0, and so on
1-0	**XPAGE[1:0]**	High Address of Offset of the flash memory sector to be programmed

Table 7.5 Offset of Flash Memory for Programming

FBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFFSET.7	IB_OFFSET.6	IB_OFFSET.5	IB_OFFSET.4	IB_OFFSET.3	IB_OFFSET.2	IB_OFFSET.1	IB_OFFSET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_OFFSET[7:0]**	Low Address of Offset of the flash memory sector to be programmed

XPAGE[1:0] and IB_OFFSET[7:0] are total 10 bits, stored all sectors within the 1024 bytes offset.

For EEPROM-like memory, one sector is 256 bytes, total 8 sectors, register defined as below:

Table 7.6 Offset Register for Programming

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-3	**XPAGE[7:3]**	Reserved
2-0	**XPAGE[2:0]**	Sector of the flash memory to be programmed, 000: sector0 001: sector1 010: sector2 011: sector3 100: sector4 101: sector5 110: sector6 111: sector7

Table 7.7 Offset of Flash Memory for Programming

FBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_OFFSET[7:0]**	Address of Offset of the flash memory sector to be programmed

IB_OFFSET[7:0] are total 8 bits, stored all EEPROM-like sectors within the 256 bytes offset.

(2) Data Register for Programming

Table 7.8 Data Register for Programming

FCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_DATA[7:0]**	Data to be programmed

(3) SSP Type select Register

Table 7.9 SSP Type select Register

F2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_CON1[7:0]**	**SSP Type select** 0xE6: Sector Erase 0x6E: Sector Programming

(4) SSP Flow Control Register

Table 7.10 SSP Flow Control Register1

F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON2[3:0]**	Must be 05H, else Flash Programming will terminate

Table 7.11 SSP Flow Control Register2

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON3[3:0]**	Must be 0AH else Flash Programming will terminate

Table 7.12 SSP Flow Control Register3

F5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

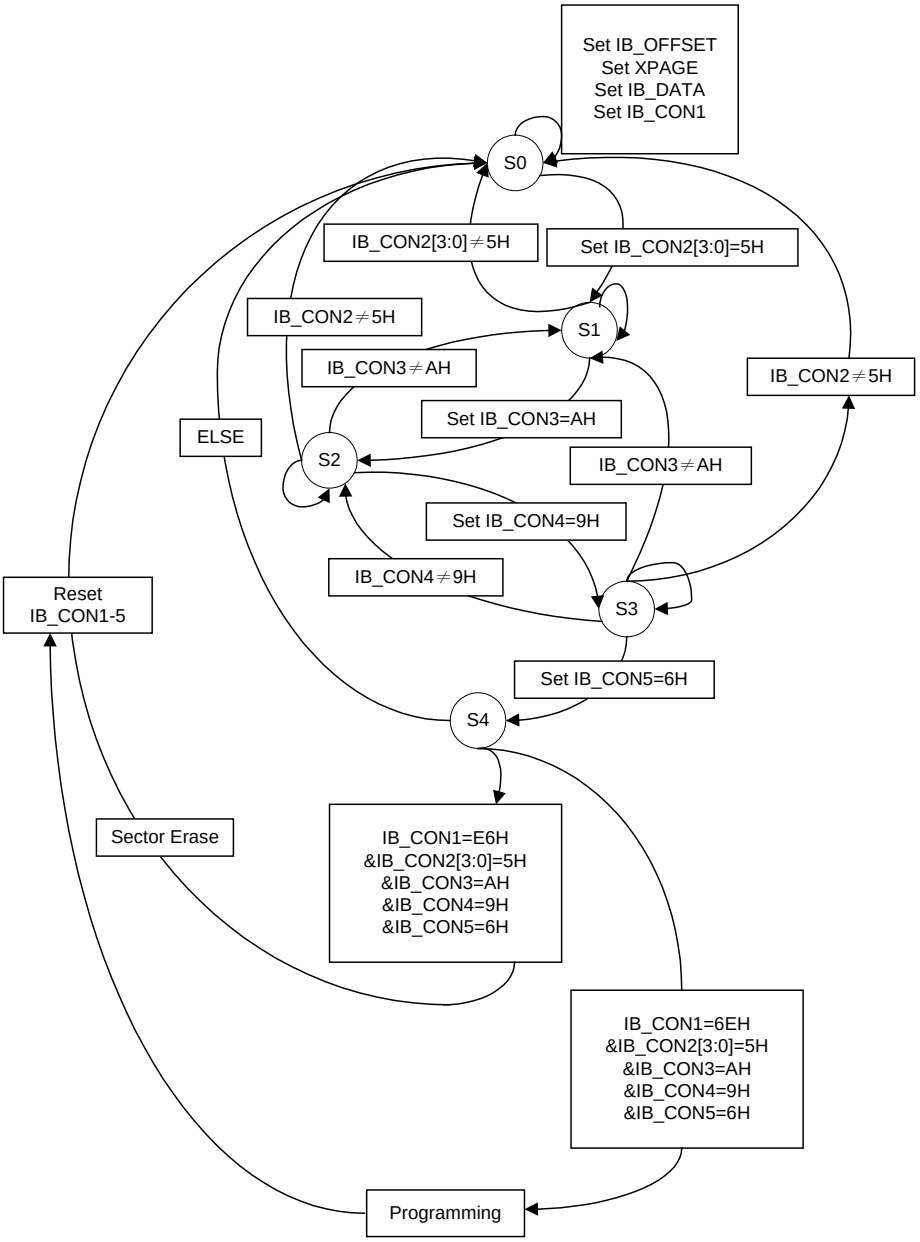
Bit Number	Bit Mnemonic	Description
3-0	**IB_CON4[3:0]**	Must be 09H, else Flash Programming will terminate

Table 7.13 SSP Flow Control Register4

F6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON5[3:0]**	Must be 06H, else Flash Programming will terminate

7.4.2 Flash Control Flow



7.4.3 SSP Programming Notice

To successfully complete SSP programming, the user's software must following the steps below:

(1) For Code/Data Programming:

1. Disable interrupt;
2. Fill in the XPAGE, IB_OFFSET for the corresponding address;
3. Fill in IB_DATA if programming is wanted;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Code/Data programming, CPU will be in IDLE mode;
7. Go to Step 2 if more data are to be programmed;
8. Clear XPAGE; enable interrupt if necessary.

(2) For Sector Erase:

1. Disable interrupt;
2. Fill in the XPAGE for the corresponding sector;
3. Fill in IB_CON1-5 sequentially;
4. Add 4 NOPs for more stable operation;
5. Sector Erase, CPU will be in IDLE mode;
6. Go to step 2 if more sectors are to be erased;
7. Clear XPAGE; enable interrupt if necessary.

(3) For Code Reading:

Just Use "MOVC A, @A+DPTR" or "MOVC A, @A+PC".

(4) For EEPROM-Like:

Steps is same as code programming,the diffenrences are:
1.Set FAC bit in FLASHCON register before programming or erase EEPROM-Like;
2.One sector of EEPROM-Like is 256 bytes.not 1024 bytes.

Table 7.14 Flash Access Control Register

A7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FLASHCON	-	-	-	-	-	-	-	FAC
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Mnemonic	Description
0	**FAC**	**FAC: Flash access control** 0: MOVC or SSP access main memory 1: MOVC or SSP access EEPROM-like

7.5 System Clock and Oscillator

7.5.1 Features

- Four oscillator types: 32.768kHz crystal, crystal oscillator, ceramic oscillator, 12MHz internal RC and PLL
- Built-in 12MHz Internal RC
- Built-in 32.768kHz speed up circuit
- Built-in system clock prescaler

7.5.2 Clock Definition

The SH79F6488/SH79F6489 have several internal clocks defined as below:

32KCRYCLK: the oscillator clock from XTAL 32.768kHz crystal oscillator. f_{32KCRY} is defined as the 32KCRYCLK frequency. t_{32KCRY} is defined as the 32KCRYCLK period.

CRYCLK: the oscillator clock from XTAL or XTALX 400k-16MHz crystal oscillator, ceramic oscillato. f_{CRY} is defined as the CRYCLK frequency. t_{CRY} is defined as the CRYCLK period.

HRCCLK: the oscillator clock from internal 12MHz RC. f_{HRC} is defined as the HRCCLK frequency. t_{HRC} is defined as the HRCCLK period.

PLLCLK: the oscillator clock from PLL. f_{PLL} is defined as the PLLCLK frequency. t_{PLL} is defined as the PLLCLK period.

SCMCLK: the oscillator clock from internal 32kHz monitor RC. f_{SCM} is defined as the SCMCLK frequency. t_{SCM} is defined as the SCMCLK period.

WDTCLK: the internal WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK period.

OSC1CLK: the oscillator clock from one of the four oscillator types. f_{OSC} is defined as the OSCCLK frequency. t_{OSC} is defined as the OSCCLK period.

OSC2CLK: the oscillator clock from one of the four oscillator types. f_{OSC2} is defined as the OSC2CLK frequency. t_{OSC2} is defined as the OSC2CLK period.

Note:

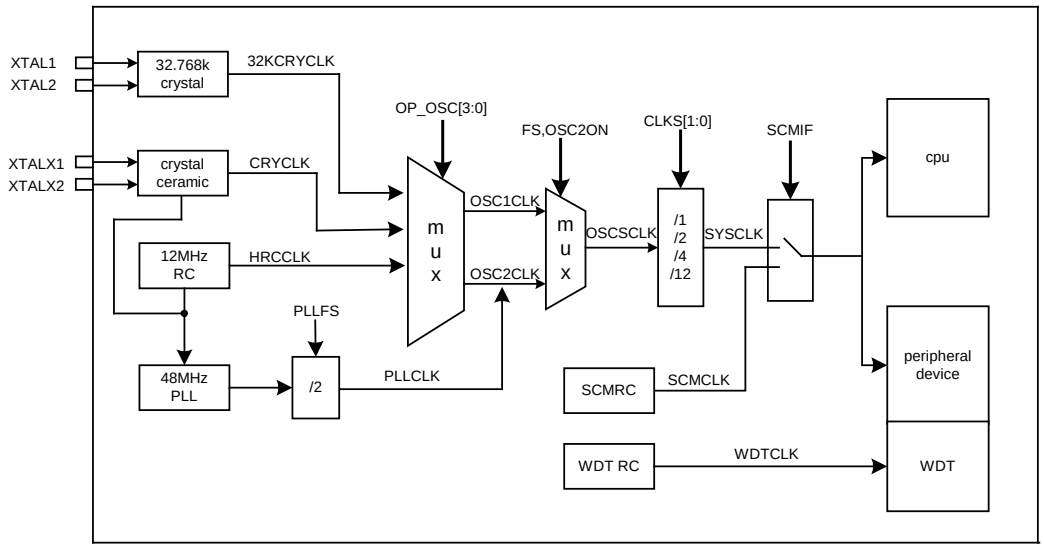
(1) *when code option OP_OSC = 0000, OSC1CLK is internal 12MHz RC,OSC2CLK is PLL (Refer to* ***code option*** *section for details)*

(2) *when code option OP_OSC = 1010, OSC1CLK is 32.768kHz* crystal oscillator*, OSC2CLK is internal 12MHz RC (Refer to* ***code option*** *section for details)*

(3) *when code option OP_OSC = 1010, OSC1CLK is 32.768kHz* crystal oscillator*, OSC2CLK is 400kHz-16Mhz* crystal/ceramic oscillator *or PLL (Refer to* ***code option*** *section for details)*

OSCSCLK: the input of system clock prescaler. It can be OSC1CLK or OSC2CLK. f_{OSCS} is defined as the OSCSCLK frequency. t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output of system clock prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency. t_{SYS} is defined as the SYSCLK period.



7.5.3 Description

SH79F6488/SH79F6489 has four oscillator types: 32.768kHz crystal oscillator, crystal/ceramic oscillator, PLL and internal RC (12MHz), which is selected by code option OP_OSC (Refer to code option section for details). SH79F6488/SH79F6489 have 4 Oscillator pin (XTAL1, XTAL2, XTALX1, XTALX2) and can generates one or two clock sources from four oscillator types. It is selected by code option OP_OSC (Refer to **code option** section for details). The oscillator generates the basic clock pulse that provides the system clock to supply CPU and on-chip peripherals.

When OSC1CLK is used as OSCSCLK (FS = 0), and the system enters Power-down mode, OSC1CLK and OSC2CLK will shut down. If base timer or LCD worked, OSC1CLK will not shut down, but OSC2CLK will.

When OSC2CLK is used as OSCSCLK (FS = 0), and the system enters Power-down mode, OSC2CLK will shut down. OSC1CLK will work for on-chip peripherals (Timer3,base timer and so on)

Internal 12MHz RC support hardware or software adjustion. When CLKRCEN = 0, internal RC is adjusted by hardware. CLKRCEN = 1, internal RC is adjusted by software, by modifying the CLKRC0 register values to adjust the RC frequency. CLKRC1 is the initial adjustion value. When adjust the RC oscillation frequency deviation is larger, users can get correction initial value by read-only register CLKRC1.

7.5.4 Registers

Table 7.15 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	32k_SPDUP	CLKS1	CLKS0	SCMIF	OSC2ON	FS	-	-
R/W	R/W	R/W	R/W	R	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	1	1	1	0	0	0	-	-

Bit Number	Bit Mnemonic	Description
7	**32k_SPDUP**	**32.768kHz oscillator speed up mode control bit** 0: 32.768kHz oscillator normal mode, cleared by software. 1: 32.768kHz oscillator speed up mode, set by hardware or software. This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. And this bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when Power-down mode wakes up. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption. Only when code option OP_OSC is 1010 or 1101, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)
6-5	**CLKS[1:0]**	**SYSCLK Prescaler Register** 00: $f_{SYS} = f_{OSCS}$ 01: $f_{SYS} = f_{OSCS}/2$ 10: $f_{SYS} = f_{OSCS}/4$ 11: $f_{SYS} = f_{OSCS}/12$ If 32.768kHz oscillator is selected as OSCSCLK, these control bits is invalid.
3	**OSC2ON**	**OSC2CLK On control Register** 0: Cleared to turn off OSC2CLK 1: Set to turn on OSC2CLK
2	**FS**	**Frequency Select Register** 0: OSC1CLK is selected as OSCSCLK 1: OSC2CLK is selected as OSCSCLK

Table 7.16 PLL Clock Control Register

B3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PLLCON	-	-	-	-	-	-	PLLON	PLLFS
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1	**PLLON**	**PLL On control Register** 0: PLL off 1: PLL on Only when OSC2ON = 1, this bit is valid.
0	**PLLFS**	**PLL system clock select Register** 0: PLL is not selected as OSC2CLK 1: PLL is selected as OSC2CLK PLL 1/2 Prescaler frequency used as OSC2CLK, OSC2CLK = 24MHz

Table 7.17 Internal RC adjust control register

BDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKLO	CLKRCEN	-	-	-	CLKLO.3	CLKLO.2	CLKLO.1	CLKLO.0
R/W	R/W	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**CLKRCEN**	**Internal RC software adjust control register** 0: software adjust disable, adjust by hardware 1: software adjust enable, and CLKRC0 is valid
3-0	**CLKLO[3:0]**	**Internal RC software adjust lock register** Only when CLKLO = 0x8A, CLKRC0 could be modified

Table 7.18 Internal RC adjust register

BEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKRC0	CLKRC0.7	CLKRC0.6	CLKRC0.5	CLKRC0.4	CLKRC0.3	CLKRC0.2	CLKRC0.1	CLKRC0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
7-0	**CLKRC0[7:0]**	**Internal RC adjust register** Only when CLKLO = 0x8A, CLKRC0 could be modified. Every adjusting range is about 0.25% Reset value is the factory correction values

Table 7.19 Internal RC initial adjust value register

BFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKRC1	CLKRC1.7	CLKRC1.6	CLKRC1.5	CLKRC1.4	CLKRC1.3	CLKRC1.2	CLKRC1.1	CLKRC1.0
R/W	R	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	u	u	u	u	u	u	u	u

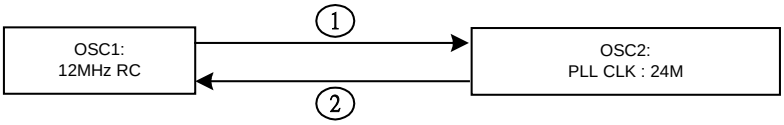
Bit Number	Bit Mnemonic	Description
7-0	**CLKRC1[7:0]**	**Internal RC initial adjust value register** This register is read-only. The data is factory correction values of 12MHz RC.

7.5.5 System Clock Select

1. If code option OP_OSC is 0000, Below for two clocks to be selected.

OSC1: internal 12MHzRC

OSC2: 48MHz PLLCLK 1/2 prescaler



① When OSCSCLK changed from OSC1 to PLL, the steps below must be done in sequence:

a. Set OSC2ON = 1
b. Set PLLON = 1 to turn on the 48MHz PLL
c. Wait at least 2ms
d. Set PLLFS=1 to select PLL as OSC2CLK
e.Set FS = 1 to select PLL as OSCSCLK

②When OSCSCLK changed from PLL to OSC1, the steps below must be done in sequence:

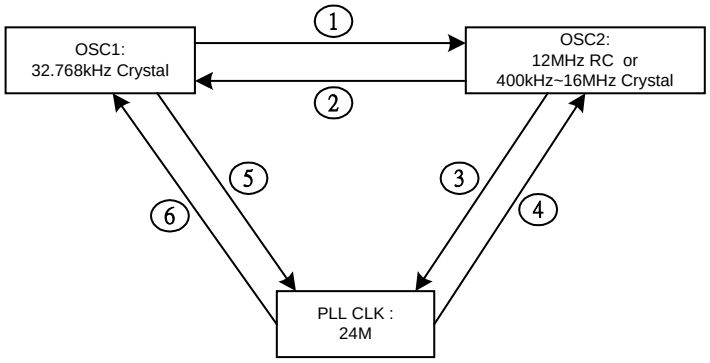
a. Set FS = 0 to select 12MHz RC as OSCSCLK
b. Set PLLON = 0 to turn off PLL, reduce the power consumption of the system

2. If code option OP_OSC is 1010 or 1101, Below for three clocks to be selected.

OSC1:32.768kHz oscillator from XTAL

OSC2: high frequncy oscillator from XTALX or internal 12MHzRC

PLLCLK:48MHz PLLCLK 1/2 prescaler



Refer to the Label, system clock is changed between OSC1/OSC2/PLL CLK, the steps below must be done in sequence:

①. When OSCSCLK changed from OSC1 to OSC2, the steps below must be done in sequence:

a. Set OSC2ON = 1 to turn on the OSC2CLK, high frequncy oscillator from XTALX or internal 12MHzRC
b. Wait at least Oscillator Warm-up timer (Refer to **Warm-up Timer** section for details)
c. Set FS = 1 to select OSC2CLK as OSCSCLK

②. When OSCSCLK changed from OSC2 to OSC1, the steps below must be done in sequence:

a. Set FS = 0 to select 32.768kHz oscillator as OSCSCLK
b. Set OSC2ON = 0 to turn off OSC2CLK, reduce the power consumption of the system

③. When OSCSCLK changed from OSC2 to PLL, the steps below must be done in sequence:

a. Set PLLON = 1 to turn on the 48MHz PLL
b. Wait at least 2ms
c. Set PLLFS =1 to select PLL as OSC2CLK,as OSCSCLK

④. When OSCSCLK changed from PLL to OSC2, the steps below must be done in sequence:

a. Set PLLFS = 0 to select OSC2CLK as OSCSCLK
b. Set PLLON = 0 to turn off PLL, reduce the power consumption of the system

⑤. When OSCSCLK changed from OSC1 to PLL, the steps below must be done in sequence:

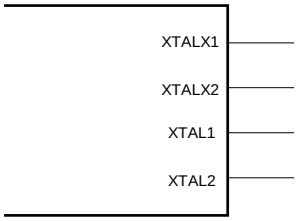
a. Set OSC2ON = 1
b. Wait at least Oscillator Warm-up timer (Refer to **Warm-up Timer** section for details)
c. Set PLLON = 1 to turn on the 48MHz PLL
d. Wait at least 2ms
e. Set PLLFS = 1 to select PLL as OSC2CLK
f. Set FS = 1 to select PLL as OSCSCLK

⑥. When OSCSCLK changed from PLL to OSC1, the steps below must be done in sequence:

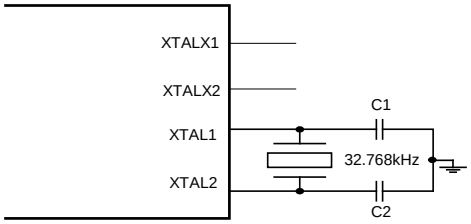
a. Set FS = 0 to select 12MHz RC as OSCSCLK
b. Set PLLON = 0 to turn off PLL, reduce the power consumption of the system
c. Set OSC2ON = 0 to turn off OSC2CLK

7.5.6 Oscillator Type

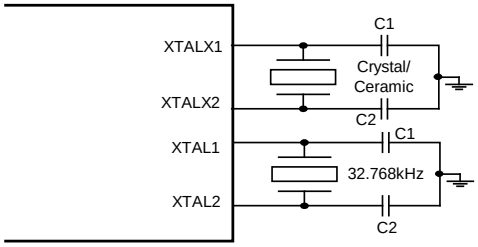
(1) OP_OSC = 0000: internal RC, XTAL and XTALX are shared with IO



(2) OP_OSC = 1010: 32.768kHz Crystal Oscillator at XTAL, Internal RC can be enabled, XTALX shared with I/O



(3) OP_OSC = 1101: 32.768kHz Crystal Oscillator at XTAL, 400k - 16M Crystal/Ceramic Oscillator at XTALX



7.5.7 Capacitor Selection for Oscillator

Ceramic Resonators		
Frequency	**C1**	**C2**
455kHz	47 - 100pF	47 - 100pF
8MHz	8 - 15pF	8 - 15pF
16MHz	8 - 15pF	8 - 15pF

Crystal Oscillator		
Frequency	**C1**	**C2**
32.768kHz	5 - 12.5pF	5 - 12.5pF
8MHz	8 - 15pF	8 - 15pF
16MHz	8 - 15pF	8 - 15pF

Notes:

(1) ***Capacitor values are used for design guidance only!***

(2) These capacitors were tested with the crystals listed above for basic start-up and operation. They are ***not optimized.***

(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

7.6 System Clock Monitor (SCM)

In order to enhance the system reliability, SH79F6488/SH79F6489 contains a system clock monitor (SCM) module. If the system clock fails (for example the oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal 32k WDTCLK and set system clock monitor bit (SCMIF) to 1. And the SCM interrupt will be generated when EA and ESCM is enabled. If the OSCCLK comes back, SCM will switch the OSCCLK back to the oscillator and clears the SCMIF automatically.

Notes:

The SCMIF is read only register; it can be clear to 0 or set to 1 by hardware only.

If SCMIF is cleared, the SCM switches the system clock to the state before system clock fail automatically.

*If Internal RC is selected as OSCCLK by code option (Refer to **code option** section for detail), the SCM can not work.*

Table 7.20 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	-	-	-	SCMIF	-	-	-	-
R/W	-	-	-	R	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
4	**SCMIF**	**System Clock Monitor bit** 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails

7.7 I/O Port

7.7.1 Features

- 72 bi-directional I/O ports
- Share with alternative functions

The SH79F6488/SH79F6489 has 72 bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x = 0-8, y = 0-7).

For SH79F6488/SH79F6489, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions be conflict when all the functions are enabled. (Refer to **Port Share** Section for details).

7.7.2 Registers

Table 7.21 Port Control Register

E1H - E5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CR (E1H, Bank0)	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR (E2H, Bank0)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR (E3H, Bank0)	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR (E4H, Bank0)	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR (E5H, Bank0)	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR (E1H, Bank1)	P5CR.7	P5CR.6	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P6CR (E2H, Bank1)	P6CR.7	P6CR.6	P6CR.5	P6CR.4	P6CR.3	P62CR.2	P6CR.1	P6CR.0
P7CR (E3H, Bank1)	P7CR.7	P7CR.6	P7CR.5	P7CR.4	P7CR.3	P7CR.2	P7CR.1	P7CR.0
P8CR (E4H, Bank1)	P8CR.7	P8CR.6	P8CR.5	P8CR.4	P8CR.3	P8CR.2	P8CR.1	P8CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxCRy x = 0-8, y = 0-7**	**Port input/output direction control Register** 0: input mode 1: output mode

Table 7.22 Port Pull up Resistor Control Register

E9H - EDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PCR (E9H, Bank0)	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR (EAH, Bank0)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR (EBH, Bank0)	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR (ECH, Bank0)	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR (EDH, Bank0)	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR (E9H, Bank1)	P5PCR.7	P5PCR.6	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
P6PCR (EAH, Bank1)	P6PCR.7	P6PCR.6	P6PCR.5	P6PCR.4	P6PCR.3	P6PCR.2	P6PCR.1	P6PCR.0
P7PCR (EBH, Bank1)	P7PCR.7	P7PCR.6	P7PCR.5	P7PCR.4	P7PCR.3	P7PCR.2	P7PCR.1	P7PCR.0
P8PCR (ECH, Bank1)	P8PCR.7	P8PCR.6	P8PCR.5	P8PCR.4	P8PCR.3	P8PCR.2	P8PCR.1	P8PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

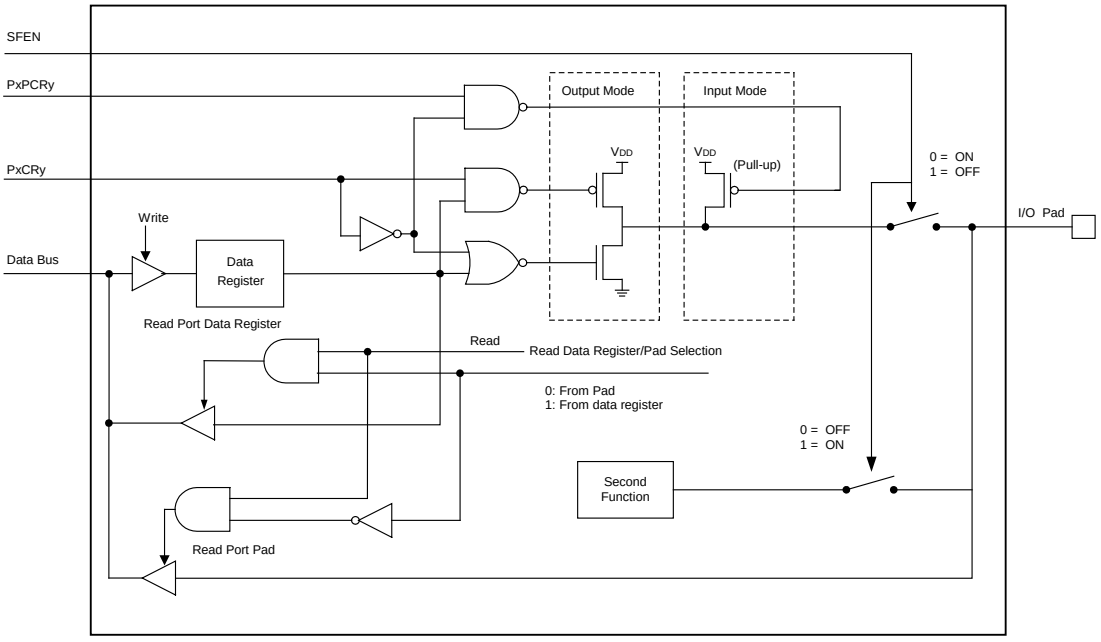
Bit Number	Bit Mnemonic	Description
7-0	**PxPCRy x = 0-8, y = 0-7**	**Input Port internal pull-high resistor enable/disable control** 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled

Table 7.23 Port Data Register

80H, 90H, A0H, B0H, C0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0 (80H, Bank0)	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1 (90H, Bank0)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2 (A0H, Bank0)	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3 (B0H, Bank0)	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4 (C0H, Bank0)	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5 (80H, Bank1)	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
P6 (90H, Bank1)	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
P7 (A0H, Bank1)	P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
P8 (B0H, Bank1)	P8.7	P8.6	P8.5	P8.4	P8.3	P8.2	P8.1	P8.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**Px.y** **x = 0-8, y = 0-7**	Port Data Register

7.7.3 Port Diagram



Note:

(1) The input source of reading input port operation is from the input pin directly.
(2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly. The read Instruction distinguishes which path is selected: The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.
(3) The destination of writing port operation is the data register regardless the port shared as the second function or not.
(4) In power-down mode:The reserve pins of LQFP64 package must be set to output or input with pull-high to avoid leakage current.

7.7.4 Port Share

The 72 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Most Inner Lest** rule:

The out most pin function in **Pin Configuration** has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin, even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 0-8), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register while the port pin keeps unchanged until all the share functions are disabled.

PORT0:

- RXD/INT46/T2 (P0.0): EUART data input/external inturrupt46/Timer2 external input/baud-rate clock output
- TXD/INT47/T3 (P0.1): EUART data output/external inturrupt47/Timer3 external input
- D+ (P0.2): USB differential data Positive input/output (for SH79F6489)
- D - (P0.3): USB differential data Negative input/output (for SH79F6489)
- T2EX/INT0 (P0.4): Timer2 reload/capture control / external inturrupt0
- INT1 (P0.5): external inturrupt1
- INT2 (P0.6): external inturrupt2
- INT3 (P0.7): external inturrupt3

Table 7.24 PORT0 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
24	16	18	1	TXD	When Write to SBUF Register
			2	T2	Set TR2 bit and C/$\overline{T2}$ bit in T2CON register (Auto Pull up) or clear C/$\overline{T2}$ bit and set T2OE bit in T2MOD register
			3	INT46	Set EX46 bit in IENC register, P0.0 in input mode
			4	P0.0	Above condition is not met
25	17	19	1	RXD	Set REN bit in SCON Register (Auto Pull up)
			2	T3	Set TR3 bit in T3CON register and T3CLKS[1:0] = 01 (Auto Pull up)
			3	INT47	Set EX47 bit in IENC register, P0.1 in input mode
			4	P0.1	Above condition is not met
26	18	20	1	D+	Set ENUSB bit in USBCON register (for SH79F6489)
			2	P0.2	Above condition is not met
27	19	21	1	D-	Set ENUSB bit in USBCON register (for SH79F6489)
			2	P0.3	Above condition is not met
28	20	22	1	T2EX	In mode0, 2, 3, set EXEN2 bit in T2CON register, or in mode 1 set DCEN bit in T2CON register or in mode1, clear DCEN bit and set EXEN2 bit (Auto Pull up)
			2	INT0	Set EX0 bit in IEN0 Register and Port0.4 is in input mode
			3	P0.4	Above condition is not met
29	-	23	1	INT1	Set EX1 bit in IEN0 Register and Port0.5 is in input mode
			2	P0.5	Above condition is not met
30	-	24	1	INT2	Set EX2 bit in IEN1 Register and Port0.6 is in input mode
			2	P0.6	Above condition is not met
31	-	25	1	INT3	Set EX3 bit in IEN1 Register and Port0.7 is in input mode
			2	P0.7	Above condition is not met

PORT1:

- VREF (P1.0): ADC reference voltage
- AIN0+ (P1.1): ADC positive differential input channel0
- AIN0- (P1.2): ADC negative differential input channel0
- AIN1+/AN0 (P1.3): ADC positive differential input channel1/ADC input channel0
- AIN1-/AN1 (P1.4): ADC negative differential input channel1/ADC input channel1
- AIN2+/AN2 (P1.5): ADC positive differential input channel2/ADC input channel2
- AIN2-/AN3 (P1.6): ADC negative differential input channel2/ADC input channel3
- VIN+ (P1.7): Positive PGA input/output

Table 7.25 PORT1 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
34/35	22	27/28	1	V_{REF}	Set VREFOS bit in ADCH register
			2	P1.0	Above condition is not met
36	23	29	1	AIN0+	Set CH0 bit in ADCH register
			2	P1.1	Above condition is not met
37	24	30	1	AIN0-	Set CH0 bit in ADCH register
			2	P1.2	Above condition is not met
38	-	31	1	AIN1+	Set CH1P bit in ADCH register
			2	AN0	Set CH1P bit in ADCH register
			3	P1.3	Above condition is not met
39	-	32	1	AIN1-	Set CH1N bit in ADCH register
			2	AN1	Set CH1N bit in ADCH register
			3	P1.4	Above condition is not met
40	25	33	1	AIN2+	Set CH2P bit in ADCH register
			2	AN2	Set CH2P bit in ADCH register
			3	P1.5	Above condition is not met
41	26	34	1	AIN2-	Set CH2N bit in ADCH register
			2	AN3	Set CH2N bit in ADCH register
			3	P1.6	Above condition is not met
42	27	35	1	VIN+	Set VINOS bit in ADCDS register
			2	P1.7	Above condition is not met

PORT2:

- VIN- (P2.0): Negative PGA input/output
- OP+/INT43 (P2.1): Positive OP input/output/external inturrupt43
- OP-/INT44 (P2.2): Negative OP input/output/external inturrupt44
- OP_O/INT45 (P2.3): OP output/external inturrupt45
- MOSI (P2.4): SPI master output slave input
- MISO (P2.5): SPI master input slave output
- SCK (P2.6): SPI serial clock
- $\overline{SS}$ (P2.7): SPI Slave Select

Table 7.26 PORT2 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
43	28	36	1	VIN-	Set VINOS bit in ADCDS register
			2	P2.0	Above condition is not met
45	29	37	1	OP+	Set OPOS bit in OPCON register
			2	INT43	Set EX43 bit in IENC Register and Port2.1 is in input mode
			3	P2.1	Above condition is not met
46	30	38	1	OP-	Set OPOS bit in OPCON register
			2	INT44	Set EX44 bit in IENC Register and Port2.2 is in input mode
			3	P2.2	Above condition is not met
47	31	39	1	OP_O	Set OPOS bit in OPCON register
			2	INT45	Set EX45 bit in IENC Register and Port2.3 is in input mode
			3	P2.3	Above condition is not met
48	-	40	1	MOSI	Set SPEN bit in SPSTA Register
			2	P2.4	Above condition is not met
49	-	41	1	MISO	Set SPEN bit in SPSTA Register
			2	P2.5	Above condition is not met
50	-	42	1	SCK	Set SPEN bit in SPSTA Register
			2	P2.6	Above condition is not met
51	-	43	1	$\overline{SS}$	Set SPEN bit in SPSTA Register, Clear SSDIS bit in SPCON Register
			2	P2.7	Above condition is not met

PORT3:

- SEG29 (P3.0): LCD SEG29
- SEG30 (P3.1): LCD SEG30
- SEG31 (P3.2): LCD SEG31
- SEG32 (P3.3): LCD SEG32
- XTAL1 (P3.4): XTAL input
- XTAL2 (P3.5): XTAL output
- XTALX1 (P3.6): XTALX input
- XTALX2 (P3.7): XTALX output

Table 7.27 PORT3 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
85	-	76	1	SEG29	Set P3S0 in PXSS register
			2	P3.0	Above condition is not met
86	-	77	1	SEG30	Set P3S1 in PXSS register
			2	P3.1	Above condition is not met
87	-	78	1	SEG31	Set P3S2 in PXSS register
			2	P3.2	Above condition is not met
88	-	79	1	SEG32	Set P3S3 in PXSS register
			2	P3.3	Above condition is not met
89	64	80	1	XTAL1	Code option: OP_OSC = 1010 or 1101
			2	P3.4	Above condition is not met
90	1	1	1	XTAL2	Code option: OP_OSC = 1010 or 1101
			2	P3.5	Above condition is not met
1	2	2	1	XTALX1	Code option: OP_OSC = 1101
			2	P3.6	Above condition is not met
2	3	3	1	XTALX2	Code option: OP_OSC = 1101
			2	P3.7	Above condition is not met

PORT4:

- TDO/SEG33 (P4.0): Test data out/LCD SEG33
- TMS/SEG34 (P4.1): Test mode select/LCD SEG34
- TDI/SEG35 (P4.2): Test data in/LCD SEG35
- TCK/SEG36 (P4.3): Test clock in/LCD SEG36
- PWM0/INT40 (P4.4): PWM0 output/interrupt 40 input pin
- PWM1/INT41 (P4.5): PWM1 output/interrupt 41 input pin
- PWM2/INT42 (P4.6): PWM2 output/interrupt 42 input pin
- $\overline{\text{RESET}}$/T4 (P4.7): Reset pin/Timer4 external output or input

Table 7.28 PORT4 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
4	4	4	1	TDO	Debug interface
			2	SEG33	Set P4S0 in PXSS register
			3	P4.0	Above condition is not met
5	5	5	1	TMS	Debug interface
			2	SEG34	Set P4S1 in PXSS register
			3	P4.1	Above condition is not met
6	6	6	1	TDI	Debug interface
			2	SEG35	Set P4S2 in PXSS register
			3	P4.2	Above condition is not met
7	7	7	1	TCK	Debug interface
			2	SEG36	Set P4S3 in PXSS register
			3	P4.3	Above condition is not met
8	8	8	1	PWM0	Set PWM0SS in PWM0CON register
			2	INT40	Set EX40 bit in IENC Register and Port4.4 is in input mode
			3	P4.4	Above condition is not met
9	9	9	1	PWM1	Set PWM1SS bit in PWM1CON register
			2	INT41	Set EX41 bit in IENC Register and Port4.5 is in input mode
			3	P4.5	Above condition is not met
10	10	10	1	PWM2	Set PWM2SS bit in PWM2CON register
			2	INT42	Set EX42 bit in IENC Register and Port4.6 is in input mode
			3	P4.6	Above condition is not met
11	11	11	1	$\overline{\text{RESET}}$	Code option:OP_RST = 0
			2	T4	When Code option:OP_RST = 1: Timer4 mode 0, TR4 = 1, T4CLKS = 1 (Auto pull high) Timer4 mode 0, TR4 = 1, T4CLKS = 0, TC4 = 1 Timer4 mode 1, TR4 = 1 (Auto pull high)
			3	P4.7	Code option: OP_RST = 1, above condition is not met

PORT5:

- COM1 (P5.0): LCD COM1
- COM2 (P5.1): LCD COM2
- COM3 (P5.2): LCD COM3
- COM4 (P5.3): LCD COM4
- COM5/SEG1 (P5.4): LCD COM5/SEG1
- COM6/SEG2 (P5.5): LCD COM6/SEG2
- SEG3 (P5.6): LCD SEG3
- SEG4 (P5.7): LCD SEG4

Table 7.29 PORT5 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
52	32	44	1	COM1	Set P5S0 in P5SS register
			2	P5.0	Above condition is not met
53	33	45	1	COM2	Set P5S1 in P5SS register
			2	P5.1	Above condition is not met
54	34	46	1	COM3	Set P5S2 in P5SS register
			2	P5.2	Above condition is not met
55	35	47	1	COM4	Set P5S3 in P5SS register
			2	P5.3	Above condition is not met
56	36	48	1	COM5	Set P5S4 in P5SS register, set DUTY[1:0] in LCDCON register 01 or 10
			2	SEG1	Set P5S4 in P5SS register, set DUTY[1:0] in LCDCON register 00 or 11
			3	P5.4	Above condition is not met
57	37	49	1	COM6	Set P5S5 in P5SS register, set DUTY[1:0] in LCDCON register 10
			2	SEG2	Set P5S5 in P5SS register, set DUTY[1:0] in LCDCON register 00, 01or 11
			3	P5.5	Above condition is not met
58	38	50	1	SEG3	Set P5S6 in P5SS register
			2	P5.6	Above condition is not met
59	39	51	1	SEG4	Set P5S7 in P5SS register
			2	P5.7	Above condition is not met

PORT6:

- SEG5 (P6.0): LCD SEG5
- SEG6 (P6.1): LCD SEG6
- SEG7 (P6.2): LCD SEG7
- SEG8 (P6.3): LCD SEG8
- SEG9 (P6.4): LCD SEG9
- SEG10 (P6.5): LCD SEG10
- SEG11 (P6.6): LCD SEG11
- SEG12 (P6.7): LCD SEG12

Table 7.30 PORT6 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
60	40	52	1	SEG5	Set P6S0 in P6SS register
			2	P6.0	Above condition is not met
61	41	53	1	SEG6	Set P6S1 in P6SS register
			2	P6.1	Above condition is not met
62	42	54	1	SEG7	Set P6S2 in P6SS register
			2	P6.2	Above condition is not met
63	43	55	1	SEG8	Set P6S3 in P6SS register
			2	P6.3	Above condition is not met
64	44	56	1	SEG9	Set P6S4 in P6SS register
			2	P6.4	Above condition is not met
65	45	57	1	SEG10	Set P6S5 in P6SS register
			2	P6.5	Above condition is not met
66	46	58	1	SEG11	Set P6S6 in P6SS register
			2	P6.6	Above condition is not met
67	47	59	1	SEG12	Set P6S7 in P6SS register
			2	P6.7	Above condition is not met

PORT7:

- SEG13 (P7.0): LCD SEG13
- SEG14 (P7.1): LCD SEG14
- SEG15 (P7.2): LCD SEG15
- SEG16 (P7.3): LCD SEG16
- SEG17 (P7.4): LCD SEG17
- SEG18 (P7.5): LCD SEG18
- SEG19 (P7.6): LCD SEG19
- SEG20 (P7.7): LCD SEG20

Table 7.31 PORT7 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
68	48	60	1	SEG13	Set P7S0 in P7SS register
			2	P7.0	Above condition is not met
69	49	61	1	SEG14	Set P7S1 in P7SS register
			2	P7.1	Above condition is not met
70	50	62	1	SEG15	Set P7S2 in P7SS register
			2	P7.2	Above condition is not met
71	51	63	1	SEG16	Set P7S3 in P7SS register
			2	P7.3	Above condition is not met
72	52	64	1	SEG17	Set P7S4 in P7SS register
			2	P7.4	Above condition is not met
73	53	65	1	SEG18	Set P7S5 in P7SS register
			2	P7.5	Above condition is not met
74	54	66	1	SEG19	Set P7S6 in P7SS register
			2	P7.6	Above condition is not met
75	55	67	1	SEG20	Set P7S7 in P7SS register
			2	P7.7	Above condition is not met

PORT8:

- SEG21 (P8.0): LCD SEG21
- SEG22 (P8.1): LCD SEG22
- SEG23 (P8.2): LCD SEG23
- SEG24 (P8.3): LCD SEG24
- SEG25 (P8.4): LCD SEG25
- SEG26 (P8.5): LCD SEG26
- SEG27 (P8.6): LCD SEG27
- SEG28 (P8.7): LCD SEG28

Table 7.32 PORT8 Share Table

Pin No.			Priority	Function	Enable bit
PAD	LQFP64	LQFP80			
77	56	68	1	SEG21	Set P8S0 in P8SS register
			2	P8.0	Above condition is not met
78	57	69	1	SEG22	Set P8S1 in P8SS register
			2	P8.1	Above condition is not met
79	58	70	1	SEG23	Set P8S2 in P8SS register
			2	P8.2	Above condition is not met
80	59	71	1	SEG24	Set P8S3 in P8SS register
			2	P8.3	Above condition is not met
81	60	72	1	SEG25	Set P8S4 in P8SS register
			2	P8.4	Above condition is not met
82	61	73	1	SEG26	Set P8S5 in P8SS register
			2	P8.5	Above condition is not met
83	62	74	1	SEG27	Set P8S6 in P8SS register
			2	P8.6	Above condition is not met
84	63	75	1	SEG28	Set P8S7 in P8SS register
			2	P8.7	Above condition is not met

7.8 Timer

7.8.1 Features

- The SH79F6488/SH79F6489 has three timers (Timer2, 3, 4)
- Timer2 is compatible with the standard 8052 and has up or down counting and programmable clock output function
- Timer3 is a 16-bit auto-reload timer and can operate even in Power-Down mode
- Timer4 is a 16-bit auto-reload timer and can be selected as a baud-rate generator

7.8.2 Timer2

The Timer 2 is implemented as a 16-bit register accessed as two cascaded data registers: TH2 and TL2. It is controlled by the register T2CON and T2MOD. The Timer2 interrupt can be enabled by setting the ET2 bit in the IEN0 register. (Refer to Interrupt Section for details)

C/$\overline{T2}$selects system clock (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows Timer 2/Counter 2 Data Register to increment by the selected input.

Timer2 Modes

Timer2 has 4 operating modes: Capture/Reload, Auto-reload mode with up or down counter, Baud Rate Generator and Programmable clock-output. These modes are selected by the combination of RCLK, TCLK and CP/RL2.

Timer2 Mode select

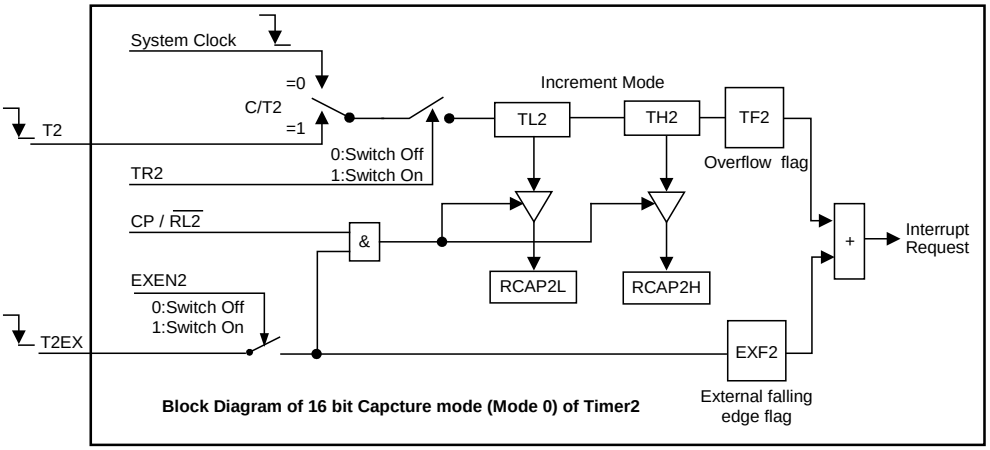
C/$\overline{T2}$	T2OE	DCEN	TR2	CP/$\overline{RL2}$	Mode	
X	0	X	1	1	0	16-bit capture
X	0	0 or 1	1	0	1	16-bit auto-reload timer
X	0	X	1	X	2	Not recommending
0	1	X	1	X	3	Programmable clock
0	1	X	1	X	3	Programmable clock

Mode0: 16-bit Capture

In the capture mode, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 is a 16-bit timer or counter which will set TF2 on overflow to generate an interrupt if ET2 is enabled.

If EXEN2 = 1, Timer2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L respectively, In addition, a 1-to-0 transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can also generate an interrupt if ET2 is enabled.



Block Diagram of 16 bit Capcture mode (Mode 0) of Timer2

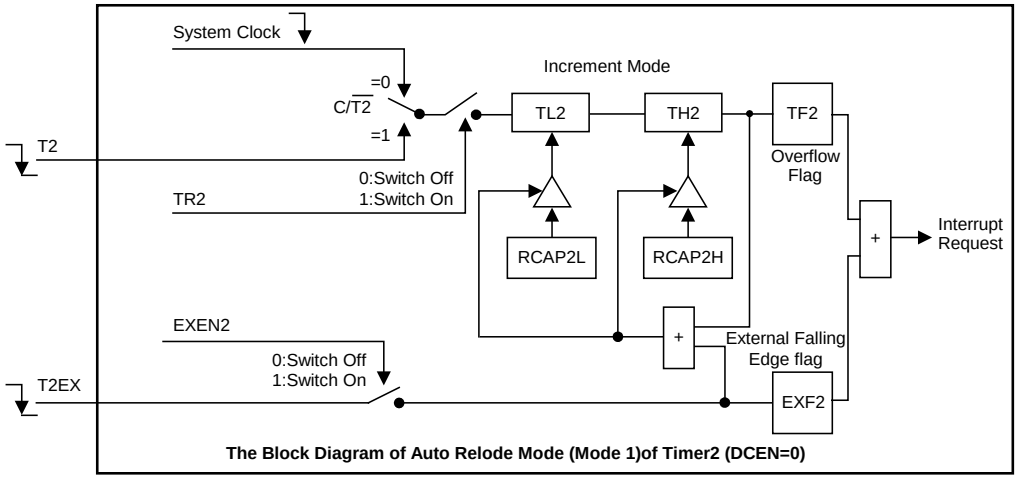
Mode1: 16-bit auto-reload Timer

Timer2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit in T2MOD. After reset, the DCEN bit is set to 0 so that Timer2 will default to count up. When DCEN is set, Timer2 can count up or down, depending on the value of the T2EX pin.

When DCEN = 0, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software.

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if ET2 is enabled.



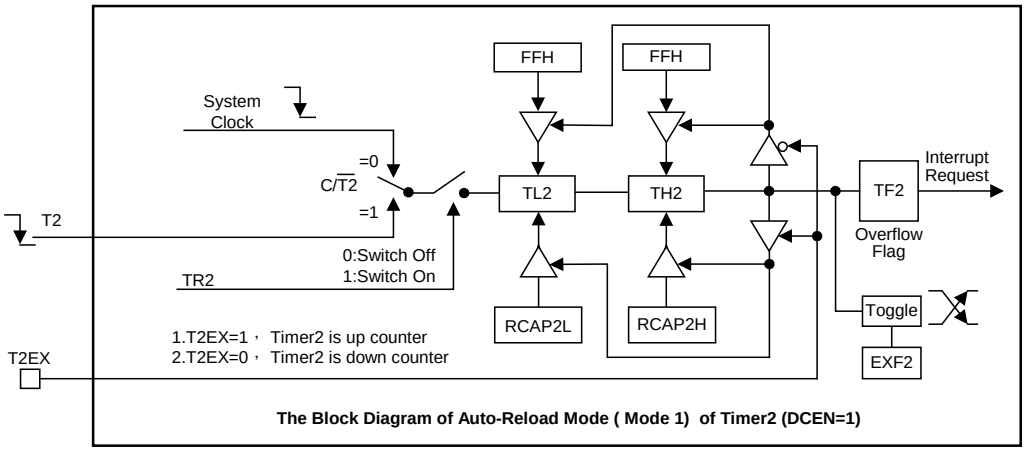
The Block Diagram of Auto Relode Mode (Mode 1)of Timer2 (DCEN=0)

Setting the DCEN bit enables Timer2 to count up or down. When DCEN = 1, the T2EX pin controls the direction of the count, and EXEN2's control is invalid.

A logical "1" at T2EX makes Timer2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logical "0" at T2EX makes Timer2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.



The Block Diagram of Auto-Reload Mode (Mode 1) of Timer2 (DCEN=1)

Mode2: (Not recommending)

Mode3: Programmable Clock Output

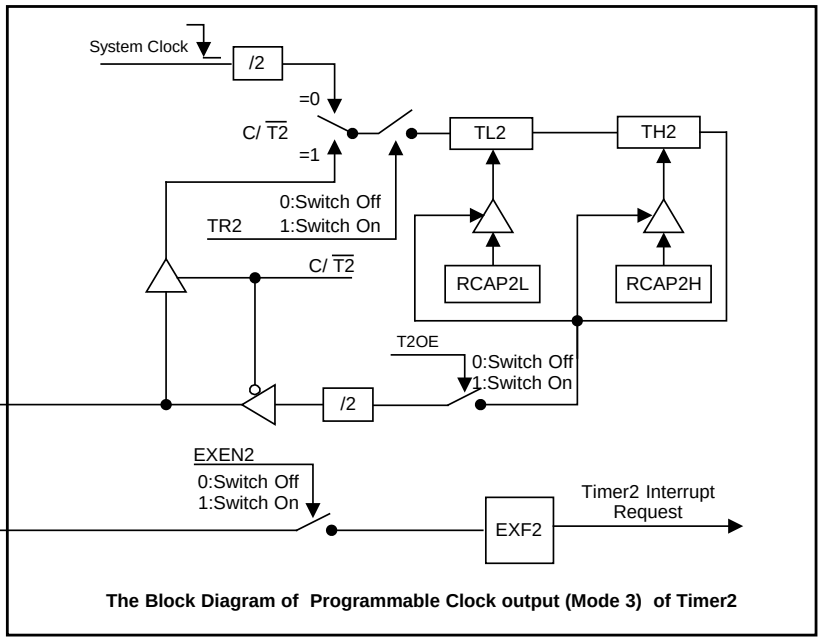
To configure the Timer2 as a clock generator, bit C/$\overline{T2}$ must be cleared and bit T2OE must be set. Bit TR2 starts and stops the timer.

In this mode T2 will output a 50% duty cycle clock:

$$\text{Clock Out Frequency} = \frac{1}{2\times 2\times 12}\times\frac{f_{SYS}}{65536-[RCAP2H,RCAP2L]} \quad ; \text{TCLKP2 = 0}$$

$$\text{Clock Out Frequency} = \frac{1}{2\times 2}\times\frac{f_{SYS}}{65536-[RCAP2H,RCAP2L]} \quad ; \text{TCLKP2 = 1}$$

Timer2 overflow will not generate an interrupt, so it is possible to use Timer2 as a baud-rate generator and a clock output simultaneously with the same frequency.



The Block Diagram of Programmable Clock output (Mode 3) of Timer2

Note:

(1) Both TF2 and EXF2 can cause timer2 interrupt request, and they have the same vector address.
(2) TF2 and EXF2 are set as 1 by hardware while event occurs. But they can also be set by software at any time. Only the software and the hardware reset will be able to clear TF2 & EXF2 to 0.
(3) When EA = 1 & ET2 = 1, setting TF2 or EXF2 as 1 will cause a timer2 interrupt.

Registers

Table 7.33 Timer2 Control Register

C8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2			EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
R/W	R/W	R/W			R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0			0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF2**	**Timer2 overflow flag bit** 0: No overflow (Must be cleared by software) 1: Overflow (Set by hardware)
6	**EXF2**	**External event input (falling edge) from T2EX pin detected flag bit** 0: No external event input (Must be cleared by software) 1: Detected external event input (Set by hardware if EXEN2 = 1)
3	**EXEN2**	**External event input (falling edge) from T2EX pin used as Reload/Capture trigger enable/disable control bit** 0: Ignore events on T2EX pin 1: Cause a capture or reload when a negative edge on T2EX pin is detected, when Timer 2 is not used to clock the EUART (T2EX always has a pull up resistor)
2	**TR2**	**Timer2 start/stop control bit** 0: Stop Timer2 1: Start Timer2
1	**C/$\overline{T2}$**	**Timer2 Timer/Counter mode selected bit** 0: Timer Mode, T2 pin is used as I/O port 1: Counter Mode, the internal pull-up resister is turned on
0	**CP/$\overline{RL2}$**	**Capture/Reload mode selected bit** 0: 16-bits timer/counter with reload function 1: 16-bits timer/counter with capture function

Table 7.34 Timer2 Mode Control Register

C9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	TCLKP2	-	-	-	-	-	T2OE	DCEN
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7	**TCLKP2**	**Prescale control bit** 0:Timer2 source is 1/12 prescale of system clock 1: Timer2 source is system clock
1	**T2OE**	**Timer2 Output Enable bit** 0: Set P0.0/T2 as clock input or I/O port 1: Set P0.0/T2 as clock output (Baud-Rate generator mode)
0	**DCEN**	**Down Counter Enable bit** 0: Disable Timer2 as up/down counter, Timer2 is an up counter 1: Enable Timer2 as up/down counter

Table 7.35 Timer2 Reload/Capture & Data Registers

CAH-CDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCAP2L	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**RCAP2L.x**	**Timer2 Reload/Capturer Data, x = 0 - 7**
	RCAP2H.x	
7-0	**TL2.x**	**Timer2 Low & High byte counter, x = 0 - 7**
	TH2.x	

7.8.3 Timer3

Timer3 is a 16-bit auto-reload timer. It is implemented as a 16-bit register accessed as two cascaded Data Registers: TH3 and TL3. It is controlled by the T3CON register. The Timer3 interrupt can be enabled by setting ET3 bit in IEN0 register (Refer to Interrupt Section for details).

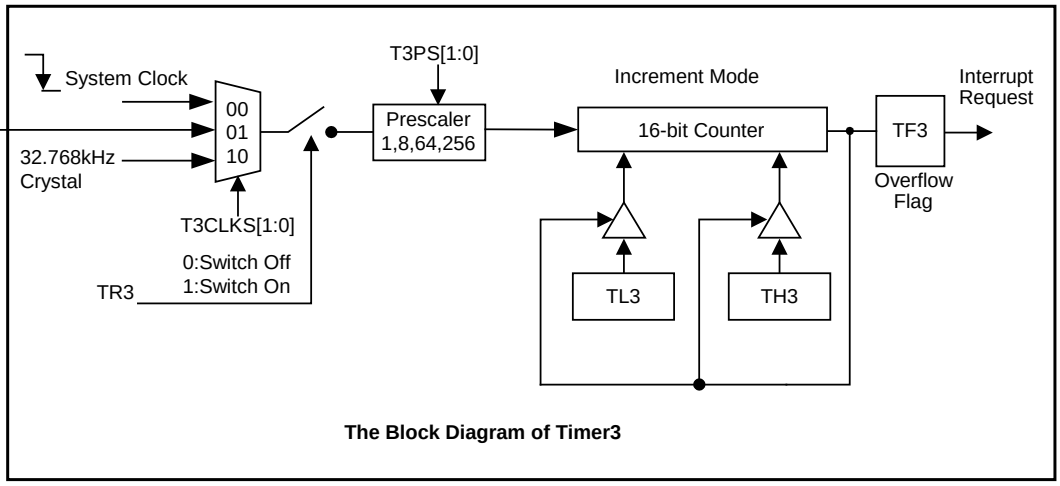
Timer3 has only one operating mode: 16-bit Counter/Timer with auto-reload. Timer3 also supports the following features: selectable pre-scaler setting and Operation during CPU Power-Down mode.

Timer3 consists of a 16-bit counter/reload register (TH3, TL3). When writing to TH3 and TL3, they are used as timer load register. When reading from TH3 and TL3, they are used as timer counter register. Setting the TR3 bit enables Timer 3 to count up. The Timer will overflow from 0xFFFF to 0x0000 and set the TF3 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH3 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH3 and TL3 should follow these steps:

Write operation: Low nibble first, High nibble to update the counter

Read operation: High nibble first, Low nibble followed.



The Block Diagram of Timer3

If T3CLKS[1:0] is 00, Timer 3 can't work in Power Down mode.

If T3CLKS[1:0] is 01,Timer3 can work in Power Down mode. Even close all oscillator, Timer 3 can count.

If T3CLKS[1:0] is 10, Timer3 can work in Power Down mode If low frequency oscillator is off,then Timer3 can not count.

It can be described in the following table.

T3CLKS[1:0]	Oscillator status	Can work in normal mode	Can work in Power Down mode
00	-	YES	NO
01	-	YES	YES
10	low frequency off in power-down	YES	NO
	low frequency on in power-down	YES	YES

Note:

(1) When TH3 and TL3 read or written, must make sure TR3 = 0.

(2) When T3 is selected as Timer3 clock source and TR3 is set 0 to 1, the first T3 down edge will be ignored.

(3) Low frequency oscillator will keep working when system entering Power-down mode with high frequency oscillator (OSC2). Low frequency oscillator will turn off when system entering Power-down mode with low frequency oscillator (32.768kHz).

Registers

Table 7.36 Timer3 Control Register

88H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T3CON	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
R/W	R/W	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF3**	**Timer3 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T3PS[1:0]**	**Timer3 input clock Prescaler Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
2	**TR3**	**Timer3 start/stop control bit** 0: Stop Timer3 1: Start Timer3
1-0	**T3CLKS[1:0]**	**Timer3 Clock Source select bits** 00: System clock, T3 pin is used as I/O port 01: External clock from pin T3, auto pull-up 10: 32.768kHz from external Crystal 11: reserved

Table 7.37 Timer3 Reload/Counter Data Registers

8CH-8DH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL3	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL3.x**	**Timer3 Low & High byte counter, x = 0 - 7**
	TH3.x	

7.8.4 Timer4

Timer4 is a 16-bit auto-reload timer. It is implemented as a 16-bit register accessed as two cascaded data registers: TH4 and TL4. It is controlled by the T4CON register. The Timer 4 interrupt can be enabled by setting ET4 bit in IEN0 register (Refer to **interrupt** Section for details).

When writing to TH4 and TL4, they are used as timer load register. When reading from TH4 and TL4, they are used as timer counter register. Setting the TR4 bit enables Timer 4 to count up. The timer will overflow from 0xFFFF to 0x0000 and set the TF4 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH4 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH4 and TL4 should follow these steps:

Write operation:Low nibble first,High nibble to update the counter.

Read operation:High nibble first,Low nibble followed.

Timer4 Modes

Timer4 has three operating modes: 16-bit auto-reload counter/timer, Baud Rate Generator and 16-bit auto-reload timer with T4 edge trig. These modes are selected by T4M[1:0] bits in T4CON Register.

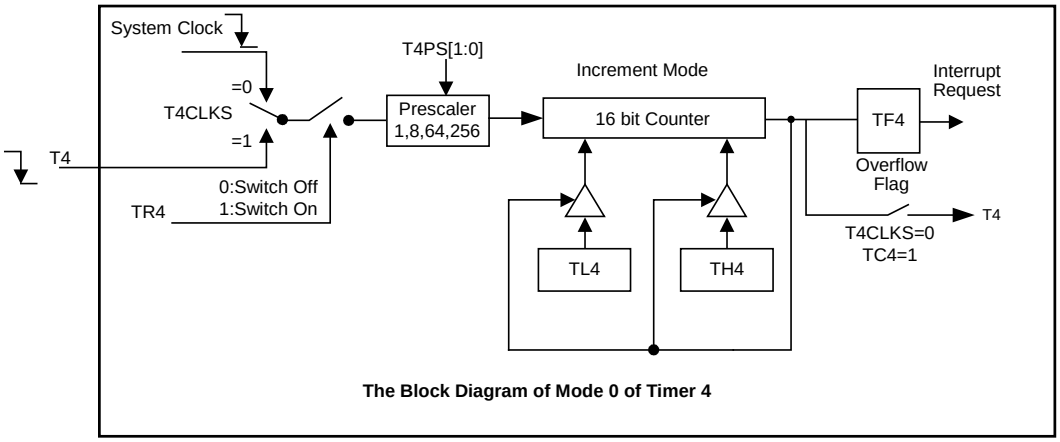
Mode0: 16-bit Auto-Reload Counter/Timer

Timer4 operates as 16-bit counter/timer in Mode 0. The TH4 register holds the high eight bits of the 16-bit counter/timer, TL4 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF4 (T4CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer 4 interrupts is enabled. The T4CLKS bit (T4CON.0) selects the counter/timer's clock source.

If T4CLKS = 1, external clock from the Pin T4 is selected as Timer4 clock, after prescaled, it will increase the Counter/Timer4 Data register. Else if T4CLKS = 0, the system clock is selected as Timer4 clock.

Setting the TR4 bit (T4CON.1) enables the timer. Setting TR4 does not force the timer to reset. The timer load register should be loaded with the desired initial value before the timer is enabled.

In Compare mode, the T4 pin is automatically set as output mode by hardware. the internal counter is constantly countered from TH4 and TL4 register value to 0xFFFF. When an overflow occurs, the T4 pin will be inverted. At the same time, interrupt flag bit of Time4 is set. Timer4 must be running in Timer mode (T4CLKS = 0) when compare function enabled.



The Block Diagram of Mode 0 of Timer 4

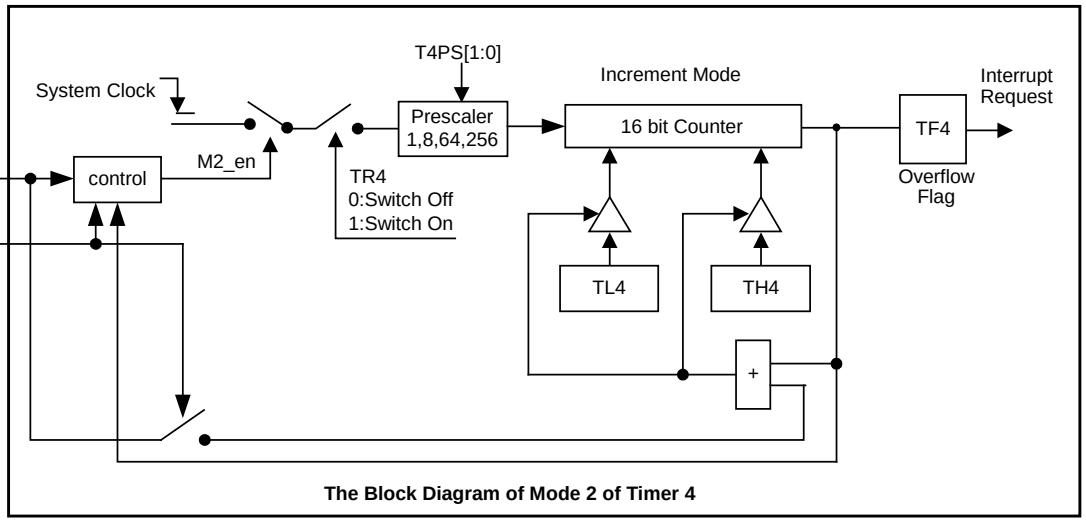
Mode1: 16-bit Auto-Reload Timer with T4 Edge Trig

Timer4 operates as 16-bit timer in Mode1. The TH4 register holds the high eight bits of the 16-bit counter/timer, TL4 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF4 (T4CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer4 interrupts is enabled. The T4CLKS bit (T4CON.0) is 0 always. Only the system clock is selected as Timer4 clock.

In Mode2, After Setting the TR4 bit (T4CON.1), Timer4 does not start counting but waits the trig signal (rising or falling edge controlled by T4M[1:0]) from T4. An active trig signal will start the Timer4. When Timer 4 overflows from 0XFFFF to 0x0000, TF4 will be set, TH4 and TL4 will be reloaded from timer load register, and Timer4 holds and waits the next trig edge.

When Timer4 is working, an active trig signal maybe come, if TC bit equals 0, the trig signal will be ignored; if TC bit equals 1, Timer4 will be re-trigged.

Setting TR4 does not force the timer to reset. The timer register should be loaded with the desired initial value before the timer is enabled.



The Block Diagram of Mode 2 of Timer 4

control : M2_en set to 1 when T4 edge trig, M2_en set to 0 when counter overflow

Note: *When Timer4 is used as a counter, the frequency of input signal of T4 pin must be less than half of system clock.*

Registers

Table 7.38 Timer4 Control Register

C8H, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T4CON	TF4	TC4	T4PS1	T4PS0	T4M1	T4M0	TR4	T4CLKS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF4**	**Timer4 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
6	**TC4**	**Compare function Enable bit** When T4M[1:0] = 00 0: Disable compare function of Timer4 1: Enable compare function of Timer4 When T4M[1:0] = 10 or 11 0: Timer4 can't be re-trigged 1: Timer4 can be re-trigged
5-4	**T4PS[1:0]**	**Timer4 input clock Prescale Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
3-2	**T4M[1:0]**	**Timer4 Mode Select bits** 00: Mode0, 16-bit auto-reload up counter/timer 01: reserved 10: Mode2 with rising edge trig from pin T4 (system clock only, T4CLKS is invalid) 11: Mode2 with falling edge trig from pin T4 (system clock only, T4CLKS is invalid)
1	**TR4**	**Timer4 start/stop control bit** 0: Stop Timer4 1: Start Timer4
0	**T4CLKS**	**Timer4 Clock Source select bit** 0: System clock, T4 pin is used as I/O port 1: External clock from pin T4 (On the falling edge), the internal pull-up resister is turned on

Table 7.39 Timer4 Reload/Counter Data Registers

CCH-CDH, Bank1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL4	TL4.7	TL4.6	TL4.5	TL4.4	TL4.3	TL4.2	TL4.1	TL4.0
TH4	TH4.7	TH4.6	TH4.5	TH4.4	TH4.3	TH4.2	TH4.1	TH4.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL4.x** **TH4.x**	**Timer4 Low & High byte counter, x = 0 - 7**

7.9 Base Timer

7.9.1 Features

- Clock source is oscillator (32.768kHz) clock
- Can generate 0.5s, 1s, 1s or 1min interrupt depending on the setting of the register

SH79F6488/SH79F6489 provided an internal base timer which clock source is oscillator clock. It will work when both BTEN bit being set and oscillator not stopping. And it can generate a BT interrupt every overflow if the EBT bit in the IEN1 register is set. The overflow time is precise 0.5s, 1s, 6s or 1min depending on the setting of the BTS [1:0] bits in BTCON register.

Note:

(1) When code option is 1010 or 1101, timer source is 32.768kHz oscillator, the base timer can generate an exact 0.5s, 1s, 1min *or 1hour interrupt.*

(2) When code option is 0000, timer source is internal 12MHz RC, the base timer can generate an approximate 0.5s, 1s, 1min *or 1hour interrupt.*

7.9.2 Registers

Table 7.40 Base Timer Control Register

C1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BTCON	BTEN	BTIF	BTS1	BTS0	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	**BTEN**	**Base Timer Control Bit** 0: Disable Base Timer 1: Enable Base Timer, the counter begins from '0' after setting BTEN bit
6	**BTIF**	**Base Timer overflow flag bit** 0: no overflow happened 1: overflow happened
5, 4	**BTS[1:0]**	**Base Timer period select** 00: Base Timer overflow every 0.5s 01: Base Timer overflow every 1s 10: Base Timer overflow every 1 min 11: Base Timer overflow every 60mins

Table 7.41 Second and Half-second Register

C2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEC	HSEC	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**HSEC**	This bit is a half second flag and it will overturn between 0 and 1 every half second.
6-0	**SEC[6:0]**	This register (bit0-bit6) contains the current value (BCD) of the second counter. This register (bit0-bit6) can be read at any time without affecting the counter count. Writing to this register (bit0-bit6) loads the value to the second counter and the counter continues to count from this new value. The second counter rolls over to 0 after reaching 59. Writing a value other than 0 to 59 to this register has no effect. Be sure not to write a data such as '0x, 1x, 2x, 3x, 4x (x = A-F)' to this register.

Table 7.42 Minute Register

C3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MIN	-	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-0	**MIN[6:0]**	This read/write register contains the current value (BCD) of the minute counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the minute counter and the counter continues to count from this new value. The minute counter rolls over to 0 after reaching 59. Writing a value other than 0 to 59 to this register has no effect. Be sure not to write a data such as '0x, 1x, 2x, 3x, 4x (x = A-F)' to this register.

Note:

When OSC1CLK is selected as system clock(OSCSCLK) (FS = 0),and entering Power-down mode:
If base timer is off, OSC1CLK and OSC2CLK will turn off.
If base timer is on, OSC1CLK will keep on,OSC2CLK will turn off.

7.10 Interrupt

7.10.1 Features

- SH79F6488 : 14 interrupt sources
- SH79F6489 : 15 interrupt sources
- 4 interrupt priority levels

The SH79F6488/SH79F6489 provides total 14 interrupt sources: 5 external interrupts (INT0/1/2/3/4; INT4 including INT40-47, which share the same vector address), 3 timer interrupts (Timer2, 3, 4), base timer interrupt, EUART interrupt, ADC Interrupt, PWM interrupts and SCM interrupt which share the same vector address. The SH79F6489 also provides USB Interrupt.

7.10.2 Interrupt Enable Control

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

7.10.3 Registers

Table 7.43 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC	ET2	ES	ET3	EX1	ET4	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**EA**	**All interrupt enable bit** 0: Disable all interrupt 1: Enable all interrupt
6	**EADC**	**ADC interrupt enable bit** 0: Disable ADC interrupt 1: Enable ADC interrupt
5	**ET2**	**Timer2 overflow interrupt enable bit** 0: Disable Timer2 overflow interrupt 1: Enable Timer2 overflow interrupt
4	**ES**	**EUART interrupt enable bit** 0: Disable EUART interrupt 1: Enable EUART interrupt
3	**ET3**	**Timer3 overflow interrupt enable bit** 0: Disable Timer3 overflow interrupt 1: Enable Timer3 overflow interrupt
2	**EX1**	**External interrupt1 enable bit** 0: Disable external interrupt1 1: Enable external interrupt1
1	**ET4**	**Timer4 overflow interrupt enable bit** 0: Disable Timer4 overflow interrupt 1: Enable Timer4 overflow interrupt
0	**EX0**	**External interrupt0 enable bit** 0: Disable external interrupt0 1: Enable external interrupt0

Table 7.44 Secondary Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	ESCM	EBT	EPWM	EUSB (for 6489)	EX4	EX3	EX2	ESPI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**ESCM**	**SCM interrupt enable bit** 0: Disable SCM interrupt 1: Enable SCM interrupt
6	**EBT**	**Base timer overflow interrupt enable bit** 0: Disable Base timer overflow interrupt 1: Enable Base timer overflow interrupt
5	**EPWM**	**PWM interrupt enable bit** 0: Disable PWM interrupt 1: Enable PWM interrupt
4	**EUSB** (for 6489)	**USB interrupt enable bit** 0: Disable USB interrupt 1: Enable USB interrupt
3	**EX4**	**External interrupt4 enable bit** 0: Disable external interrupt4 1: Enable external interrupt4
2	**EX3**	**External interrupt3 enable bit** 0: Disable external interrupt3 1: Enable external interrupt3
1	**EX2**	**Enternal interrupt2 enable bit** 0: Disenable external interrupt2 1: Enable external interrupt2
0	**ESPI**	**SPI interrupt enable bit** 0: Disable SPI interrupt 1: Enable SPI interrupt

Table 7.45 Interrupt channel Enable Register

BAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IENC	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**EXS4x (x = 0-7)**	**External interrupt4 channel select bit (x = 0-7)** 0: Disable external interrupt 4x 1: Enable external interrupt 4x

7.10.4 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in Table bellow.

For **external interrupt (INT0/1/2/3)**, when an external interrupt0/1/2/3 is generated, if the interrupt was edge trigged, the flag (IE0-3 in TCON) that generated this interrupt is cleared by hardware when the service routine is vectored. If the interrupt was level trigged, then the requesting external source directly controls the request flag, rather than the on-chip hardware.

When an **external interrupt4** is generated, the flag (IF4x (x = 0-7) in EXF1 register) that generated this interrupt should be cleared by user's program because the same vector entrance was used in INT4. But if INT4 is setup as level trigged, the flag can't be cleared by user's program, it only be controlled by peripheral signal level that connect to INT source pin.

The **Timer2 interrupt** is generated by the logical OR of flag TF2 and bit EXF2 in T2CON register, which is set by hardware. None of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, so the flag must be cleared by software.

The **Timer3 interrupt** is generated when they overflow, the flag TF3 in T3CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **Timer4 interrupt** is generated when they overflow, the flag TF4 in T4CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **Base Timer interrupt** is generated when they overflow, the flag BTIF in BTCON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **EUART interrupt** is generated by the logical OR of flag RI and TI in SCON register, which is set by hardware. Neither of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the receive interrupt flag or the transmission interrupt flag that generated the interrupt, so the flag must be cleared by software.

The **ADC interrupt** is generated by ADCIF bit in ADCON. If an interrupt is generated, the converted result in ADCDH/ADCDL will be valid. If continuous compare function in ADC module is Enable, ADCIF will not be set at each conversion, but set if converted result is larger than compare value. The flag must be cleared by software.

The **SPI interrupts** are generated by SPIF in SPSTA or set MODF. The flags can be cleared by software.

The **SCM interrupt** is generated by SCMIF in SCM register, which is set by hardware. And the flag can only be cleared by hardware.

The **PWMx interrupts** are generated by PWMxIF in PWMxCON (x = 0-2). The flags can be cleared by software.

SH79F6489: The **USB interrupts** are generated by setting the relative flags of the USB. The flags must be cleared by software. (Refer to the USB section for the details of the relative flags)

Table 7.46 External Interrupt 0/1 Control Register

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	-	-	-	-	IE1	IT1	IE0	IT0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
1, 3	**IEx (x = 0, 1)**	**External interrupt x request flag bit** 0: No interrupt pending 1: Interrupt is pending
0, 2	**ITx (x = 0, 1)**	**External interrupt x trigger mode selection bit** 0: Low level trigger 1: Falling edge trigger

Table 7.47 External Interrupt Flag Register0

E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF0	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**IT4[1:0]**	**External interrupt4 trigger mode selection bits** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge IT4 [1:0] is effect on external interrupt 4x at the same mode
5-4	**IT3[1:0]**	**External interrupt3 trigger mode selection bits** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
3-2	**IT2[1:0]**	**External interrupt2 trigger mode selection bits** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
1	**IE3**	**External interrupt3 request flag bit** 0: No interrupt pending 1: Interrupt is pending
0	**IE2**	**External interrupt2 request flag bit** 0: No interrupt pending 1: Interrupt is pending

Table 7.48 External Interrupt Flag Register1

D8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF1	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IF4x (x = 0-7)**	**External interrupt4 request flag bit** 0: No interrupt pending 1: Interrupt is pending IF4x is cleared by software

7.10.5 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in **Interrupt Summary table**.

7.10.6 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. But the OVL NMI interrupt has the highest Priority Level (except RESET) of all the interrupt sources, with no IPH/IPL control. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction cycle, an internal polling sequence determines which request is serviced.

Interrupt Priority		
Priority bits		**Interrupt Lever Priority**
IPHx	**IPLx**	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.49 Interrupt Priority Control Registers

B8H, B4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL0	-	PADCL	PT2L	PS0L	PT3L	PX1L	PT4L	PX0L
IPH0	-	PADCH	PT2H	PS0H	PT3H	PX1H	PT4H	PX0H
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0
B9H, B5H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
IPL1	PSCM	PBTL	PPWML	PUSBL (for 6489)	PX4L	PX3L	PX2L	PSPIL
IPH1	PSCM	PBTH	PPWMH	PUSBH (for 6489)	PX4H	PX3H	PX2H	PSPIH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxxxL/H**	Corresponding interrupt source xxx's priority level selection bits

7.10.7 Interrupt Handling

The interrupt flags are sampled and polled at the fetch cycle of each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current cycle is not in the final cycle of the instruction in progress. This ensures that the instruction in progress is completed before vectoring to any service routine.

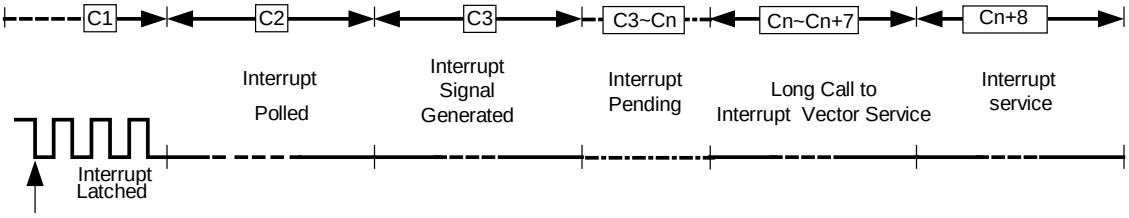
The instruction in progress is RETI. This ensures that if the instruction in progress is RETI then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Note:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.

The polling cycle/LCALL sequence is illustrated below:



Interrupt Response Timing

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with corresponding address that depends on the source of the interrupt being vectored too, as shown in Interrupt Summary table.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt service. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt with this priority was still in progress. In this case, no interrupt of the same or lower priority level would be acknowledged.

7.10.8 Interrupt Response Time

If an interrupt is recognized, its request flag is set in every machine cycle after recognize. The value will be polled by the circuitry until the next machine cycle; the CPU will generate an interrupt at the third machine cycle. If the request is active and conditions are right for it to be acknowledged, hardware LCALL to the requested service routine will be the next instruction to be executed. Else the interrupt will pending. The call itself takes 7 machine cycles. Thus a minimum of 3+7 complete machine cycles will elapse between activation and external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine.

If the instruction in progress is not in its final cycle and the instruction in progress is RETI, the additional wait time is 8 machine cycles. For a single interrupt system, if the next instruction is 20 machine cycles long (the longest instructions DIV & MUL are 20 machine cycles long for 16-bit operation), adding the LCALL instruction 7 machine cycles the total response time is 2+8+20+7 machine cycles.

Thus interrupt response time is always more than 10 machine cycles and less than 37 machine cycles.

7.10.9 External Interrupt Inputs

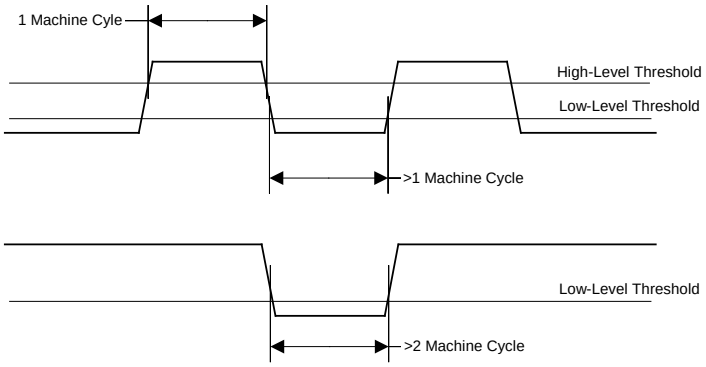
The SH79F6488/SH79F6489 has 5 external interrupt inputs. External interrupt0-3 each has one vector address. External interrupt 4 has 7 inputs; all of them share one vector address. These external interrupts can be programmed to be level-triggered or edge-triggered by clearing or setting bit IT1 or IT0 in register TCON and register EXF1. If ITn = 0 (n = 0 - 1), external interrupt 0/1 is triggered by a low level detected at the INT0/1 pin. If ITn = 1 (n = 0 - 1), external interrupt 0/1 is edge triggered. In this mode if consecutive samples of the INT0/1 pin show a high level in one cycle and a low level in the next cycle, interrupt request flag in register r EXF1 is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

If the external interrupt is edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag is set. Notice that IE0-1 is automatically cleared by CPU when the service routine is called while IF4x should be cleared by software. External interrupt4 operates in the similar ways except have different registers and have more selection of trigger.

If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag IEx (x = 0, 1, 2, 3) when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the SH79F6488/SH79F6489 is put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation.

***Note**: IE0-3 is automatically cleared by CPU when the service routine is called while IF40-47 should be cleared by software.*



External Interrupt Detecting

7.10.10 Interrupt Summary

Source	Vector Address	Enable bits	Flag bits	Polling Priority	Interrupt No. (C51)
Reset	0000H	-	-	0 (higest)	-
INT0	0003H	EX0	IE0	1	0
Timer4	000BH	ET4	TF4	2	1
INT1	0013H	EX1	IE1	3	2
Timer3	001BH	ET3	TF3	4	3
EUART	0023H	ES	RI+TI	5	4
Timer2	002BH	ET2	TF2+EXF2	6	5
ADC	0033H	EADC	ADCIF	7	6
SPI	003BH	ESPI	SPIF	8	7
INT2	0043H	EX2	IE2	9	8
INT3	004BH	EX3	IE3	10	9
INT4	0053H	EX4+IENC	IF45-40	11	10
USB (for 6489)	005BH	EUSB	Refers to the USB	12(6489)	11
PWM	0063H	EPWM+PWM0/1/2IE	PWM0/1/2IF	12(6488)/13(6489)	12
BaseTimer	006BH	EBT	BTIF	13(6488)/14(6489)	13
SCM	0073H	ESCM	SCMIF	14(6488)/15(6489) (Lowest)	14

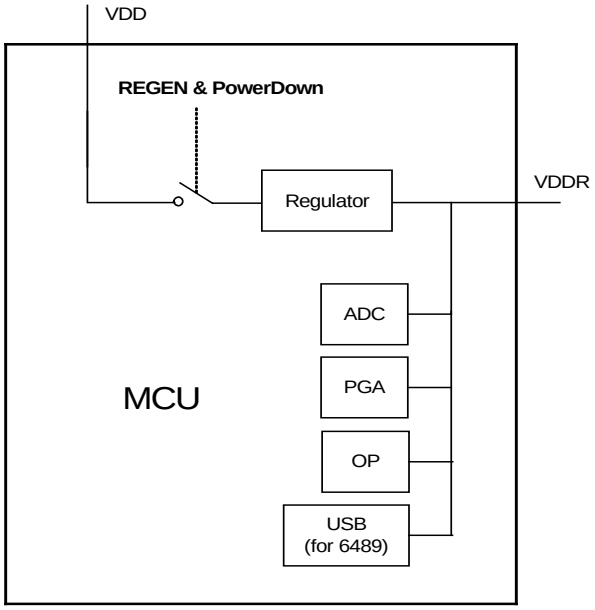
8. Enhanced Function

8.1 Regulator

8.1.1 Features

- Stable voltage output
- Selectable on/off of regulator

The SH79F6488/SH79F6489 has one regulator. The regulator can output the optional voltage 2.7V or 3.3V for analog device such as OP, PGA, USB (for 6489) and ADC. as well as sensor. The output voltage can be selected by register REGS. This regulator will shutdown by clearing REGEN of REGCON register in Power-Down.



8.1.2 Registers

Table 8.1 Regulator Control Register

A1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REGCON	-	-	-	-	-	-	REGS	REGEN
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1	**REGS**	**Regulator output voltage selection bit** 0: regulator output 2.7V 1: regulator output 3.3V
0	**REGEN**	**Regulator control bit** 0: shutdown regulator 1: start regulator The regulator will shut down by software when MCU in Power-Down mode.

8.2 LCD Driver

SH79F6488/SH79F6489 has two LCD drive mode: Normal Resistor LCD Driver with Fast charge and low power

LCD driver can work in IDLE and Power-down mode.

8.2.1 Normal Resistor LCD Driver with Fast charge

The LCD driver contains a controller, a duty cycle generator with 4/5/6 Common signal pins and 34/35/36 Segment driver pins. Segment 1-36 and COM1-COM4 can also be used as I/O port, it is controlled by the P5SS、P6SS、P7SS、P8SS、PXSS register.

The 36 bytes display data RAM is addressed to 900H-923H, which could be used as data memory if needed.

The MCU consists normal display topologies with contrast adjustment which supports both 1/4duty-1/3bias and 1/5duty-1/3 bias and 1/6duty-1/3 bias driving mode. Fast Charge mode can effectively reduce the power consumption.

In addition, the LCD also provide another kind of work mode:Low power consumptionLCD (SLP), supports both 1/2/3/4COM duty.

V_{LCD} equals to V_{DD}.

When MCU enters the Power-Down mode, the SLP LCD will be tsuggested.

During the Power on Reset or Pin Reset or LVR Reset or Watch-dog Reset, the LCD will be turned off, and Common and Segment will output low.

The features of the LCD Normal Display Mode include the following:

- 1/4duty -1/3 bias or 1/5 duty - 1/3 bias by configuring the DUTY bit in LCDCON register.
- LCD frame = 64Hz.
- 4 levels contrast adjustment by configuring the CONTR[1:0] bits in LCDCON1 register.

LCD bias resistor (R_{LCD}) can be selected as 20K/150KΩ.The relatively high current drain through the 20k resistor will get better LCD display effect, but it may not be suitable for some low current consume application. Lowering this current is possible by configucring the MOD[1:0] for switching the R_{LCD} value to 150K.

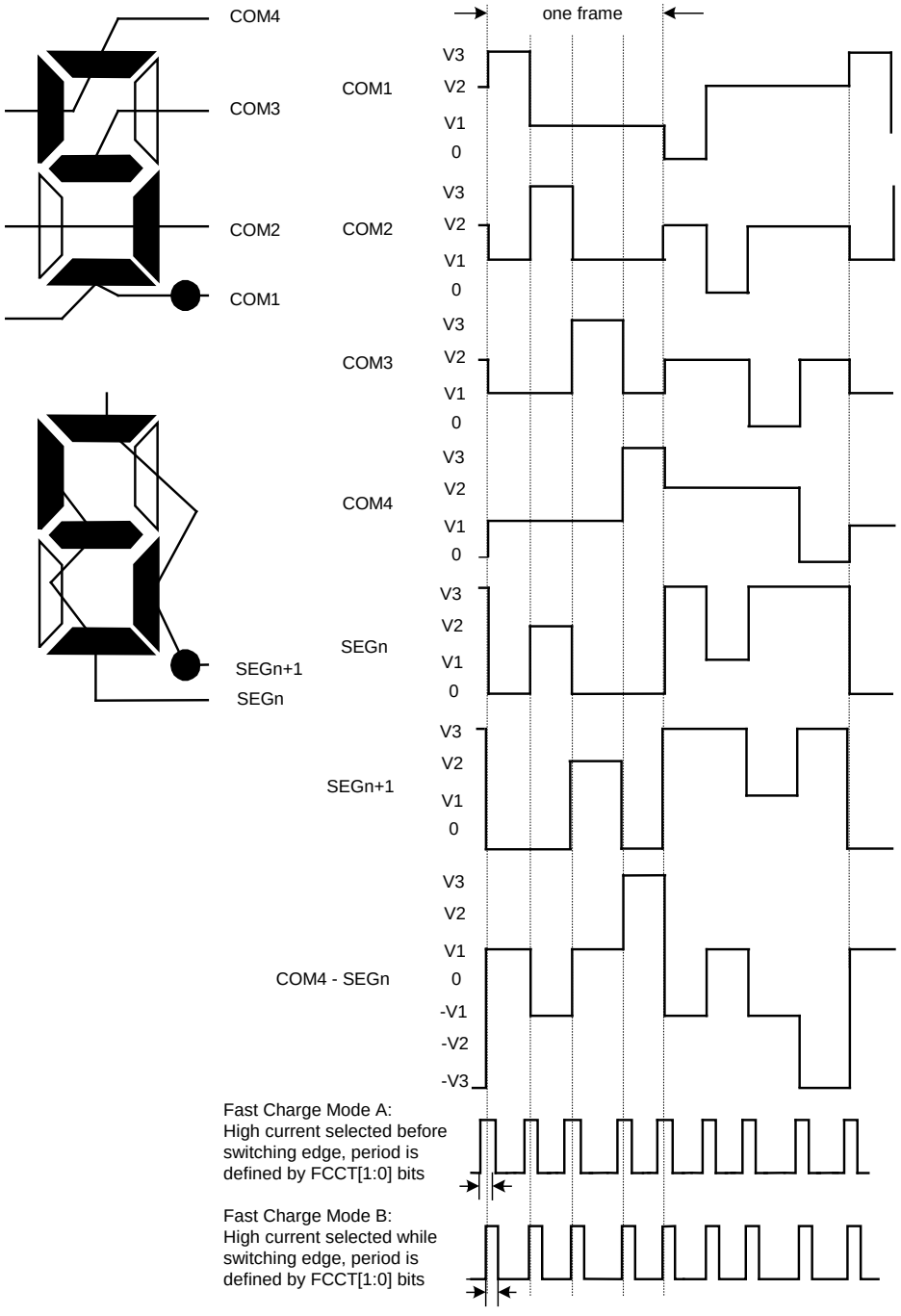
Therefore, SH79F6488/SH79F6489 provides both the low power consumption and display effect of the display mode:fast charge mode.

When refresh the display data 20k bias resistors are selected to provide larger current.When keep the display data 150K bias resistors are selected to save drive current. Charging time is selected as 1/4、1/8、1/16 or 1/32 of LCD com period by FCCTL[1:0] in DISPCLK1 register.

The definition of the LCD clock is as following:

(1) when code option OP_OSC = 0000, LCDCLK is about 32kHz from internal 12MHz RC prescaler. (Refer to code option section for details)

(2) when code option OP_OSC = 1010, LCDCLK is 32.768kHz crystal oscillator. (Refer to code option section for details)



LCD Waveform (1/4duty, 1/3bias)

Registers

Table 8.2 LCD Control Register

ABH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCON	LCDON	MOD1	MOD0	-	DUTY1	DUTY0	-	-
R/W	R/W	R/W	R/W	-	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	-	-

Bit Number	Bit Mnemonic	Description
7	**LCDON**	**LCD control bit** 0: turn off LCD driver 1: turn on LCD driver
6-5	**MOD[1:0]**	**LCD Drive mode selection bits** 00: traditional mode, bias resistor sum is 150K 01: traditional mode, bias resistor sum is 20K 10: fast charge mode, bias resistor sum switch between 20K and 150K 11: SLP LCD
3-2	**DUTY[1:0]**	**LCD duty selection bits** 00: 1/4 duty 01: 1/5 duty 10: 1/6 duty 11: 1/4 duty

Table 8.3 LCD CONTRAST Register

AAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON1	FCMOD	-	FCCTL1	FCCTL0	-	-	CONTR1	CONTR0
R/W	R/W	-	R/W	R/W			R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0			0	0

Bit Number	Bit Mnemonic	Description
7	**FCMOD**	**Fast charge mode control bit** 0: fast charge modeA 1: fast charge modeB
5-4	**FCCTL[1:0]**	**Fast charge time control bits** 00: 1/4 LCD com period 01: 1/8 LCD com period 10: 1/16 LCD com period 11: 1/32 LCD com period
1-0	**CONTR[1:0]**	**LCD Contrast control** 00: V_{LCD} = 0.60V_{DD} 01: V_{LCD} = 0.75V_{DD} 10: V_{LCD} = 0.85V_{DD} 11: V_{LCD} = 1.00V_{DD}

Note: *In SLPLCD mode, the operation of FCCTL, DUTY, CONTR registers will have no effect.*

Table 8.4 P5 Mode Select Register

9EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5SS	P5S7	P5S6	P5S5	P5S4	P5S3	P5S2	P5S1	P5S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P5S[7:0]**	**P0 mode select** 0: P5.0-P5.7 is I/O 1: P5.0-P5.7 is Com or Segment

Table 8.5 P6 Mode Select Register

9FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6SS	P6S7	P6S6	P6S5	P6S4	P6S3	P6S2	P6S1	P6S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P6S[7:0]**	**P1 mode select** 0: P6.0-P6.7 is I/O 1: P6.0-P6.7 is Segment

Table 8.6 P7 Mode Select Register

ACH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7SS	P7S7	P7S6	P7S5	P7S4	P7S3	P7S2	P7S1	P7S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P7S[7:0]**	**P7 mode select bit** 0: P7.0-P7.7 is I/O 1: P7.0-P7.7 share as Segment

Table 8.7 P8 Mode Select Register

ADH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P8SS	P8S7	P8S6	P8S5	P8S4	P8S3	P8S2	P8S1	P8S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**P3S[7:0]**	**P8 mode select bit** 0: P8.0-P8.7 is I/O 1: P8.0-P8.7 share as Segment

Table 8.8 PX Mode Select Register

AEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PXSS	P4S3	P4S2	P4S1	P4S0	P3S3	P3S2	P3S1	P3S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-4	**P4S[3:0]**	**P4 mode select bit** 0: P4.3-P4.0 is I/O 1: P4.3-P4.0 share as Segment
3-0	**P3S[3:0]**	**P3 mode select bit** 0: P3.3-P3.0is I/O 1: P3.3-P3.0 share as Segment

8.2.2 Super Low Power LCD (SLP LCD) Display Mode

The SLP LCD mode support 1/2/3/4COM duty .

The LCD module will work in SLP LCD Display Mode by Configuring the MOD[1:0] bits as '11' in LCDCON register, and the LCD module will switch to this mode without contrast adjustment automatically.

In this mode, the operation of FCCTL[1:0], DUTY, CONTR[2:0] bits will have no effect.

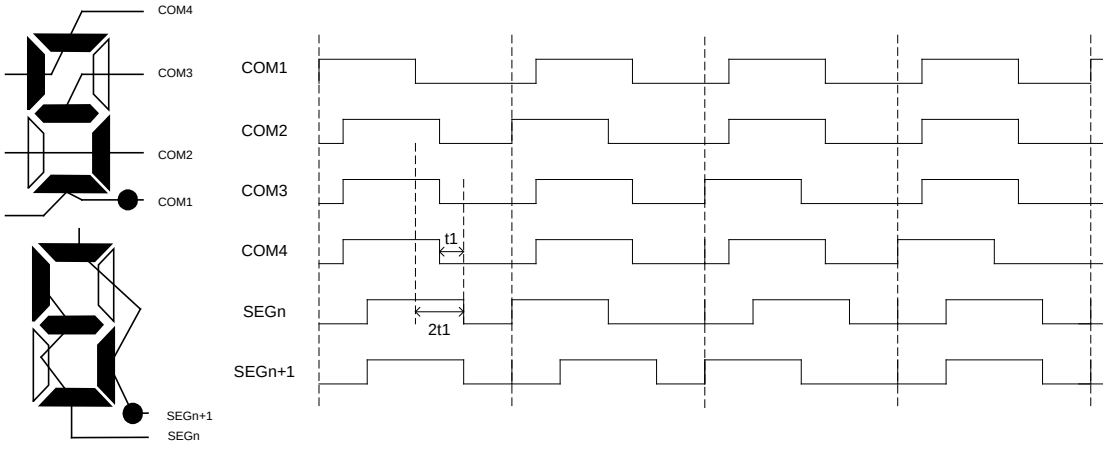
The SLP LCD clock source is 256Hz, and the frame frequency is 64Hz. Changing the value of SLPD[4:0] will adjust the SLP LCD display effect.

The SLP LCD Display Mode control registers are described in the following Table.

Table 8.9 SLP LCD Control Register

AFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PLCON	-	SLPDUTY1	SLPDUTY0	SLPD4	SLPD3	SLPD2	SLPD1	SLPD0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-5	**SLPDUTY[1:0]**	**LCD duty control** 00: 1COM, LCD COM: COM1 01: 2COM, LCD COM: COM1-2 10: 3COM, LCD COM: COM1-3 11: 4COM, LCD COM: COM1-4
4-0	**SLPD [4:0]**	**SLP LCD Duty select** SLP LCD clock source: $F_{pl} = \frac{LCDCLK}{128}$ Frame Frequency: $F_{frame} = \frac{LCDCLK}{128 \times 4}$ $t1 = \frac{SLPD[4:0]+1}{F_{pl} \times 2 \times 2 \times 32}$ LCDCLK = 32KHz



SLP LCD Mode Waveform

8.2.3 Configuration of LCD RAM

LCD 1/4 duty, 1/3 bias (COM1 - 4, SEG1 - 36)

Address	7	6	5	4	3	2	1	0
	-	-	-	-	COM4	COM3	COM2	COM1
$900h	-	-	-	-	SEG1	SEG1	SEG1	SEG1
$901h	-	-	-	-	SEG2	SEG2	SEG2	SEG2
$902h	-	-	-	-	SEG3	SEG3	SEG3	SEG3
$903h	-	-	-	-	SEG4	SEG4	SEG4	SEG4
$904h	-	-	-	-	SEG5	SEG5	SEG5	SEG5
$905h	-	-	-	-	SEG6	SEG6	SEG6	SEG6
$906h	-	-	-	-	SEG7	SEG7	SEG7	SEG7
$907h	-	-	-	-	SEG8	SEG8	SEG8	SEG8
$908h	-	-	-	-	SEG9	SEG9	SEG9	SEG9
$909h	-	-	-	-	SEG10	SEG10	SEG10	SEG10
$90Ah	-	-	-	-	SEG11	SEG11	SEG11	SEG11
$90Bh	-	-	-	-	SEG12	SEG12	SEG12	SEG12
$90Ch	-	-	-	-	SEG13	SEG13	SEG13	SEG13
$90Dh	-	-	-	-	SEG14	SEG14	SEG14	SEG14
$90Eh	-	-	-	-	SEG15	SEG15	SEG15	SEG15
$90Fh	-	-	-	-	SEG16	SEG16	SEG16	SEG16
$910h	-	-	-	-	SEG17	SEG17	SEG17	SEG17
$911h	-	-	-	-	SEG18	SEG18	SEG18	SEG18
$912h					SEG19	SEG19	SEG19	SEG19
$913h					SEG20	SEG20	SEG20	SEG20
$914h					SEG21	SEG21	SEG21	SEG21
$915h					SEG22	SEG22	SEG22	SEG22
$916h					SEG23	SEG23	SEG23	SEG23
$917h					SEG24	SEG24	SEG24	SEG24
$918h					SEG25	SEG25	SEG25	SEG25
$919h	-	-	-	-	SEG26	SEG26	SEG26	SEG26
$91Ah					SEG27	SEG27	SEG27	SEG27
$91Bh					SEG28	SEG28	SEG28	SEG28
$91Ch					SEG29	SEG29	SEG29	SEG29
$91Dh					SEG30	SEG30	SEG30	SEG30
$91Eh					SEG31	SEG31	SEG31	SEG31
$91Fh					SEG32	SEG32	SEG32	SEG32
$920h					SEG33	SEG33	SEG33	SEG33
$921h					SEG34	SEG34	SEG34	SEG34
$922h					SEG35	SEG35	SEG35	SEG35
$923h					SEG36	SEG36	SEG36	SEG36

LCD 1/5 duty, 1/3 bias (COM1 - 5, SEG2 - 36)

Address	7	6	5	4	3	2	1	0
	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1
$900h	-	-	-	-	-	-	-	-
$901h	-	-	-	SEG2	SEG2	SEG2	SEG2	SEG2
$902h	-	-	-	SEG3	SEG3	SEG3	SEG3	SEG3
$903h	-	-	-	SEG4	SEG4	SEG4	SEG4	SEG4
$904h	-	-	-	SEG5	SEG5	SEG5	SEG5	SEG5
$905h	-	-	-	SEG6	SEG6	SEG6	SEG6	SEG6
$906h	-	-	-	SEG7	SEG7	SEG7	SEG7	SEG7
$907h	-	-	-	SEG8	SEG8	SEG8	SEG8	SEG8
$908h	-	-	-	SEG9	SEG9	SEG9	SEG9	SEG9
$909h	-	-	-	SEG10	SEG10	SEG10	SEG10	SEG10
$90Ah	-	-	-	SEG11	SEG11	SEG11	SEG11	SEG11
$90Bh	-	-	-	SEG12	SEG12	SEG12	SEG12	SEG12
$90Ch	-	-	-	SEG13	SEG13	SEG13	SEG13	SEG13
$90Dh	-	-	-	SEG14	SEG14	SEG14	SEG14	SEG14
$90Eh	-	-	-	SEG15	SEG15	SEG15	SEG15	SEG15
$90Fh	-	-	-	SEG16	SEG16	SEG16	SEG16	SEG16
$910h	-	-	-	SEG17	SEG17	SEG17	SEG17	SEG17
$911h	-	-	-	SEG18	SEG18	SEG18	SEG18	SEG18
$912h	-	-	-	SEG19	SEG19	SEG19	SEG19	SEG19
$913h	-	-	-	SEG20	SEG20	SEG20	SEG20	SEG20
$914h	-	-	-	SEG21	SEG21	SEG21	SEG21	SEG21
$915h	-	-	-	SEG22	SEG22	SEG22	SEG22	SEG22
$916h	-	-	-	SEG23	SEG23	SEG23	SEG23	SEG23
$917h	-	-	-	SEG24	SEG24	SEG24	SEG24	SEG24
$918h	-	-	-	SEG25	SEG25	SEG25	SEG25	SEG25
$919h	-	-	-	SEG26	SEG26	SEG26	SEG26	SEG26
$91Ah	-	-	-	SEG27	SEG27	SEG27	SEG27	SEG27
$91Bh	-	-	-	SEG28	SEG28	SEG28	SEG28	SEG28
$91Ch	-	-	-	SEG29	SEG29	SEG29	SEG29	SEG29
$91Dh	-	-	-	SEG30	SEG30	SEG30	SEG30	SEG30
$91Eh	-	-	-	SEG31	SEG31	SEG31	SEG31	SEG31
$91Fh	-	-	-	SEG32	SEG32	SEG32	SEG32	SEG32
$920h	-	-	-	SEG33	SEG33	SEG33	SEG33	SEG33
$921h	-	-	-	SEG34	SEG34	SEG34	SEG34	SEG34
$922h	-	-	-	SEG35	SEG35	SEG35	SEG35	SEG35
$923h	-	-	-	SEG36	SEG36	SEG36	SEG36	SEG36

LCD 1/6 duty, 1/3 bias (COM1 - 6, SEG3 - 36)

Address	7	6	5	4	3	2	1	0
	-	-	COM6	COM5	COM4	COM3	COM2	COM1
$900h	-	-	-	-	-	-	-	-
$901h	-	-	-	-	-	-	-	-
$902h	-	-	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
$903h	-	-	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
$904h	-	-	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5
$905h	-	-	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
$906h	-	-	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
$907h	-	-	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
$908h	-	-	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
$909h	-	-	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
$90Ah	-	-	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
$90Bh	-	-	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
$90Ch	-	-	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
$90Dh	-	-	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
$90Eh	-	-	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
$90Fh	-	-	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16
$910h	-	-	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17
$911h	-	-	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18
$912h	-	-	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19
$913h	-	-	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20
$914h	-	-	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21
$915h	-	-	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22
$916h	-	-	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23
$917h	-	-	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24
$918h	-	-	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25
$919h	-	-	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26
$91Ah	-	-	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27
$91Bh	-	-	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28
$91Ch	-	-	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29
$91Dh	-	-	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30
$91Eh	-	-	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31
$91Fh	-	-	SEG32	SEG32	SEG32	SEG32	SEG32	SEG32
$920h	-	-	SEG33	SEG33	SEG33	SEG33	SEG33	SEG33
$921h	-	-	SEG34	SEG34	SEG34	SEG34	SEG34	SEG34
$922h	-	-	SEG35	SEG35	SEG35	SEG35	SEG35	SEG35
$923h	-	-	SEG36	SEG36	SEG36	SEG36	SEG36	SEG36

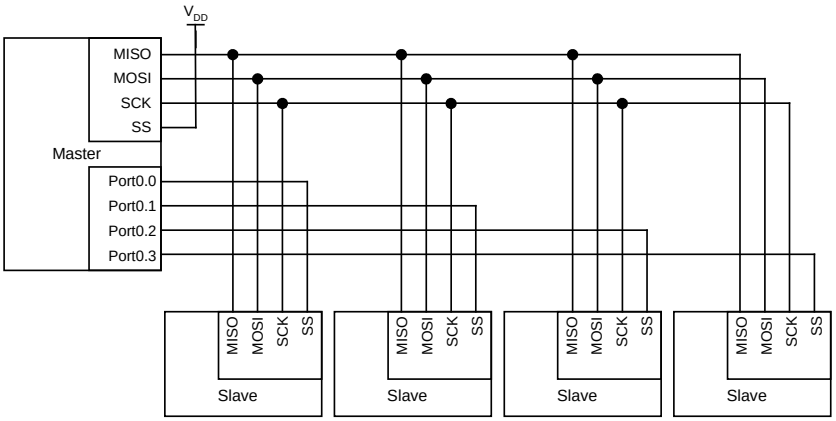
8.3 Serial Peripheral Interface (SPI)

8.3.1 Features

- Full-duplex, three-wire synchronous transfers
- Master or slave operation
- Six programmable master clock rates
- Serial clock with programmable polarity and phase
- Master mode fault error flag with MCU interrupt capability
- Write collision flag protection
- Selectable LSB or MSB transfer

The Serial Peripheral Interface (SPI) Module allows full-duplex, synchronous, serial communication between the MCU and peripheral devices, including other MCUs.

The following diagram shows a typical SPI bus configuration using one master controller and many slave peripherals. The bus is made of three wires connecting all the devices. The master device selects the individual slave devices by using four pins of a parallel port to control the four SS pins of the Slave devices.



8.3.2 Signal Description

(1) Master Output Slave Input (MOSI)

This 1-bit signal is directly connected between the master device and slave devices. The MOSI line is used to transfer data in series from the master to the slave. Therefore, it is an output signal from the master, and an input signal to a slave.

(2) Master Input Slave Output (MISO)

This 1-bit signal is directly connected between the slave devices and master device. The MISO line is used to transfer data in series from the slave to the master. Therefore, it is an output signal from the slave, and an input signal to the master. The MISO pin is placed in a high-impedance state when the SPI operates as a slave that is not selected ($\overline{SS}$ high).

A static high level on the $\overline{SS}$ pin puts the MISO line of a slave in a high-impedance state.

(3) SPI Serial Clock (SCK)

This signal is used to synchronize the data movement both in and out of the devices through their MOSI and MISO lines. It is driven by the master for eight clock cycles, which allows exchanging one byte on the serial lines. The SCK signal is ignored by a SPI slave when the slave is not selected ($\overline{SS}$ high).

(4) Slave Select ($\overline{SS}$)

Each slave peripheral is selected by one slave select pin ($\overline{SS}$). This signal must stay low for any active slave. It is obvious that only one master ($\overline{SS}$ high) can drive the network. The master may select each slave device by software through port pins. To prevent bus conflicts on the MISO line, only one slave should be selected at a time by the master for a transmission.

In a master configuration, the $\overline{SS}$ line can be used in conjunction with the MODF flag in the SPI status register to prevent multiple masters from driving MOSI and SCK.

The $\overline{SS}$ pin could be used as a general IO if the following conditions are met:

(a) The device is configured as a master and the SSDIS control bit in SPCON is set. This kind of configuration can happen when only one master is driving the network. Therefore, the MODF flag in the SPSTA will never be set.

(b) The device is configured as a slave with CPHA and SSDIS control bits set. This kind of configuration can happen when the network comprises only one master and one slave only. Therefore, the device should always be selected and the master will never use the slave's $\overline{SS}$ pin to select the target communication slave.

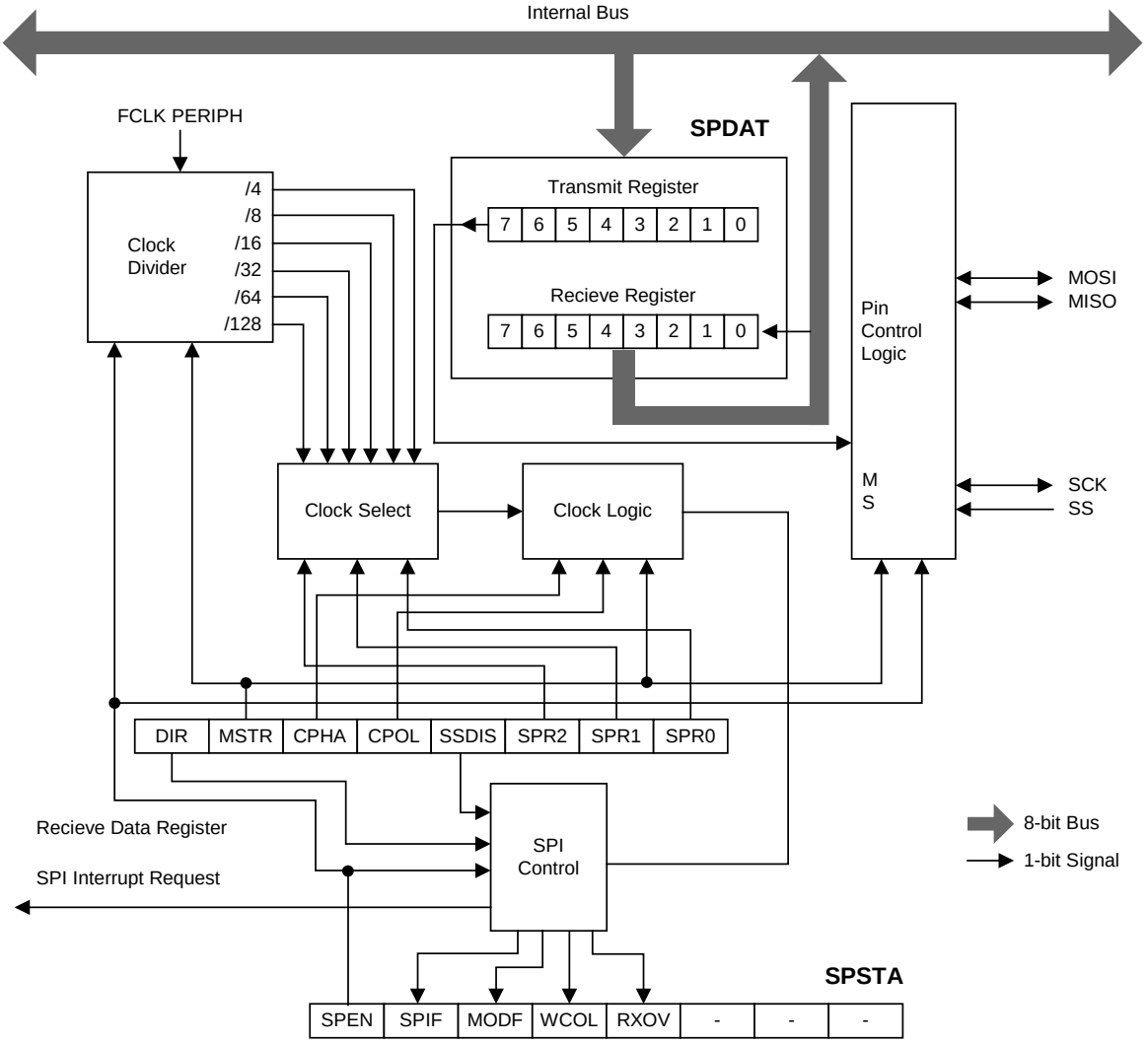
Note: *When CPHA = '0', a falling edge of $\overline{SS}$ pin is used to start the transmission.*

8.3.3 Baud Rate

In master mode, the baud rate is chosen from one of the six clock rates by the division of the internal clock by 4, 8, 16, 32, 64 or 128 set by the three bits SPR[2:0] in the SPCON register.

8.3.4 Functional Description

The following diagram shows a detailed structure of the SPI module.



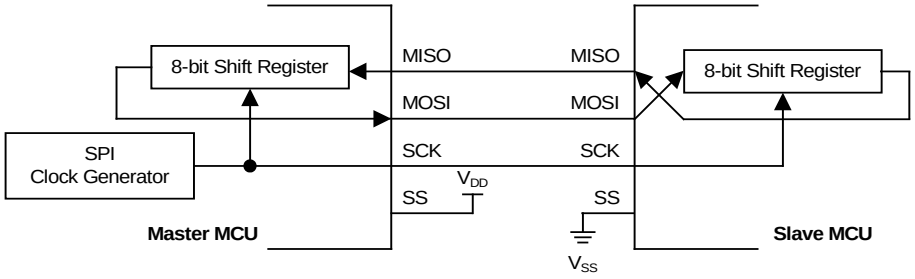
SPI Module Block Diagram

8.3.5 Operating Modes

The Serial Peripheral Interface can be configured as one of the two modes, master mode or slave mode. The configuration and initialization of the SPI module is made through SPCON (the serial peripheral control register) and SPSTA (the serial peripheral status register). Once the SPI is configured, the data exchange is made using SPCON, SPSTA and SPDAT (the serial peripheral data register).

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (SCK) synchronizes shifting and sampling on the two serial data lines (MOSI and MISO). A slave select line ($\overline{SS}$) allows individual selection of a SPI slave; SPI slaves that are not selected do not interfere with SPI bus activities.

When the SPI master transmits data to the SPI slave via the MOSI line, the SPI slave responds by sending data to the SPI master via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock. Both transmit shift register and receive shift register uses the same SFR Address, a write operation to SPDAT will write to the transmit shift register, and a read operation from SPDAT will retrieve the data in receive shift register.



Full-Duplex Master-Slave Interconnection Diagram

Master Mode

(1) Enable

A SPI master device initiates all data transfers on a SPI bus. The SPI operates in master mode when the MSTR is set in SPCON register. Only one master can initiate transmission.

(2) Transmit

When in SPI master mode, writing a byte of data to the SPI data register (SPDAT) will write to the transmit shift buffer. If the transmit shift register already contains data, the SPI master will generate a WCOL signal to indicate writing too fast. But the data in transmit shift register will not be affected, and the transmission continues uninterrupted. Else if the transmit shift register is empty, the SPI master will immediately shifts out the data serially on the MOSI line while providing the serial clock on SCK. The SPIF flag in SPSTA register is set to logic '1' at the end of the transfer. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set.

(3) Receive

While the master transfers data to a slave on the MOSI line, the addressed slave simultaneously transfers the contents of its transmit shift register to the master's receive shift register on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first or LSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPDAT. If an overrun occurs, RXOV signal will be set to indicate data over-run occurs, and the receive shift register keep the byte that SPIF was lastly set, also the SPI master will not receive any further data until SPIF was cleared.

Slave Mode

(1) Enable

The SPI operates in slave mode when the MSTR is cleared in the SPCON register. Before a data transmission occurs, the slave select ($\overline{SS}$) pin of the Slave device must be set to '0'. The $\overline{SS}$ pin must remain low until the 1-byte transmission is complete.

(2) Transmit & Receive

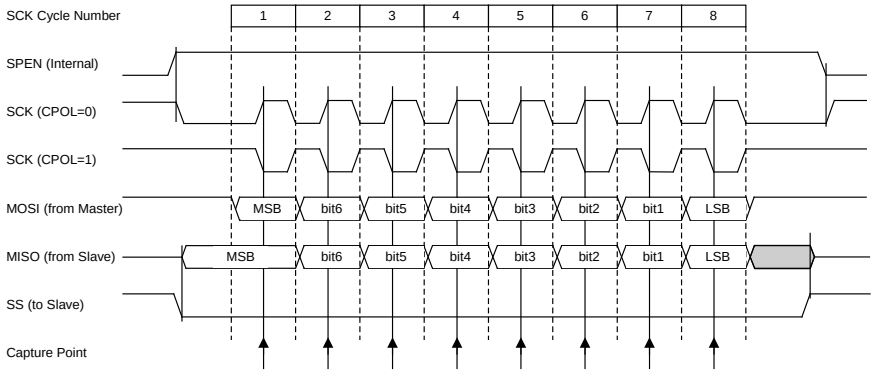
When in SPI slave mode, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter counts SCK edges. When 8 bits have been shifted in the receive shift register and another 8 bits have been shifted out the transmit shift register, the SPIF flag is set to logic '1'. Data is read from the receive shift register by reading SPDAT. If interrupts are enabled, an interrupt request is generated when the SPIF flag is set.

To prevent an overflow condition, the SPI slave software must clear the SPIF bit in SPSTA register before another byte enters the receive shift register. Else a RXOV signal will be set to indicate data over-run occurs, and the receive shift register keep the byte that SPIF was lastly set, also the SPI slave will not receive any further data until SPIF was cleared.

A SPI slave cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPDAT. Writes to SPDAT are placed in the transmit buffer first. So a SPI slave must complete the write to the SPDAT (transmit shift register) in one SPI clock before the master starts a new transmission. If the write to SPDAT is late in the first transmission, the SPI slave will transmit a '0x00' byte in the following transmission. if the write operation occurs during this time, a WCOL signal will be set. If the transmit shift register already contains data, the SPI slave will generate a WCOL signal to indicate writing too fast. But the data in transmit shift register will not be affected, and the transmission continues uninterrupted.

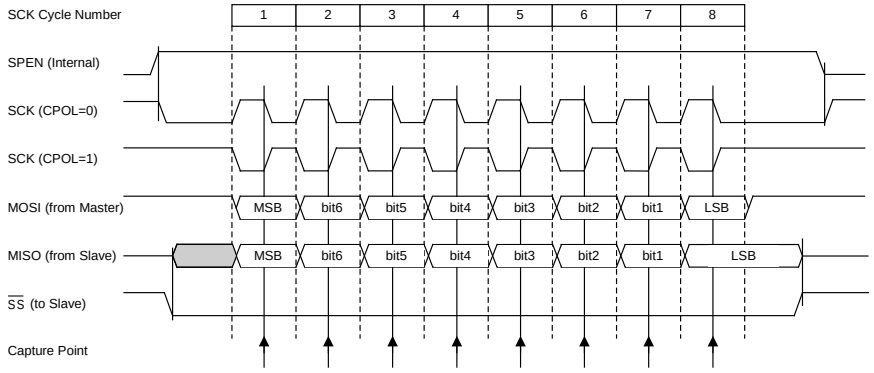
8.3.6 Transmission Formats

Software can select any of four combinations of serial clock (SCK) phase and polarity using two bits in the SPCON, the clock polarity CPOL and the clock phase CPHA. CPOL defines the default SCK line level in idle state. It has no significant effect on the transmission format. CPHA defines the edges on which the input data are sampled and the edges on which the output data are shifted. The clock phase and polarity should be identical for the master and the communicating slave.



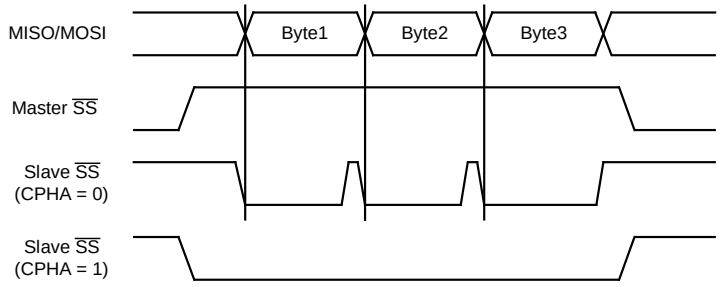
Data Transmission Format (CPHA = 0)

If CPHA = 0, the first SCK edge is the capture strobe. Therefore the slave must begin driving its data before the first SCK edge, and a falling edge on the $\overline{SS}$ pin is used to start the transmission. The $\overline{SS}$ pin must be toggled high and then low between each byte transmitted. So SSDIS bit is invalid when CPHA = 0.



Data Transmission Format (CPHA = 1)

If CPHA = 1, the master begins driving its MOSI pin on the first SCK edge. Therefore the slave uses the first SCK edge as a start transmission signal. So the user must put the SPDAT before the second edge of the first SCK. The $\overline{SS}$ pin can remain low between transmissions. This format may be preferred in systems with only one master and only one slave.



CPHA/$\overline{SS}$ Timing

Note: *Before SPI is configured as Slave mode and CPOL bit in SPCON is cleared, the P2.4SCK pin must be set to input mode and enable pull-high resistor before SPEN bit in SPSTA is set to logic '1'.*

8.3.7 Error Conditions

The following flags in the SPSTA signal SPI error conditions:

(1) Mode Fault (MODF)

Mode fault error in master mode SPI indicates that the level on the $\overline{SS}$ pin is inconsistent with the actual mode of the device. MODF is set to warn that there may be a multi-master conflict for system control. In this case, the SPI system is affected in the following ways:

- An SPI receiver/error CPU interrupt request is generated;
- The SPEN bit in SPSTA is cleared. This disables the SPI;
- The MSTR bit in SPCON is cleared.

When $\overline{SS}$ Disable (SSDIS bit in the SPCON register) is cleared, the MODF flag is set when the $\overline{SS}$ signal becomes '0'. However, as stated before, for a system with one Master, if the $\overline{SS}$ pin of the master device is pulled low, there is no way that another master attempts to drive the network. In this case, to prevent the MODF flag from being set, software can set the SSDIS bit in the SPCON register and therefore making the $\overline{SS}$ pin as a general-purpose I/O pin.

The user must clear the MODF bit by software, and enable SPEN in SPCON register again for further communication, and enable MSTR bit to continue master mode.

(2) Write Collision (WCOL)

A write collision (WCOL) flag in the SPSTA is set when a write to the SPDAT register is done during a transmit sequence. WCOL does not cause an interruption, and the transfer continues uninterrupted. The WCOL bit is cleared by software.

(3) Overrun Condition (RXOV)

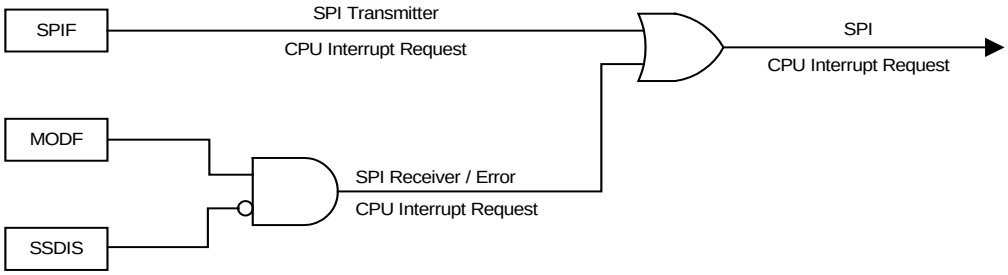
An overrun condition occurs when the master or slave tries to send several data bytes and the slave or master has not cleared the SPIF bit issuing from the previous data byte transmitted. In this case, the receive shift register keep the byte that SPIF was lastly set, also the SPI device will not receive any further data until SPIF was cleared. The SPIF still keep on invoke interrupt before it is cleared, though the transmission can still be driven by SCK. RXOV does not generate an interruption, the RXOV bit is cleared by software.

8.3.8 Interrupts

Two SPI status flags can generate a CPU interrupt requests SPIF & MODF.

Serial Peripheral data transfer flag: SPIF. This bit is set by hardware when a transfer has been completed.

Mode Fault flag: MODF. This bit becomes set to indicate that the level on the $\overline{SS}$ pin is inconsistent with the mode of the SPI. MODF with SSDIS reset will generate receiver/error CPU interrupt requests. When SSDIS is set, no MODF interrupt request is generated.



SPI Interrupt Requests Generation

8.3.9 Registers

Table 8.10 Serial Peripheral Control Register

A4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPCON	DIR	MSTR	CPHA	CPOL	SSDIS	SPR2	SPR1	SPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**DIR**	**Transfer Direction Selection** 0: MSB first 1: LSB first
6	**MSTR**	**Serial Peripheral Master** 0: Configure the SPI as a Slave 1: Configure the SPI as a Master
5	**CPHA**	**Clock Phase** 0: Data sampled on first edge of SCK period 1: Data sampled on second edge of SCK period
4	**CPOL**	**Clock Polarity** 0: SCK line low in idle state 1: SCK line high in idle state
3	**SSDIS**	**$\overline{SS}$ Disable** 0: Enable $\overline{SS}$ pin in both Master and Slave modes 1: Disable $\overline{SS}$ pin in both master and slave modes MODF interrupt request will not generate, if SSDIS is set. In Slave mode, this bit has no effect if CPHA = 0.
2-0	**SPR[2:0]**	**Serial Peripheral Clock Rate** 000: $f_{SYS}/4$ 001: $f_{SYS}/8$ 010: $f_{SYS}/16$ 011: $f_{SYS}/32$ 100: $f_{SYS}/64$ Others: $f_{SYS}/128$

Table 8.11 Serial Peripheral Status Register

A5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPSTA	SPEN	SPIF	MODF	WCOL	RXOV	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	-	-	-

Bit Number	Bit Mnemonic	Description
7	**SPEN**	**SPI Enable** 0: Disable the SPI interface 1: Enable the SPI interface
6	**SPIF**	**Serial Peripheral data transfer flag** 0: Clear by software 1: Set by hardware to indicate that the data transfer has been completed
5	**MODF**	**Mode Fault** 0: Cleared by software 1: Set by hardware to indicate that the $\overline{SS}$ pin is at inappropriate logic level
4	**WCOL**	**Write Collision flag** 0: Cleared by software to indicate write collision has bee processed 1: Set by hardware to indicate that a collision has been detected
3	**RXOV**	**Receive Overrun** 0: Cleared by software to indicate receive overrun has bee processed 1: Set by hardware to indicate that a receive overrun has been detected

Table 8.12 Serial Peripheral Data Register

A6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPDAT	SPDAT7	SPDAT6	SPDAT5	SPDAT4	SPDAT3	SPDAT2	SPDAT1	SPDAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SPDAT[7:0]**	A write to SPDAT places data directly into the transfer shift register. A Read of the SPDAT returns the value located in the receive shift register.

***Note**: When SPI is disabled, the data of SPDAT is invalid.*

8.4 PWM (Pulse Width Modulation)

8.4.1 Features

- Three 12-bit PWM output
- Provided interrupt function on period
- Selectable output polarity

The SH79F6488/SH79F6489 has three 12-bit PWM modules. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMxEN (x = 0-2) is used to enable three PWM modules. The PWMxCON (x = 0-2) is used to control the clock source, output mode and cycle interrupt of the PWM module output, and so on. The PWMxPH/L (x = 0-2) is used to control the period cycle of the PWM module output. PWMxDH/L (x = 0-2) is used to control the duty in the waveform of the PWM module output.

8.4.2 PWM Registers

Table 8.13 PWMx (x = 0-2) Control Registers

C5H, C6H, C7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0CON (C5H)	PWM0EN	PWM0S	PWM0CK1	PWM0CK0	-	PWM0IE	PWM0IF	PWM0SS
PWM1CON (C6H)	PWM1EN	PWM1S	PWM1CK1	PWM1CK0	-	PWM1IE	PWM1IF	PWM1SS
PWM2CON (C7H)	PWM2EN	PWM2S	PWM2CK1	PWM2CK0	-	PWM2IE	PWM2IF	PWM2SS
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0		0	0	0

Bit Number	Bit Mnemonic	Description
7	**PWMxEN**	**PWMx enable bit** 0: Disable PWMx 1: Enable PWMx
6	**PWMxS**	**PWMx output normal mode of duty cycle** 0: high active, PWMx output high during duty time, output low during remain period time 1: low active, PWMx output low during duty time, output high during remain period time
5-4	**PWMxCK[1:0]**	**PWMx clock selector:** 00: system clock/1 01: system clock/2 10: system clock/4 11: system clock/8
2	**PWMxIE**	**PWMx interrupt enable bit** 0: Disable PWMx interrupt 1: Enable PWMx interrupt
1	**PWMxIF**	**PWMx interrupt flag** 0: Clear by software 1: Set by hardware to indicate that the PWM0 period counter overflow
0	**PWMxSS**	**Enable 12-bit PWMx** 0: I/O port 1: PWM output

Table 8.14 PWM0 Period Register PWM0PH/L

D2H, D1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0PH (D2H)	-	-	-	-	PWM0P.11	PWM0P.10	PWM0P.9	PWM0P.8
PWM0PL (D1H)	PWM0P.7	PWM0P.6	PWM0P.5	PWM0P.4	PWM0P.3	PWM0P.2	PWM0P.1	PWM0P.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
11-0	**PWM0P[11:0]**	12-bit PWM0 period registers

When PWM0PH/L = 0, PWM0 outputs GND if the PWM0S bit is set to “0”. PWM0 outputs high level if the PWM0S bit is set to “1”.

Table 8.15 PWM1 Period Register PWM1PH/L

D4H, D3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1PH (D4H)	-	-	-	-	PWM1P.11	PWM1P.10	PWM1P.9	PWM1P.8
PWM1PL (D3H)	PWM1P.7	PWM1P.6	PWM1P.5	PWM1P.4	PWM1P.3	PWM1P.2	PWM1P.1	PWM1P.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
11-0	**PWM1P[11:0]**	12-bit PWM1 period registers

When PWM1PH/L = 0, PWM1 outputs GND if the PWM1S bit is set to “0”. PWM1 outputs high level if the PWM1S bit is set to “1”.

Table 8.16 PWM2 Period Register PWM2PH/L

D6H, D5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2PH (D6H)	-	-	-	-	PWM2P.11	PWM2P.10	PWM2P.9	PWM2P.8
PWM2PL (D5H)	PWM2P.7	PWM2P.6	PWM2P.5	PWM2P.4	PWM2P.3	PWM2P.2	PWM2P.1	PWM2P.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
11-0	**PWM2P[11:0]**	12-bit PWM2 period registers

When PWM2PH/L = 0, PWM2 outputs GND if the PWM2S bit is set to “0”. PWM2 outputs high level if the PWM2S bit is set to “1”.

Note: *The change of PWMxPH will take affect at the next PWMx period. The user must change PWMxPL at first, and then change PWMxPH for changing PWMx period.*

Table 8.17 PWM Duty Control Register (PWM0DH/L)

DAH, D9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0DH (DAH)	-	-	-	-	PWM0D.11	PWM0D.10	PWM0D.9	PWM0D.8
PWM0DL (D9H)	PWM0D.7	PWM0D.6	PWM0D.5	PWM0D.4	PWM0D.3	PWM0D.2	PWM0D.1	PWM0D.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
11-0	**PWM0D[11:0]**	**12-bit PWM duty registers** If PWM0P ≤ PWM0D, PWM0 outputs high level when the PWM0S bit is set to “0”. PWM0 outputs GND level when the PWM0S bit is set to “1”. If PWM0D = 00H, PWM0 outputs GND level when the PWM0S bit is set to “0”. PWM0 outputs high level when the PWM0S bit is set to “1”.

Table 8.18 PWM Duty Control Register(PWM1DH/L)

DCH, DBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DH (DCH)	-	-	-	-	PWM1D.11	PWM1D.10	PWM1D.9	PWM1D.8
PWM1DL (DBH)	PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
11-0	**PWM1D[11:0]**	**12-bit PWM duty registers** If PWM1P ≤ PWM1D, PWM1 outputs high level when the PWM1S bit is set to “0”. PWM1 outputs GND level when the PWM1S bit is set to “1”. If PWM1D = 00H, PWM1 outputs GND level when the PWM1S bit is set to “0”. PWM1 outputs high level when the PWM1S bit is set to “1”.

Table 8.19 PWM Duty Control Register (PWM2DH/L)

DEH, DDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM2DH (DEH)	-	-	-	-	PWM2D.11	PWM2D.10	PWM2D.9	PWM2D.8
PWM2DL (DDH)	PWM2D.7	PWM2D.6	PWM2D.5	PWM2D.4	PWM2D.3	PWM2D.2	PWM2D.1	PWM2D.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
11-0	**PWM2D[11:0]**	**12-bit PWM duty registers** If PWM2P ≤ PWM2D, PWM2 outputs high level when the PWM2S bit is set to “0”. PWM2 outputs GND level when the PWM2S bit is set to “1”. If PWM2D = 00H, PWM2 outputs GND level when the PWM2S bit is set to “0”. PWM2 outputs high level when the PWM2S bit is set to “1”.

Note: *The change of PWMxDH will take affect at the next PWMx period. The user must change PWMxDL at first, and then change PWMxDH for changing PWMx duty.*

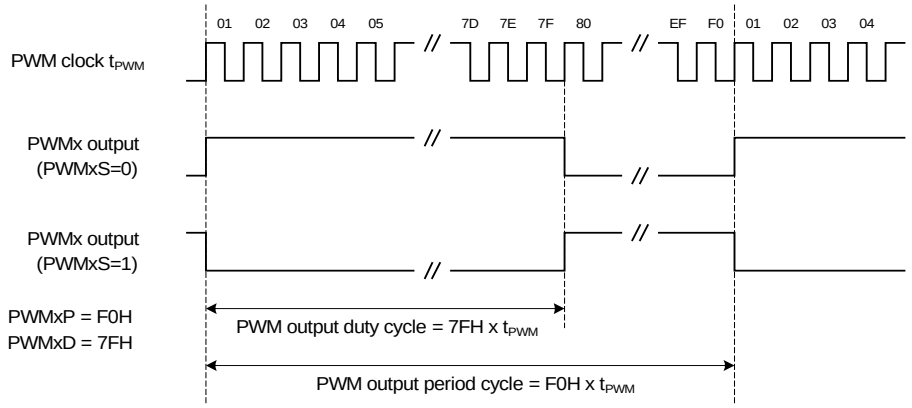
Programming Note:

(1) PWMxEN bit can enable the PWMx module.

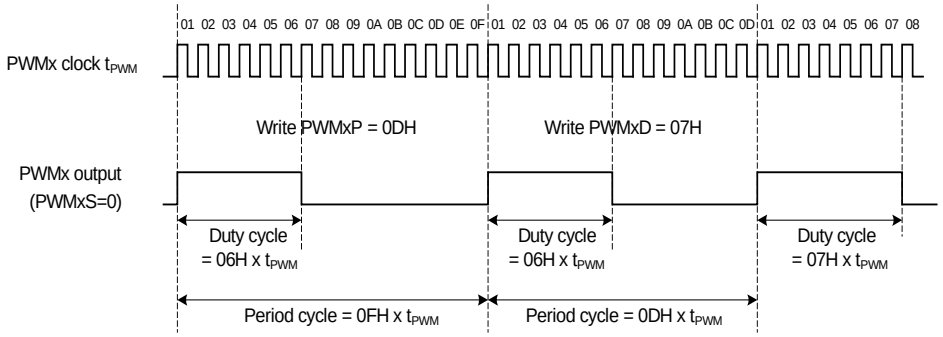
(2) PWMxSS (x = 0-2) bit is used to select the ports used as I/O ports or PWM outputs.

(3) EPWMx in IEN1 register and PWMxIE in PWMxCON can enable the PWMx Timer interrupt.

(4) The PWMx timer is control by PWMENx bit. If this bit is set to 1, but the PWMxSS (x = 0-2) bit is cleared to '0', the PWMx module used as a Timer, if the EPWMx bit in IEN1 register is set to '1' and PWMxIF = 1, the interrupt also can be generated.



PWM output example



PWM output Period or Duty cycle changing example

8.5 EUART

8.5.1 Features

- The SH79F6488/SH79F6489 has one enhanced EUART with own baud rate generator
- The baud rate generator is an 15-bit up-counting timer
- Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
- The EUART can be operated in four modes

8.5.2 EUART Mode Description

The EUART can be operated in 4 modes. Users must initialize the SCON before any communication can take place. This involves selection of the Mode and the baud rate.

In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if RI = 0 and REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

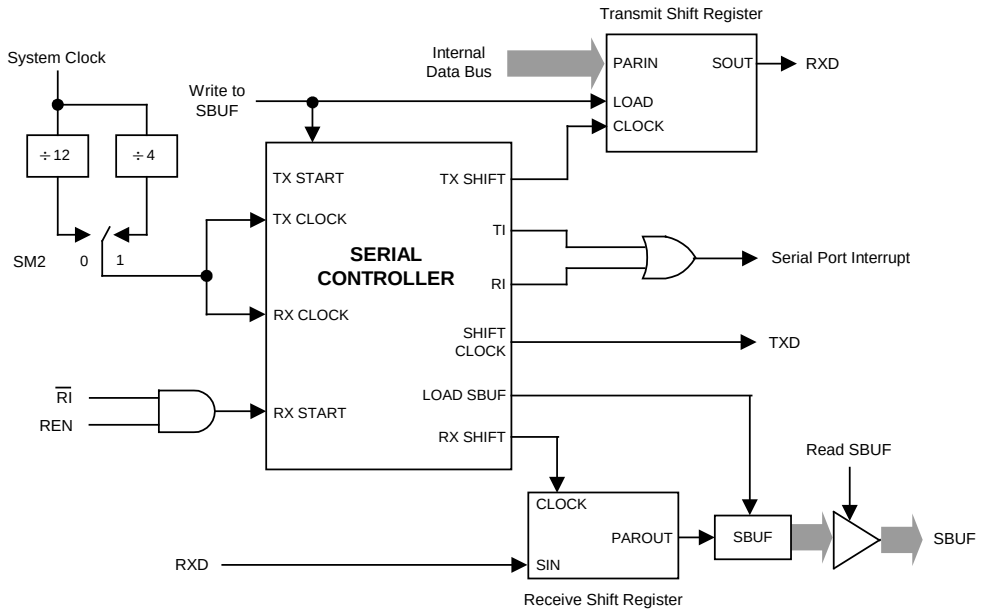
SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit
0	0	0	Sych	f_{SYS}/(4 or 12)	8 bits	NO	NO	None
0	1	1	Ansych	own baud rate/16	10 bits	1	1	None
1	0	2	Ansych	f_{SYS}/(32 or 64)	11 bits	1	1	0, 1
1	1	3	Ansych	own baud rate/16	11 bits	1	1	0, 1

Mode0: Synchronous Mode, Half duplex

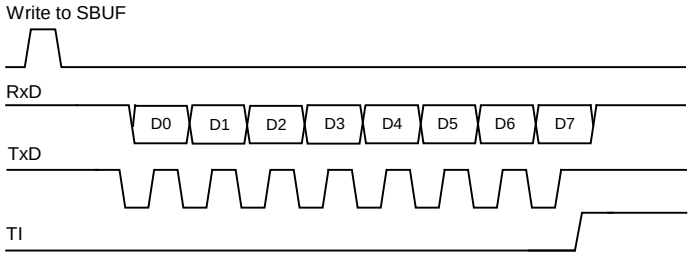
This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RxD line. TxD is used to output the shift clock. The TxD clock is provided by the SH79F6488/SH79F6489 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first.

The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

The functional block diagram is shown below. Data enters and exits the serial port on the RxD line. The TxD line is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the SH79F6488/SH79F6489.

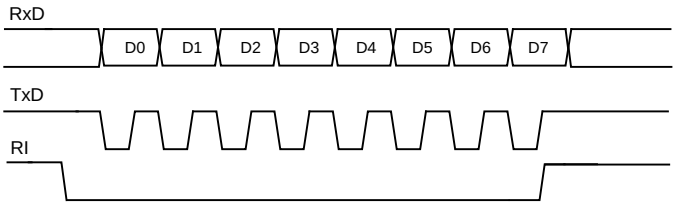


Any instruction that uses SBUF as a destination register (“write to SBUF” signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivates SEND and sets TI (SCON.1) at the rising edge of the next system clock.



Send Timing of Mode 0

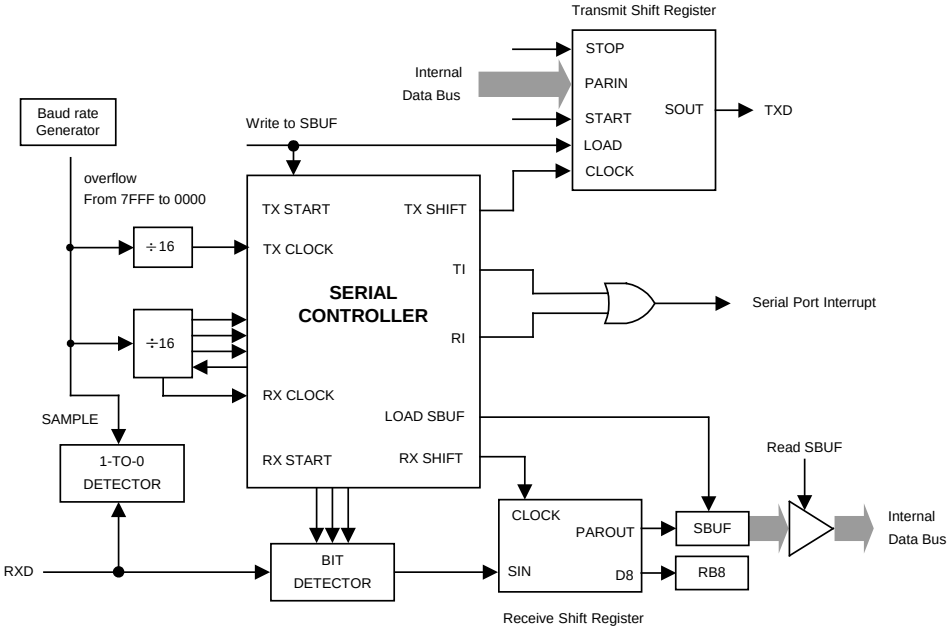
Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivates RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.



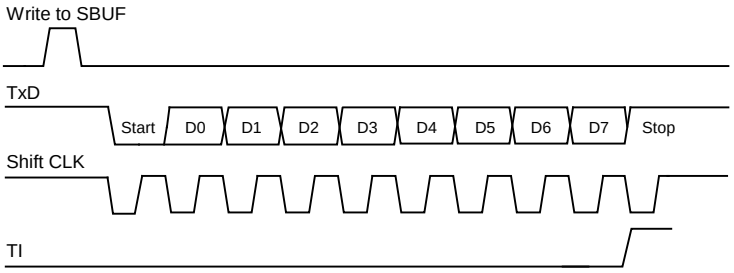
Receive Timing of Mode 0

Mode1: 8-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The baud rate in this mode is 1/16 of own baud rate. The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal. The start bit is firstly put out on TxD pin, then are the 8 bits of data. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time that the stop is send.



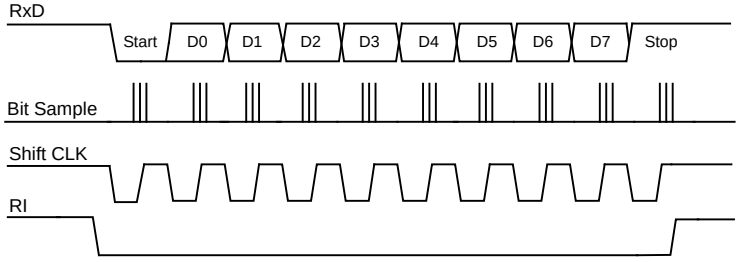
Send Timing of Mode 1

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7^{th}, 8^{th} and 9^{th} counter states of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI are set if the following conditions are met:

1. RI must be 0
2. Either SM2 = 0, or the received stop bit = 1

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

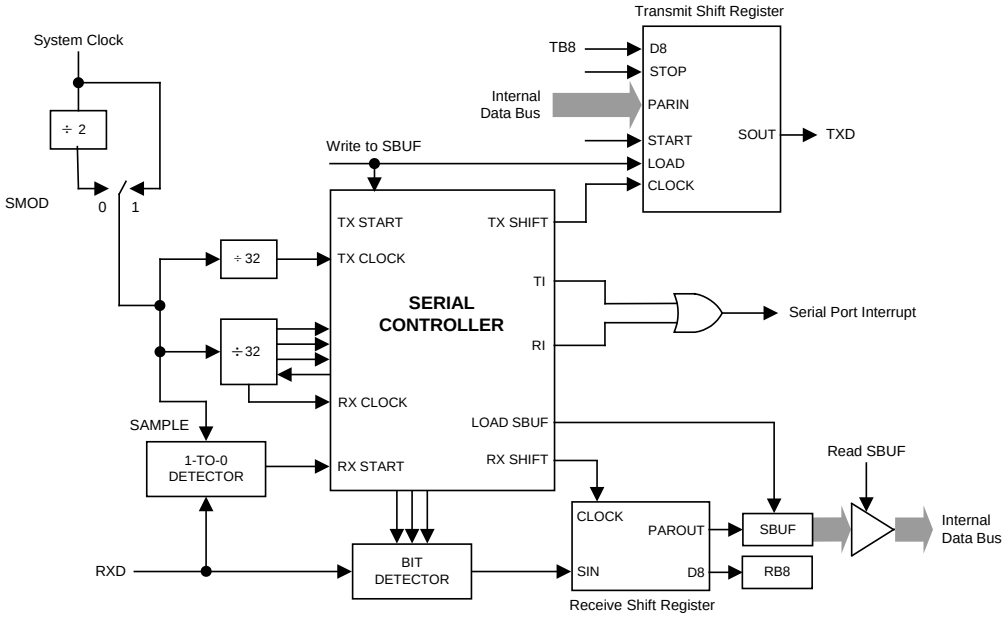
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



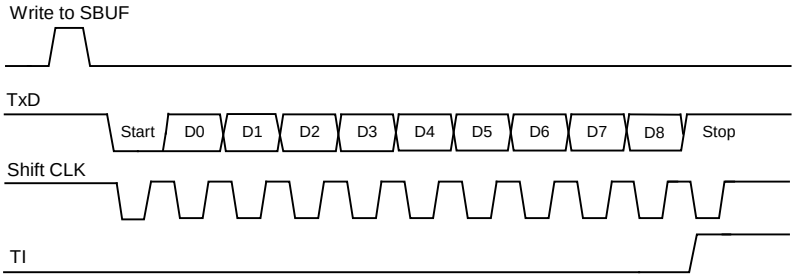
Receive Timing of Mode 1

Mode2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

This mode provides the 11 bits full duplex asynchronous communication. The 11 bits consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition (Refer to Multiprocessor Communication Section for details). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below:



Transmission begins with a “write to SBUF” signal, the “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal). The start bit is firstly put out on TxD pin, then are the 9 bits of data. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time, this will be at the 11th rollover of the divide-by-16 counter after a write to SBUF.



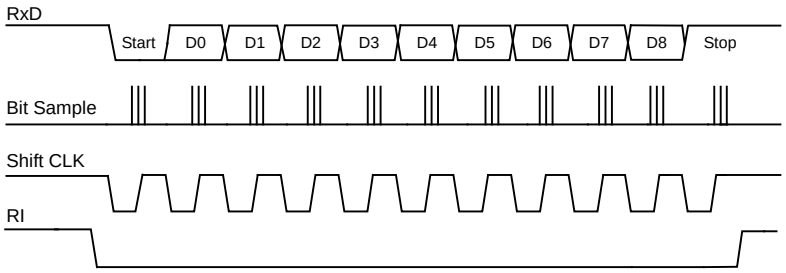
Send Timing of Mode 2

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter. The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7th, 8th and 9th counter state of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit detected after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set if the following conditions are met:

1. RI must be 0
2. Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

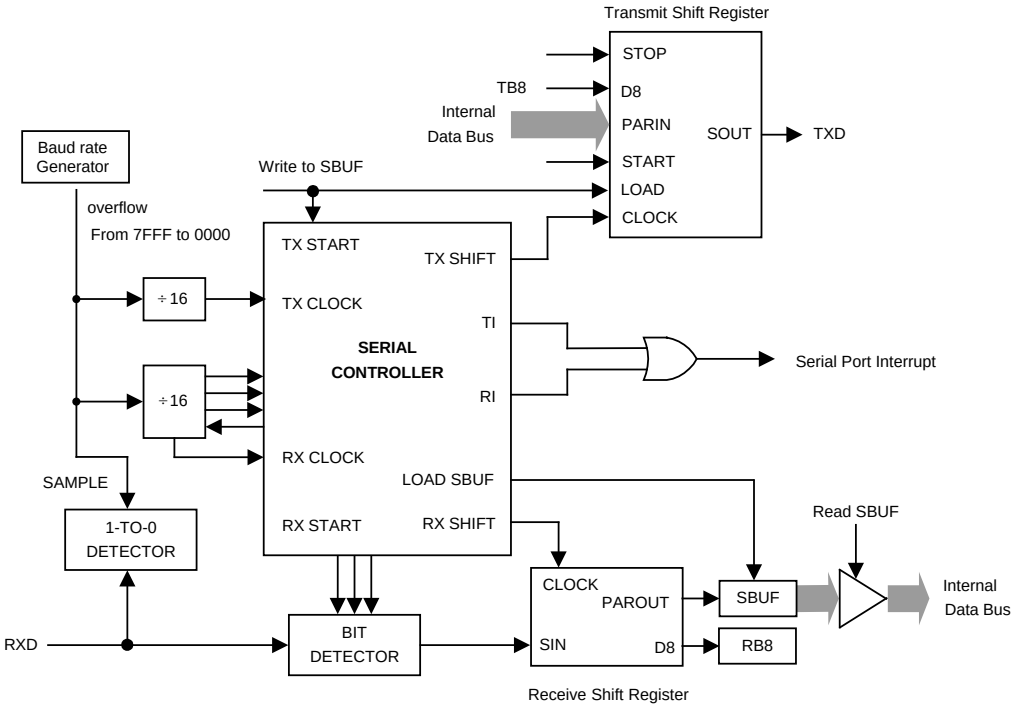
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

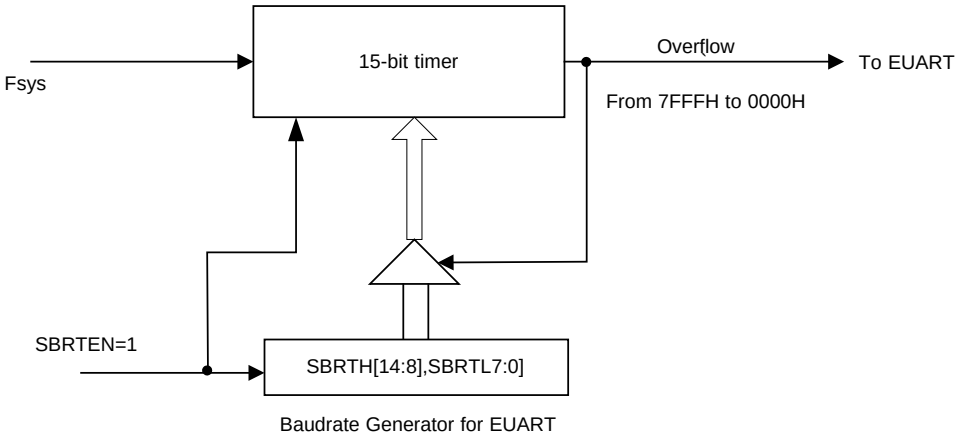
Mode3: 9-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

Mode3 uses transmission protocol of the Mode2 and baud rate generation of the Mode1.



8.5.3 Baud Rate Generate

The baud rate generator is an 15-bit up-counting timer



$$SBRToverflowrate = \frac{Fsys}{32768 - SBRT},\ SBRT = [SBRTH, SBRTL]$$

In Mode0, the baud rate is programmable to either 1/12 or 1/4 of the system frequency. This baud rate is determined by SM2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

In Mode1 & Mode3, the baud rate can be fine adjusted.

The Mode1 & 3 baud rate equations are shown below,

$$BaudRate = \frac{Fsys}{16 \times (32768 - SBRT) + BFINE}$$

For example: Fsys = 8MHz, to get 115200Hz baud rate, computing method of SBRT and SFINE as shown below:

8000000/16/115200 = 4.34

SBRT = 32768 - 4 = 32764

115200 = 8000000/(16 X 4 + BFINE)

BFINE = 5.4 $\approx$ 5

This fine tuning method to calculate the actual baud rate is 115942Hz and the error is 0.64%, but the error is 8.5% In the past computing method.

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, the serial port runs at 1/64 of the clock. When set to 1, the serial port runs at 1/32 of the clock.

$$BaudRate = 2^{SMOD} \times (\frac{f_{SYS}}{64})$$

8.5.4 Multi-Processor Communication

Software Address Recognition

Modes 2 and 3 of the EUART have a special provision for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the EUART interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte.

With SM2 = 1, no other slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed leave their SM2 set and go on with their business, ignoring the incoming data bytes.

Note: *In Mode0, SM2 is used to select baud rate doubling. In Mode1, SM2 can be used to check the validity of the stop bit. If SM2 = 1 in Mode1, the receive interrupt will not be activated unless a valid stop bit is received.*

Automatic (Hardware) Address Recognition

In Mode2 & 3, setting the SM2 bit will configure EUART act as following: when a stop bit is received, EUART will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts on the reception of the following data byte(s).

The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the addressed slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the addressed slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, as they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all transmissions until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. The slave address is an 8-bit value specified in the SADDR register. The SADEN register is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR. Use of the Given Address allows multiple slaves to be recognized while excluding others.

	Slave 1	**Slave 2**
SADDR	10100100	10100111
SADEN (0 mask)	11111010	11111001
Given Address	10100x0x	10100xx1
Broadcast Address (OR)	1111111x	11111111

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as don't cares. In most cases, the Broadcast Address is FFh, this address will be acknowledged by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXXXXXX (all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUART 0 will reply to any address, which it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor by software address recognition mentioned above.

8.5.5 Error Detection

Error detection is available when the SSTAT bit in register PCON is set to logic 1.The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).All the 3 bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Transmit Collision

The Transmit Collision bit (TXCOL bit in register SCON) reads '1' if RI is set 0 and user software writes data to the SBUF register while a transmission is still in progress. If this occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overrun

The Receive Overrun bit (RXOV in register SCON) reads '1' if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happen.

Frame Error

The Frame Error bit (FE in register SCON) reads '1' if an invalid (low) STOP bit is detected.

Note: *Before transmitting, TXD pin must be setted output high.*

8.5.6 Registers

Table 8.20 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**SMOD**	**Baud rate doubler** 0: in Mode2, the baud-rate of EUART is 1/64 of the system clock 1: in Mode2, the baud-rate of EUART is 1/32 of the system clock
6	**SSTAT**	**SCON[7:5] function select bit** 0: SCON[7:5] operates as SM0, SM1, SM2 1: SCON[7:5] operates as FE, RXOV, TXCOL
3-2	**GF[1:0]**	**General purpose flags for software use**
1	**PD**	**Power-Down mode control bit**
0	**IDL**	**Idle mode control bit**

Table 8.21 EUART Control & Status Register

98H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0 /FE	SM1 /RXOV	SM2 /TXCOL	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**SM[0:1]**	**EUART Serial mode control bits, when SSTAT = 0** 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8-bit Asynchronous Mode, variable baud rate 10: mode 2, 9-bit Asynchronous Mode, fixed baud rate 11: mode 3, 9-bit Asynchronous Mode, variable baud rate
7	**FE**	**EUART Frame Error flag, when FE bit is read, SSTAT bit must be set 1** 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware
6	**RXOV**	**EUART Receive Over flag, when RXOV bit is read, SSTAT bit must be set 1** 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware
5	**SM2**	**EUART Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0** 0: In Mode0, baud-rate is 1/12 of system clock In Mode1, disable stop bit validation check, any stop bit will set RI to generate interrupt In Mode2 & 3, any byte will set RI to generate interrupt 1: In Mode0, baud-rate is 1/4 of system clock In Mode1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In Mode2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	**TXCOL**	**EUART Transmit Collision flag, when TXCOL bit is read, SSTAT bit must be set 1** 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware
4	**REN**	**EUART Receiver enable bit** 0: Receive Disable 1: Receive Enable
3	**TB8**	**The 9th bit to be transmitted in Mode2 & 3 of EUART, set or clear by software**
2	**RB8**	**The 9th bit to be received in Mode1, 2 & 3 of EUART** In Mode0, RB8 is not used In Mode1, if receive interrupt occurs, RB8 is the stop bit that was received In Mode2 & 3 it is the 9th bit that was received
1	**TI**	**Transmit interrupt flag of EUART** 0: cleared by software 1: Set by hardware at the end of the 8th bit time in Mode0, or at the beginning of the stop bit in other modes
0	**RI**	**Receive interrupt flag of EUART** 0: cleared by software 1: Set by hardware at the end of the 8th bit time in Mode0, or during the stop bit time in other modes

Table 8.22 EUART Data Buffer Register

99H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SBUF[7:0]**	This SFR accesses two registers; a transmit shift register and a receive latch register A write of SBUF will send the byte to the transmit shift register and then initiate a transmission A read of SBUF returns the contents of the receive latch

Table 8.23 EUART Slave Address & Address Mask Register

9AH-9BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR (9AH)	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN (9BH)	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SADDR[7:0]**	**SFR SADDR defines the EUART's slave address**
7-0	**SADEN[7:0]**	**SFR SADEN is a bit mask to determine which bits of SADDR are checked** 0: Corresponding bit in SADDR is a "don't care" 1: Corresponding bit in SADDR is checked against a received address

Table 8.24 EUART Baudrate generator register

9CH-9DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRTH (9CH)	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL (9DH)	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**SBRTEN**	**EUART Baudrate enable control bit** 0: disable (deault) 1: enable
6-0, 7-0	**SBRT[14:0]**	**EUART Baudrate bits**

Table 8.25 EUART Baudrate generator fine-tune register

B6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SFINE	-	-	-	-	SFINE.3	SFINE.2	SFINE.1	SFINE.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-		-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**SFINE[3:0]**	**EUART Baudrate generator fine-tune register**

8.6 Analog Digital Converter (ADC)

8.6.1 Features

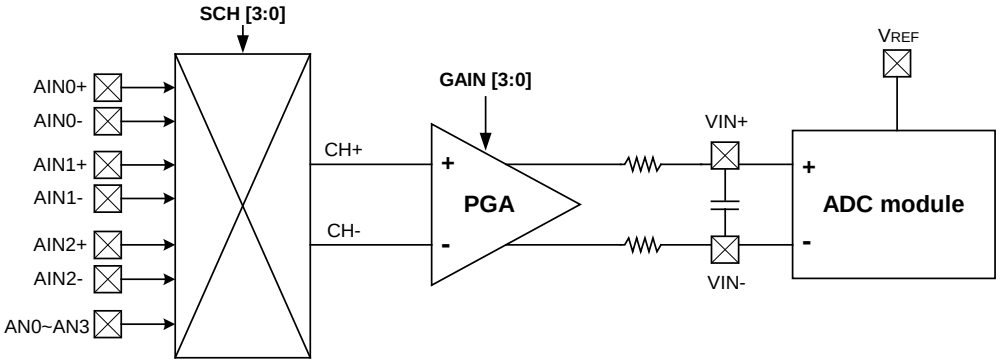
- 20-bit data output
- 16-bit resolution
- Internal or external reference voltage can be selected by user
- 3 differential input/4 Single-ended inputs
- Multipath correction inputs

The SH79F6488/SH79F6489 include a full-differential 20-bit Σ-Δ analog to digital converter. This ADC built-in 2 reference voltage VREF1 and VREF2. User can also select external reference voltage. The analog input will be amplified by the PGA (Programmable Gain Amplifier) before being input to ADC module. There are two kinds of analog input, differential input and calibration input.

When set ADON bit in ADCON register, the conversion is always doing. When one conversion is complete, the data in ADC data register will be updated and ADCIF bit in ADCON register will be set. If ADC interrupt is enabled, the ADC interrupt will generate.

The ADC module can also work in IDLE mode and the ADC interrupt will wake up the IDLE mode. But the module is disabled in Power-Down mode.

8.6.2 ADC Diagram



8.6.3 Registers

Table 8.26 ADC Control Register

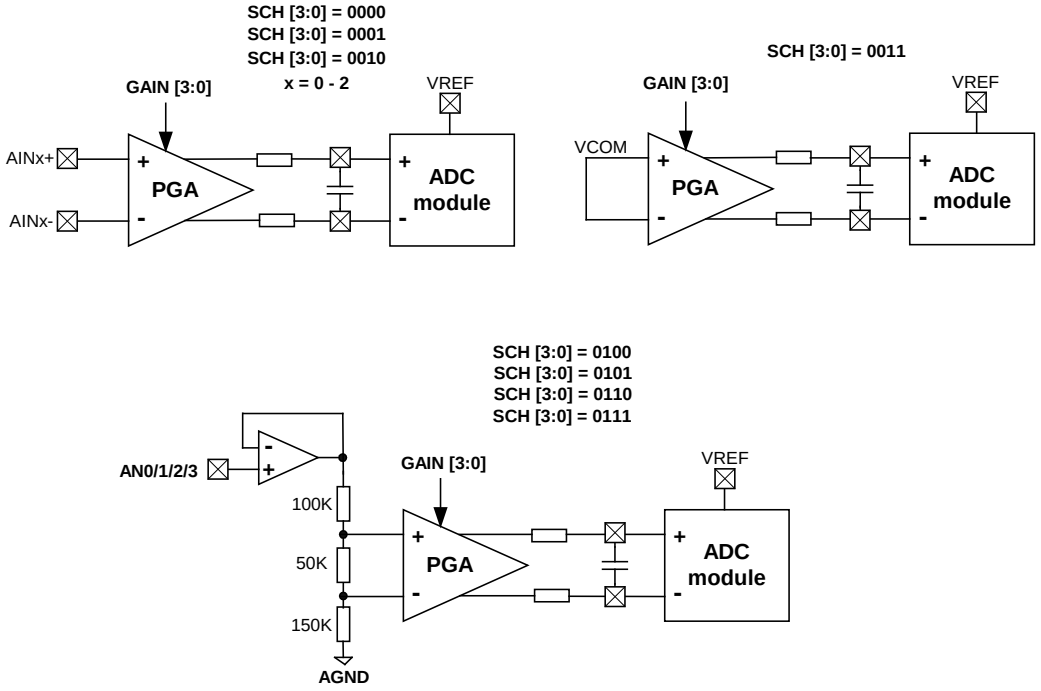
93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	VREFIN	VREFS	SCH3	SCH2	SCH1	SCH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**ADON**	**ADC Control bit** 0: Disable ADC module 1: Enable ADC module, set to start AD convert
6	**ADCIF**	**ADC Interrupt Flag bit** 0: No ADC interrupt generate, must be cleared by software 1: Set by hardware, one conversion complete
5	**VREFIN**	**Internal Reference voltage select bit** 0: Select VREF1, the value is controlled by VREF[1:0], divided by VDDR, same source of VDDR 1: Select VREF2, the voltage is 1.19V,not the same source of VDDR.
4	**VREFS**	**ADC Reference voltage select bit** 0: Select internal reference voltage, VREFOS bit must write “1” 1: Select external reference voltage in VREF pin, VREFOS bit must write “1”
3-0	**SCH[3:0]**	**ADC Channel Select bits** 0000: ADC differential input AIN0+, AIN0- 0001: ADC differential input AIN1+, AIN1- 0010: ADC differential input AIN2+, AIN2- 0011: PGA internal short, connect with VCOM 0100: ADC input AN0 0101: ADC input AN1 0110: ADC input AN2 0111: ADC input AN3 1000: reserved 1001: PGA Positive connect with V_{REF}, PGA Negative connect with AGND 1010: PGA Positive connect with AGND, PGA Negative connect with V_{REF} Others: ADC differential input AIN0+, AIN0-

Notes:

(1) Clearing ADON bit during converting time will stop current AD conversion.
(2) AN0/1/2/3 inputs are Isolated by OP, connect to PGA through divider resistors, keep input voltage < VDDR-0.3V.
(3) V_{REF} pin needs to be connect 104 capacitance between AGND.
*(4) AN0/1/2/3 Single-ended input. PGA gain can't be more than eight times.make sure PGA input voltage *gain < V_{REF}.*

ADC Channel Diagram:



Note:

(1) If SCH[3:0] = 0100, 0101, 0110 or0111 it used to measure voltage value of V_{DD}. AN0/1/2/3 inputs are Isolated by OP, connect to PGA through divider resistors, ADC will sample 1/6 voltage of the sigle-ended inputs. keep input voltage < VDDR-0.3V.

(2) VCOM = 0.5VDDR

Table 8.27 ADC Clock Register

94H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	TADC7	TADC6	TADC5	TADC4	TADC3	TADC2	TADC1	TADC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TADC[7:0]**	**ADC Clock Register** ADC Clock = f_{SYS}/2/(256-TADC[7:0])

Note:

(1) The f_{SYS} is system Clock, it will affect ADC clock when system clock prescaler is changed;
(2) ADT register sets ADC working clock, 100kHz is recommended as ADC clock;
(3) The relation between ADC clock and ADT: ADC clock = f_{SYS}/2/(256-TADC[7:0]);
(4) ADC conversion rate: ADC clock/4000;
(5) AC power 50Hz noise will be filtered out when ADC conversion rate is 25Hz;
(6) AC power 60Hz noise will be filtered out when ADC conversion rate is 20Hz;
(7) Both AC power 50Hz and 60Hz noise will be filtered out when ADC conversion rate is 10Hz;
(8) ADC precision will affect when conversion rate more than 50Hz.(Refer to electrical characteristics section for details).

Table 8.28 ADC Channel Configuration Register

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH	VREF1	VREF0	VREFOS	CH2N	CH2P	CH1N	CH1P	CH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**VREF[1:0]**	**Internal Reference Voltage Select bits** 00: V_{REF} = 0.15 X VDDR 01: V_{REF} = 0.22 X VDDR 10: V_{REF} = 0.30 X VDDR 11: V_{REF} = 0.40 X VDDR This bit is available when VREFIN is 0
5	**VREFOS**	**V_{REF} pin Configuration bit** 0: P1.0 as I/O Ports 1: P1.0 as ADC reference voltage input pin
4	**CH2N**	**AIN2- Channel Configuration bit** 0: P1.6 as I/O Ports 1: P1.6 as ADC input (AIN2- or AN3)
3	**CH2P**	**AIN2+ Channel Configuration bit** 0: P1.5 as I/O Ports 1: P1.5 as ADC input (AIN2+ or AN2)
2	**CH1N**	**AIN1- Channel Configuration bit** 0: P1.4 as I/O Ports 1: P1.4 as ADC analog input (AIN1-, AIN1)
1	**CH1P**	**AIN1+ Channel Configuration bit** 0: P1.3 as I/O Ports 1: P1.3 as ADC analog input (AIN1+, AIN0)
0	**CH0**	**AIN0 Channel Configuration bit** 0: P1.1-P1.2 as I/O Ports 1: P1.1-P1.2 as ADC analog input (AIN0+, AIN0-)

Table 8.29 AD Converter Data Register

91H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDL	-	-	-	-	A3	A2	A1	A0
R/W	-	-	-	-	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0
96H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDM	A11	A10	A9	A8	A7	A6	A5	A4
R/W	R	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0
97H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDH	A19	A18	A17	A16	A15	A14	A13	A12
R/W	R	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
19-0	**A19-A0**	**20-bit ADC data register**

Note:

(1) ADC conversion result is stored in A19-A0. The A19 is the sign bit of ADC data. Refer to the following formula to calculate ADC conversion data value:
ADC data = ((VIN+) - (VIN-))/V_{REF} X 524288
If ADCDF = 0, ADC output data is bipolar mode (complement)
When (VIN+) > (VIN-) is positive, A19 is 0 which means the ADC data is positive. The ADC value is A19-A0;
When (VIN+) < (VIN-) is negative, A19 is 1 which means the ADC data is negative. The ADC value is 100000H minus A19-A0.
If ADCDF = 1, ADC output data is unipolar mode
When (VIN+) = (VIN-) , ADC data = 80000H;
When (VIN+) > (VIN-) , ADC data > 80000H;
When (VIN+) < (VIN-) , ADC data < 80000H;

(2) Due to the zero offset voltage ADC or PGA, actual output will has certain error code value.

(3) When the ADC conversion is complete, the data register will not be updated.

(4) To obtain maximum range of ADC output, the maximum absolute of ADC input voltage of ((VIN+) - (VIN-)) should be close to reference voltage value, bit can't over the reference voltage value.

Table 8.30 ADC data output mode register

92H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCDS	-	-	-	-	-	ADCRATE	VINOS	ADCDF
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	0	1	0

Bit Number	Bit Mnemonic	Description
2	**ADCRATE**	**ADC data output rate mode** 0:normal mode 1:standby test mode, not recommended
1	**VINOS**	**VIN Configuration bit** 0: P1.7 and P2.0 as I/O 1: P1.7 and P2.0 as VIN
0	**ADCDF**	**ADC output data Storage format** 0: ADC output data is bipolar mode 1: ADC output data is unipolar mode

ADC Conversion Data Value refer to following:

ADCDF = 0, ADC output data is bipolar mode

ADC input	VREF	VREF/2	+1LSB	0	-1LSB	-VREF/2	-VREF
ADC Data (hexadecimal)	7FFFFH	40000H	00001H	00000H	FFFFFH	C0000H	80000H
ADC Data (Decimal)	524287	262144	1	0	-1	-262144	-524288

ADCDF = 1, ADC output data is unipolar mode

ADC input	VREF	VREF/2	+1LSB	0	-1LSB	-VREF/2	-VREF
ADC Data (hexadecimal)	FFFFFH	C0000H	80001H	80000H	7FFFFH	40000H	0
ADC Data (Decimal)	1048575	786432	524289	524288	524287	262144	0

Start ADC Conversion Step:

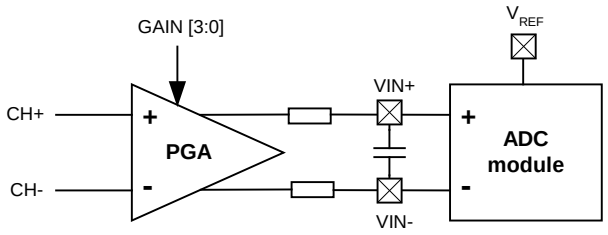
(1) Select ADC channel and reference voltage.
(2) Enable ADC function start ADC conversion.
(3) ADCIF will be set when ADC conversion is finished, If ADC interrupt is enabled, an interrupt will generate.
(4) Obtain ADC conversion data by ADDH/ADDM/ADDL.
(5) Repeat step (3)-(4) to Obtain next ADC conversion data.

8.7 Programmable Gain Amplifier (PGA)

8.7.1 Features

- Low noise programmable gain amplifier
- 8-level Programmable gain range
- Chopper

The SH79F6488/SH79F6489 provides a low noise programmable gain amplifier. This PGA provides amplification setting of 1, 2, 4, 8, 16, 32, 64 and 128. A chopper is included, which can be used for eliminate PGA offset. Chopper work clock can select 1kHz, 2kHz, 3kHz, or 4kHz. Work clock of 1kHz is recommended.



8.7.2 Registers

Table 8.31 PGA Mode Control Register

A3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PGAM	GAIN3	GAIN2	GAIN1	GAIN0	VINON	CHOP	CHOPC1	CHOPC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-4	**GAIN[3:0]**	**PGA Gain select bits** 0000: gain = 1 0001: gain = 2 0010: gain = 4 0110: gain = 8 1000: gain = 16 1001: gain = 32 1010: gain = 64 1110: gain = 128 others: gain = 1
3	**VINON**	**VIN analog input enable bit** 0: Disable analog input, analog input from AINx± or ANx 1: Enable analog input, analog input from VIN±, AINx± or ANx used as I/O
2	**CHOP**	**Chopper Enable bit** 0: Disable chopper function 1: Enable chopper function
1-0	**CHOPC[1:0]**	**Chopper Work Clock Select bit** 00: 1kHz 01: 2kHz 10: 3kHz 11: 4kHz Work clock of 1kHz is recommended

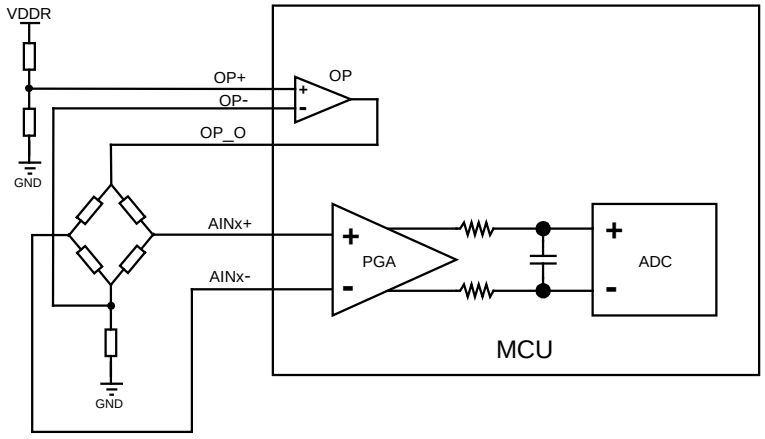
8.8 High-performance Operational Amplifier (OP)

8.8.1 Features

- Single power supply
- Internally frequency compensated

The SH79F6488/SH79F6489 provides 1 high-performance operational amplifiers. The Operational amplifier can be applied to constant current source circuit, constant voltage source circuit, small signal amplifier circuit, etc. Such as driving resistance type pressure sensor.

Application diagram.



8.8.2 Registers

Table 8.32 OP Control Register

A2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPCON	-	-	-	-	-	-	OPOS	OPEN
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	1	0

Bit Number	Bit Mnemonic	Description
1	**OPOS**	**OP Configuration bit** 0: P2.1-P2.3 as I/O 1: P2.1-P2.3 as OP
0	**OPEN**	**OP enable Control bit** 0: disable OP function 1: enable OP function

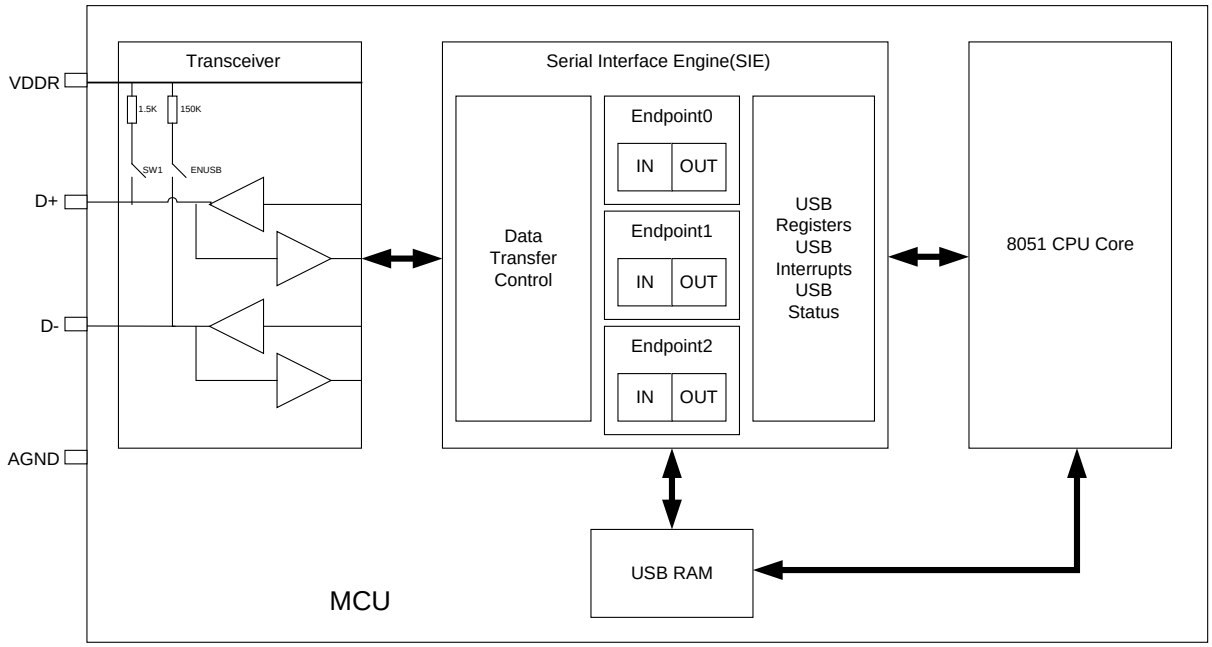
8.9 SH79F6489: Universal Serial Bus (USB)

8.9.1 Features

Compatible with USB2.0 Full speed (12Mbps)

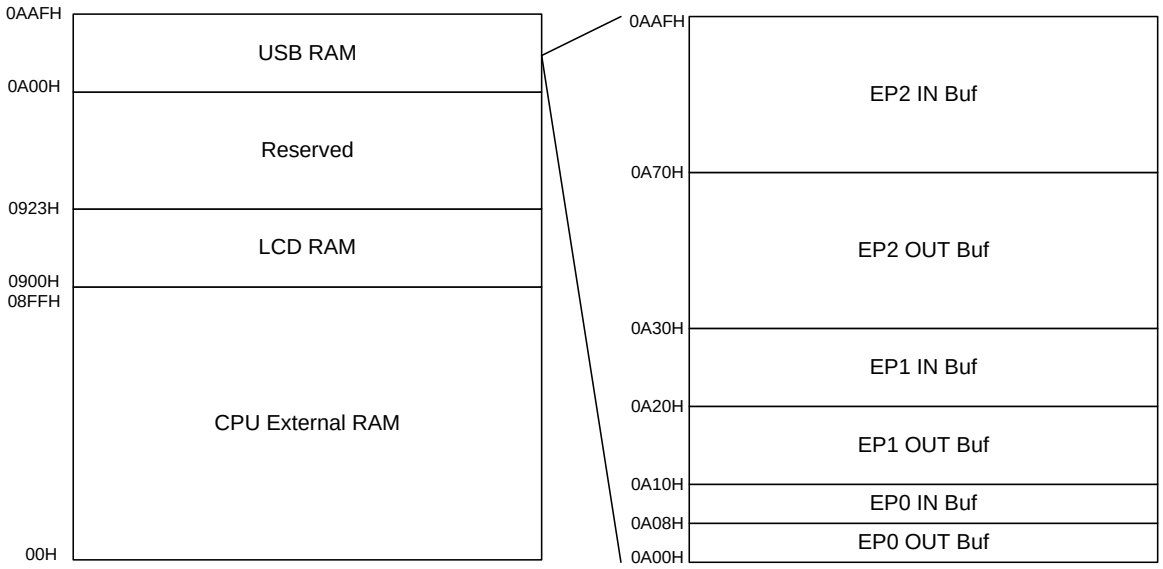
- Support control, interrupt and buck data transfer
- Support three endpoints (EP0, EP1, EP2)
- On-chip USB transceiver with an internal regulator
- Support software reconnect and automatic detect USB host connection

SH79F6489 provided an internal USB Serial Interface Engine(SIE) which supports any high speed communication between USB Host and MCU. The internal regulator can provide power supply for the internal transceiver in 5V application.



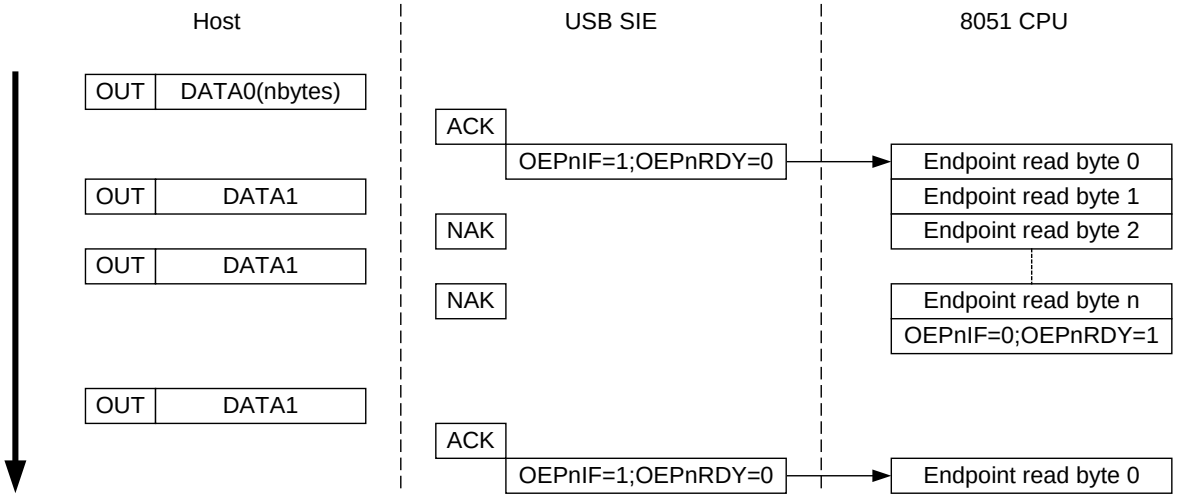
The Universal Serial Bus (USB) support three endpoints: EP0, EP1, EP2. The EP0 is the USB control endpoint, which is used for USB control data transfer. The EP1 and EP2 can support IN/OUT transaction of the bulk/interrupt data transfer. The following table shows the maximum package size of each endpoint.

Endpoint	Type	Maximum Package Size
EP0	Control	IN0: 8 bytes
		OUT0: 8 bytes
EP1	Bulk/Interrupt	IN1: 16 bytes
		OUT1: 16 bytes
EP2	Bulk/Interrupt	IN2: 64 bytes
		OUT2: 64 bytes

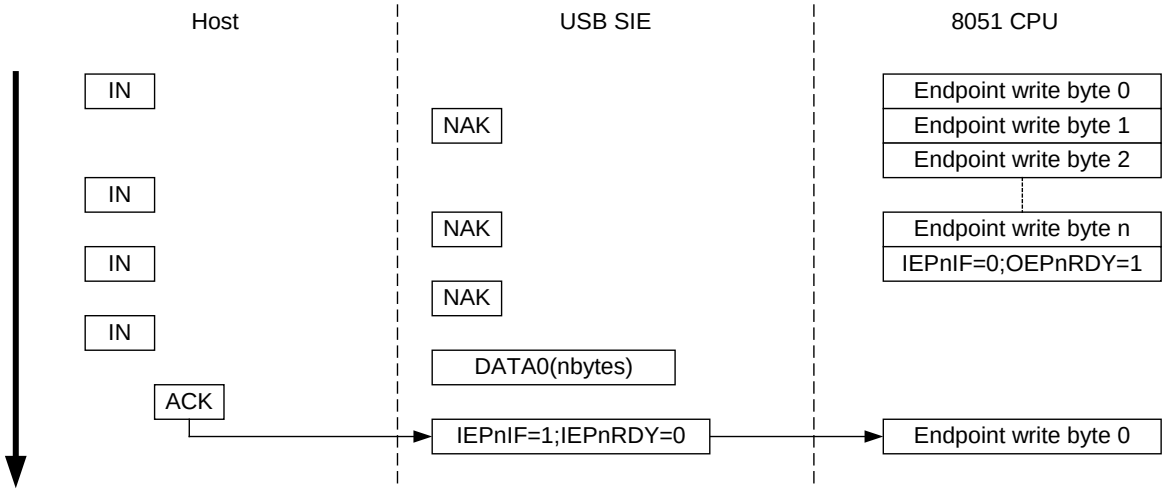


USB RAM Distributing

8.9.2 USB Flow



USB Bulk/Interrupt Transfer (OUT transaction) Flow



USB Bulk/Interrupt Transfer (IN transaction) Flow

8.9.3 Suspend/Resume Control

When the USB controller detected suspend signal, the SUSPIF will be setted by hardware, the USB interrupt will be generated, if the USB interrupt has been enable. The device must be setted to suspend state by software in 7ms (Set GOSUSP bit in USBCON register). To reduce power consumption maximumly, the software may close high frequency clock by following the steps below.

When code option OP_OSC = 1010 or 1101:

(1) Set GOSUSP bit in USBCON register
(2) Clear FS bit in CLKCON register (32.768kHz oscillator is selected as OSCSCLK)
(3) Clear PLLFS bit in PLLCON register
(4) Clear PLLON bit in PLLCON register (Close PLL)
(5) Clear OSC2ON bit in CLKCON register (Close OSC2)
(6) Set EUSB bit in IEN1 register. Set EA bit in IEN0 register. Set PUPIE, RESMIE, PBRSTIE bits in USBIE1 register
(7) Make CPU entering Idle mode to reduce power consumption

When code option OP_OSC = 0000:

(1) Set GOSUSP bit in USBCON register
(2) Clear FS bit in CLKCON register (Internal 12MHz RC oscillator is selected as OSCSCLK)
(3) Clear PLLFS bit in PLLCON register
(4) Clear PLLON bit in PLLCON register (Close PLL)
(5) Clear OSC2ON bit in CLKCON register (Close OSC2)
(6) Set EUSB bit in IEN1 register. Set EA bit in IEN0 register. Set PUPIE, RESMIE, PBRSTIE bits in USBIE1 register
(7) Make CPU entering Power-down mode to reduce power consumption

When the USB controller detected the following three USB states below in suspend state, the interrupt will be generated, if the related interrupt has been enable.

(1) Detected Resume Command
(2) Detected BUS RESET Command
(3) Detected Plug/Unplug

If CPU is in Power-down/Idle mode, theCPU will be waked, and entering the related interrupt. The software may open high frequency clock refer to 7.5 System Clock and Oscillator section in sequence. And then clear GOSUSP.

8.9.4 Registers

There are three reset sources for USB registers control

(1) POR/WDT/LVR/PIN etc traditional reset sources.

(2) Bus Reset. It is the USB bus reset. Some registers will be reset by bus reset.

(3) USB Software Reset. It is generated by setting SWRST bit in USBCON register. Some USB module registers will be reset, and the USB status machine resume to initial states.

Table 8.33 USB Control Register

99H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBCON	ENUSB	SW1CON	SWRST	DPSTA	DMSTA	-	-	GOSUSP
R/W	R/W	R/W	R/W	R	R	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	-	-	0
Bus Reset Value (USB RESET)	U	U	U	U	U	-	-	U
USB Software Reset Value	U	U	U	U	U	-	-	0

Bit No.	Bit Mnemonic	Description
7	**ENUSB**	**USB Module Enable bit** 0: Disable USB module 1: Enable USB module
6	**SW1CON**	**SW1 On-Off Control bit** 0: Open 1.5K Pull-high resistor on the D+ line 1: Connect 1.5K Pull-high resistor on the D+ line User's program may simulate the USB plug/unplug process by SW1 on-off bit. If disable the USB module, this bit will be auto-cleared.
5	**SWRST**	**USB Software Reset** 0: Exit USB Software Reset 1: Writing '1' will generate USB Software Reset. Some USB module registers will be reset, and the USB status machine resume to initial states
4	**DPSTA**	**D+ State** 0：D+ Low 1：D+ High
3	**DMSTA**	**D- State** 0：D- Low 1：D- High
0	**GOSUSP**	**USB Suspend State Selection bit** 0: Exit Suspend State 1: Enter Suspend State When user's program need to set the device into suspend state, this bit should be setted. When the USB port received Resume Command or Bus Reset Command, this bit should be cleared to exit suspend state.

Table 8.34 USB Interrupt Vector Register 1

E8H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBIF1	PUPIF	OVERIF	OW	SETUPIF	SOFIF	RESMIF	SUSPIF	USBRSTIF
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0
Bus Reset Value (USB RESET)	U	U	U	U	U	U	U	U
USB Software Reset Value	U	0	0	0	U	0	0	0

Bit No.	Bit Mnemonic	Description
7	**PUPIF**	**Plug/Unplug Interrupt Flag bit** 0: No Plug/Unplug interrupt generating, cleared by software 1: Set by hardware to indicate the USB device plugged or unplugged in the host
6	**OVERIF**	**Setup Transaction Overwrite Interrupt Flag bit** 0: No setup transaction overwrite interrupt flag generating, cleared by software. Befor this bit cleared by software, cleared SETUPIF bit first 1: Set by hardware to indicate setup transaction is received when output buffer of EP0 is not empty and data is written into the output buffer of EP0 and input/output data package is received again
5	**OW**	**Setup Transaction Overwrite State Flag bit** 0: No setup transaction overwrite generating 1: Set by hardware to indicate setup transaction is received again when output buffer of EP0 is not empty (OEP0RDY=0, When setup transaction is received, regardlessly error or returned an ACK lastly) and data is written into the output buffer of EP0 USB software reset or cleared by software. OVERIF may clear this bit.
4	**SETUPIF**	**Setup Transaction Interrupt Flag bit** 0: No setup transaction received 1: Setup transaction is received, returns an ACK, and asserts setup transaction interrupt When data is read out from the output buffer of EP0, this bit will be cleared
3	**SOFIF**	**Start-Of-Frame(SOF) Transaction Interrupt Flag bit** 0: No SOF transaction received, cleared by software 1: SOF transaction received, and asserts SOF transaction interrupt
2	**RESMIF**	**Resume Command Interrupt Flag bit** 0: No resume command received, cleared by software 1: Resume command received, and asserts resume command interrupt
1	**SUSPIF**	**Suspend Command Interrupt Flag bit** 0: No suspend command received, cleared by software 1: Suspend command received, and asserts suspend command interrupt When suspend command is received, the device must be setted to suspend state by software in 7ms (Set GOSUSP bit in USBCON register), if the device obtain current from USB bus not more than suspend current (Refer to USB SPEC for details).
0	**USBRSTIF**	**Bus Reset Command Interrupt Flag bit** 0: No bus reset command received, cleared by software 1: Bus reset command received, and asserts bus reset command interrupt

Table 8.35 USB Interrupt Vector Register 2

F8H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBIF2	-	OEP2IF	OEP1IF	OEP0IF	-	IEP2IF	IEP1IF	IEP0IF
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	-	0	0	0
Bus Reset Value (USB RESET)	-	U	U	U	-	U	U	U
USB Software Reset Value	-	0	0	0	-	0	0	0

Bit No.	Bit Mnemonic	Description
6	**OEP2IF**	**Endpoint 2 OUT Interrupt Flag bit** 0: No Endpoint 2 OUT transaction occurred, cleared by software 1: Set by hardware to indicate Endpoint 2 OUT transaction occurred
5	**OEP1IF**	**Endpoint 1 OUT Interrupt Flag bit** 0: No Endpoint 1 OUT transaction occurred, cleared by software 1: Set by hardware to indicate Endpoint 1 OUT transaction occurred
4	**OEP0IF**	**Endpoint 0 OUT Interrupt Flag bit** 0: No Endpoint 0 OUT transaction occurred, cleared by software 1: Set by hardware to indicate Endpoint 0 OUT transaction occurred
2	**IEP2IF**	**Endpoint 2 IN Interrupt Flag bit** 0: No Endpoint 2 IN transaction occurred, cleared by software 1: Set by hardware to indicate Endpoint 2 IN transaction occurred
1	**IEP1IF**	**Endpoint 1 IN Interrupt Flag bit** 0: No Endpoint 1 IN transaction occurred, cleared by software 1: Set by hardware to indicate Endpoint 1 IN transaction occurred
0	**IEP0IF**	**Endpoint 0 IN Interrupt Flag bit** 0: No Endpoint 0 IN transaction occurred, cleared by software 1: Set by hardware to indicate Endpoint 0 IN transaction occurred

Table 8.36 USB Interrupt Enable Register 1

9AH (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBIE1	PUPIE	OVERIE	-	SETUPIE	SOFIE	RESMIE	SUSPIE	PBRSTIE
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	0	0	0	0	0
Bus Reset Value (USB RESET)	U	U	-	U	U	U	U	U
USB Software Reset Value	U	0	-	0	U	0	0	0

Bit No.	Bit Mnemonic	Description
7	**PUPIE**	**Plug/Unplug Interrupt Enable bit** 0: Disable Plug/Unplug interrupt 1: Enable Plug/Unplug interrupt
6	**OVERIE**	**Setup Transaction Overwrite Interrupt Enable bit** 0: Disable setup transaction overwrite interrupt 1: Enable setup transaction overwrite interrupt
4	**SETUPIE**	**Setup Transaction Interrupt Enable bit** 0: Disable setup transaction interrupt 1: Enable setup transaction interrupt
3	**SOFIE**	**SOF Transaction Interrupt Enable bit** 0: Disable SOF transaction interrupt 1: Enable SOF transaction interrupt
2	**RESMIE**	**Resume Command Interrupt Enable bit** 0: Disable resume command interrupt 1: Enable resume command interrupt
1	**SUSPIE**	**Suspend Command Interrupt Enable bit** 0: Disable suspend command interrupt 1: Enable suspend command interrupt
0	**PBRSTIE**	**Bus Reset Command Interrupt Enable bit** 0: Disable bus reset command interrupt 1: Enable bus reset command interrupt

Table 8.37 USB Interrupt Enable Register 2

9BH (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBIE2	-	OEP2IE	OEP1IE	OEP0IE	-	IEP2IE	IEP1IE	IEP0IE
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	-	0	0	0
Bus Reset Value (USB RESET)	-	U	U	U	-	U	U	U
USB Software Reset Value	-	0	0	0	-	0	0	0

Bit No.	Bit Mnemonic	Description
6	**OEP2IE**	**Endpoint 2 OUT Interrupt Enable bit** 0: Disable Endpoint 2 OUT transaction interrupt 1: Enable Endpoint 2 OUT transaction interrupt
5	**OEP1IE**	**Endpoint 1 OUT Interrupt Enable bit** 0: Disable Endpoint 1 OUT transaction interrupt 1: Enable Endpoint 1 OUT transaction interrupt
4	**OEP0IE**	**Endpoint 0 OUT Interrupt Enable bit** 0: Disable Endpoint 0 OUT transaction interrupt 1: Enable Endpoint 0 OUT transaction interrupt
2	**IEP2IE**	**Endpoint 2 IN Interrupt Enable bit** 0: Disable Endpoint 2 IN transaction interrupt 1: Enable Endpoint 2 IN transaction interrupt
1	**IEP1IE**	**Endpoint 1 IN Interrupt Enable bit** 0: Disable Endpoint 1 IN transaction interrupt 1: Enable Endpoint 1 IN transaction interrupt
0	**IEP0IE**	**Endpoint 0 IN Interrupt Enable bit** 0: Disable Endpoint 0 IN transaction interrupt 1: Enable Endpoint 0 IN transaction interrupt

Table 8.38 USB Device Address Register

9CH (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBADDR	-	USBADDR6	USBADDR5	USBADDR4	USBADDR3	USBADDR2	USBADDR1	USBADDR0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0
Bus Reset Value (USB RESET)	-	0	0	0	0	0	0	0
USB Software Reset Value	-	0	0	0	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	**USBADDR**	USB communication device address

Table 8.39 Endpoint 0 Control Register

98H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EP0CON	IEP0DTG	OEP0DTG	-	-	IEP0STL	IEP0RDY	OEP0STL	OEP0RDY
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0
Bus Reset Value (USB RESET)	0	0	-	-	0	U	0	U
USB Software Reset Value	0	0	-	-	0	0	0	0

Bit No.	Bit Mnemonic	Description
7	**IEP0DTG**	**Endpoint 0 IN Data Toggle bit** 0: Reading out '0' indicates that the next data toggle bit is Data1, writing in '0' indicates that the next data toggle bit will be setted as Data1 1: Reading out '1' indicates that the next data toggle bit is Data0, writing in '1' indicates that the next data toggle bit will be setted as Data0
6	**OEP0DTG**	**Endpoint 0 OUT Data Toggle bit** 0: Reading out '0' indicates that the next data toggle bit is Data1, writing in '0' indicates that the next data toggle bit will be setted as Data1 1: Reading out '1' indicates that the next data toggle bit is Data0, writing in '1' indicates that the next data toggle bit will be setted as Data0
3	**IEP0STL**	**Endpoint 0 IN STALL Enable bit** 0: Disable Endpoint 0 IN STALL 1: Enable Endpoint 0 IN STALL, When the host sends IN transaction to Endpoint 0, returns a STALL When setup transaction is received, IEP0STL is auto-cleared
2	**IEP0RDY**	**Endpoint 0 IN State bit** 0: Endpoint 0 IN is not ready, When the host sends IN transaction to Endpoint 0, returns a NAK 1: Endpoint 0 IN is ready When the host sends IN transaction to Endpoint 0, if this bit is '1', the USB transceiver sends data in Endpoint 0 buffer, and after receiving an ACK from the host, this bit is cleared, generate Endpoint 0 IN interrupt. Writing the data (need to be sent to the host) into Endpoint 0 buffer again by software, and setting this bit indicates the next IN transaction can be received. Software write 0 has no effect.
1	**OEP0STL**	**Endpoint 0 OUT STALL Enable bit** 0: Disable Endpoint 0 OUT STALL 1: Enable Endpoint 0 OUT STALL, when the host sends OUT transaction to Endpoint 0, returns a STALL When setup transaction is received, OEP0STL is auto-cleared
0	**OEP0RDY**	**Endpoint 0 OUT State bit** 0: Endpoint 0 OUT is not ready, When the host sends OUT transaction to Endpoint 0, returns a NAK 1: Endpoint 0 OUT is ready When the host sends OUT transaction to Endpoint 0, if this bit is '1', the USB transceiver writes data into Endpoint 0 buffer, and after returning an ACK to the host, this bit is cleared, generate Endpoint 0 OUT interrupt. After reading out the data in Endpoint 0 buffer by software, setting this bit indicates the next OUT transaction can be received. Software write 0 has no effect.

Table 8.40 Endpoint 1 Control Register

C0H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EP1CON	IEP1DTG	OEP1DTG	-	-	IEP1STL	IEP1RDY	OEP1STL	OEP1RDY
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0
Bus Reset Value (USB RESET)	0	0	-	-	0	U	0	U
USB Software Reset Value	0	0	-	-	0	0	0	0

Bit No.	Bit Mnemonic	Description
7	**IEP1DTG**	**Endpoint 1 IN Data Toggle bit** 0: Reading out '0' indicates that the next data toggle bit is Data1, writing in '0' indicates that the next data toggle bit will be setted as Data1 1: Reading out '1' indicates that the next data toggle bit is Data0, writing in '1' indicates that the next data toggle bit will be setted as Data0
6	**OEP1DTG**	**Endpoint 1 OUT Data Toggle bit** 0: Reading out '0' indicates that the next data toggle bit is Data1, writing in '0' indicates that the next data toggle bit will be setted as Data1 1: Reading out '1' indicates that the next data toggle bit is Data0, writing in '1' indicates that the next data toggle bit will be setted as Data0
3	**IEP1STL**	**Endpoint 1 IN STALL Enable bit** 0: Disable Endpoint 1 IN STALL 1: Enable Endpoint 1 IN STALL, When the host sends IN transaction to Endpoint 1, returns a STALL
2	**IEP1RDY**	**Endpoint 1 IN State bit** 0: Endpoint 1 IN is not ready, When the host sends IN transaction to Endpoint 1, returns a NAK 1: Endpoint 1 IN is ready When the host sends IN transaction to Endpoint 1, if this bit is '1', the USB transceiver sends data in Endpoint 1 buffer, and after receiving an ACK from the host, this bit is cleared, generate Endpoint 1 IN interrupt. Writing the data(need to be sent to the host) into Endpoint 1 buffer again by software, and setting this bit indicates the next IN transaction can be received. Software write 0 has no effect.
1	**OEP1STL**	**Endpoint 1 OUT STALL Enable bit** 0: Disable Endpoint 1 OUT STALL 1: Enable Endpoint 1 OUT STALL, When the host sends OUT transaction to Endpoint 1, returns a STALL
0	**OEP1RDY**	**Endpoint 1 OUT State bit** 0: Endpoint 1 OUT is not ready, When the host sends OUT transaction to Endpoint 1, returns a NAK 1: Endpoint 1 OUT is ready When the host sends OUT transaction to Endpoint 1, if this bit is '1', the USB transceiver writes data into Endpoint 1 buffer, and after returning an ACK to the host, this bit is cleared, generate Endpoint 1 OUT interrupt. After reading out the data in Endpoint 1 buffer by software, setting this bit indicates the next OUT transaction can be received. Software write 0 has no effect.

Table 8.41 Endpoint 2 Control Register

D8H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EP2CON	IEP2DTG	OEP2DTG	-	-	IEP2STL	IEP2RDY	OEP2STL	OEP2RDY
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0
Bus Reset Value (USB RESET)	0	0	-	-	0	U	0	U
USB Software Reset Value	0	0	-	-	0	0	0	0

Bit No.	Bit Mnemonic	Description
7	**IEP2DTG**	**Endpoint 2 IN Data Toggle bit** 0: Reading out '0' indicates that the next data toggle bit is Data1, writing in '0' indicates that the next data toggle bit will be setted as Data1 1: Reading out '1' indicates that the next data toggle bit is Data0, writing in '1' indicates that the next data toggle bit will be setted as Data0
6	**OEP2DTG**	**Endpoint 2 OUT Data Toggle bit** 0: Reading out '0' indicates that the next data toggle bit is Data1, writing in '0' indicates that the next data toggle bit will be setted as Data1 1: Reading out '1' indicates that the next data toggle bit is Data0, writing in '1' indicates that the next data toggle bit will be setted as Data0
3	**IEP2STL**	**Endpoint 2 IN STALL Enable bit** 0: Disable Endpoint 2 IN STALL 1: Enable Endpoint 2 IN STALL, When the host sends IN transaction to Endpoint 2, returns a STALL
2	**IEP2RDY**	**Endpoint 2 IN State bit** 0: Endpoint 2 IN is not ready, When the host sends IN transaction to Endpoint 2, returns a NAK 1: Endpoint 2 IN is ready When the host sends IN transaction to Endpoint 2, if this bit is '1', the USB transceiver sends data in Endpoint 2 buffer, and after receiving an ACK from the host, this bit is cleared, generate Endpoint 2 IN interrupt. Writing the data(need to be sent to the host) into Endpoint 2 buffer again by software, and setting this bit indicates the next IN transaction can be received. Software write 0 has no effect.
1	**OEP2STL**	**Endpoint 2 OUT STALL Enable bit** 0: Disable Endpoint 2 OUT STALL 1: Enable Endpoint 2 OUT STALL, When the host sends OUT transaction to Endpoint 2, returns a STALL
0	**OEP2RDY**	**Endpoint 2 OUT State bit** 0: Endpoint 2 OUT is not ready, When the host sends OUT transaction to Endpoint 2, returns a NAK 1: Endpoint 2 OUT is ready When the host sends OUT transaction to Endpoint 2, if this bit is '1', the USB transceiver writes data into Endpoint 2 buffer, and after returning an ACK to the host, this bit is cleared, generate Endpoint 2 OUT interrupt. After reading out the data in Endpoint 2 buffer by software, setting this bit indicates the next OUT transaction can be received. Software write 0 has no effect.

Table 8.42 Endpoint 0 IN Data Buffer Length Register

9DH (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEP0CNT	-	-	-	-	IEP0CNT3	IEP0CNT2	IEP0CNT1	IEP0CNT0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0
Bus Reset Value (USB RESET)	-	-	-	-	U	U	U	U
USB Software Reset Value	-	-	-	-	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	IEP0CNT	The length of Endpoint 0 IN data buffer

Table 8.43 Endpoint 1 IN Data Buffer Length Register

9EH (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEP1CNT	-	-	-	IEP1CNT4	IEP1CNT3	IEP1CNT2	IEP1CNT1	IEP1CNT0
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	0	0	0	0
Bus Reset Value (USB RESET)	-	-	-	U	U	U	U	U
USB Software Reset Value	-	-	-	0	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	IEP1CNT	The length of Endpoint 1 IN data buffer

Table 8.44 Endpoint 2 IN Data Buffer Length Register

9FH (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEP2CNT	-	IEP2CNT6	IEP2CNT5	IEP2CNT4	IEP2CNT3	IEP2CNT2	IEP2CNT1	IEP2CNT0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0
Bus Reset Value (USB RESET)	-	U	U	U	U	U	U	U
USB Software Reset Value	-	0	0	0	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	IEP2CNT	The length of Endpoint 2 IN data buffer

Table 8.45 Endpoint 0 OUT Data Buffer Length Register

A5H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OEP0CNT	-	-	-	-	OEP0CNT3	OEP0CNT2	OEP0CNT1	OEP0CNT0
R/W	-	-	-	-	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0
Bus Reset Value (USB RESET)	-	-	-	-	U	U	U	U
USB Software Reset Value	-	-	-	-	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	OEP0CNT	The length of Endpoint 0 OUT data buffer

Table 8.46 Endpoint 1 OUT Data Buffer Length Register

A6H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OEP1CNT	-	-	-	OEP1CNT4	OEP0CNT3	OEP0CNT2	OEP0CNT1	OEP0CNT0
R/W	-	-	-	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	0	0	0	0
Bus Reset Value (USB RESET)	-	-	-	U	U	U	U	U
USB Software Reset Value	-	-	-	0	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	OEP1CNT	The length of Endpoint 1 OUT data buffer

Table 8.47 Endpoint 2 OUT Data Buffer Length Register

A7H (Bank1)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OEP2CNT	-	OEP2CNT6	OEP2CNT5	OEP1CNT4	OEP0CNT3	OEP0CNT2	OEP0CNT1	OEP0CNT0
R/W	-	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0
Bus Reset Value (USB RESET)	-	U	U	U	U	U	U	U
USB Software Reset Value	-	0	0	0	0	0	0	0

Bit No.	Bit Mnemonic	Description
7-0	OEP2CNT	The length of Endpoint 2 OUT data buffer

8.10 Low Voltage Reset (LVR)

8.10.1 Features

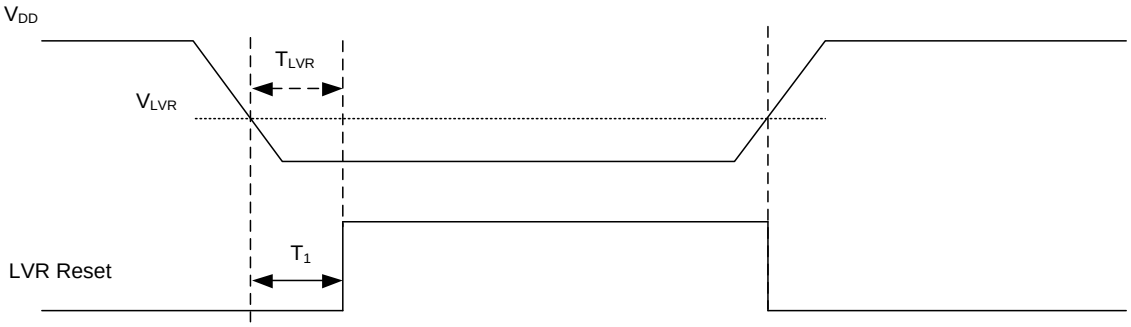
- Enabled by the code option and V_{LVR} is 3.1V or 4.0V
- LVR de-bounce timer T_{LVR} is about 60μs
- An internal reset flag indicates low voltage reset generates

The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage below the specified value V_{LVR}. The LVR de-bounce timer T_{LVR} is about 60μs.

The LVR circuit has the following functions when the LVR function is enabled: (T_1 means the time of the supply voltage below V_{LVR})

Generates a system reset when $V_{DD} \leq V_{LVR}$ and $T_1 \geq T_{LVR}$;

Cancels the system reset when $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$, but $T_1 < T_{LVR}$.



The LVR function is enabled by the code option.

It is typically used in AC line or large battery supplier applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage. This feature can protect system from working under bad power supply environment.

8.11 Watchdog Timer (WDT) and Reset State

8.11.1 Features

- Auto detect Program Counter(PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH79F6488/SH79F6489 built in Program Counter (PC) over range detect circuit, if program counter value is larger than flash romsize, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash rom with A5H.

Watchdog Timer

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled permanently by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow frequency. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

Note: *After base timer or LCD on, if WDT is on ,WDT cannot be turn off in Power-Down mode. Therefore, users need to read or write RSTSTAT register in case to WDT overflow.*

8.11.2 Registers

Table 8.48 Reset Control Register

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Mnemonic	Description
7	**WDOF**	**Watch Dog Timer Overflow or OVL Reset Flag** Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows and no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	**PORF**	**Power On Reset Flag** Set only by Power On Reset, cleared only by software 0: No Power On Reset 1: Power On Reset occurred
4	**LVRF**	**Low Voltage Reset Flag** Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	**CLRF**	**Pin Reset Flag** Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred
2-0	**WDT[2:0]**	**WDT Overflow period control bits** 000: Overflow period minimal value= 4096ms 001: Overflow period minimal value= 1024ms 010: Overflow period minimal value = 256ms 011: Overflow period minimal value = 128ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms ***Notes:*** *If WDT_opt is enable in application, you must clear WatchDog periodically, and the interval must be less than the value list above.*

8.12 Power Management

8.12.1 Features

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH79F6488/SH79F6489 supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

8.12.2 Idle Mode

In this mode, the clock to CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH79F6488/SH79F6489 enter Idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter Idle mode. The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

(1) An interrupt generated. The clock to the CPU will be restored, and the hardware will clear SUSLO register and IDL bit in PCON register. Then the program will execute the interrupt service routine first, and then jumps to the instruction immediately following the instruction that activated Idle mode.

(2) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled), this will restore the clock to the CPU, the SUSLO register and the IDL bit in PCON register will be cleared by hardware, finally the SH79F6488/SH79F6489 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

8.12.3 Power-Down Mode

The Power-Down mode places the SH79F6488/SH79F6489 in a very low power state. Power-Down mode will stop all the clocks including CPU and peripherals. If WDT is enabled, WDT block will keep on working. When entering Power-Down mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79F6488/SH79F6489 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

The setting of PD bit will be the last instruction that CPU executed.

Note: *If IDL bit and PD bit are set simultaneously, the SH79F6488/SH79F6489 enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit form Power-Down mode.*

There are four ways to exit the Power-Down mode:

(1) An active external Interrupt such as INT0, INT1 ,INT2 ,INT3 & INT4 will make SH79F6488/SH79F6489 exit Power-Down mode. The oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) Timer3 interrupt will make SH79F6488/SH79F6489 exit Power-Down mode when 32.768kHz is the clock source. The oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(3) Base Timer interrupt will make SH79F6488/SH79F6489 exit Power-Down mode when 32.768kHz or 12MHz internal RC is the clock source. The oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(4) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled). This will restore the clock to the CPU after warm-up time, the SUSLO register and the PD bit in PCON register will be cleared by hardware, finally the SH79F6488/SH79F6489 will be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note:

(1) In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.

(2) In order to entering Idle/Power-Down,all ports are not floating,set to output or input with pull-high.

(3) In order to entering Idle/Power-Down,reserved pin of LQFP 64 package must be set to output or input with pull-high.

(4) After base timer or LCD on, if WDT is on ,WDT cannot be turn off in Power-Down mode.Therefore, users need to read or write RSTSTAT register in case to WDT overflow.

8.12.4 Registers

Table 8.49 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**SMOD**	**Baud rate double bit**
6	**SSTAT**	**SCON[7:5] function selection bit**
3-2	**GF[1:0]**	**General purpose flags for software use**
1	**PD**	**Power-Down mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode
0	**IDL**	**Idle mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode

Table 8.50 Suspend Mode Control Register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**SUSLO[7:0]**	This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise the either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle.

Example:

```
IDLE_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #01H
        NOP
        NOP
        NOP

POWERDOWN_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #02H
        NOP
        NOP
        NOP
```

8.13 Warm-up Timer

8.13.1 Features

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation startup

SH79F6488/SH79F6489 has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read customer option etc.

SH79F6488/SH79F6489 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from Power-down mode.

After power-on, SH79F6488/SH79F6489 will start power warm-up procedure first, and then oscillator warm-up procedure.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		**WDT Reset (Not in Power-Down Mode)**		**WDT Reset (Wakeup from Power-Down Mode)**		**Wakeup from Power-Down Mode (Only for interrupt)**	
TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*
11ms	YES	500us	NO	500us	YES	32us	YES

OSC Warm-up Time

Option: OP_WMT / Oscillator Type	**00**	**01**	**10**	**11**
Ceramic/Crystal	2^{17} X Tosc	2^{14} X Tosc	2^{11} X Tosc	2^{8} X Tosc
32kHz Crystal	2^{13} X Tosc			
Internal RC	2^{7} X Tosc			

8.14 Code Option

OP_WDT:

0: Disable WDT function (default)
1: Enable WDT function

OP_WDTPD:

0: Disable WDT function in Power-Down mode (default)
1: Enable WDT function in Power-Down mode
Note: *invalid when base timer or LCD on in Power-Down mode*

OP_RST:

0: P4.7 used as RST pin (default)
1: P4.7 used as I/O pin

OP_WMT: (unavailable for 32kHz crystal and Internal RC)

00: longest warm up time (default)
01: longer warm up time
10: shorter warm up time
11: shortest warm up time

OP_CRMC:

0: Other oscillator types exclude 400k-2M ceramic is used (default)
1: 400k-2M ceramic is used

OP_LVREN:

0: Disable LVR function (default)
1: Enable LVR function

OP_LVRLEVEL:

0: 3.1V LVR level 1 (default)
1: 4.0V LVR level 2

OP_SCM:

0: SCM is invalid in warm up period (default)
1: SCM is valid in warm up period

OP_OSC:

0000: Oscillator1 is internal 12M RC (default)
1010: Oscillator1 is 32.768k crystal oscillator, oscillator2 is internal 12M RC
1101: Oscillator1 is 32.768k crystal oscillator, oscillator2 is 400k-16MHz crystal/ceramic oscillator
Others: Oscillator1 is internal 12M RC

OP_ISP:

0: Enable ISP function (default)
1: Disable ISP function

OP_ISPPIN:

0: Enter ISP mode only when P8.6 and P8.7 are connected to GND, simultaneously (default)
1: Enter ISP mode directly regardless the condition of P8.6 and P8.7
Note: *When OP_ISP[7] = 0 available*

OP_OSCDRV:

00: Oscillator drive ability: weak
01: Oscillator drive ability: normal (default)
10: Oscillator drive ability: strong
Note*: Normal ability is recommend*

Code Option OP_CRMC and OP_OSCDRV combinated functions as below:

No.	OP_CRMC	OP_OSCDRV	Drive Ability	Oscillator Type
1	0	00	weak	Crystal Oscillator 400KHz - 4MHz
2	0	01	normal	Crystal Oscillator 4MHz - 16MHz
3	1	00	weak	Ceramic Oscillator < 2MHz
4	1	01	normal	Ceramic Oscillator 2MHz - 8MHz
5	1	10	strong	Ceramic Oscillator 8MHz - 16MHz

9. Instruction Set

ARITHMETIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ADD A, Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A, direct	Add direct byte to accumulator	0x25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data	Add immediate data to accumulator	0x24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data	Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	2	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	1	3
INC DPTR	Increment data pointer	0xA3	1	4
MUL AB 8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB 8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A	Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES					
Opcode		**Description**	**Code**	**Byte**	**Cycle**
ACALL addr11		Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16		Long subroutine call	0x12	3	7
RET		Return from subroutine	0x22	1	8
RETI		Return from interrupt	0x32	1	8
AJMP addr11		Absolute jump	0x01-0xE1	2	4
LJMP addr16		Long jump	0x02	3	5
SJMP rel		Short jump (relative address)	0x80	2	4
JMP @A+DPTR		Jump indirect relative to the DPTR	0x73	1	6
JZ rel	(not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel	(not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel	(not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel	(not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit, rel	(not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit, rel	(not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel	(not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A, direct, rel	(not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A, #data, rel	(not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn, #data, rel	(not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel	(not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn, rel	(not taken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel	(not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP		No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

10. Electrical Characteristics

Absolute Maximum Ratings

DC Supply Voltage. . . . . .-0.3V to +6.0V

Input/Output Voltage. . . . . GND-0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . . . -40℃ to +85℃

FLASH write/erase operating. . . . . 0℃ to +85℃

Storage Temperature . . . .-55℃ to +125℃

Comments

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V - 5.5V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Operating Voltage	V_{DD}	3.0	5.0	5.5	V	f_{OSC} = 24MHz
Operating Current	I_{OP1}	-	6	12	mA	f_{OSC} = 24MHz, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, LVR on, all other function block off
	I_{OP2}	-	4	8	mA	f_{OSC} = 12MHz, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, LVR on, all other function block off
	I_{OP3}	-	25	35	μA	f_{OSC} = 32.768kHz, OSCX off, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), LVR on, all other function block off
Stand by Current (IDLE)	I_{SB1}	-	3	6	mA	f_{OSC} =24MHz, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, LVR on, all other function block off
	I_{SB2}	-	2	5	mA	f_{OSC} = 12MHz, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating), CPU off (IDLE), WDT off,LVR off, all other function block off
	I_{SB3}	-	15	30	μA	f_{OSC} = 32.768kHz, V_{DD} = 5.0V All output pins unload (including all digital input pins unfloating) CPU off (IDLE), WDT off,LVR off, all other function block off
Stand by Current (Power-Down)	I_{SB4}	-	8	15	μA	f_{OSC} = 32.768kHz, V_{DD} = 5.0V All output pins unload(including all digital input pins unfloating), CPU off (Power-Down), LVR on, WDT on, BT on, all other function block off
	I_{SB5}	-	5	10	μA	Osc off, V_{DD} = 5.0V All output pins unload(including all digital input pins unfloating), CPU off (Power-Down), LVR off, WDT off, all other function block off

(to be continued)

(continue)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
WDT Current	I_{WDT}	-	1	3	μA	All output pins unload, WDT on, V_{DD} = 5.0V
Input Low Voltage 1	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O Ports
Input High Voltage 1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O Ports
Input Low Voltage 2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T2, T3, T4, INT0/1/2/3/4, T2EX, RXD
Input High Voltage 2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T2, T3, T4, INT0/1/2/3/4, T2EX, RXD
Input Leakage Current	I_{IL}	-1	-	1	μA	Input pad, V_{IN} = V_{DD} or GND
Pull-high Resistor	R_{PH}	-	30	-	kΩ	V_{DD} = 5.0V, V_{IN} = GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O Ports, I_{OH} = -10mA, V_{DD} = 5.0V
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O Ports, I_{OL} = 15mA, V_{DD} = 5.0V
LCD Resistor	R_{ON}	-	5	-	kΩ	SEG1 - 36, COM1 - 4

Note:

(1) "" Data in "Typ." Column is at 5.0V, 25°C, unless otherwise specified.*
(2) Maximum value of the supply current to V_{DD} is less than 100mA.
(3) Maximum value of the output current from GND is less than 150mA.

A/D Converter Electrical Characteristics (V_{DD} = 3.0 - 5.5V, V_{DDR} = 2.7V, GND = 0V, T_A = 25℃, Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DDR}	-	2.7	-	V	
Resolution	N_R	-	16	-	bit	$0.4 \le V_{AIN} \le 1.6$
A/D reference Voltage	V_{REF}	0.4	-	1.6	V	
A/D Input Voltage	V_{AIN}	0.4	-	1.6	V	
Differential linearity error	D_{LE}	-	±0.5	±1.0	LSB	V_{REF} = 0.6V, F_{AD} = 25Hz
Integral linearity error	I_{LE}	-	±0.010	±0.015	%FS	V_{REF} = 0.6V, F_{AD} = 25Hz
A/D conversion current	I_{AD}	-	1	1.5	mA	ADC module operating
A/D clock	F_{ADCLK}	-	100	400	kHz	
A/D conversion rate	F_{AD}	-	25	100	Hz	
reference Voltage2	V_{REF2}	-	1.19	-	V	reference Voltage2
reference Voltage2 temperature coefficient	D_{REF2}	-	±25	±40	ppm/℃	reference Voltage2

Programmable Gain Amplifier (PGA) Electrical Characteristics
(V_{DD} = 3.0 - 5.5V, V_{DDR} = 2.7V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Operating Voltage	V_{DDR}	-	2.7	-	V	
Input Offset Voltage1	V_{IO1}	-	±20	±50	uV	Chopper on
Input Offset Voltage2	V_{IO2}	-	±1	±2.5	mV	Chopper off
Common-mode Output range	V_{O_PGA}	0.4	-	1.6	V	
Common-mode Input Range	V_{ICR1}	0.4	-	2.0	V	AIN0 - AIN2
Single-end mode Input Range	V_{ICR2}	0.6	-	V_{DDR} - 0.3	V	AN0 - AN3

Operational Amplifier Electrical Characteristics
(V_{DD} = 3.0 - 5.5V, V_{DDR} = 2.7V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DDR}	-	2.7	-	V	
Operating Current	I_{OP}	-	270	350	μA	
Input Offset Voltage	V_{IO}	-	3	7	mV	V_{DDR} = 2.7V, V_{O_OP} = 0.5V_{DDR}
Input Offset Voltage temperature coefficient	V_{IOD}	-	7	-	uV/°C	
Input Common Mode Voltage Range	V_{I_OP}	0.1	-	0.5V_{DDR}	V	
Output Voltage Range	V_{O_OP}	0.3	-	V_{DDR}-0.3	V	
Drive Current	I_{DR_OP}	-	1	-	mA	

Regulator Electrical Characteristics (V_{DD} = 3.0 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ*	Max.	Unit	Condition
Operating Voltage	V_{DD}	3.0	-	5.5	V	
Output Voltage1	V_{DDR1}	2.6	2.7	2.8	V	I_{VDDR1} = 0 - 30mA, V_{DD} = 3.0 - 5.5V
Output Voltage2	V_{DDR2}	3.2	3.3	3.4	V	I_{VDDR2} = 0 - 30mA, V_{DD} = 3.6 - 5.5V
Output Current	I_{DRV}	-	30	-	mA	
Supply Current	I_{SS}	-	50	100	uA	

AC Electrical Characteristics (V_{DD} = 3.0V - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	T_{OSC1}	-	1	2	ms	f_{OSC} = 12MHz
	T_{OSC2}	-	1	2	s	f_{OSC}= 32.768kHz
RESET pulse width	t_{RESET}	10	-	-	μs	Low active
RESET Pin Pull-high Resistor	R_{RPH}	-	30	-	kΩ	V_{DD} = 3.0V, V_{IN} = GND
WDT RC Frequency	F_{WDT}	1	2	3	kHz	
RC Frequency	F_{RC}	11.88	12	12.12	MHz	12M internal RC, Contains the changes between piece and piece (V_{DD} = 3.0 - 5.5V,T_A = 25°C)
PLL Frequency	F_{PLL}	-	48	-	MHz	48M PLL Oscillator, Contains the changes between piece and piece 32.768kHz oscillator starting error < 0.01% (V_{DD} = 3.0 - 5.5V,T_A = 25°C)

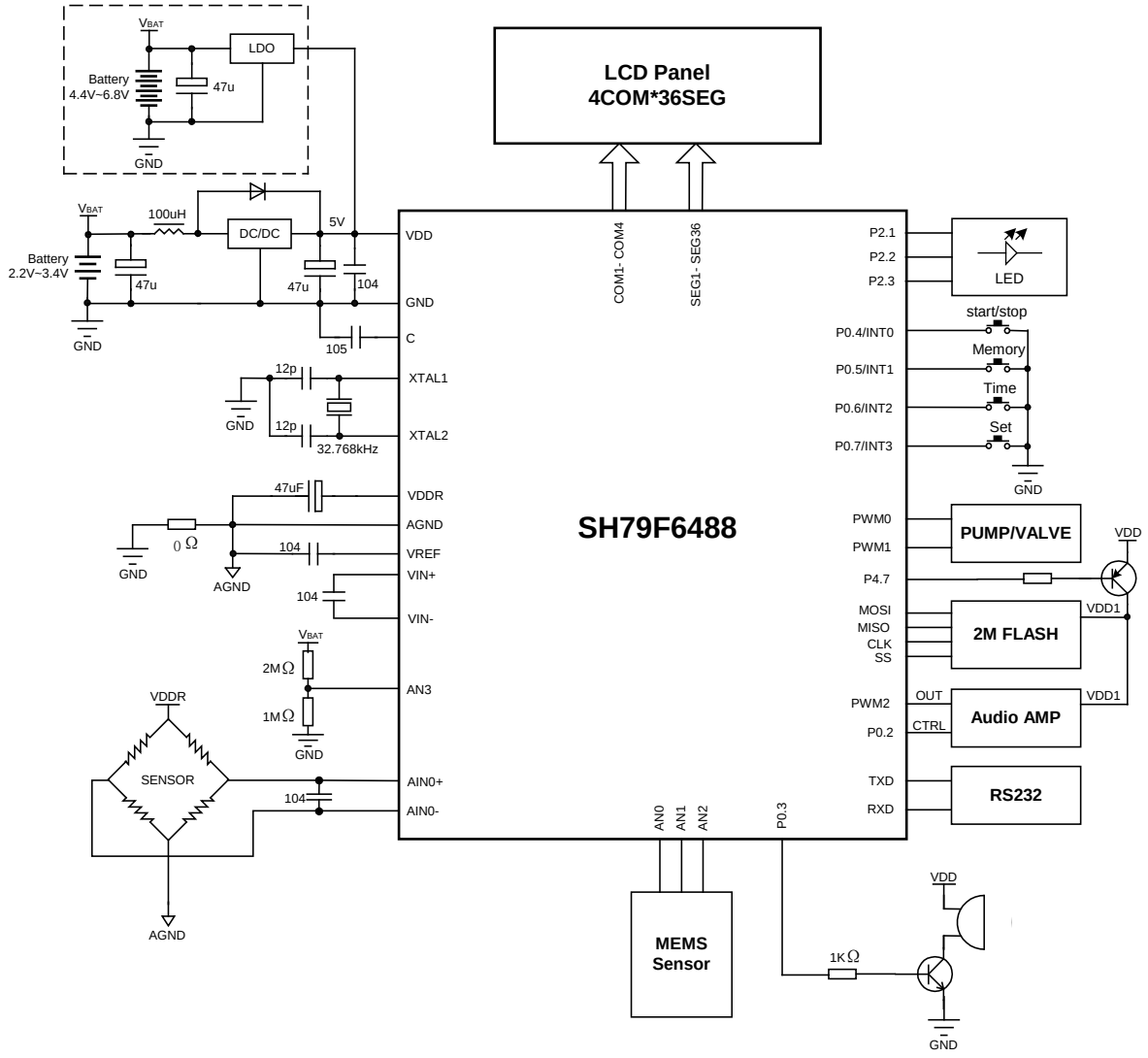
Low Voltage Reset Electrical Characteristics (V_{DD} = 3.0V - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage1	V_{LVR1}	3.0	3.1	3.2	V	LVR enable V_{DD} = V_{LVR1} - 5.5V, f_{OSC} = 12MHz
LVR Voltage2	V_{LVR2}	3.85	4.0	4.15	V	LVR enable V_{DD} = V_{LVR2} - 5.5V, f_{OSC} = 12MHz
Drop-Down Pulse Width for LVR	T_{LVR}	-	60	-	μs	f_{OSC} = 12MHz

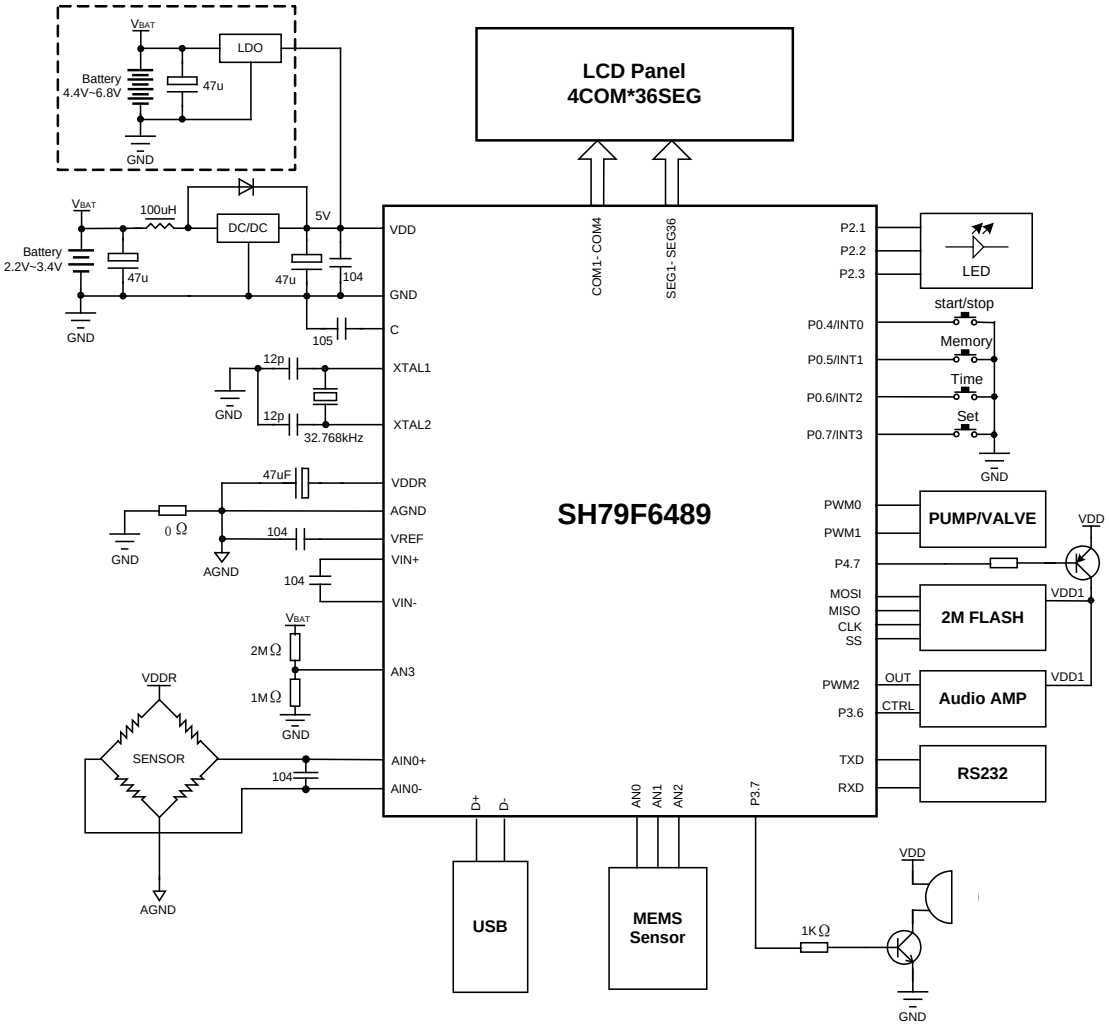
SH79F6489: USB Electrical Characteristics (V_{DD} = 4.0 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input High Voltage (Driving)	$V_{IH(USB)}$	2.0	-	-	V	D-, D+
Input High Voltage (Floating)	$V_{IHZ(USB)}$	2.7	-	3.6	V	D-, D+
Input Low Voltage	$V_{IO(USB)}$	-	-	0.8	V	D-, D+
Differential Input Sensitivity	$V_{DI(USB)}$	0.2	-	-	V	D-, D+ ($\|V_{D+}-V_{D-}\|$)
Differential Common Mode Input Range	$V_{CM(USB)}$	0.8	-	2.5	V	D-, D+ (Include V_{DI} range)
Output Low Voltage	$V_{OL(USB)}$	0.0	-	0.3	V	D-, D+
Output High Voltage (Driving)	$V_{OH(USB)}$	2.8	-	3.6	V	D-, D+
Output Cross Voltage	$V_{CRS(USB)}$	1.3	-	2.0	V	D-, D+, V_{DD} = 4.0V - 5.5V

11. Application



SH79F6488 Application Circuit Diagram



SH79F6489 Application Circuit Diagram

Note:

(1) LDO and DC/DC can be chosen one for external power module.

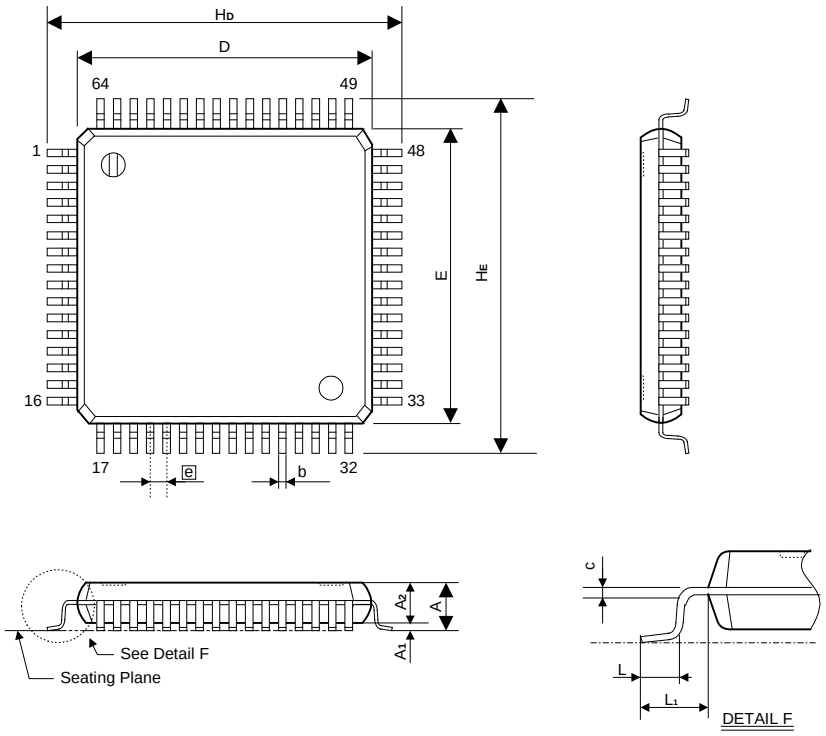
(2) Sensor can be drived by V_{DDR} or constant current source of OP.

12. Ordering Information

Part No.	Package
SH79F6488P/064PR	LQPF64
SH79F6488P/080PR	LQPF80
SH79F6488H	CHIP
SH79F6489P/064PR	LQPF64
SH79F6489P/080PR	LQPF80
SH79F6489H	CHIP

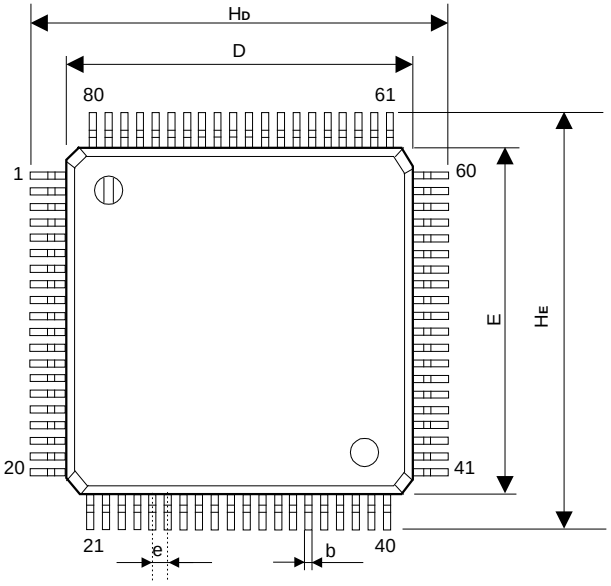
13. Package Information

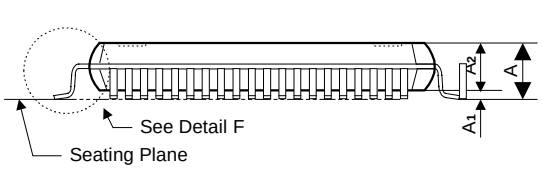
LQFP64 Outline Dimensions unit: inch/mm

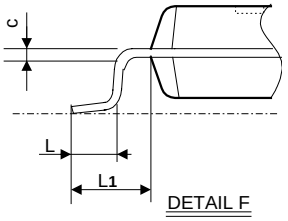


Symbol	Dimensions in inches	Dimensions in mm
A	0.063 (MAX)	1.60 (MAX)
A_1	0.002 (MIN.), 0.006(MAX.)	0.05 (MIN), 0.15 (MAX)
A_2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.004 (MIN), 0.008 (MAX)	0.09 (MIN), 0.20 (MAX)
D	0.394 BASIC	10.00 BASIC
E	0.394 BASIC	10.00 BASIC
e	0.020 BASIC	0.50 BASIC
H_D	0.472 BASIC	12.00 BASIC
H_E	0.472 BASIC	12.00 BASIC
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 REF	1.00 REF

LQFP80 Outline Dimensions unit: inch/mm

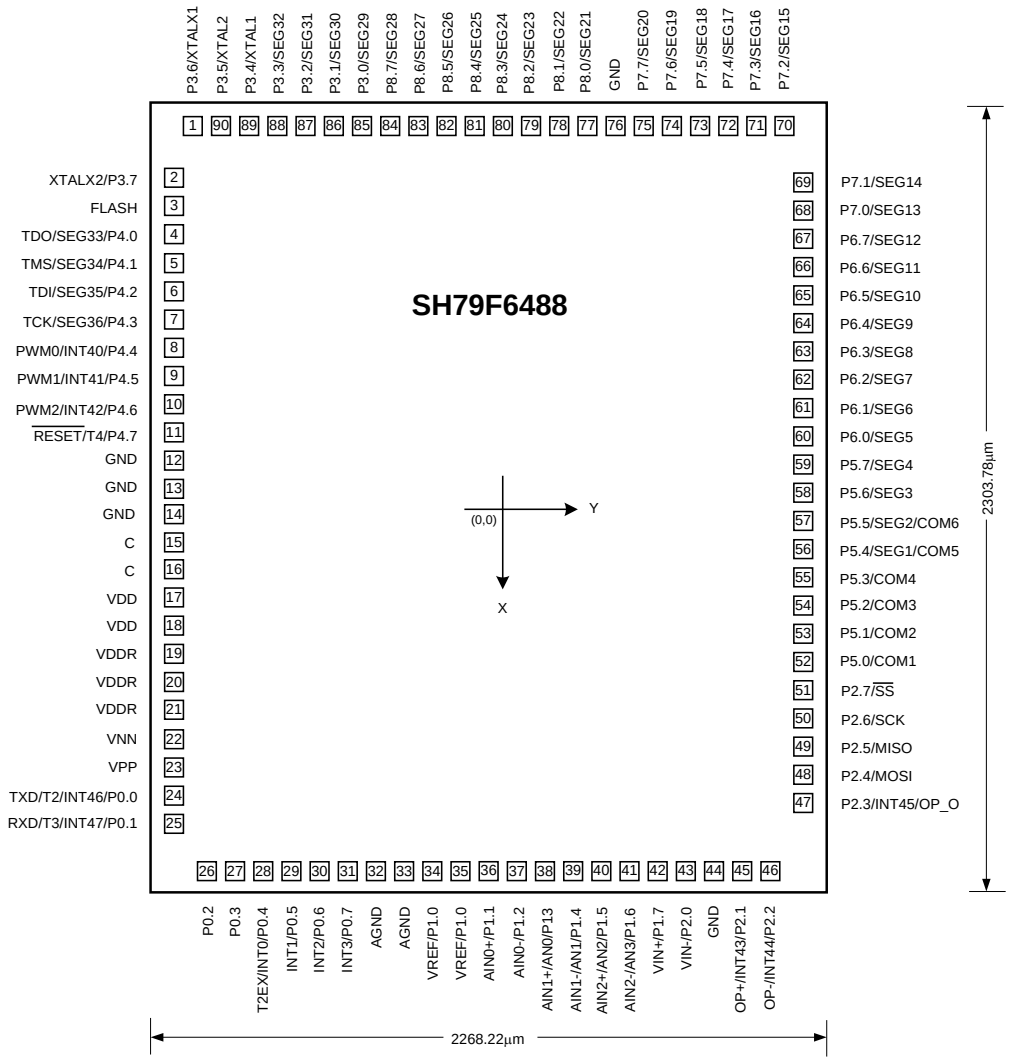




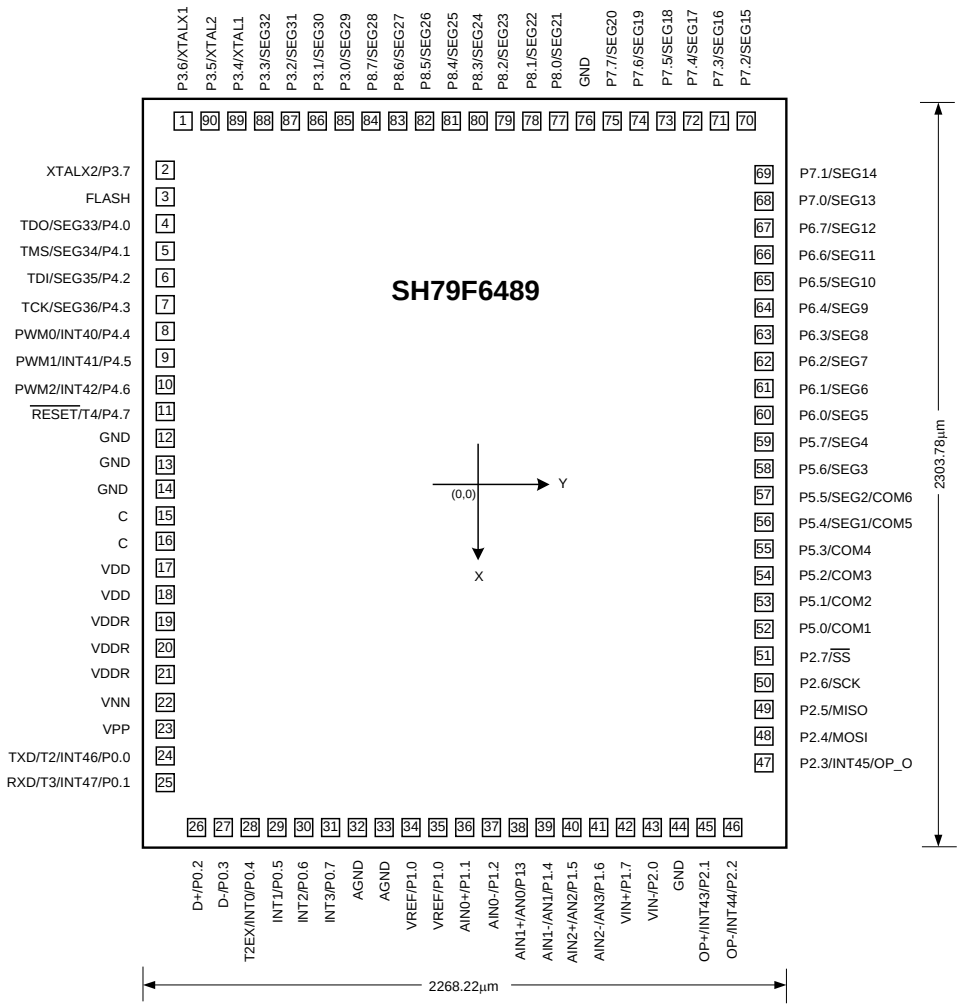


Symbol	Dimensions in inches		Dimensions in mm	
	Min	Max	Min	Max
A	---	0.063	---	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
D	0.469	0.476	11.90	12.10
E	0.469	0.476	11.90	12.10
H_D	0.545	0.557	13.85	14.15
H_E	0.545	0.557	13.85	14.15
b	0.007	0.011	0.17	0.27
e	0.020BSC		0.50BSC	
c	0.004	0.008	0.09	0.20
L	0.018	0.030	0.45	0.75
L1	0.033	0.045	0.85	1.15
θ	0°	10°	0°	10°

Chip Bonding Information unit: um



SH79F6488 Pad Coordinates Diagram



SH79F6489 Pad Coordinates Diagram

SH79F6488/SH79F6489 Bonding

Pad No.	Pin Name	X	Y	Pin No.		Pad No.	Pin Name	X	Y	Pin No.	
				LQFP64	LQFP80					LQFP64	LQFP80
1	XTALX1/P3.6	-1040.84	-924.12	2	2	46	OP-/INT44/P2.2	1040.84	928.88	30	38
2	XTALX2/P3.7	-1017.71	-1058.26	3	3	47	OP_O/INT45/P2.3	978.54	1058.26	31	39
3	/	-897.01	-1058.26	/	/	48	MOSI/P2.4	857.84	1058.26	/	40
4	TDO/SEG33/P4.0	-776.3	-1058.26	4	4	49	MISO/P2.5	737.14	1058.26	/	41
5	TMS/SEG34/P4.1	-686.21	-1058.26	5	5	50	SCK/P2.6	647.04	1058.26	/	42
6	TDI/SEG35/P4.2	-596.1	-1058.26	6	6	51	$\overline{SS}$/P2.7	556.94	1058.26	/	43
7	TCK/SEG36/P4.3	-506.01	-1058.26	7	7	52	COM1/P5.0	466.84	1058.26	32	44
8	PWM0/INT40/P4.4	-429.51	-1058.26	8	8	53	COM2/P5.1	372.83	1058.26	33	45
9	PWM1/INT41/P4.5	-353.01	-1058.26	9	9	54	COM3/P5.2	296.33	1058.26	34	46
10	PWM2/INT42/P4.6	-276.51	-1058.26	10	10	55	COM4/P5.3	219.83	1058.26	35	47

(to be continued)

(Continue)

Pad No.	Pin Name	X	Y	Pin No.		Pad No.	Pin Name	X	Y	Pin No.	
				LQFP64	LQFP80					LQFP64	LQFP80
11	$\overline{\text{RESET}}$/T4/P4.7	-200.01	-1058.26	11	11	56	COM5/SEG1/P5.4	143.33	1058.26	36	48
12	GND	-106	-1058.26	12&bond to frame	12&bond to frame	57	COM6/SEG2/P5.5	49.93	1058.26	37	49
13	GND	-29.5	-1058.26	12	12	58	SEG3/P5.6	-45.95	1058.26	38	50
14	GND	47.01	-1058.26	12	12	59	SEG4/P5.7	-122.45	1058.26	39	51
15	C	123.5	-1058.26	13	13	60	SEG5/P6.0	-198.95	1058.26	40	52
16	C	200.01	-1058.26	13	13	61	SEG6/P6.1	-275.45	1058.26	41	53
17	VDD	276.51	-1058.26	14	14	62	SEG7/P6.2	-351.95	1058.26	42	54
18	VDD	353.01	-1058.26	14	14	63	SEG8/P6.3	-428.45	1058.26	43	55
19	VDDR	429.51	-1058.26	15	15	64	SEG9/P6.4	-504.95	1058.26	44	56
20	VDDR	506.01	-1058.26	15	16	65	SEG10/P6.5	-595.05	1058.26	45	57
21	VDDR	596.1	-1058.26	15	17	66	SEG11/P6.6	-685.15	1058.26	46	58
22	/	686.21	-1058.26	/	/	67	SEG12/P6.7	-775.25	1058.26	47	59
23	/	776.3	-1058.26	/	/	68	SEG13/P7.0	-895.95	1058.26	48	60
24	TXD/T2/INT46/P0.0	897.01	-1058.26	16	18	69	SEG14/P7.1	-1016.65	1058.26	49	61
25	RXD/T3/INT47/P0.1	1017.71	-1058.26	17	19	70	SEG15/P7.2	-1040.84	928.88	50	62
26	SH79F6488: P0.2 SH79F6489: D+/P0.2	1040.84	-928.88	18	20	71	SEG16/P7.3	-1040.84	808.18	51	63
27	SH79F6488: P0.3 SH79F6489: D-/P0.3	1040.84	-808.18	19	21	72	SEG17/P7.4	-1040.84	704.48	52	64
28	T2EX/INT0/P0.4	1040.84	-687.48	20	22	73	SEG18/P7.5	-1040.84	614.38	53	65
29	INT1/P0.5	1040.84	-597.38	/	23	74	SEG19/P7.6	-1040.84	524.28	54	66
30	INT2/P0.6	1040.84	-507.28	/	24	75	SEG20/P7.7	-1040.84	447.78	55	67
31	INT3/P0.7	1040.84	-430.78	/	25	76	bond to frame	-1040.84	368.73	bond to frame	bond to frame
32	AGND	1040.84	-354.28	21	26	77	SEG21/P8.0	-1040.84	292.23	56	68
33	AGND	1040.84	-277.78	21	26	78	SEG22/P8.1	-1040.84	215.73	57	69
34	VREF/P1.0	1040.84	-201.28	22	27	79	SEG23/P8.2	-1040.84	139.23	58	70
35	VREF/P1.0	1040.84	-124.78	22	28	80	SEG24/P8.3	-1040.84	62.73	59	71
36	AIN0+/P1.1	1040.84	-48.28	23	29	81	SEG25/P8.4	-1040.84	-13.77	60	72
37	AIN0-/P1.2	1040.84	45.73	24	30	82	SEG26/P8.5	-1040.84	-90.27	61	73
38	AIN1+/AN0/P1.3	1040.84	139.74	/	31	83	SEG27/P8.6	-1040.84	-166.77	62	74
39	AIN1-/AN1/P1.4	1040.84	233.75	/	32	84	SEG28/P8.7	-1040.84	-290.02	63	75
40	AIN2+/AN2/P1.5	1040.84	327.76	25	33	85	SEG29/P3.0	-1040.84	-366.52	/	76
41	AIN2-/AN3/P1.6	1040.84	421.77	26	34	86	SEG30/P3.1	-1040.84	-443.02	/	77
42	VIN+/P1.7	1040.84	515.78	27	35	87	SEG31/P3.2	-1040.84	-519.52	/	78
43	VIN-/P2.0	1040.84	605.88	28	36	88	SEG32/P3.3	-1040.84	-609.62	/	79
44	bond to frame	1040.84	695.98	bond to frame	bond to frame	89	XTAL1/P3.4	-1040.84	-699.72	64	80
45	OP+/INT43/P2.1	1040.84	808.18	29	37	90	XTAL2/P3.5	-1040.84	-803.42	1	1

14. Product SPEC. Change Notice

Version	Content	Date
2.1	Original	Sep. 2014

Content