SINO WEALTH

SH86263
FEATURE DATASHEET

Released
Ver 1.0
August 19, 2009

CONTENT

1. FEATURES

- Enhanced single-cycle 8051 MCU core
- Integrated line regulators for system power supply and Li-battery charging.
- Built-in enhanced flexible flash controller:
  - Support SLC/MLC NAND and AG-AND flashes
  - Support 4k page flash
  - Support up to 4 flash CEs.
- Built-in Multi-bit/1KB BCH ECC
- USB interface
  - High-speed USB 2.0 interface, backward compatible with USB 1.1
  - Support one device address
  - Support 3 endpoints: one control endpoint, one bulk-in endpoint and one bulk-out endpoint
- Built-in LCD module interface:
  - Support CSTN/TFT/STN/OLED driver 8080-series 8-bit parallel bus interface and serial bus interface.
  - Support bit antitone.
- On-chip CODEC:
  - 16-bit Sigma-Delta stereo DAC
  - 2 channels SAR ADC for power detection and key scan
  - Stereo headphone amplifier with short-circuit protection
- Built-in 9 GPIO (PA [3:0] and PC [4:0]) with flexible I/O setting
- 12MHz external clock input with on-chip PLL
- Four reset sources:
  - Power on reset (POR)
  - Lower voltage reset (LVR)
  - Watchdog reset (WDR)
  - External pin reset (EPR)
- Support MPEG1/2/2.5 Audio Layer 3 decoding: 8k~48kHz sampling frequencies, 8k~320kbps bit rates, single/dual channel, mono/stereo format, equalizer
- Support AMT2.0: Automatic Music Format Transformer
- Available in standard 48-pin TQFP package.

2. GENERAL DESCRIPTION

SH86263 is a new generation single-chip highly integrated digital multimedia SOC for devices such as dedicated audio players and mass storage. It includes audio CODEC, a high performance dual core (DSP and MCU) structure with embedded RAM and ROM and USB2.0 high-speed SIE and PHY functional block for downloading and uploading. SH86263 also provides an interface to flash memory, button and switch inputs and headphones control.

SH86263 provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized digital multimedia players.

3. PAD AND PIN ASSIGNMENT

3.1. TQFP48 Pin Out

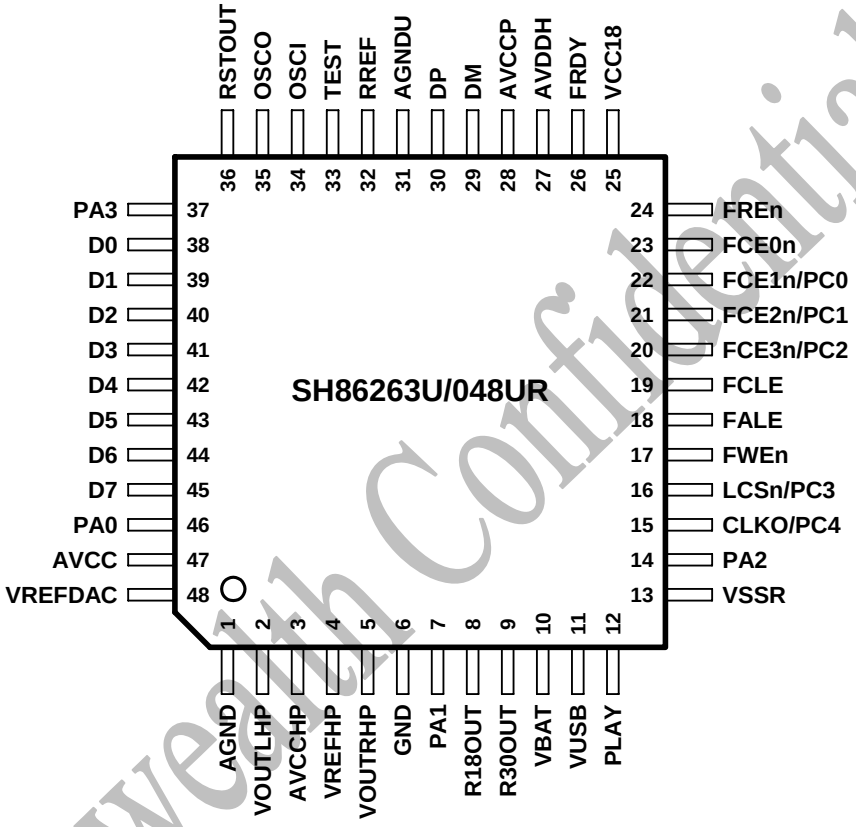

Figure 1. TQFP48 Pin Out

No.	Name	No.	Name	No.	Name	No.	Name
1	AGND	13	VSSR	25	VCC18	37	PA3
2	VOUTLHP	14	PA2	26	FRDY	38	D0
3	AVCCHP	15	CLKO/PC4	27	AVDDH	39	D1
4	VREFHP	16	LCSn/PC3	28	AVCCP	40	D2
5	VOUTRHP	17	FWEn	29	DM	41	D3
6	GND	18	FALE	30	DP	42	D4
7	PA1	19	FCLE	31	AGNDU	43	D5
8	R18OUT	20	FCE3n/PC2	32	RREF	44	D6
9	R30OUT	21	FCE2n/PC1	33	TEST	45	D7
10	VBAT	22	FCE1n/PC0	34	OSCI	46	PA0
11	VUSB	23	FCE0n	35	OSCO	47	AVCC
12	PLAY	24	FREn	36	RSTOUT	48	VREFDAC

Table 1. TQFP48 Pin Out

3.2. Pad and Pin Description

Pin Name	Type[1]	State[2]	Description	Pin No.
AGND	P	-	Analog ground	1
VOUTLHP	O	-	Headphone driver left channel output (15mW)	2
AVCCHP	P	-	Analog supply for headphone driver (1.8V Typ.)	3
VREFHP	O	-	Headphone driver reference voltage	4
VOUTRHP	O	-	Headphone driver right channel output. (15mW)	5
GND	P	-	Digital power ground	6
PA1	I/O	CP	Bit1 of general purpose port A	7
R18OUT	P	-	Regulator 1.8V power output.	8
R30OUT	P	-	Regulator 3.0V power output.	9
VBAT	P	-	Battery power input.	10
VUSB	P	-	USB power input.	11
PLAY	I	-	PLAY key connection pin.	12
VSSR	P	-	Regulator power ground.	13
PA2	I/O	CP	Bit2 of general purpose port A	14
CLKO/PC4	O I/O	-	Clock out pin (PC4SEL=1) Bit4 of general purpose port A (PC4SEL=0)	15
LCSn/PC3	O I/O	-	LCD driver chip selection (PC3SEL=1) Bit3 of general purpose port C (PC3SEL=0)	16
FWEn	O	-	Flash write enable	17
FALE	O	-	Flash address latch enable	18
FCLE	O	-	Flash command latch enable	19
FCE3n/PC2	O I/O	-	Flash 4th chip enable (PC2SEL=1) Bit2 of general purpose port C (PC2SEL=0)	20
FCE2n/PC1	O I/O	-	Flash 3rd chip enable (PC1SEL=1) Bit1 of general purpose port C (PC1SEL=0)	21
FCE1n/PC0	O I/O	-	Flash 2nd chip enable (PC0SEL=1) Bit0 of general purpose port C (PC0SEL=0)	22
FCE0n	O	-	Flash 1st chip enable	23
FREn	O	-	Flash read enable	24
VCC18	P	-	1.8V digital power supply.	25
FRDY	I	PH	Flash ready/busy detection input	26
AVDDH	P	-	3V analog supply for USB receiver and transmitter.	27
AVCCP	P	-	1.8V analog supply for USB PLL	28
DM	I/O	-	USB data negative pin terminal	29
DP	I/O	-	USB data positive pin terminal	30
AGNDU	P	-	Analog ground for USB	31
RREF	I	-	Connect external reference resistor (12kΩ±1%) to analog ground	32
TEST	I	PL	Test mode enable pin. TEST=0 selects normal mode. TEST=1 selects test mode.	33
OSCI	I	-	12MHz crystal oscillator or external clock input.	34
OSCO	O	-	12MHz crystal oscillator output.	35
RSTOUT	O	-	Reset out control pin.	36
PA3	I/O	CP	Bit3 of general purpose port A	37

Table 2. Pad & Pin Description

PAD Name	Type[1]	State[2]	Description	Pin No.
D0	I/O	CP	Bit0 of flash data bus (SFC active) Bit0 of LCD data bus (LCMI active)	38
D1	I/O	CP	Bit1 of flash data bus (SFC active) Bit1 of LCD data bus (LCMI active)	39
D2	I/O	CP	Bit2 of flash data bus (SFC active) Bit2 of LCD data bus (LCMI active)	40
D3	I/O	CP	Bit3 of flash data bus (SFC active) Bit3 of LCD data bus (LCMI active)	41
D4	I/O	CP	Bit4 of flash data bus (SFC active) Bit4 of LCD data bus (LCMI active)	42
D5	I/O	CP	Bit5 of flash data bus (SFC active) Bit5 of LCD data bus (LCMI active)	43
D6	I/O	CP	Bit6 of flash data bus (SFC active) Bit6 of LCD data bus (LCMI active)	44
D7	I/O	CP	Bit7 of flash data bus (SFC active) Bit7 of LCD data bus (LCMI active)	45
PA0	I/O	CP	Bit0 of general purpose port A	46
AVCCADC	P	-	1.8V analog supply for ADC	47
VREFDAC	O	-	DAC reference voltage	48

Table 3. PAD & PIN Description (Continue)

Note: 1. Type: P→Power, I→Input, O→Output, I/O→Input/Output
2. State: PL→Pull-low to GND, PH→Pull-high to VDD3, CP→Configurable Pull-low/Pull-high

4. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Symbol	Parameter	Min.	Max.	Unit
VREGIN	Regulator supply voltage	-0.3	5.5	V
VDD	VDD3 / AVDDH supply voltage	-0.3	3.6	V
VCC	VCC18 / AVCCP supply voltage	-0.3	2.0	V
AVCC	AVCCADC / AVCCDAC / AVCCHP supply voltage relative to AGND	-0.3	2.0	V
USBIO	Input voltage on DP and DM pins	-0.3	3.6	V
VIN	Input voltage on any digital I/O pin relative to GND	-0.3	VDD+0.3	V
VINA	Input voltage on any analog pin relative to AGND	-0.3	AVCC+0.3	V
T_{AMB}	Ambient operating temperature	-10	70	℃
T_{STG}	Storage Temperature	-55	125	℃

Table 4. Absolute Maximum Ratings

4.2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VREGIN	Regulator supply voltage	3.2	4.2	5.0	V
VDD3	Digital I/O supply voltage	2.8	3.0	3.3	V
VCC18	Digital core supply voltage	1.71	1.8	1.89	V
AVDDH	Analog supply for USB receiver and transmitter	3.0	3.0	3.3	V
AVCCP	Analog supply for USB PLL	1.71	1.8	1.89	V
AVCCDAC	Analog supply for DAC	1.71	1.8	1.89	V
AVCCADC	Analog supply for ADC	1.71	1.8	1.89	V
AVCCHP	Analog supply for headphone driver	1.71	1.8	1.89	V

Table 5. Recommended Operating Conditions

4.3. DC Characteristics

(V_{DD3} = 3.0V, V_{DD18} = 1.8V, GND = 0V, T_{AMB} = 25°C, F_{OSC} = 12MHz, unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	High-level Output Voltage	2.1	-	3.0	V	$\|I_{OH}\|$ = 4mA
V_{OL}	Low-level Output Voltage	0	-	0.9	V	$\|I_{OH}\|$ = 4mA
V_{IH}	High-level Input Voltage	2.1	-	3.0	V	
V_{IL}	Low-level Input Voltage	0	-	0.9	V	
R_H	Internal Pull-high Resistor	-	75	-	kΩ	
R_L	Internal Pull-low Resistor	-	75	-	kΩ	
R_{FRDY}	FRDY Internal Pull-high Resistor	2	4	6	kΩ	

Table 6. DC Characteristics

5. PACKAGE OUTLINE INFORMATION

5.1. TQFP48 Outline Dimensions (For main Chip Package)

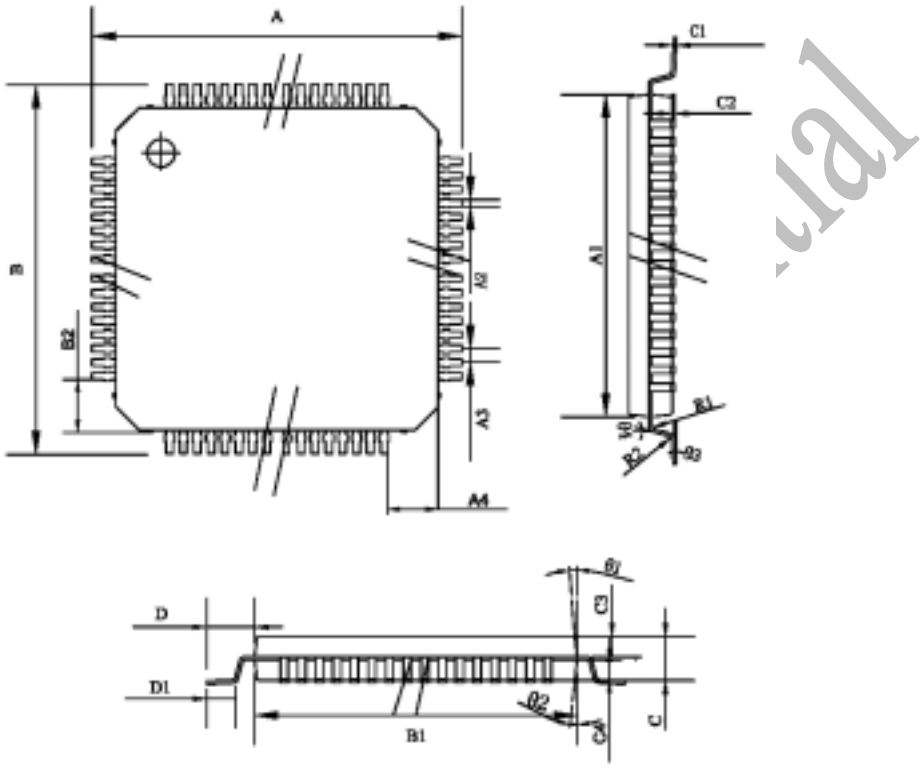

Figure 2. TQFP48 Outline Dimensions

Symbol	Minimum (mm)	Maximum (mm)	Symbol	Minimum (mm)	Maximum (mm)
A	8.80	9.20	**C**	0.90	1.05
A1	6.85	7.05	**C1**	0.09	0.20
A2	0.15	0.25	**C2**	0.05	0.15
A3	0.5 TYP		**C3**	0.4365 TYP	
A4	0.65 TYP		**C4**	0.4365 TYP	
B	8.80	9.20	**D**	0.85	1.15
B1	6.85	7.05	**D1**	0.45	0.75
B2	0.65 TYP		**θ1**	12° TYP	
R1	0.15 TYP		**θ2**	12° TYP	
R2	0.15 TYP		**θ3**	0° ~ 7°	
			θ4	7° TYP	

Table 7. TQFP48 Outline Dimensions

6. HISTORY

Version	Date	Modify Content
1.0	2009.8.19	1. Original