SINO WEALTH

SH86313U/048UR

Highly-integrated Digital Music Controller

FEATURE DATASHEET

Confidential
V1.0
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CONTENT

1. FEATURES

- Enhanced single-cycle 8051 MCU core
- Built-in 64K Byte Flash Program Block and 2K Byte Flash Data block
- Built-in USB2.0 full speed OTG controller
  - Act as host support one device address
  - Act as device support setup/bulk/isochronous transfer
  - Support full speed (12Mbps) USB transfer
- Built-in simplified MMC/SD card engine
  - Support 1-Line mode
  - Support write & read operation
- Software information:
  - Support MPEG1/2/2.5 Audio Layer 3 decoding: 8k~48kHz sampling frequencies, 8k~320kbps bit rates, single/dual channel, mono/stereo format, equalizer
  - Support WMA decoding: 8k~48kHz sampling frequencies, 5k~384kbps bit rates, single/dual channel, mono/stereo format, equalizer
  - Support tone/balance adjust. Support 8 EQ mode
- On-chip CODEC:
  - 16-bit Sigma-Delta stereo DAC with 3.3V operation voltage
  - Build-in 2 groups dual-channel Aux-in
  - 6-channel 8-bit SAR ADC support key-scan, digital voice recording and power detection
- 32 GPIOs with flexible I/O setting, 4 GPIOs output 1/2 bias voltage for LCD driver
- Typical power voltage: 3.3V (for I/O) and 1.8V (for core)
- Internal or external oscillator optional
  - Support external 12MHz oscillator with on chip PLL and 32.768KHZ for RTC
  - Built-in 12MHz RC oscillator
- Embedded in SPI interface for external serial flash
- Built-in 5V-to-3.3V and 5V-to-1.8V regulators
- Built-in infrared remote control module
- Support 1/2 bias voltage 4-COM x 12-SEG LCD (VCC=3.3V)
- In-system firmware program/upgrade through U-disk or MMC/SD. Support code protect
- USB/SD/Key/RTC wakeup STOP
- Three reset sources:
  - Power-on reset (POR)
  - Lower voltage reset (LVR)
  - Watchdog reset (WDR)
- Low power mode & wake up by RTC/USB/KEY/SD
  - Support IDLE mode. LDO enter suspend mode
  - Support SLEEP mode. Disable 12M OSCI and LDO enter suspend mode
  - Support STOP mode. Disable LDO output 1.8V & 3.3V voltage
- Available in standard TQFP48 packages

2. GENERAL DESCRIPTION

SH86313 is a new generation single-chip highly integrated digital multimedia SOC designed for Boombox.

SH86313 combines a high performance MCU core with embedded RAM and ROM, a 16-bit Sigma-Delta stereo DAC, an 8-bit SAR ADC, USB Host into a single chip.

SH86313 also provides an interface to SPI flash, MMC/SD, STN LCD, Infrared receiver, button & switch inputs and FM control.

3. PAD AND PIN

3.1. TQFP48 Pin Assignment

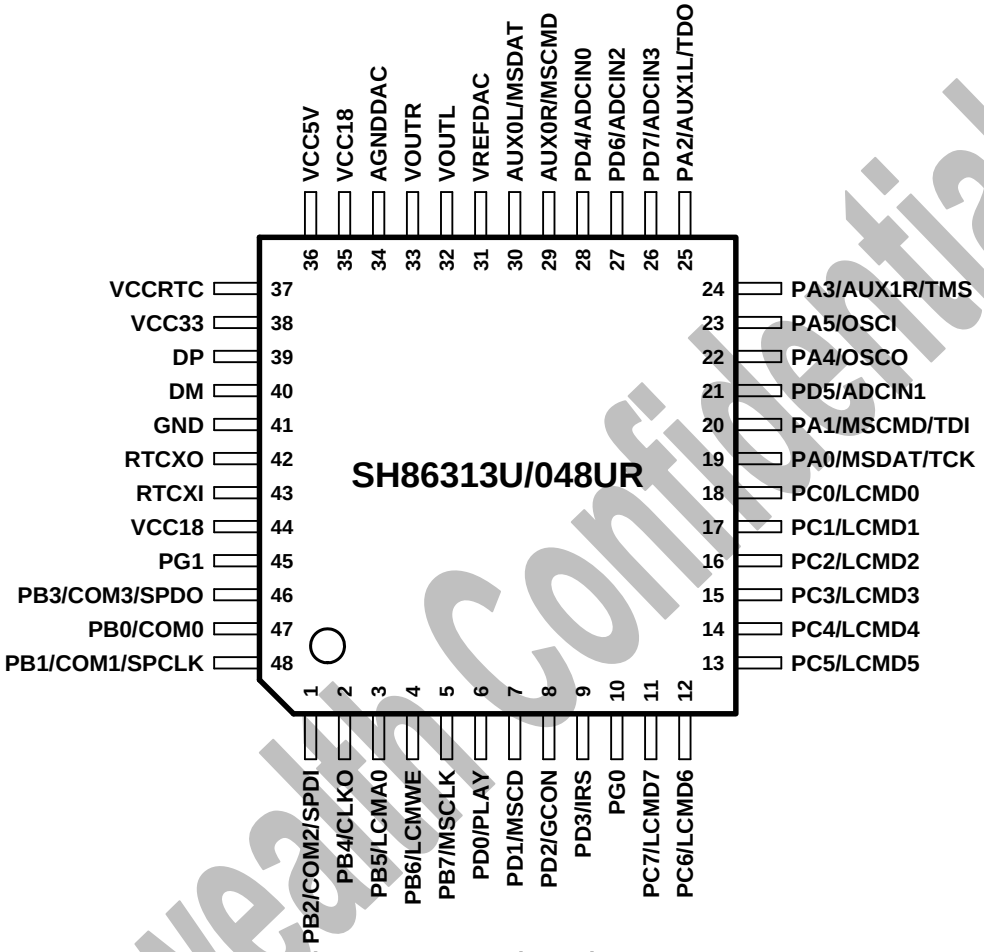

Figure 1. TQFP48 Pin Assignment

No.	Name	No.	Name	No.	Name	No.	Name
1	PB2/COM2/SPDI	13	PC5/LCMD5	25	PA2/AUX1L/TDO	37	VCCRTC
2	PB4/CLKO	14	PC4/LCMD4	26	PD7/ADCIN3	38	VCC33
3	PB5/LCMA0	15	PC3/LCMD3	27	PD6/ADCIN2	39	DP
4	PB6/LCMWE	16	PC2/LCMD2	28	PD4/ADCIN0	40	DM
5	PB7/MSCLK	17	PC1/LCMD1	29	AUX0R/MSCMD	41	GND
6	PD0/PLAY	18	PC0/LCMD0	30	AUX0L/MSDAT	42	RTCXO
7	PD1/MSCD	19	PA0/TCK	31	VREFDAC	43	RTCXI
8	PD2/GCON	20	PA1/TDI	32	VOUTL	44	VCC18
9	PD3/IRS	21	PD5/ADCIN1	33	VOUTR	45	PG1
10	PG0	22	PA4/OSCO	34	AGNDDAC	46	PB3/COM3/SPDO
11	PC7/LCMD7	23	PA5/OSCI	35	VCC18	47	PB0/COM0
12	PC6/LCMD6	24	PA3/AUX1R/TMS	36	VCC5V	48	PB1/COM1/SPCLK

Table 1. TQFP48 Pin Assignment

3.2. Pin Description

Pin Name	Type	Description	Pin No.
PB2 COM2 SPDI	I/O O I	Bit2 of general purpose port B LCD 1/2-bias voltage output 2 SPI data input	1
PB4 CLKO	I/O O	Bit4 of general purpose port B Clock output	2
PB5 LCMA0	I/O O	Bit5 of general purpose port B LCD driver data/command selection	3
PB6 LCMWE	I/O O	Bit6 of general purpose port B LCD driver write enable (active low)	4
PB7 MSCLK	I/O O	Bit7 of general purpose port B MMC/SD interface clock line	5
PD0 PLAY	I/O I	Bit0 of general purpose port D PLAY key detection pin	6
PD1 MSCD	I/O I	Bit1 of general purpose port D MMC/SD card detection pin	7
PD2 GCON	I/O O	Bit2 of general purpose port D Global control pin	8
PD3 IRS	I/O I	Bit3 of general purpose port D Infrared receiver interface signal	9
PG0	I/O	Bit0 of general purpose port G	10
PC7 LCMD7	I/O I/O	Bit7 of general purpose port C Bit7 of LCD driver data bus	11
PC6 LCMD6	I/O I/O	Bit6 of general purpose port C Bit6 of LCD driver data bus	12
PC5 LCMD5	I/O I/O	Bit5 of general purpose port C Bit5 of LCD driver data bus	13
PC4 LCMD4	I/O I/O	Bit4 of general purpose port C Bit4 of LCD driver data bus	14
PC3 LCMD3	I/O I/O	Bit3 of general purpose port C Bit3 of LCD driver data bus	15
PC2 LCMD2	I/O I/O	Bit2 of general purpose port C Bit2 of LCD driver data bus	16
PC1 LCMD1	I/O I/O	Bit1 of general purpose port C Bit1 of LCD driver data bus	17
PC0 LCMD0	I/O I/O	Bit0 of general purpose port C Bit0 of LCD driver data bus	18
PA0 TCK	I/O I	Bit0 of general purpose port A Debug interface: test clock in	19
PA1 TDI	I/O I	Bit1 of general purpose port A Debug interface: test data in	20
PD5 ADCIN1	I/O I	Bit5 of general purpose port D ADC channel 1 analog input	21
PA4 OSCO	I/O O	Bit4 of general purpose port A 12MHz crystal osc. output	22
PA5 OSCI	I/O I	Bit5 of general purpose port A 12MHz crystal osc. or external clock input	23
PA3 AUX1R TMS	I/O I I	Bit3 of general purpose port A Aux-in 1 right channel analog input Debug interface: test mode select	24
PA2 AUX1L TDO	I/O I O	Bit2 of general purpose port A Aux-in 1 left channel analog input Debug interface: test data out	25
PD7 ADCIN3	I/O I	Bit7 of general purpose port D ADC channel 3 analog input	26
PD6 ADCIN2	I/O I	Bit6 of general purpose port D ADC channel 2 analog input	27
PD4 ADCIN0	I/O I	Bit4 of general purpose port D ADC channel 0 analog input	28

Table 2. PIN Description

Pin Name	Type	Description	Pin No.
AUX0R MSCMD	I I/O	Aux-in 0 right channel analog input MMC/SD interface command line	29
AUX0L MSDAT	I I/O	Aux-in 0 left channel analog input MMC/SD interface data line	30
VREFDAC	O	DAC reference voltage output	31
VOUTL	O	DAC left channel analog output	32
VOUTR	O	DAC right channel analog output	33
AGNDDAC	P	Analog ground for DAC	34
VCC18	P	1.8V power supply	35
VCC5V	P	5V power supply	36
VCCRTC	P	5V power supply for RTC	37
VCC33	P	3.3V power supply	38
DP	I/O	USB data positive pin terminal	39
DM	I/O	USB data negative pin terminal	40
GND	P	Power ground	41
RTCXO	O	32.768kHz crystal oscillator output	42
RTCXI	I	32.768kHz crystal oscillator or external clock input	43
VCC18	P	1.8V power supply	44
PG1	I/O	Bit1 of general purpose port G	45
PB3 COM3 SPDO	I/O O O	Bit3 of general purpose port B LCD 1/2-bias voltage output 3 SPI Data output	46
PB0 COM0	I/O O	Bit0 of general purpose port B LCD 1/2-bias voltage output 0	47
PB1 COM1 SPCLK	I/O O O	Bit1 of general purpose port B LCD 1/2-bias voltage output 1 SPI serial clock	48

Table 3. PIN Description (continue)

4. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC5V	5V power supply	-0.3	-	5.5	V
VCC33	3.3V power supply	-0.3	-	3.6	V
VCC18	1.8V power supply	-0.3	-	2.0	V
VIN	Input signal voltage	-0.3	-	3.6	V
T_{OPR}	Operating temperature	-10	-	70	℃
T_{STG}	Storage temperature	-40	-	125	℃

Table 4. Absolute Maximum Ratings

4.2. System Electrical Characteristics

V_{CC5V}=5V, V_{CC33}=3.3V, V_{CC18}=1.8V, V_{SSR}=GND=0V, T_{AMB}=25°C, unless otherwise specified.

4.2.1. System DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OL}	3.3V I/O output low-level voltage	0	-	1.0	V	$\|I_{OL3}\|$ = 4mA or 16mA
V_{OH}	3.3V I/O output high-level voltage	2.3	-	3.3	V	$\|I_{OH3}\|$ = 4mA or 16mA
V_{IL}	3.3V I/O input low-level voltage	0	-	1.0	V	
V_{IH}	3.3V I/O input high-level voltage	2.3	-	3.3	V	
V_{IL5}	5V I/O input low-level voltage	0	-	1.0	V	
V_{IH5}	5V I/O input high-level voltage	2.3	-	5.0	V	
V_{BIOS}	PB port BIAS state output voltage	1.63	1.65	1.67	V	V_{CC33}=3.3V
R_H	Internal pull-high resistor value	-	75	-	kΩ	(except MSCMD)
R_L	Internal pull-low resistor value	-	75	-	kΩ	(except MSCMD)
R_{H-CMD}	MSCMD internal pull-high resistor	10	-	20	kΩ	
R_{L-CD}	MSCD internal pull-low resistor value	1	-	-	MΩ	

Note: 1. V_{OH} / V_{OL} / V_{IH} / V_{IL} are applicable to the following pins: PA0 ~ PA7, PB0 ~ PB7, PC0 ~ PC7, PD0 ~ PD7, PE0 ~ PE7, PF0 ~ PF7 and PG0 ~ PG3.
2. V_{IH5} / V_{IL5} are applicable to the PLAY and MSCD pins.
3. R_H and R_L are applicable to the following pins: PA0 ~ PA7, PB0 ~ PB7, PD0, PD2 ~ PD7, MSDAT, PLAY and GCON.
4. R_{H-CMD} is applicable to the MSCMD pin.
5. R_{L-CD} is applicable to the MSCD pin.

Table 5. System DC Characteristics

5. PACKAGE OUTLINE INFORMATION

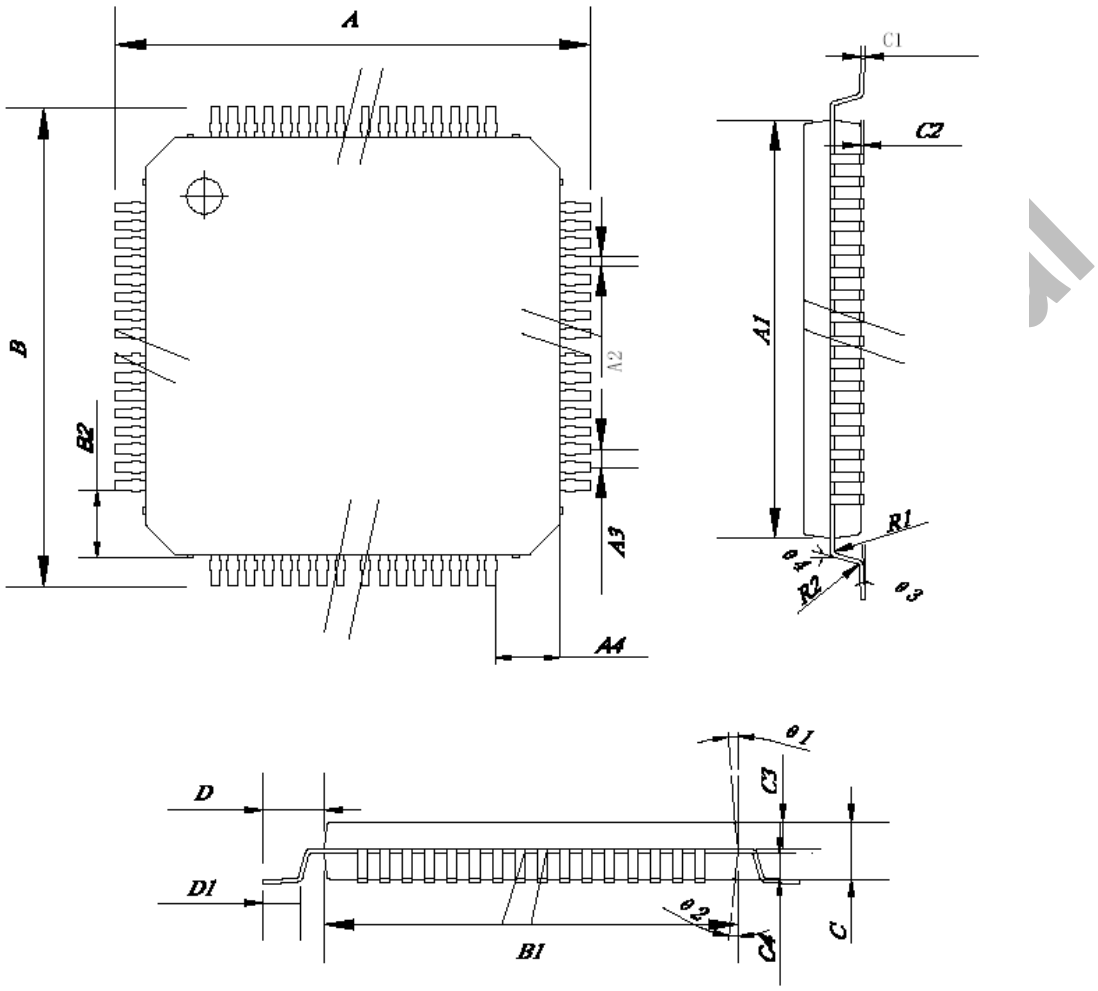

Figure 2. TQFP48 Outline Dimensions

Symbol	Dimensions (inch)		Dimensions (mm)		Symbol	Dimensions (inch)		Dimensions (mm)	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.346	0.362	8.80	9.20	C	0.035	0.041	0.90	1.05
A1	0.270	0.278	6.85	7.05	C1	0.004	0.008	0.09	0.20
A2	0.006	0.010	0.15	0.25	C2	0.002	0.006	0.05	0.15
A3	0.020 Typ.		0.5 Typ.		C3	0.017 Typ.		0.4365 Typ.	
A4	0.026 Typ.		0.65 Typ.		C4	0.017 Typ.		0.4365 Typ.	
B	0.346	0.362	8.80	9.20	D	0.033	0.045	0.85	1.15
B1	0.270	0.278	6.85	7.05	D1	0.018	0.003	0.45	0.75
B2	0.026 Typ.		0.65 Typ.		R1	0.006 Typ.		0.15 Typ.	
θ1	12° Typ.		12° Typ.		R2	0.006 Typ.		0.15 Typ.	
θ2	12° Typ.		12° Typ.						
θ3	0° - 7°		0° - 7°						
θ4	7° Typ.		7° Typ.						

Table 6. TQFP48 Outline Dimensions

6. HISTORY

Version	Date	Modify Content
1.0	2011.5.18	1. Original