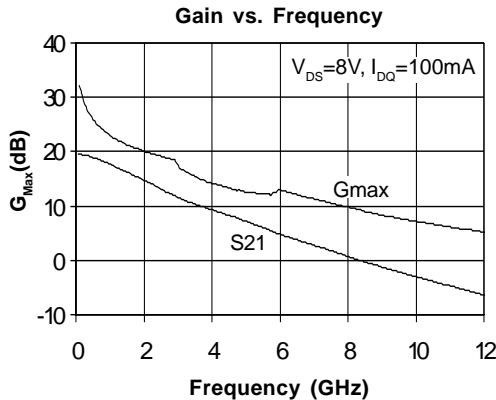


## Product Description

Stanford Microdevices' SHF-0186 is a high performance GaAs Heterostructure FET housed in a low-cost surface-mount plastic package. HFET technology improves breakdown voltage while minimizing Schottky leakage current for higher power added efficiency and improved linearity.

Output power at 1dB compression for the SHF-0186 is +28 dBm when biased for Class AB operation at 8V and 100mA. The +40 dBm third order intercept makes it ideal for high dynamic range, high intercept point requirements. It is well suited for use in both analog and digital wireless communication infrastructure and subscriber equipment including cellular PCS, CDPD, wireless data, and pagers.



# SHF-0186

## DC-12 GHz, 0.5 Watt

### AlGaAs/GaAs HFET



## Product Features

- Patented AlGaAs/GaAs Heterostructure FET Technology
- +28 dBm P1dB Typical
- +40 dBm Output IP3 Typical
- High Drain Efficiency: Up to 46% at Class AB
- 17 dB Gain at 900 MHz (Application circuit)
- 15 dB Gain at 1900 MHz (Application circuit)
- Gmax Guaranteed at 12 GHz

## Applications

- Analog and Digital Wireless System
- Cellular PCS, CDPD, Wireless Data, Pagers
- AN-020 Contains detailed application circuits

Symbol	Device Characteristics, T = 25°C V <sub>DS</sub> = 8V, I <sub>DQ</sub> = 100 mA	Units	Min.	Typ.	Max.	
G <sub>MAX</sub>	Maximum Available Gain	f = 900 MHz, Z <sub>S</sub> =Z <sub>S</sub> <sup>*</sup> , Z <sub>L</sub> =Z <sub>L</sub> <sup>*</sup> f = 1960 MHz, Z <sub>S</sub> =Z <sub>S</sub> <sup>*</sup> , Z <sub>L</sub> =Z <sub>L</sub> <sup>*</sup> f = 12000 MHz, Z <sub>S</sub> =Z <sub>S</sub> <sup>*</sup> , Z <sub>L</sub> =Z <sub>L</sub> <sup>*</sup>	dB	4.0	23.4 20.1 5.0	
S <sub>21</sub>	Insertion Power Gain	f = 900 MHz, Z <sub>S</sub> =Z <sub>L</sub> = 50 Ohms f = 1960 MHz, Z <sub>S</sub> =Z <sub>L</sub> = 50 Ohms	dB	13.7	18.0 15.2	
S <sub>21</sub>	Gain	f = 900 MHz, Z <sub>S</sub> =Z <sub>SOPT1</sub> , Z <sub>L</sub> =Z <sub>LLOPT</sub> f = 1960 MHz, Z <sub>S</sub> =Z <sub>SOPT1</sub> , Z <sub>L</sub> =Z <sub>LLOPT</sub>	dB		17.9 14.6	
P1dB	Output 1 dB compression point	f = 900 MHz, Z <sub>S</sub> =Z <sub>SOPT1</sub> , Z <sub>L</sub> =Z <sub>LLOPT</sub> f = 1960 MHz, Z <sub>S</sub> =Z <sub>SOPT1</sub> , Z <sub>L</sub> =Z <sub>LLOPT</sub>	dBm		28.0 28.8	
OIP <sub>3</sub>	Output Third Order Intercept Point	f = 900 MHz, Z <sub>S</sub> =Z <sub>SOPT1</sub> , Z <sub>L</sub> =Z <sub>LLOPT</sub> f = 1960 MHz, Z <sub>S</sub> =Z <sub>SOPT1</sub> , Z <sub>L</sub> =Z <sub>LLOPT</sub>	dBm		40.9 40.4	
I <sub>DSS</sub>	Saturated Drain Current V <sub>DS</sub> = 3V, V <sub>GS</sub> = 0V		mA	300		
g <sub>m</sub>	Transconductance V <sub>DS</sub> = 3V, V <sub>GS</sub> = 0V		mS	175		
V <sub>P</sub>	Pinch-Off Voltage V <sub>DS</sub> = 3V, I <sub>DQ</sub> = 1mA		V	-2.7	-1.9	-1.0
V <sub>BGS</sub>	Gate-to-Source Breakdown Voltage, I <sub>GS</sub> = 1.2mA		V		-20	-17
V <sub>BGD</sub>	Gate-to-Drain Breakdown Voltage, I <sub>GD</sub> = 1.2mA		V		-20	-17
R <sub>th</sub>	Thermal Resistance (junction to lead)		°C/W		66	

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**SHF-0186 DC-12 GHz 0.5 Watt AlGaAs/GaAs HFET**

**Absolute Maximum Ratings**

Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression:  $I_{DS}V_{DS} (max) < (T_J - T_L)/R_{TH}$

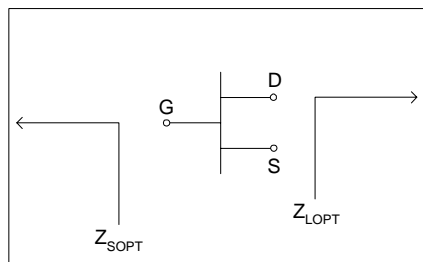
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	+12	V
Gate-to-Source Voltage	$V_{GS}$	-5 to 0	V
RF Input Power	$P_{IN}$	200	mW
Operating Temperature	$T_{OP}$	-45 to +85	C
Storage Temperature Range	$T_{stor}$	-65 to +175	C
Operating Junction Temperature	$T_J$	+175	C

**Typical Performance - Engineering Application Circuits (See AN-020)**

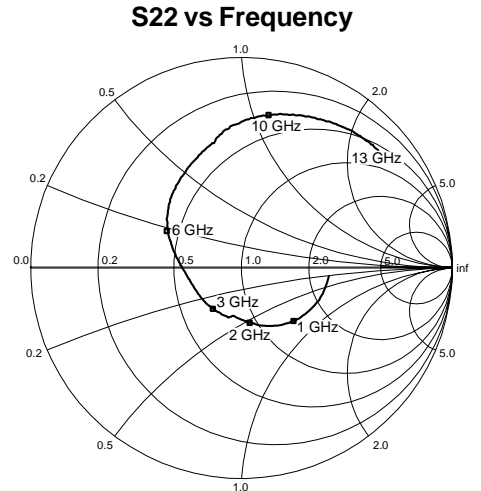
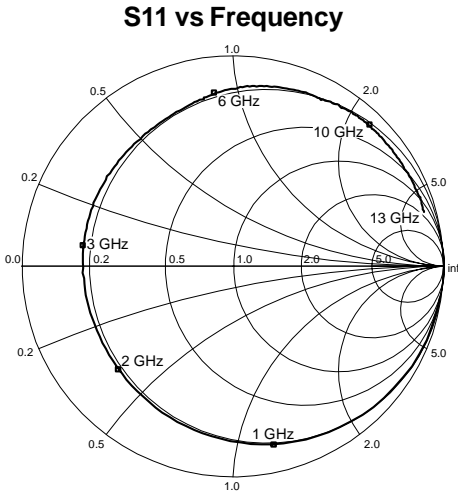
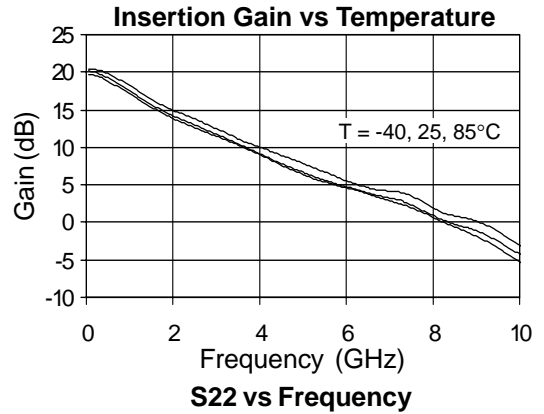
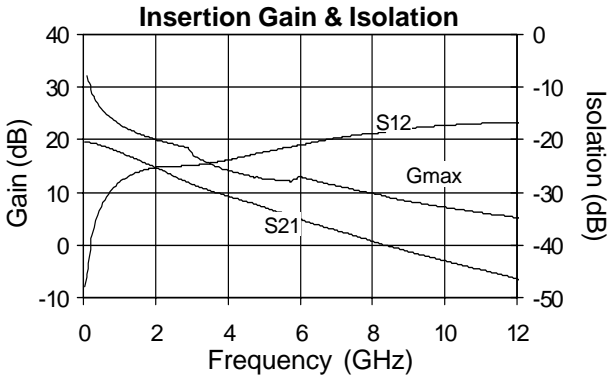
Freq (MHz)	$V_{DS}$ (V)	$I_{DQ}$ (mA)	P1dB (dBm)	OIP3* (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)	$Z_{SOPT}$		$Z_{LOPT}$	
									Mag	∠ Ang	Mag	∠ Ang
945	8	100	28.0	41.0	17.9	-19.4	-9.62	3.1	.45	∠ 40	.02	∠ 50
1960	8	100	28.8	39.5	14.6	-15.8	-5.31	2.5	.50	∠ 105	.16	∠ -168
2140	8	100	28.7	39.0	14.5	-12.3	-7.02	3.0	.50	∠ 120	.18	∠ 170
2450	8	100	28.5	39.5	14.0	-14.7	-5.28	2.9	.60	∠ 130	.08	∠ 130

\* 15dBm per tone

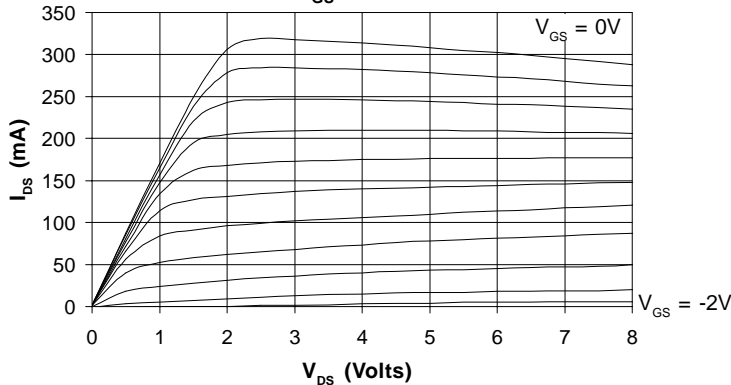
Data above represents typical performance of the application circuits noted in Application Note AN-020. Refer to the application note for additional RF data, PCB layouts, and BOMs for each application circuit. The application note also includes biasing instructions and other key issues to be considered. For the latest application notes please visit our site at [www.stanfordmicro.com](http://www.stanfordmicro.com) or call your local sales representative.



De-embedded S-Parameters ( $Z_s=Z_L=50\ \text{Ohms}$ ,  $V_{DS}=8\text{V}$ ,  $I_{DQ}=100\text{mA}$ ,  $25^\circ\text{C}$ )



DC-IV Curves ( $V_{GS} = -2\text{ to }0\text{V}$ ,  $0.2\text{V steps}$ )



Note: S-parameters are de-embedded to the device leads. The data represents typical performance of the device. Measured s-parameter data files can be downloaded using a link found on the SHF-0186 device page from our web site at [www.stanfordmicro.com](http://www.stanfordmicro.com).

## SHF-0186 DC-12 GHz 0.5 Watt AlGaAs/GaAs HFET



**Caution: ESD sensitive**  
 Appropriate precautions in handling, packaging and testing devices must be observed.

### Part Number Ordering Information

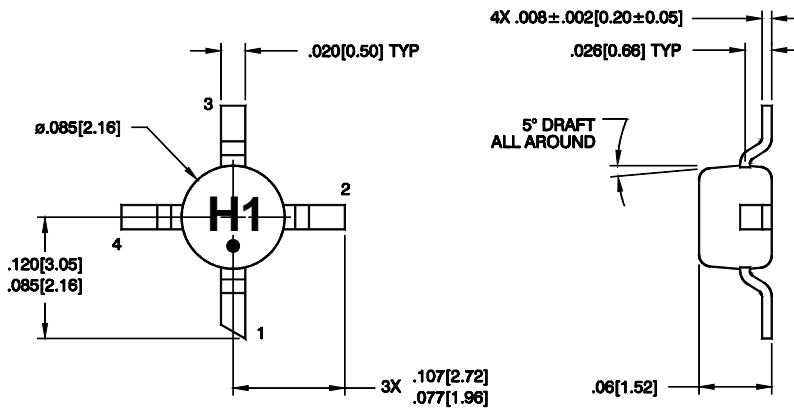
Part Number	Reel Size	Devices/Reel
SHF-0186	7"	1000

Pin #	Function	Description
1	Gate	Gate pin.
2	GND & Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	Drain pin.
4	GND & Source	Same as Pin 2

### Part Symbolization

The part will be symbolized with an "H1" designator on the top surface of the package.

### Package Dimensions



### PCB Pad Layout

