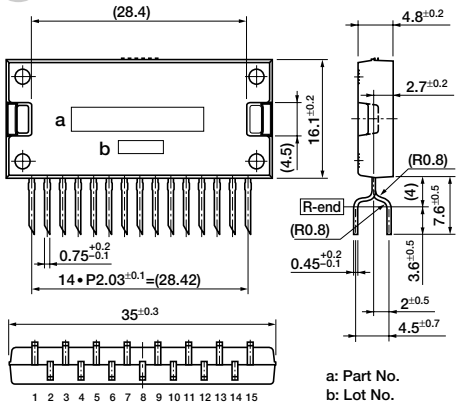
Full Bridge PWM Control DC Motor Driver ICs SI-5300

Features

- P-ch MOS for high side and N-ch MOS for low side in one package
- Enable to drive DC±5V
- Possible to drive a motor at the LS-TTL, C-MOS Logic level
- Guarantee Tj=Tch=150°C
- Built-in over current protection and thermal shut down circuits
- Built-in diagnosis function to monitor and signal the state of each protection circuits
- Built-in vertical current prevention circuits (Dead time is defined internally.)
- No insulator required for Sanken's original package (SPM package)

External Dimensions (unit: mm)



Absolute Maximum Ratings

(Ta=25°C)

Parameter	Symbol	Ratings	Unit	Conditions
Motor supply voltage	V_M	40	V	
Input terminal voltage	IN1	–0.3 to 7	V	
	IN2	–0.3 to 7	V	
	PWM	–0.3 to 7	V	
Output current	I_O	±5	A	
	$I_{O\ (p\text{-}p)}$	±17	A	P_W≦1ms, Duty≦50%
PWM control frequency	f_{PWM}	20	kHz	Duty=20% to 80%
Forward • reverse rotation switch frequency*	f_{CW}	500	Hz	
Operating temperature	T_{OP}	–40 to +85	°C	
Junction and channel temperature	Tj, Tch	–40 to +150	°C	
Storage temperature	Tstg	–40 to +150	°C	
Thermal resistance	θj-c	3.7	°C/W	
	θj-a	35	°C/W	
Power dissipation	P_{D1}	3.6	W	Without heatsink
	P_{D2}	33.7	W	With infinite heatsink

Note: * The dead time for the length current prevention in positive and the reversing switch is set by internal control IC. The set point in internal IC at the dead time is 20μs (typical). Please take into account the dead time and consider the load conditions when you use the IC.

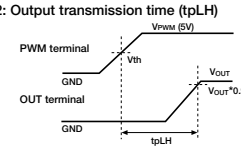
Electrical Characteristics

(Unless, otherwise specified, Tj=Tch=25°C, V_M=14V, I_O=3A)

Parameter	Symbol	Ratings min	Ratings typ	Ratings max	Unit	Conditions
Motor supply voltage	V_{IN}	6		18	V	V_M=24V (2 min.)
Output saturation voltage	V, V_M-V_O			0.8	V	I_O=3A
	V, V_O-PG			0.3	V	I_O=3A
Output leakage current	I_L, L			100	μA	V_M=40V
	I_L, H			100	μA	V_M=40V
Output transmission time	tpLH			10 *2	μs	V_{PWM}: L→H (Vth=2.5V typ)
	tpHL			15 *3	μs	V_{PWM}: H→L (Vth=2.5V typ)
	tpHL-tpLH			10	μs	
Forward voltage characteristic of diode between drain and source	V_F•L		0.8		V	I_O=3A
			1.0		V	I_O=10A
	V_F•H		0.8		V	I_O=3A
			1.0		V	I_O=10A
Static circuit current	IM1		22		mA	Stop mode
	IM2		22		mA	Forward and reverse mode
	IM3		16		mA	Brake mode
Input terminal voltage	$V_{IN,\ H}$	3.0			V	$V_{IN}1=V_{IN}2=V_{PWM}$
	$V_{IN,\ L}$			2.0	V	$V_{IN}1=V_{IN}2=V_{PWM}$
Input terminal current	$I_{IN,\ L}$	–100			μA	$V_{IN}1=V_{IN}2=V_{PWM}$=0V
	$I_{IN,\ H}$			200	μA	$V_{IN}1=V_{IN}2=V_{PWM}$=5V
OPC start current	I_{OCP}	16			A	*1
DIAG output pulse width	t_{DIAG}	20			ms	C=1μF (typ)
DIAG terminal voltage	V_D•L			0.3	V	ID•SINK=1mA *4

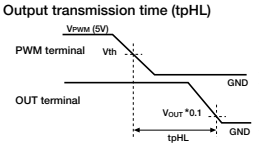
Note:
*1: The standard value of I_{OCP} is assumed to be a value by which the output of each Power MOS FET cuts off. When the protection circuit of OCP and TSD operates, Power MOS FETs keeps cutoff. When a signal (5V: H → 0V: L) is input to the terminal PWM, the cutoff operation will be released. Moreover, three minutes (Ta=25°C, f_{PWM}=10kHz, V_M=14V) are assumed to be max at the overcurrent state continuance time in the V_M operation and the ground of output terminal (OUT1, OUT2). It is not the one to assure the operation including reliability in the state that the short-circuit continues for a long time.

*2: Output transmission time (tpLH)



Output transmission time tpLH is time from Vth (2.5V typ) of the terminal of PWM to output (V_{OUT} *0.9) of the output terminal.

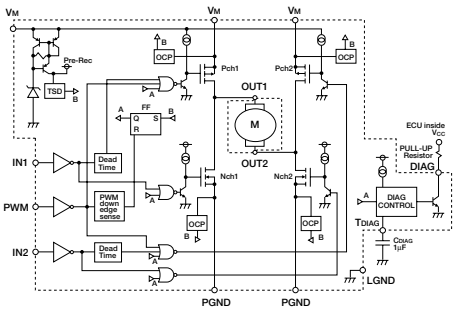
*3: Output transmission time (tpHL)



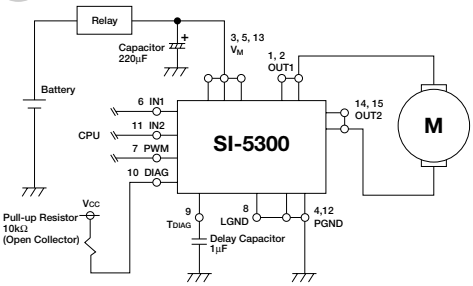
Output transmission time tpHL is time from Vth (2.5V typ) of the terminal of PWM to output (V_{OUT} *0.1) of the output terminal.

*4: DIAG signal output terminal is an open collector output. Use a pull-up resistor when connecting it to a logic circuit.

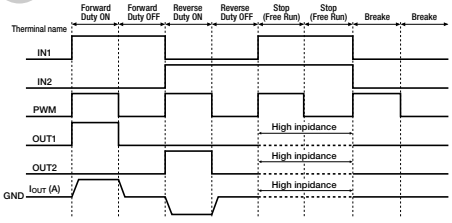
Equivalent Circuit

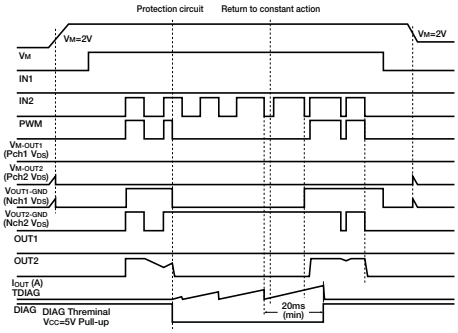


Standard Connection Diagram



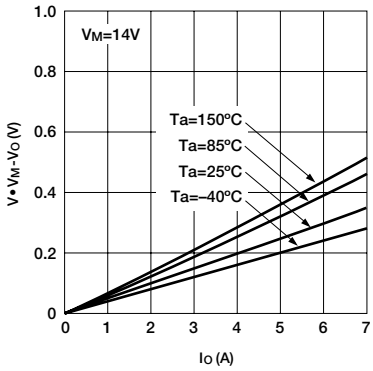
Timing Chart



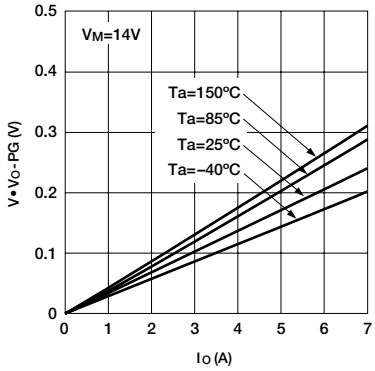


Electrical Characteristics

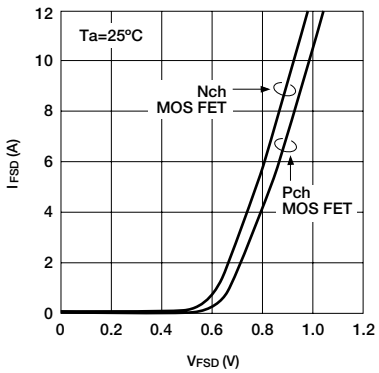
■ Output saturation voltage (Pch)



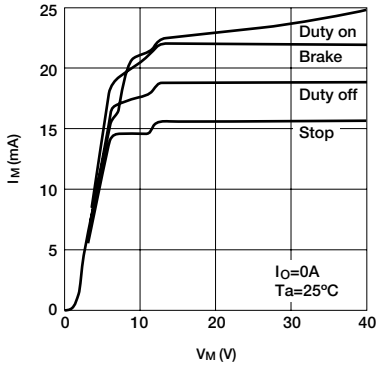
■ Output saturation voltage (Nch)



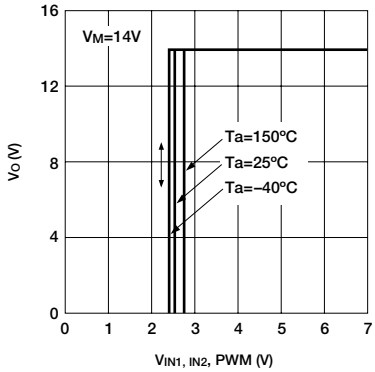
■ Forward voltage of Diode between drain and source



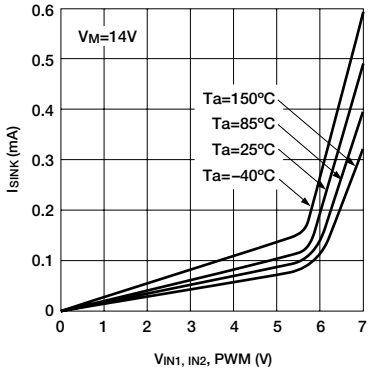
■ Quiescent circuit current



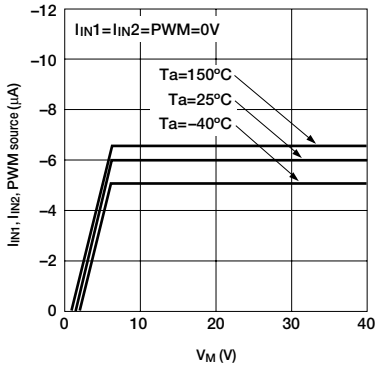
■ Voltage of input terminal (Threshold voltage)



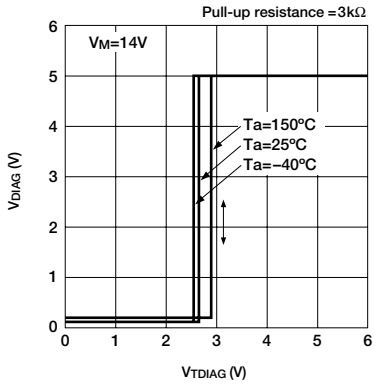
■ Current of input terminal (SINK current)



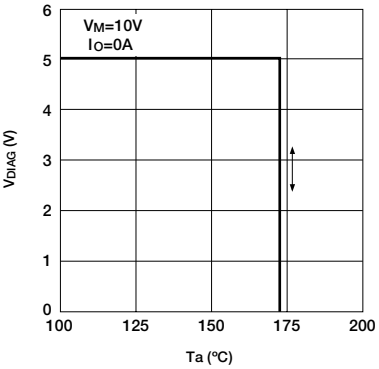
■ Current of input terminal (Source current)



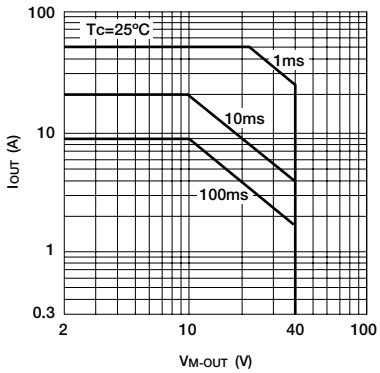
■ VTDIAG – VDIAG Characteristics



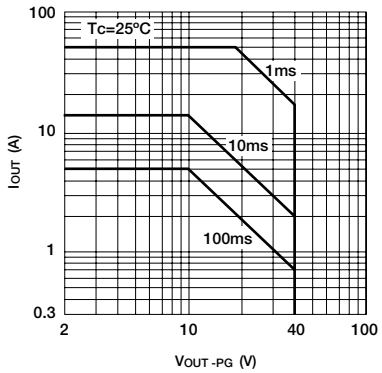
■ Thermal shut down protection



■ Pch MOS FET Safe Operating Area (SOA)



■ Nch MOS FET Safe Operating Area (SOA)



■ PD—Ta Characteristics