# SI2304

PUOLOP 迪浦

## 30V N-Channel Enhancement Mode MOSFET

**VDS= 30V**

RDS(ON), Vgs@ 10V, Ids@ 3.5A ＜70mΩ

RDS(ON), Vgs@ 4.5V, Ids@ 2.8A ＜80mΩ

### Features

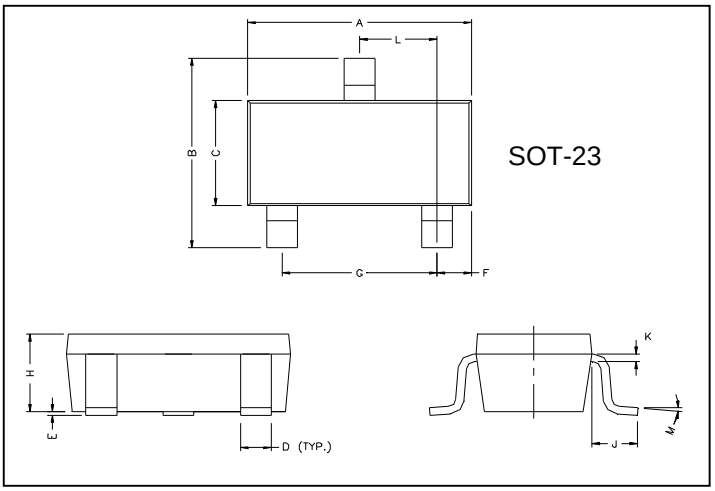
Advanced trench process technology

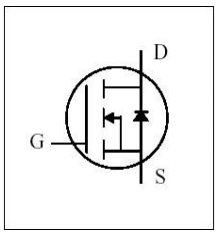
High Density Cell Design For Ultra Low On-Resistance

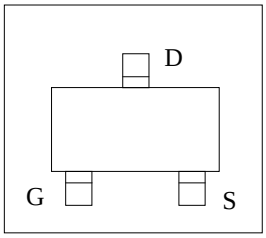
High Power and Current handing capability

Ideal for Li ion battery pack applications

Package Dimensions




| REF. | Millimeter | | REF. | Millimete | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 2.80 | 3.00 | G | 1.80 | 2.00 |
| B | 2.30 | 2.50 | H | 0.90 | 1.1 |
| C | 1.20 | 1.40 | K | 0.10 | 0.20 |
| D | 0.30 | 0.50 | J | 0.35 | 0.70 |
| E | 0 | 0.10 | L | 0.92 | 0.98 |
| F | 0.45 | 0.55 | M | 0° | 10° |

**ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C UNLESS OTHERWISE NOTED)**

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current ($T_J$ = 150°C)[a, b] | $T_A$ = 25°C | $I_D$ | 3.5 | A |
| | $T_A$ = 70°C | | 2.8 | |
| Pulsed Drain Current | | $I_{DM}$ | 16 | |
| Continuous Source Current (Diode Conduction)[a, b] | | $I_S$ | 1.25 | |
| Maximum Power Dissipation[a, b] | $T_A$ = 25°C | $P_D$ | 1.25 | W |
| | $T_A$ = 70°C | | 0.80 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | -55 to 150 | °C |

**THERMAL RESISTANCE RATINGS**

| Parameter | | Symbol | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient[a] | t ≤ 5 sec | $R_{thJA}$ | | 100 | °C/W |
| | Steady State | | 130 | | |

Notes

a. Surface Mounted on FR4 Board.

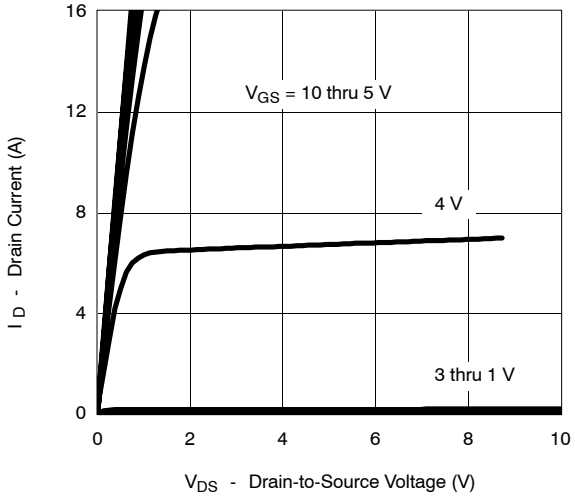
b. t ≤ 5 sec.

| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Condition** | **Min** | **Typ** | **Max** | **Unit** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{DS}$ = 0 V, $I_D$ = 250 μA | 30 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | | | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | | | 0.5 | μA |
| | | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | | 10 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ ≥ 4.5 V, $V_{GS}$ = 10 V | 6 | | | A |
| | | $V_{DS}$ ≥ 4.5 V, $V_{GS}$ = 4.5 V | 4 | | | |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 3.5 A | | 0.046 | 0.057 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 2.8 A | | 0.070 | 0.094 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 4.5 V, $I_D$ = 3.5 A | | 6.9 | | S |
| Diode Forward Voltage[a] | $V_{SD}$ | $I_S$ = 1.25 A, $V_{GS}$ = 0 V | | 0.8 | 1.2 | V |
| **Dynamic[b]** | | | | | | |
| Gate Charge | $Q_g$ | $V_{DS}$ = 15 V, $V_{GS}$ = 5 V, $I_D$ = 3.5 A | | 4.2 | 7 | nC |
| Total Gate Charge | $Q_{gt}$ | $V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A | | 8.5 | 20 | |
| Gate-Source Charge | $Q_{gs}$ | | | 1.9 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 1.35 | | |
| Gate Resistance | $R_g$ | | 0.5 | | 2.4 | Ω |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f= 1 MHz | | 555 | | pF |
| Output Capacitance | $C_{oss}$ | | | 120 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 60 | | |
| **Switching** | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15 V, $R_L$ = 15 Ω<br>$I_D$ ≅ 1 A, $V_{GEN}$ = 10 V, $R_G$ = 6 Ω | | 9 | 20 | ns |
| Rise Time | $t_r$ | | | 7.5 | 18 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 17 | 35 | |
| Fall Time | $t_f$ | | | 5.2 | 12 | |

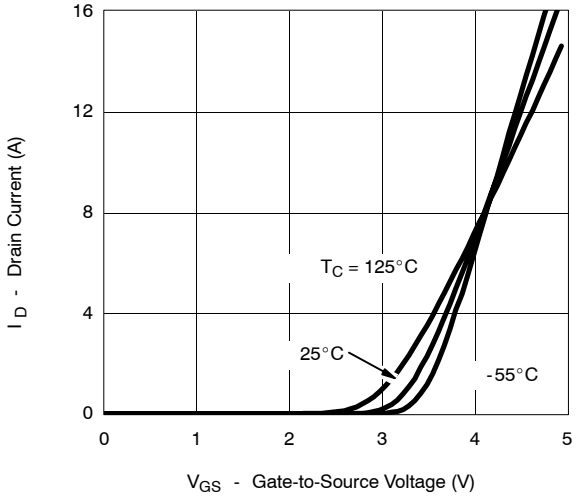
Notes
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

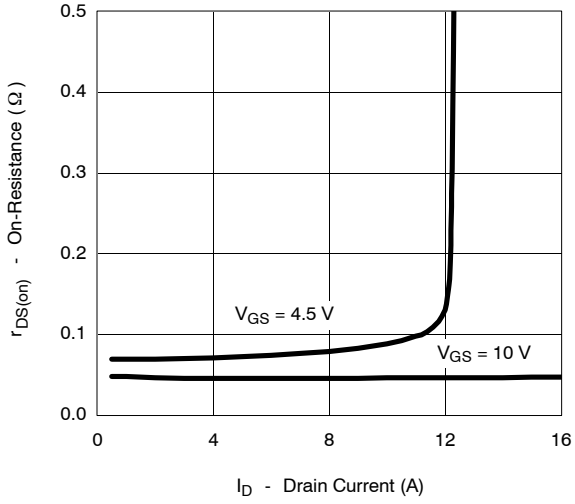
**Output Characteristics**



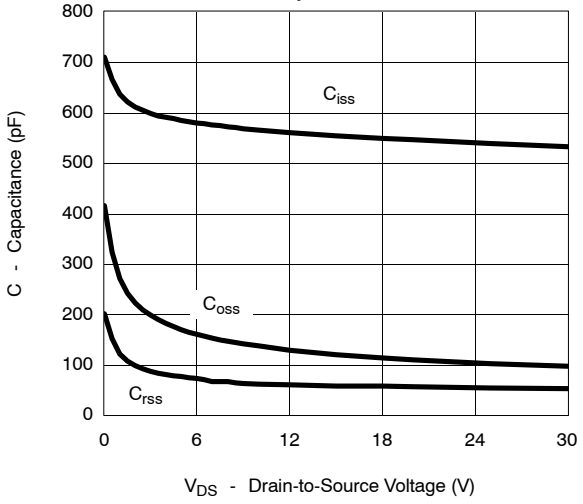

**Transfer Characteristics**



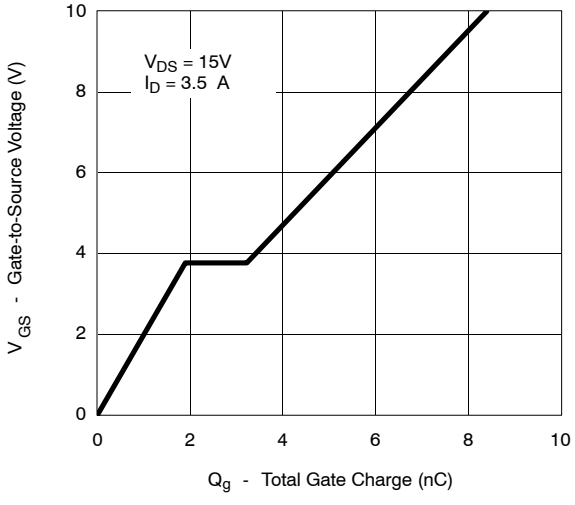

**On-Resistance vs. Drain Current**



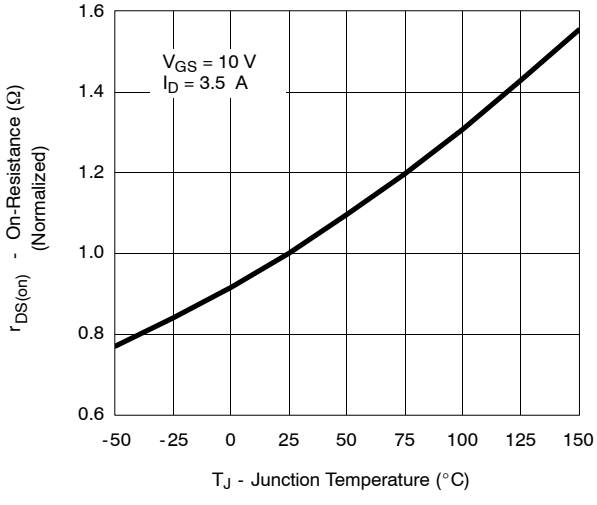

**Capacitance**




**Gate Charge**

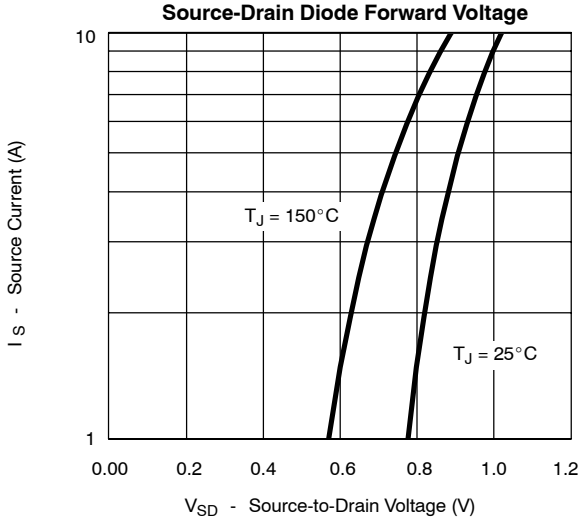



**On-Resistance vs. Junction Temperature**

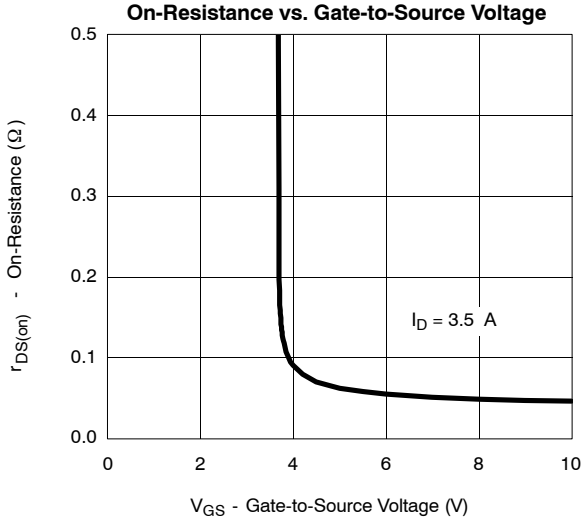


## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

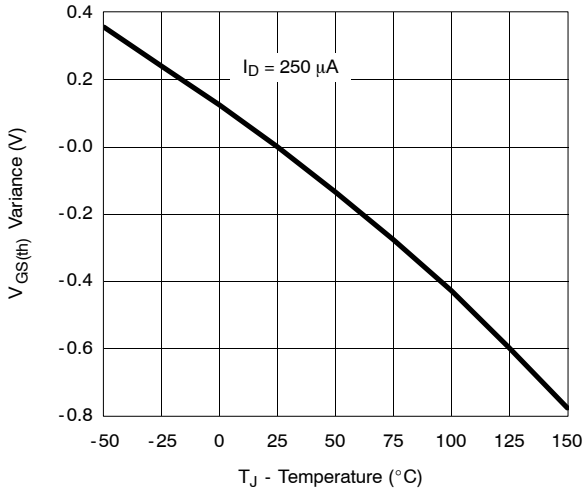
**Source-Drain Diode Forward Voltage**



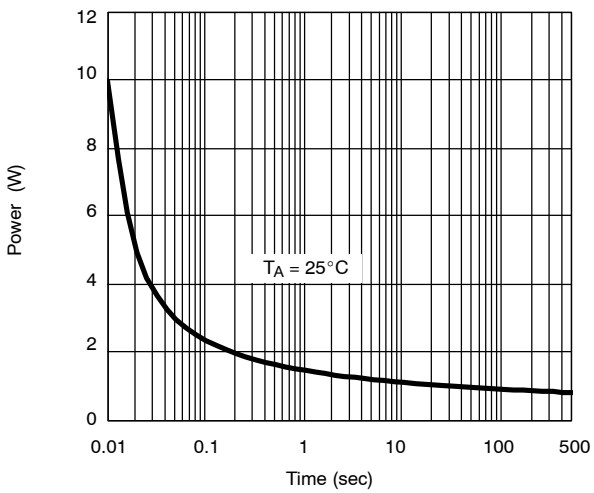

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**




**Single Pulse Power**




**Normalized Thermal Transient Impedance, Junction-to-Ambient**