P-Channel Power MOSFE

SI2305DS

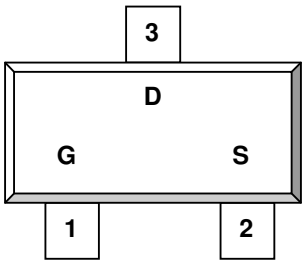
DESCRIPTION

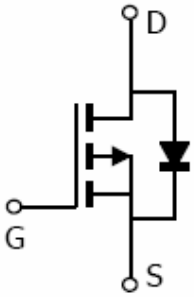
SI2305DS is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This hight-density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits,and low in-line power loss are required. The product is in a very small outline surface mount package.

FEATURE

- 20V/3.3A, $R_{DS(ON)}$ = 68mΩ @V_{GS} = 4.5V
- 20V/2.2A, $R_{DS(ON)}$ = 89mΩ @V_{GS} = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PIN CONFIGURATION SOT-23





1.Gate 2.Source 3.Drain

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current		I_D	-3.3	A
Pulsed Drain Current [1]		I_{DM}	-10	
Maximum Power Dissipation [2]	TA = 25°C	P_D	1.25	W
	TA = 75°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		R_{thJA}	100	°C/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [3]			166	

Notes
1) Pulse width limited by maximum junction temperature.
2) Surface Mounted on FR4 Board, t ≤ 5 sec.
3) Surface Mounted on FR4 Board.

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	**Test Condition**	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-20			V
Drain-Source On-State Resistance[1)]	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -3.3A		64	110	mΩ
		V_{GS} = -2.5V, I_D = -2.2A		89	140	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	0.4		1	V
Zero Gate Voltage Drain Current 0	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V			-1	uA
		V_{DS} = -16V, V_{GS} = 0V TJ=55°C			-10	
Gate Body Leakage	I_{GSS}	V_{GS} = ± 10V, V_{DS} = 0V			±100	nA
Forward Transconductance[1)]	g_{fs}	V_{DS} = -5V, I_D = -2.8A		6.5	—	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = -6V, I_D ≅ -2.3A V_{GS} = -4.5V		5.8	10	nC
Gate-Source Charge	Q_{gs}			0.85		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6V, RL=6Ω I_D ≅ -1.A, V_{GEN} = -4.5V R_G = 6Ω		13	25	ns
Turn-On Rise Time	t_r			36	60	
Turn-Off Delay Time	$t_{d(off)}$			42	70	
Turn-Off Fall Time	t_f			34	60	
Input Capacitance	C_{iss}	V_{DS} = -6V, V_{GS} = 0V f = 1.0 MHz		415		pF
Output Capacitance	C_{oss}			223		
Reverse Transfer Capacitance	C_{rss}			87		
Source-Drain Diode						
Max. Diode Forward Current	I_S				-1.6	A
Diode Forward Voltage	V_{SD}	I_S = -1.0A, V_{GS} = 0V		-0.8	-1.2	V

1) Pulse test: pulse width <= 300us, duty cycle<= 2%

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

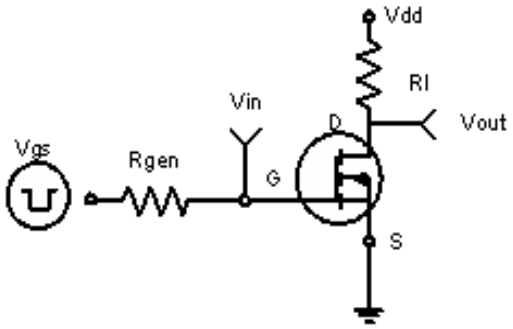

Figure 1:Switching Test Circuit

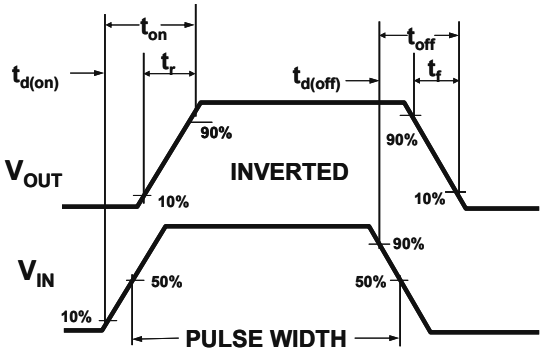

Figure 2:Switching Waveforms

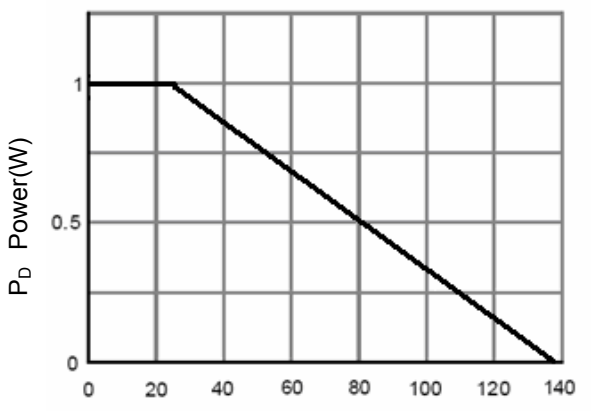

Figure 3 Power Dissipation

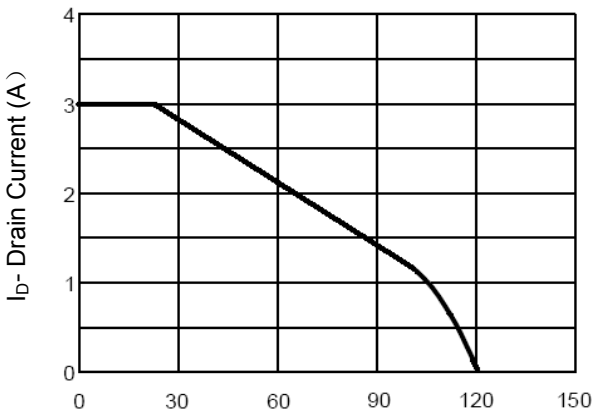

Figure 4 Drain Current

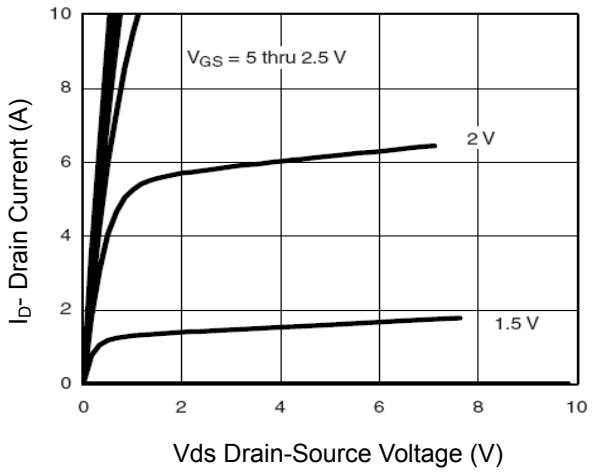

Figure 5 Output CHARACTERISTICS

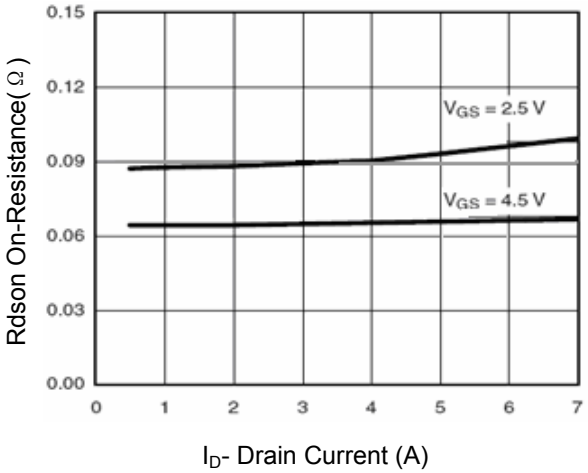

Figure 6 Drain-Source On-Resistance

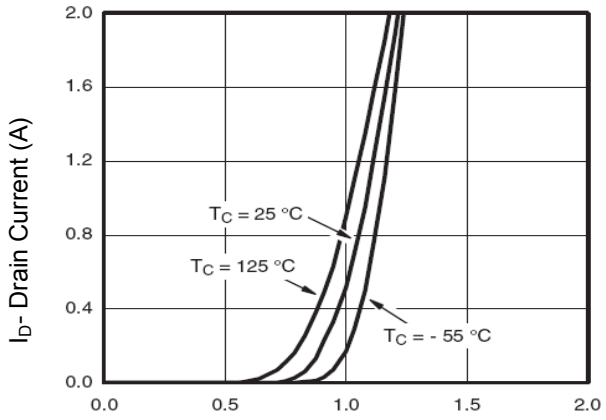

Figure 7 Transfer Characteristics

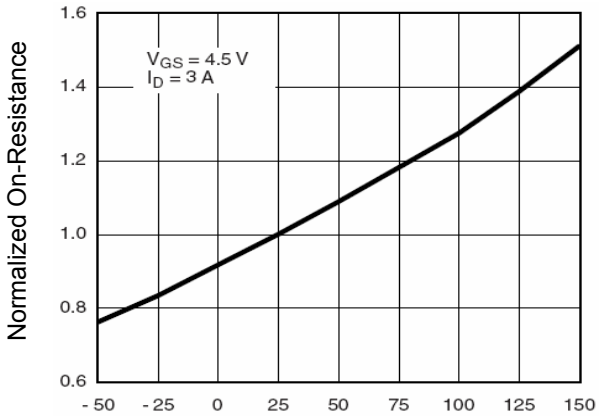

Figure 8 Drain-Source On-Resistance

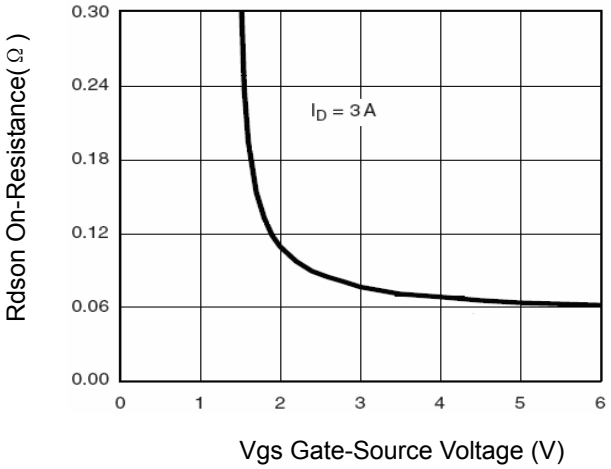

Figure 9 Rdson vs Vgs

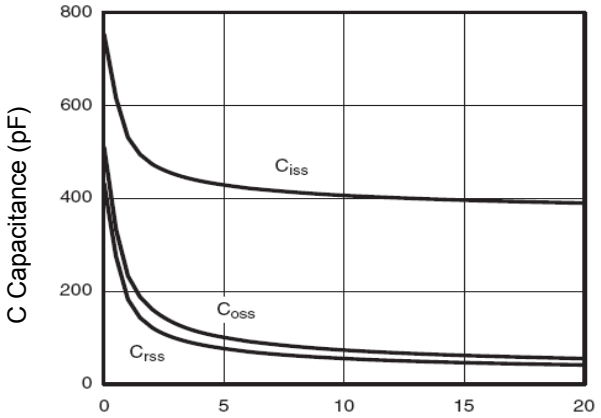

Figure 10 Capacitance vs Vds

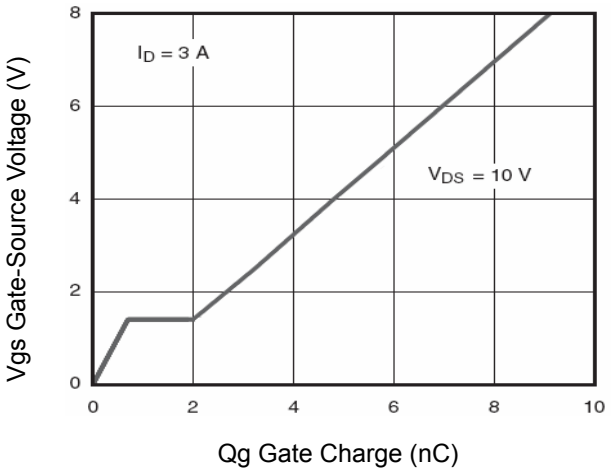

Figure 11 Gate Charge

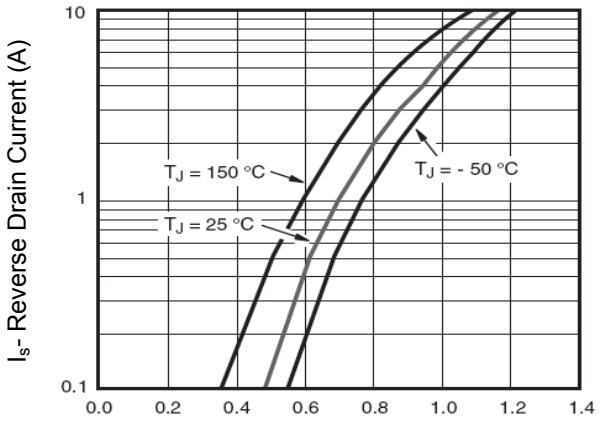

Figure 12 Source- Drain Diode Forward

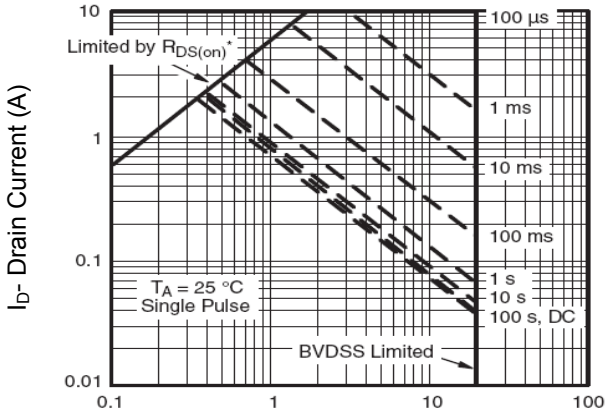

Figure 13 Safe Operation Area

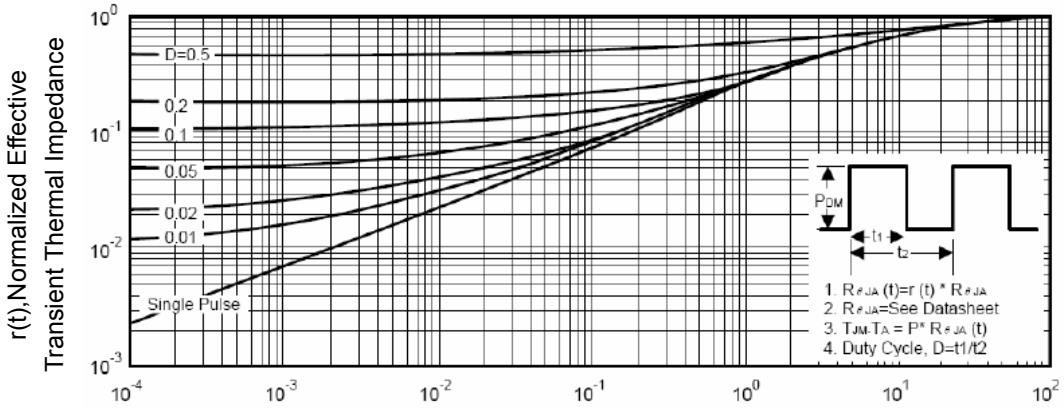

Figure 14 Normalized Maximum Transient Thermal Impedance

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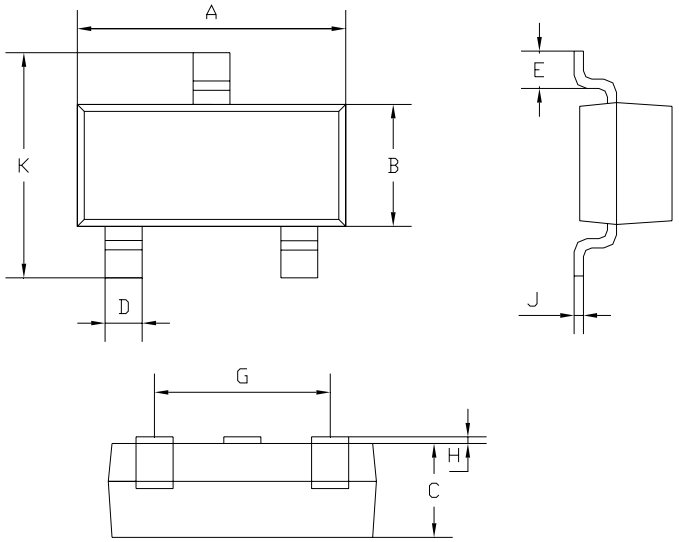
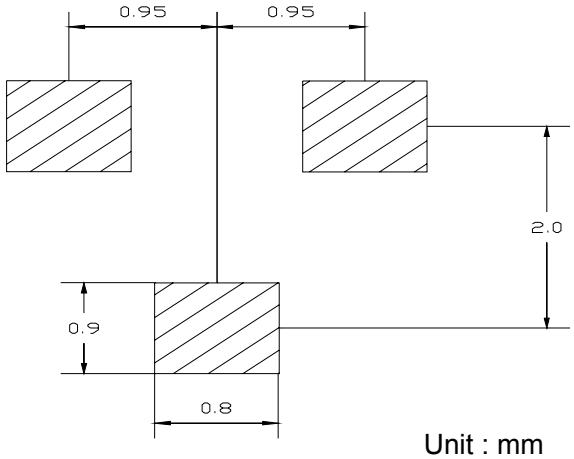
PACKAGE OUTLINE

Plastic surface mounted package SOT-23



SOT-23		
Dim	Min	Max
A	2.85	2.95
B	1.25	1.35
C	1.0Typical	
D	0.37	0.43
E	0.35	0.48
G	1.85	1.95
H	0.02	0.1
J	0.1Typical	
K	2.35	2.45
All Dimensions in mm		

SOLDERING FOOTPRINT



Unit : mm

PACKAGE INFORMATION

Device-marking	Device	Package	Shipping
A1SHB	SI2305DS	SOT-23	3000/Tape&Reel